

- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT I²C BUS Serial EEPROMs
- ◇ SERIES SIGNATURE SERIES
- ◇ FAMILY BR24C□□ family
- ◇ TYPE Supply voltage 4.5V~5.5V/Operating temperature -40°C~+85°Ctype
- ◇ PART NUMBER BR24C□□-□□6TP

| PART NUMBER | PACKAGE | DENSITY |
|---------------|--------------------------------|---------|
| BR24C01-MN6TP | SO8 narrow | 1Kbit |
| BR24C02-MN6TP | | 2Kbit |
| BR24C04-MN6TP | | 4Kbit |
| BR24C08-MN6TP | | 8Kbit |
| BR24C16-MN6TP | | 16Kbit |
| BR24C32-MN6TP | | 32Kbit |
| BR24C64-MN6TP | | 64Kbit |
| BR24C01-DW6TP | TSSOP8 | 1Kbit |
| BR24C02-DW6TP | | 2Kbit |
| BR24C04-DW6TP | | 4Kbit |
| BR24C08-DW6TP | | 8Kbit |
| BR24C16-DW6TP | | 16Kbit |
| BR24C32-DW6TP | | 32Kbit |
| BR24C01-DS6TP | TSSOP8 3 × 3mm ² | 1Kbit |
| BR24C02-DS6TP | | 2Kbit |
| BR24C04-DS6TP | | 4Kbit |
| BR24C08-DS6TP | | 8Kbit |
| BR24C16-DS6TP | | 16Kbit |

◇ FEATURES

Two wire serial interface
 Endurance : 1,000,000 erase/write cycles
 Data retention : 40years
 Initial Data FFh in all address

◇ ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---------------------|------|----------------------|------|
| Tstg | Storage Temperature | -65 | 125 | °C |
| V _{IO} | Terminal Voltage | -0.3 | V _{CC} +0.3 | V |
| V _{CC} | Supply Voltage | -0.3 | 6.5 | V |

◇ POWER DISSIPATION (T_a=25°C)

| PACKAGE | Rating | Unit |
|-----------------------------|--------|------|
| SO8 narrow | 450 *1 | mW |
| TSSOP8 | 330 *2 | mW |
| TSSOP8 3 × 3mm ² | 310 *3 | mW |

* Degradation is done at 4.5mW/°C(*1), 3.3mW/°C(*2), 3.1mW/°C(*3) for operation above 25°C

◇ RECOMMENDED OPERATING CONDITION

| Symbol | Parameter | Min | Max | Unit |
|-----------------|-------------------------------|-----|-----|------|
| V _{cc} | Supply Voltage | 4.5 | 5.5 | V |
| T _A | Ambient Operating Temperature | -40 | 85 | °C |

◇ DC OPERATING CHARACTERISTICS
(Unless otherwise specified Ta=-40~85°C, V_{cc}=4.5~5.5V)

| Parameter | Symbol | Min. | Max. | Unit | Test condition |
|---|------------------|--------------------|-----------------------|------|--------------------------------|
| Input Leakage Current (SCL,SDA) | I _{LI} | - | ±2 | μA | VIN=Vss or Vcc |
| Output Leakage Current | I _{LO} | - | ±2 | μA | VOUT= Vss or Vcc (SDA in Hi-Z) |
| Supply Current | I _{CC} | - | 2 | mA | Vcc=5V, f _c =400kHz |
| Stand-by Supply Current | I _{CC1} | - | 1 *1 | μA | VIN =Vss or Vcc, Vcc=5V |
| | | - | 10 *2 | | |
| Input Low Voltage (E2,E1,E0,SCL,SDA) | V _{IL} | - | 0.3V _{cc} | V | |
| Input Low Voltage (\overline{WC}) | V _{IL} | - | 0.5 *1 | V | |
| | | - | 0.3V _{cc} *2 | | |
| Input High Voltage (E2,E1,E0,SCL,SDA, \overline{WC}) | V _{HI} | 0.7V _{cc} | - | V | |
| Output Low Voltage | V _{OL} | - | 0.4 | V | IOL=3mA, Vcc=5V |

*1 BR24C01/02/04/08/16

*2 BR24C32/64

◇ AC OPERATING CHARACTERISTICS
(Unless otherwise specified Ta=-40~85°C, V_{cc}=4.5~5.5V)

| Parameter | Symbol | Min | Max | Unit |
|--|---------------------|------|-----|------|
| Clock Frequency | f _c | - | 400 | kHz |
| Clock Pulse Width High | t _{CHCL} | 600 | - | ns |
| Clock Pulse Width Low | t _{CLCL} | 1300 | - | ns |
| SDA Fall Time *1 | t _{OL,OLZ} | 20 | 300 | ns |
| Data In Set Up Time | t _{DSX} | 100 | - | ns |
| Data In Hold Time | t _{CDX} | 0 | - | ns |
| Data Out Hold Time | t _{CDX} | 200 | - | ns |
| Clock Low to Next Data Valid(Access Time) | t _{CLDV} | 200 | 900 | ns |
| Start Condition Set Up Time | t _{DSX} | 600 | - | ns |
| Start Condition Hold Time | t _{PLX} | 600 | - | ns |
| Stop Condition Set Up Time | t _{CHSX} | 600 | - | ns |
| Time between Stop Condition and Next Start Condition | t _{MDL} | 1300 | - | ns |
| Write Time | t _w | - | 5 | ms |

*1 Not 100% TESTED

○This product is not designed for protection against radioactive rays.

◇ BLOCK DIAGRAM

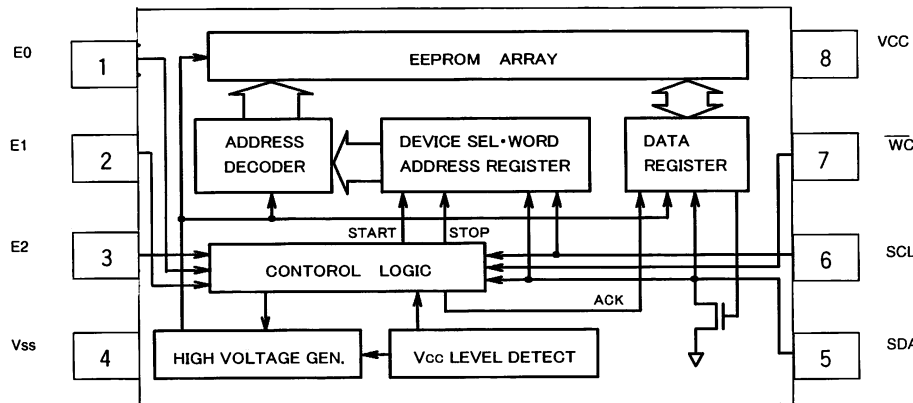


Fig.-1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

| PIN No. | PIN NAME |
|---------|-----------------|
| 1 | E0 |
| 2 | E1 |
| 3 | E2 |
| 4 | Vss |
| 5 | SDA |
| 6 | SCL |
| 7 | \overline{WC} |
| 8 | Vcc |

◇NOTES FOR POWER SUPPLY

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit. To prevent this, the device has the feature of P.O.R. and LVCC. In the case of power up, keep the following conditions to ensure functions of P.O.R. and LVCC.

1. It is necessary to be "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.

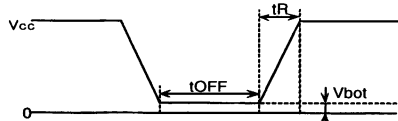


Fig.-2 Vcc RISING WAVEFORM

◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

| tR | tOFF | Vbot |
|-------------|------------|------------|
| Below 10ms | Above 10ms | Below 0.3V |
| Below 100ms | Above 10ms | Below 0.2V |

3. Prevent SDA and SCL from being "High-Z".

In case that condition 1. and/or 2. cannot be met, take following actions.

- A) Unable to keep condition 1.
(SDA is "LOW" during power up.)
→ Control SDA ,SCL to be "HIGH" as Fig.-3(a), 3(b).
- B) Unable to keep condition 2.
→ After power becomes stable, execute software reset.
- C) Unable to keep both conditions 1 and 2.
→ Follow the instruction A first, then the instruction B.

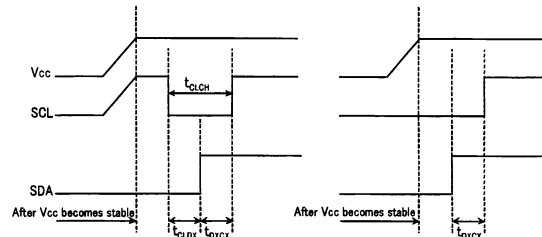


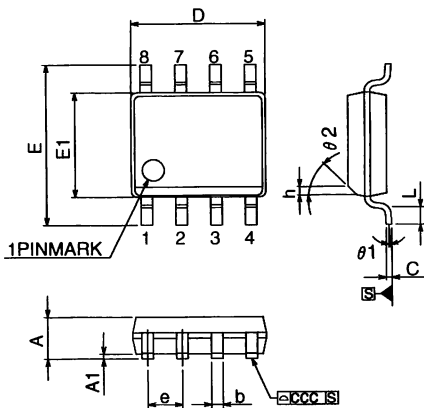
Fig.-3(a) SCL='H' and SDA='L'

Fig.-3(b) SCL='L' and SDA='L'

◇CAUTIONS ON USE

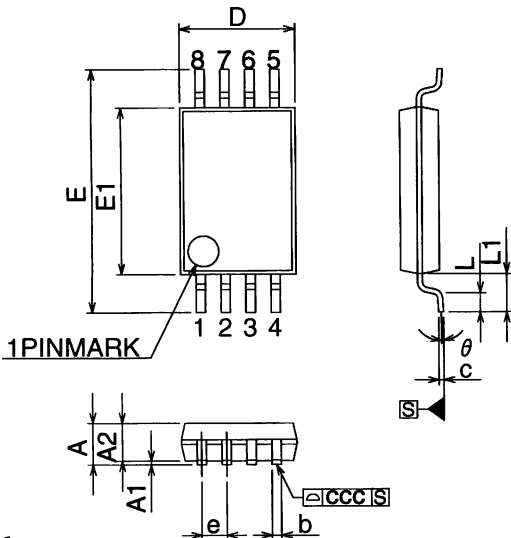
- (1) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- (2) Vss electric potential
Set the voltage of Vss terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of Vss terminal.
- (3) Thermal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.
- (4) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and Vss owing to foreign matter, LSI may be destructed.
- (5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION



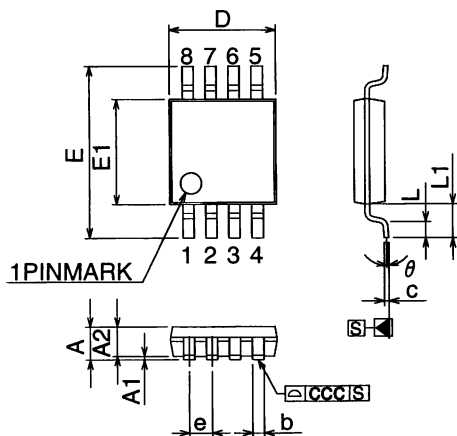
Notes
 1.This drawing is subject to change without notice.
 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 3.Reference JEDEC MS-012 variation AA.

Fig.-4 SO8 narrow Package Outline



Notes
 1.This drawing is subject to change without notice.
 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 3.Reference JEDEC MO-153 variation AA.

Fig.-5 TSSOP Package Outline



Notes
 1.This drawing is subject to change without notice.
 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 3.Reference JEDEC MO-187 variation AA.

Fig.-6 TSSOP 3 x 3mm² Package Outline

◇ SO8 narrow Package size data

| Symb. | mm | | | inches | | |
|---------|------|------|------|--------|-------|-------|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | - | 1.35 | 1.75 | - | 0.053 | 0.069 |
| A1 | - | 0.10 | 0.25 | - | 0.004 | 0.010 |
| b | - | 0.33 | 0.51 | - | 0.013 | 0.020 |
| c | - | 0.19 | 0.25 | - | 0.007 | 0.010 |
| D | - | 4.80 | 5.00 | - | 0.189 | 0.197 |
| e | 1.27 | - | - | 0.050 | - | - |
| E | - | 5.80 | 6.20 | - | 0.228 | 0.244 |
| E1 | - | 3.80 | 4.00 | - | 0.150 | 0.157 |
| L | - | 0.40 | 1.27 | 0.050 | 0.016 | 0.050 |
| theta 1 | - | 0° | 8° | - | 0° | 8° |
| ccc | - | - | 0.10 | - | - | 0.004 |
| h | - | 0.25 | 0.50 | - | 0.010 | 0.020 |
| theta 2 | 45° | - | - | 45° | - | - |

◇ TSSOP8 Package size data

| Symb. | mm | | | inches | | |
|-------|-------|-------|-------|--------|--------|--------|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | - | 0.050 | 0.150 | - | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.800 | 1.050 | 0.0394 | 0.0315 | 0.0413 |
| b | - | 0.190 | 0.300 | - | 0.0075 | 0.0118 |
| c | - | 0.090 | 0.200 | - | 0.0035 | 0.0079 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | - | - | 0.0256 | - | - |
| E | 6.400 | 6.200 | 6.600 | 0.2520 | 0.2441 | 0.2598 |
| E1 | 4.400 | 4.300 | 4.500 | 0.1732 | 0.1693 | 0.1772 |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | - | - | 0.0394 | - | - |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| theta | - | 0° | 8° | - | 0° | 8° |

◇ TSSOP8 3 x 3mm² Package size data

| Symb. | mm | | | inches | | |
|-------|-------|-------|-------|--------|--------|--------|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | - | - | 1.100 | - | - | 0.0433 |
| A1 | - | 0.050 | 0.150 | - | 0.0020 | 0.0059 |
| A2 | 0.850 | 0.750 | 0.950 | 0.0335 | 0.0295 | 0.0374 |
| b | - | 0.250 | 0.400 | - | 0.0098 | 0.0157 |
| c | - | 0.120 | 0.230 | - | 0.0047 | 0.0091 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | - | - | 0.0256 | - | - |
| E | 4.900 | 4.650 | 5.150 | 0.1929 | 0.1831 | 0.2028 |
| E1 | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| L | 0.550 | 0.400 | 0.700 | 0.0217 | 0.0157 | 0.0276 |
| L1 | 0.950 | - | - | 0.0374 | - | - |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| theta | - | 0° | 6° | - | 0° | 6° |

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