



**THE DATASHEET OF  
LP3944ISQX/NOPB**



## LP3944 RGB/White/Blue 8-LED Fun Light Driver

Check for Samples: [LP3944](#)

### FEATURES

- Internal Power-on Reset
- Active Low Reset
- Internal Precision Oscillator
- Variable Dim Rates (from 6.25 ms to 1.6s; 160 Hz–0.625 Hz)

### APPLICATIONS

- Customized Flashing LED Lights for Cellular Phones
- Portable Applications
- Digital Cameras
- Indicator Lamps
- General Purpose I/O Expander
- Toys

### KEY SPECIFICATIONS

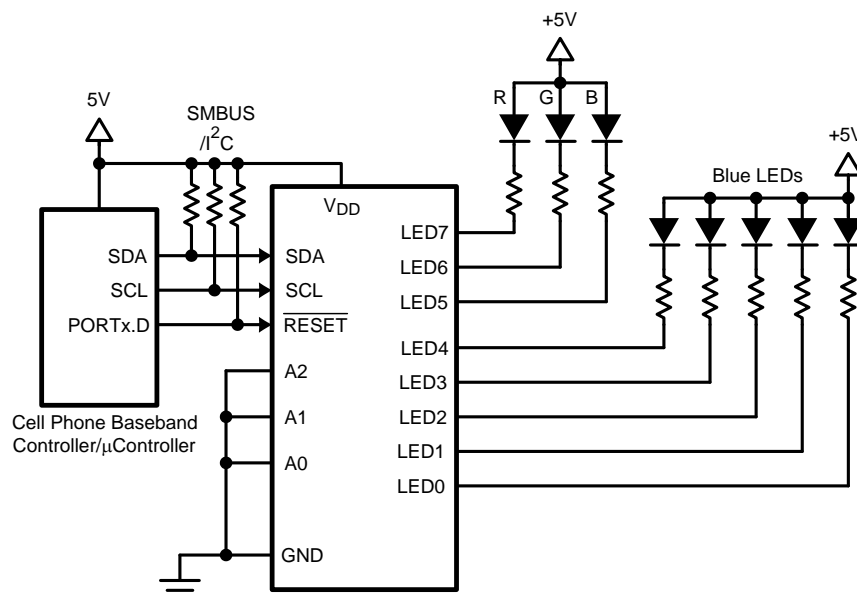
- 8 LED Driver (Multiple Programmable States—On, Off, Input, and Dimming at a Specified Rate)
- 8 Open Drain Outputs Capable of Driving up to 25 mA per LED

### DESCRIPTION

LP3944 is an integrated device capable of independently driving 8 LEDs. This device also contains an internal precision oscillator that provides all the necessary timing required for driving each LED. Two prescaler registers along with two PWM registers provide a versatile duty cycle control. The LP3944 contains the ability to dim LEDs in SMBUS/I<sup>2</sup>C applications where it is required to cut down on bus traffic.

Traditionally, to dim LEDs using a serial shift register such as 74LS594/5 would require a large amount of traffic to be on the serial bus. LP3944 instead requires only the setup of the frequency and duty cycle for each output pin. From then on, only a single command from the host is required to turn each individual open drain output ON, OFF, or to cycle a programmed frequency and duty cycle. Maximum output sink current is 25 mA per pin and 200 mA per package. Any ports not used for controlling the LEDs can be used for general purpose input/output expansion.

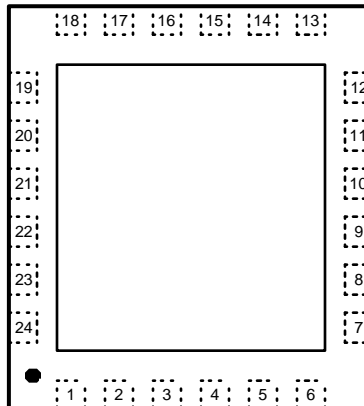
### Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**LP3944 Pin Out**

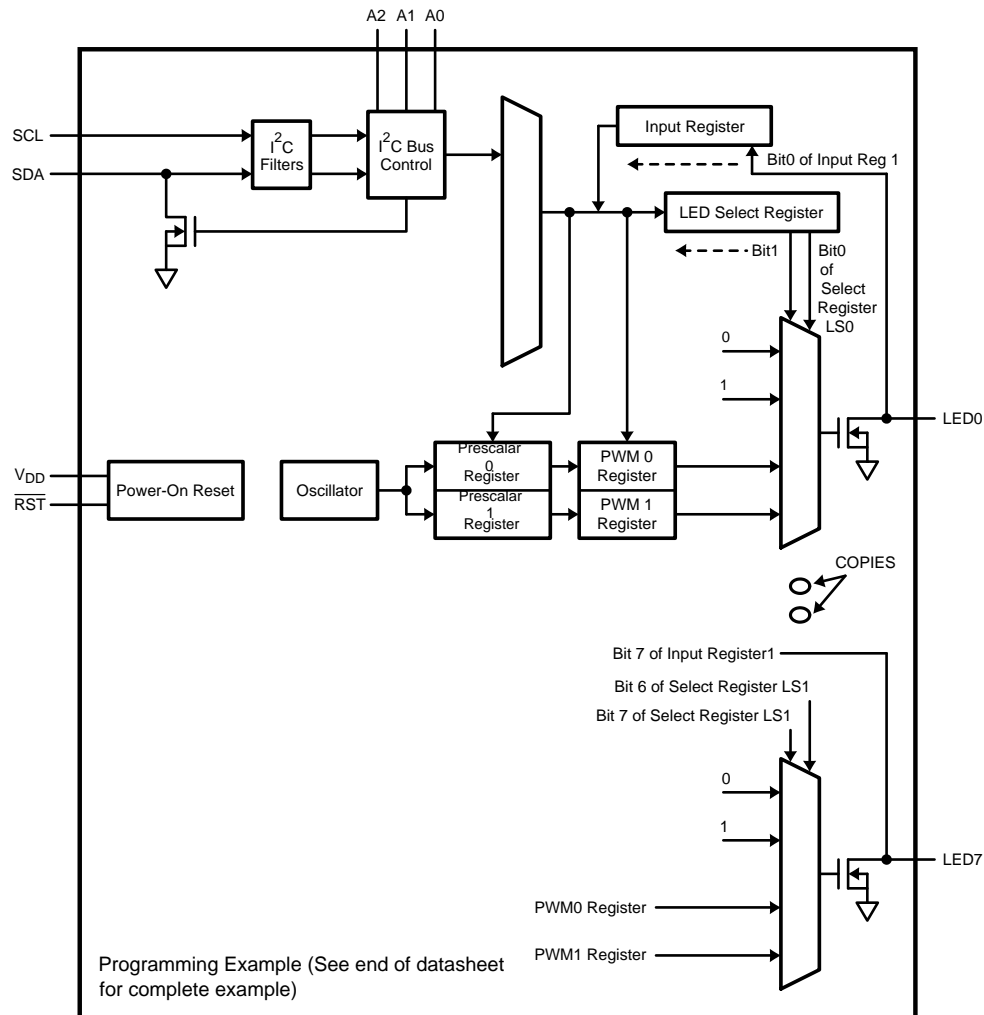


**Figure 1. (Top View)  
Package Number RTW0024A**

**LP3944 PIN DESCRIPTION**

Pin #	Name	Description
1	LED0	Output of LED0 Driver
2	LED1	Output of LED1 Driver
3	LED2	Output of LED2 Driver
4	LED3	Output of LED3 Driver
5	LED4	Output of LED4 Driver
6	LED5	Output of LED5 Driver
7	LED6	Output of LED6 Driver
8	LED7	Output of LED7 Driver
9	GND	Ground
10	NC	No Connect
11	NC	No Connect
12	NC	No Connect
13	NC	No Connect
14	NC	No Connect
15	NC	No Connect
16	NC	No Connect
17	NC	No Connect
18	$\overline{\text{RST}}$	Active Low Reset Input
19	SCL	Clock Line for I <sup>2</sup> C Interface
20	SDA	Serial Data Line for I <sup>2</sup> C Interface
21	V <sub>DD</sub>	Power Supply
22	A0	Address Input 0
23	A1	Address Input 1
24	A2	Address Input 2

### Architectural Block Diagram



For explanation of LP3944 operation, please refer to [Theory of Operation](#) in Application Notes.

**Figure 2. Block Diagram**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

V <sub>DD</sub>		-0.5V to 6V
A0, A1, A2, SCL, SDA, $\overline{\text{RST}}$ (Collectively called digital pins)		6V
Voltage on LED pins		V <sub>SS</sub> -0.5V to 6V
Junction Temperature		150°C
Storage Temperature		-65°C to 150°C
Power Dissipation <sup>(4)</sup>		1.76W
ESD <sup>(5)</sup>	Human Body Model	2 kV
	Machine Model	150V
	Charge Device Model	1 kV

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) If Military/Aerospace specified devices are required, please contact Texas Instruments for availability and specifications.
- (4) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula  $P = (T_J - T_A) / \theta_{JA}$ , where  $T_J$  is the junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance. The 1.76W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for  $T_J$ , 85°C for  $T_A$ , and 37°C/W for  $\theta_{JA}$ . More power can be dissipated safely at ambient temperature below 85°C. Less power can be dissipated safely at ambient temperatures above 85°C. The Absolute Maximum power dissipation can be increased by 27 mW for each degree below 85°C, and it must be de-rated by 27 mW for each degree above 85°C. For Operating Ratings maximum power dissipation,  $T_J = 125^\circ\text{C}$  and  $T_A = 85^\circ\text{C}$ .
- (5) The human-body model is 100 pF discharged through 1.5 k $\Omega$ . The machine model is 0 $\Omega$  in series with 220 pF.

### Operating Ratings<sup>(1)(2)</sup>

V <sub>DD</sub>		2.3V to 5.5V
Junction Temperature		-40°C to +125°C
Operating Ambient Temperature		-40°C to +85°C
Thermal Resistance ( $\theta_{JA}$ )	WQFN-24 <sup>(3)</sup>	37°C/W
Power Dissipation		1.08W

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula  $P = (T_J - T_A) / \theta_{JA}$ , where  $T_J$  is the junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance. The 1.76W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for  $T_J$ , 85°C for  $T_A$ , and 37°C/W for  $\theta_{JA}$ . More power can be dissipated safely at ambient temperature below 85°C. Less power can be dissipated safely at ambient temperatures above 85°C. The Absolute Maximum power dissipation can be increased by 27 mW for each degree below 85°C, and it must be de-rated by 27 mW for each degree above 85°C. For Operating Ratings maximum power dissipation,  $T_J = 125^\circ\text{C}$  and  $T_A = 85^\circ\text{C}$ .

## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 5.5V$ . Typical values and limits appearing in normal type apply for  $T_J = 25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40^\circ C$  to  $+125^\circ C$ .<sup>(1)</sup>

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
<b>POWER SUPPLY</b>						
$V_{DD}$	Supply Voltage		5	<b>2.3</b>	<b>5.5</b>	V
$I_Q$	Supply Current	No Load	350		<b>550</b>	$\mu A$
		Standby	2.0		<b>5</b>	
$\Delta I_Q$	Additional Standby Current	$V_{DD} = 5.5V$ , every LED pin at 4.3V			<b>2</b>	mA
$V_{POR}$	Power-On Reset Voltage		1.8		<b>1.96</b>	V
$t_w$	Reset Pulse Width		10			ns
<b>LED</b>						
$V_{IL}$	LOW Level Input Voltage			<b>-0.5</b>	<b>0.8</b>	V
$V_{IH}$	HIGH Level Input Voltage			<b>2.0</b>	<b>5.5</b>	V
$I_{OL}$	Low Level Output Current <sup>(2)</sup>	$V_{OL} = 0.4V$ , $V_{DD} = 2.3V$		<b>9</b>		mA
		$V_{OL} = 0.4V$ , $V_{DD} = 3.0V$		<b>12</b>		
		$V_{OL} = 0.4V$ , $V_{DD} = 5.0V$		<b>15</b>		
		$V_{OL} = 0.7V$ , $V_{DD} = 2.3V$		<b>15</b>		
		$V_{OL} = 0.7V$ , $V_{DD} = 3.0V$		<b>20</b>		
		$V_{OL} = 0.7V$ , $V_{DD} = 5.0V$		<b>25</b>		
$I_{LEAK}$	Input Leakage Current	$V_{DD} = 3.6$ , $V_{IN} = 0V$ or $V_{DD}$		<b>-1</b>	<b>1</b>	$\mu A$
$C_{I/O}$	Input/Output Capacitance	See <sup>(3)</sup>	2.6		<b>5</b>	pF
<b>ALL DIGITAL PINS (EXCEPT SCL AND SDA PINS)</b>						
$V_{IL}$	LOW Level Input Voltage			<b>-0.5</b>	<b>0.8</b>	V
$V_{IH}$	HIGH Level Input Voltage			<b>2.0</b>	<b>5.5</b>	V
$I_{LEAK}$	Input Leakage Current			<b>-1</b>	<b>1</b>	$\mu A$
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$ <sup>(3)</sup>	2.3		<b>5</b>	pF
<b>I<sup>2</sup>C INTERFACE (SCL AND SDA PINS)</b>						
$V_{IL}$	LOW Level Input Voltage			<b>-0.5</b>	<b><math>0.3V_{DD}</math></b>	V
$V_{IH}$	HIGH Level Input Voltage			<b><math>0.7V_{DD}</math></b>	<b>5.5</b>	V
$V_{OL}$	LOW Level Output Voltage			<b>0</b>	<b><math>0.2V_{DD}</math></b>	V
$I_{OL}$	LOW Level Output Current	$V_{OL} = 0.4V$	6.5	<b>3</b>		mA
$F_{CLK}$	Clock Frequency	See <sup>(3)</sup>			<b>400</b>	kHz
$t_{HOLD}$	Hold Time Repeated START Condition	See <sup>(3)</sup>		<b>0.6</b>		$\mu s$
$t_{CLK-LP}$	CLK Low Period	See <sup>(3)</sup>		<b>1.3</b>		$\mu s$
$t_{CLK-HP}$	CLK High Period	See <sup>(3)</sup>		<b>0.6</b>		$\mu s$
$t_{SU}$	Set-Up Time Repeated START Condition	See <sup>(3)</sup>		<b>0.6</b>		$\mu s$
$t_{DATA-HOLD}$	Data Hold Time	See <sup>(3)</sup>		<b>300</b>		ns
$t_{DATA-SU}$	Data Set-Up Time	See <sup>(3)</sup>		<b>100</b>		ns
$t_{SU}$	Set-Up Time for STOP Condition	See <sup>(3)</sup>		<b>0.6</b>		$\mu s$
$t_{TRANS}$	Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA & CLK Signals	See <sup>(3)</sup>	50			ns

(1) Limits are ensured. All electrical characteristics having room-temperature limits are tested during production with  $T_J = 25^\circ C$ . All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) Each LED pin should not exceed 25 mA and the package should not exceed a total of 200 mA.

(3) Ensured by design.

### Typical Performance Characteristics

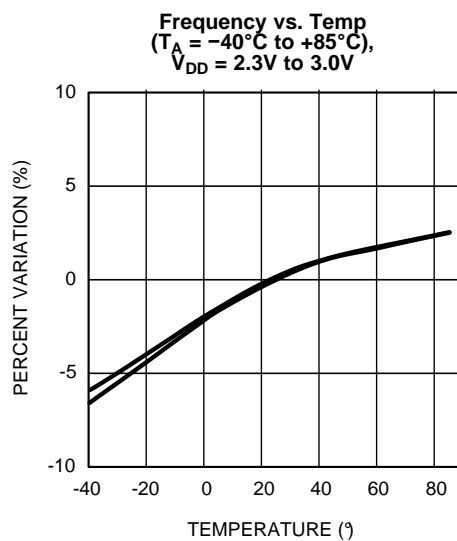


Figure 3.

## APPLICATION INFORMATION

### Theory of Operation

The LP3944 takes incoming data and feed them into several registers that control the frequency and the duty cycle of the LEDs. Two prescaler registers and two PWM registers provide two individual rates to dim or blink the LEDs (for more information on these registers, refer to [Table 1](#)). The baseband controller/microprocessor can program each LED to be in one of four states—on, off, DIM0 rate or DIM1 rate. One read-only registers provide status on all 8 LEDs. The LP3944 can be used to drive RGB LEDs and/or single-color LEDs to create a colorful, entertaining, and informative setting. This is particularly suitable for accessory functions in cellular phones and toys. Any LED pins not used to drive LED can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The LP3944 is equipped with Power-On Reset that holds the chip in a reset state until  $V_{DD}$  reaches  $V_{POR}$  during power up. Once  $V_{POR}$  is achieved, the LP3944 comes out of reset and initializes itself to the default state.

To bring the LP3944 into reset, hold the  $\overline{RST}$  pin LOW for a period of  $TW$ . This will put the chip to its default state. The LP3944 can only be programmed after  $\overline{RST}$  signal is HIGH again.

### I<sup>2</sup>C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

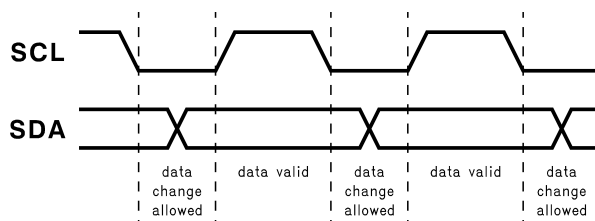


Figure 4. I<sup>2</sup>C Data Validity

### I<sup>2</sup>C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

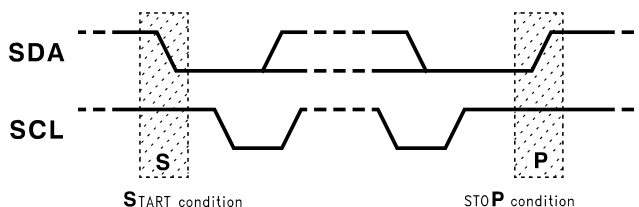


Figure 5. I<sup>2</sup>C START and STOP Conditions

### Transferring Data

Every byte put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I<sup>2</sup>C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3944 hardwires bits 7 to 4 and leaves bits 3 to 1 selectable, as shown in Figure 6. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The LP3944 supports only a WRITE during chip addressing. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

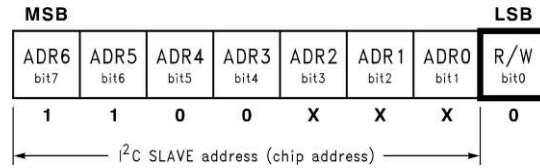
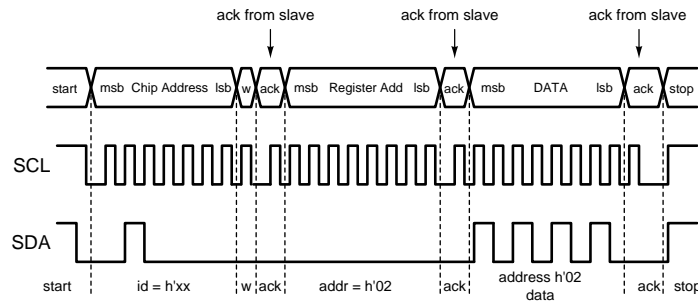


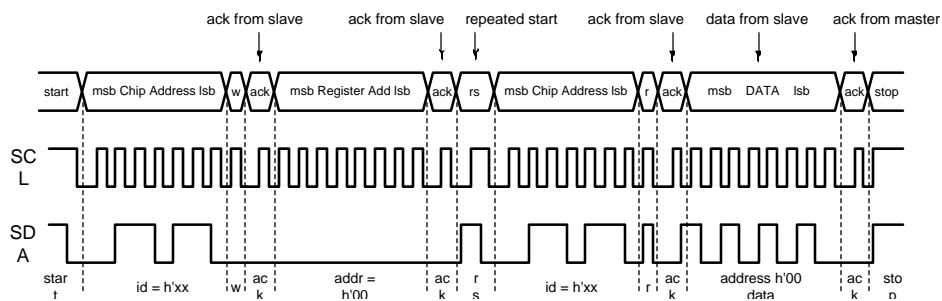
Figure 6. Chip Address Byte



w = write (SDA = “0”)  
 r = read (SDA = “1”)  
 ack = acknowledge (SDA pulled down by either master or slave)  
 rs = repeated start  
 xx = 60 to 67

Figure 7. LP3944 Register Write

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 8.



w = write (SDA = “0”)  
 r = read (SDA = “1”)  
 ack = acknowledge (SDA pulled down by either master or slave)  
 rs = repeated start  
 xx = 60 to 67

Figure 8. LP3944 Register Read

### Auto Increment

Auto increment is a special feature supported by the LP3944 to eliminate repeated chip and register addressing when data are to be written to or read from registers in sequential order. The auto increment bit is inside the register address byte, as shown in Figure 9. Auto increment is enabled when this bit is programmed to “1” and disabled when it is programmed to “0”.

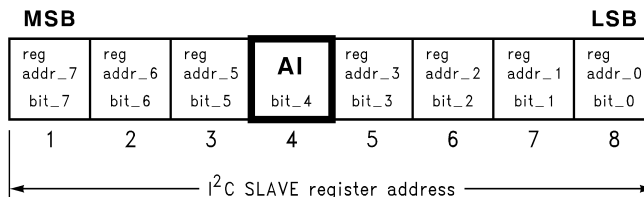


Figure 9. Register Address Byte

In the READ mode, when auto increment is enabled, I<sup>2</sup>C master could receive any number of bytes from LP3944 without selecting chip address and register address again. Every time the I<sup>2</sup>C master reads a register, the LP3944 will increment the register address and the next data register will be read. When I<sup>2</sup>C master reaches the last register (09H register), the register address will roll over to 00H.

In the WRITE mode, when auto increment is enabled, the LP3944 will increment the register address every time I<sup>2</sup>C master writes to register. When the last register (09H register) is reached, the register address will roll over to 02H, because the first two registers in LP3944 are read-only registers. It is possible to write to these two registers, and the LP3944 will acknowledge, but the data will be ignored.

In the LP3944, registers 0x01, 0x08 and 0x09 are not functional. However, it is still necessary to read from 0x01 and to write to 0x08 and 0x09 in Auto Increment mode. They cannot be skipped.

If auto increment is disabled, and the I<sup>2</sup>C master does not change register address, it will continue to write data into the same register.

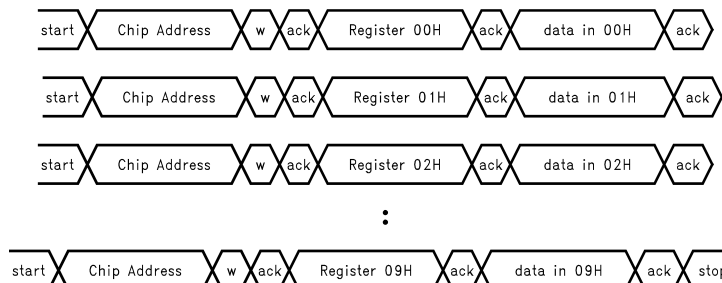


Figure 10. Programming with Auto Increment Disabled (in WRITE Mode)

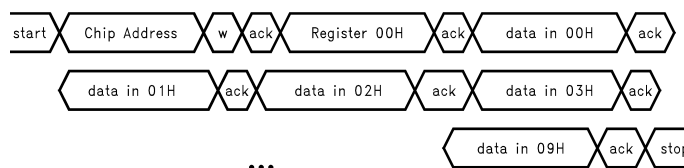


Figure 11. Programming with Auto Increment Enabled (in WRITE Mode)

**Table 1. LP3944 Register Table<sup>(1)</sup>**

Address (Hex)	Register Name	Read/Write	Register Function
0x00	Input 1	Read Only	LED0–7 Input Register
0x01	Register 1	Read Only	None
0x02	PSC0	R/W	Frequency Prescaler 0
0x03	PWM0	R/W	PWM Register 0
0x04	PSC1	R/W	Frequency Prescaler 1
0x05	PWM1	R/W	PWM Register 1
0x06	LS0	R/W	LED0–3 Selector
0x07	LS1	R/W	LED4–7 Selector
0x08	Register 8	R/W	None
0x09	Register 9	R/W	None

(1) Note: Registers 1, 8 and 9 are empty and non-functional registers. Register 1 is read-only, with all bits hard-wired to zero. Registers 8 and 9 can be written and read, but the content does not have any effect on the operation of the LP3944.

### Binary Format for Input Registers (Read Only)—Address 0x00 and 0x01

**Table 2. Address 0x00<sup>(1)</sup>**

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

(1) X = don't care

### Binary Format for Frequency Prescaler and PWM Registers — Address 0x02 to 0x05

**Table 3. Address 0x02 (PSC0)<sup>(1)</sup>**

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

(1) PSC0 register is used to program the period of DIM0.  
 $DIM0 = (PSC0+1)/160$   
 The maximum period is 1.6s when PSC0 = 255.

**Table 4. Address 0x03 (PWM0)<sup>(1)</sup>**

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

(1) PWM0 register determines the duty cycle of DIM0. The LED outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 0x00, LED output is always HIGH (LED off).

The duty cycle of DIM0 is:  $PWM0/256$   
 Default value is 50% duty cycle.

**Table 5. Address 0x04 (PSC1)<sup>(1)</sup>**

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

(1) PSC1 register is used to program the period of DIM1.  
 $DIM1 = (PSC1 + 1)/160$   
 The maximum period is 1.6s when PSC1 = 255.

**Table 6. Address 0x05 (PWM1)<sup>(1)</sup>**

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

(1) PWM1 register determines the duty cycle of DIM1. The LED outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 0x00, LED output is always HIGH (LED off).

The duty cycle of DIM1 is:  $PWM1/256$   
 Default value is 50% duty cycle.

**Binary Format for Selector Registers — Address 0x06 to 0x07** [Table 7](#)
**Table 7. Address 0x06 (LS0)**

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED3		LED2		LED1		LED0	

**Table 8. Address 0x07 (LS1)**

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED7		LED6		LED5		LED4	

**Table 9. LED States With Respect To Values in "B1" and "B0"**

B1	B0	Function
0	0	Output Hi-Z (LED off)
0	1	Output LOW (LED on)
1	0	Output dims (DIM0 rate)
1	1	Output dims (DIM1 rate)

**Programming Example:**

Dim LEDs 0 to 7 at 1 Hz at 25% duty cycle

1. Set PSC0 to achieve DIM0 of 1s
2. Set PWM0 duty cycle to 25%
3. Set PSC1 to achieve DIM1 of 0.2s
4. Set LEDs 0 to 7 to point to DIM0

Step	Description	Register Name	Set to (Hex)
1	Set DIM0 = 1s $1 = (PSC0 + 1)/160$ PSC0 = 159	PSC0	0x09F
2	Set duty cycle to 25% Duty Cycle = $PWM0/256$ PWM0 = 64	PWM0	0x40
3	Set DIM1 = 0.2s $0.2 = (PSC1 + 1)/160$ PSC1 = 31	PSC1	0x1F
4	LEDs 0 to 7 Output = DIM0	LS0, LS1	LS0 = 0xAA LS1 = 0xAA

### Reducing $I_Q$ When LEDs are Off

In many applications, the LEDs and the LP3944 share the same  $V_{DD}$ , as shown in [Typical Application Circuit](#). When the LEDs are off, the LED pins are at a lower potential than  $V_{DD}$ , causing extra supply current ( $\Delta I_Q$ ). To minimize this current, consider keeping the LED pins at a voltage equal to or greater than  $V_{DD}$ .

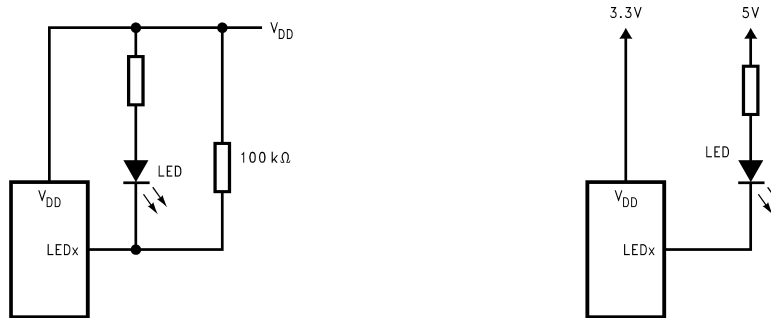


Figure 12. Methods to Reduce  $I_Q$  When LEDs Are Off

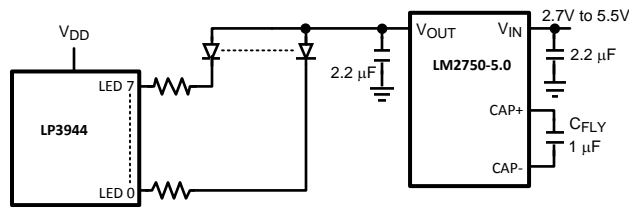


Figure 13. Application Circuit

---

**REVISION HISTORY**

<b>Changes from Original (April 2013) to Revision A</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">12</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3944ISQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	3944SQ	<a href="#">Samples</a>
LP3944ISQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	3944SQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

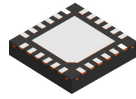
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3944ISQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3944ISQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3944ISQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LP3944ISQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

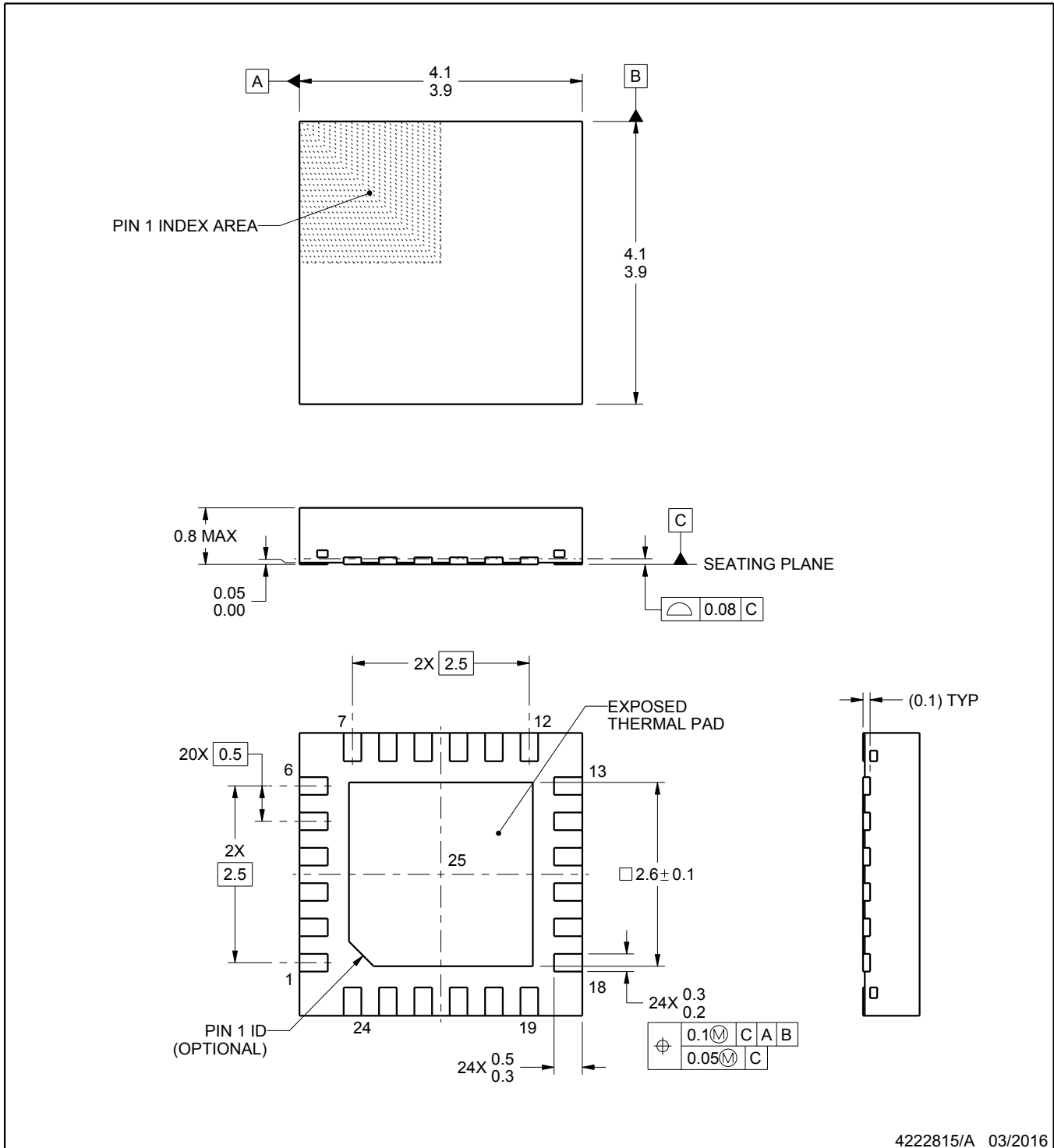
RTW0024A



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222815/A 03/2016

NOTES:

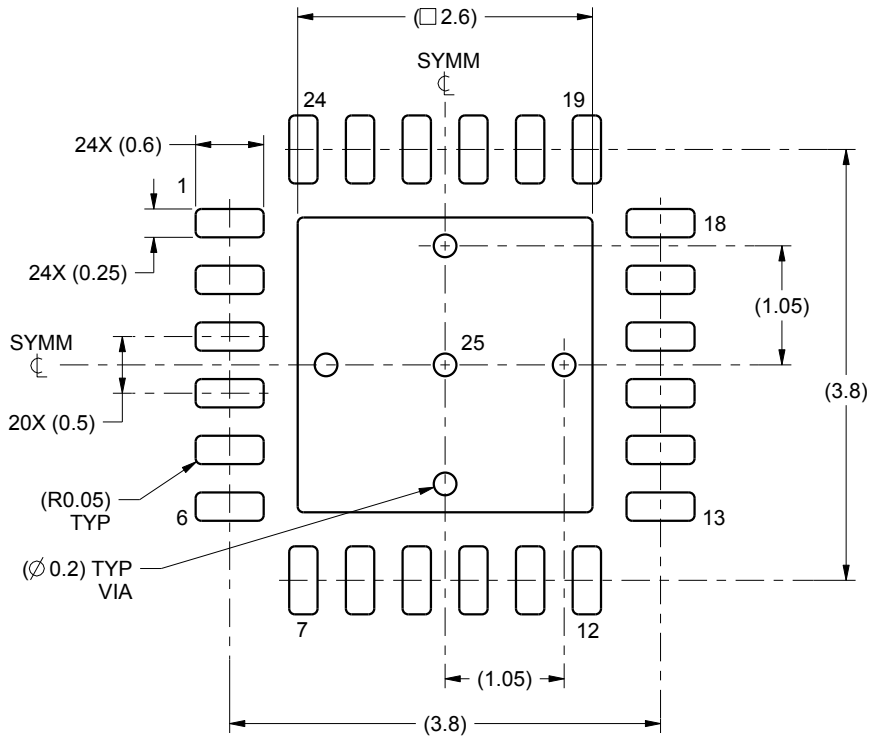
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

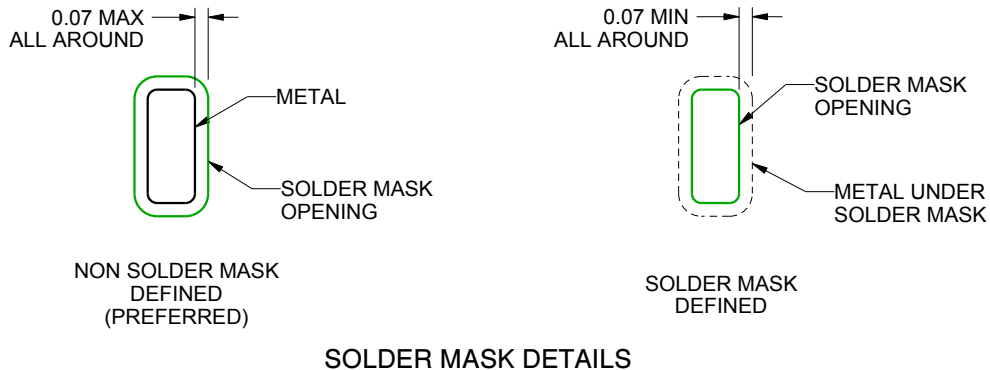
RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

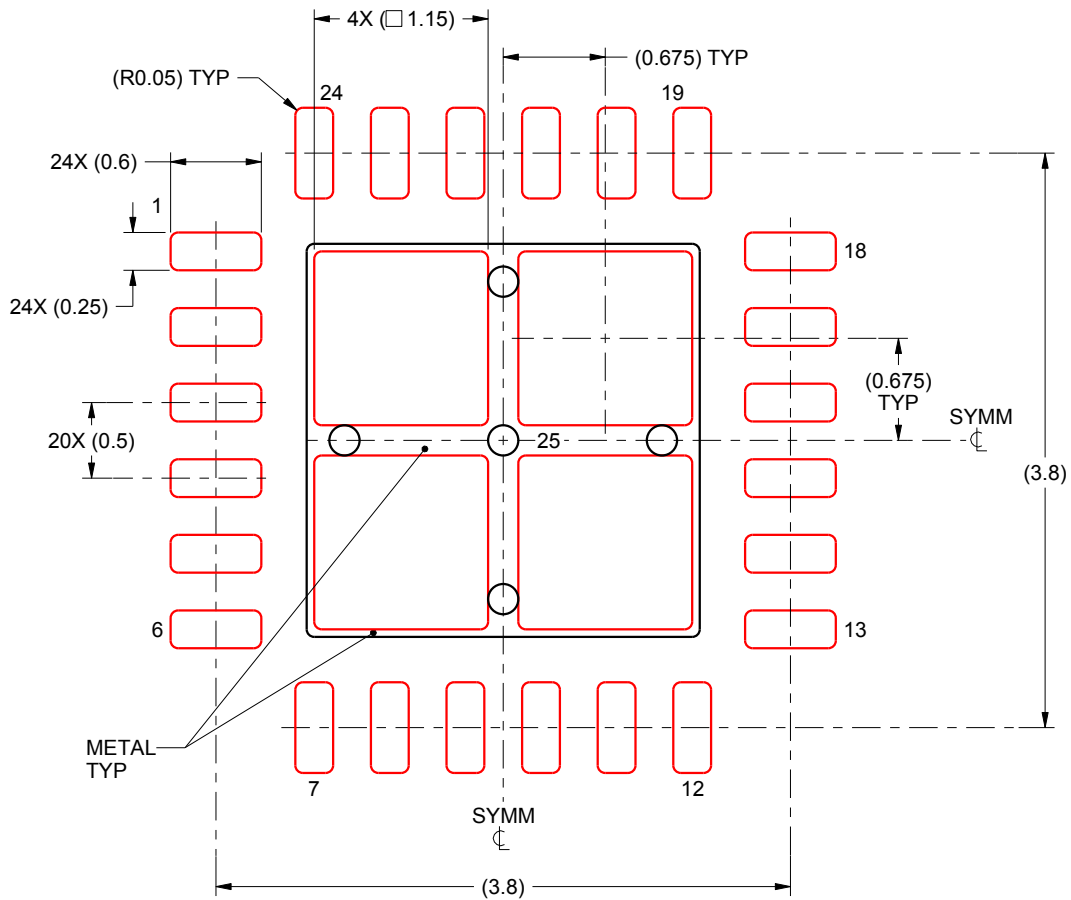
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LP3944ISQX/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management