THE DATASHEET OF

LMC555CM/NOPB

www.win-source.net 0086-755-83957316

LMC555 CMOS Timer

1 Features

- Industry's Fastest Astable Frequency of 3 MHz
- Available in Industry's Smallest 8-Bump DSBGA Package (1.43mm × 1.41mm)
- Less Than 1 mW Typical Power Dissipation at 5 V Supply
- 1.5 V Supply Operating Voltage Ensured
- Output Fully Compatible With TTL and CMOS Logic at 5 V Supply
- Tested to −10 mA, 50 mA Output Current Levels
- Reduced Supply Current Spikes During Output Transitions
- Extremely Low Reset, Trigger, and Threshold Currents
- Excellent Temperature Stability
- Pin-for-Pin Compatible With 555 Series of Timers

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generators

3 Description

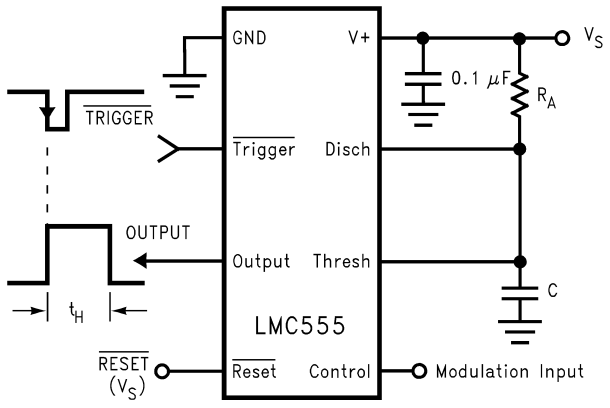
The LMC555 device is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard package (SOIC, VSSSOP, and PDIP) the LMC555 is also available in a chip-sized package (8-bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of TI's LMCMOS process extends both the frequency range and the low supply capability.

Device Information(1)

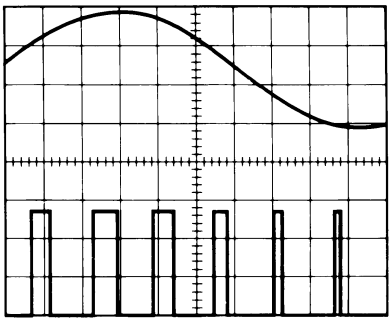
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC555	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm
	DSBGA (8)	1.43 mm × 1.41 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pulse Width Modulator



Pulse Width Modulator Waveform:
Top Waveform - Modulation
Bottom Waveform - Output Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision L (February 2016) to Revision M — **Page**

- Changed order of Features list. ... 1
- Changed stable to astable - typo. ... 1
- Changed stable to astable - typo. ... 7
- Changed beings to begins typo. ... 8
- Changed typo LM555 to LMC555. ... 12
- Changed typo LM555 to LMC555. ... 12
- Added additional applications. ... 14

Changes from Revision K (January 2015) to Revision L — **Page**

- Changed typo - temp range from 185 to 85 ... 4

Changes from Revision J (March 2013) to Revision K — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision I (March 2013) to Revision J — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 17

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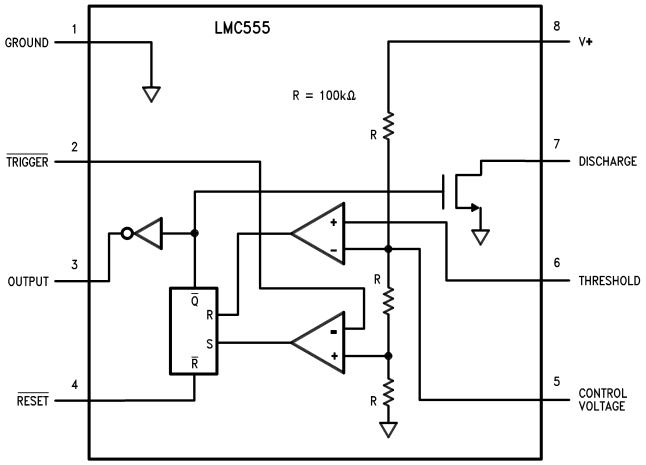
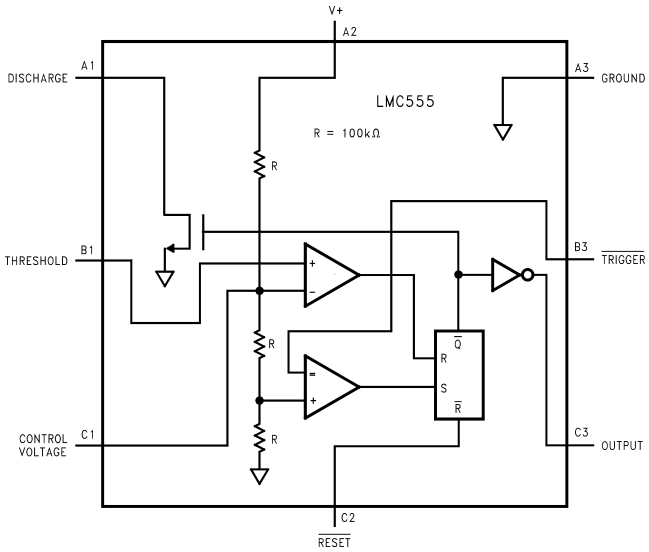
5 Pin Configuration and Functions

D, DGK, and P Packages
8-Pin SOIC, VSSOP, and PDIP
(Top View)



YPB Package
8-Pin DSBGA
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
SOIC, VSSOP, and PDIP NO.	DSBGA NO.	NAME		
1	A3	GND	O	Ground reference voltage
2	B3	$\overline{\text{Trigger}}$	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin
3	C3	Output	O	Output driven waveform
4	C2	$\overline{\text{Reset}}$	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering
5	C1	Control Voltage	I	Control voltage controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform
6	B1	Threshold	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop.
7	A1	Discharge	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage
8	A2	V^+	I	Supply voltage with respect to GND

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)(2)(3)

		MIN	MAX	UNIT
Voltage	Supply		15	V
	Input	–0.3	(V+) + 0.3	V
	Output		15	V
Curent	Output		100	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See AN-1112 (SNVA009) for DSBGA considerations.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature Range	LMC555IM	−40		125	°C
	LMC555CM/MM/N/TP	−40		85	°C
Maximum Allowable Power Dissipation at 25°C	PDIP-8			1126	mW
	SOIC-8			740	mW
	VSSOP-8			555	mW
	8-bump DSBGA			568	mW

6.4 Thermal Information

THERMAL METRIC(1)		LMC555				UNIT
		SOIC	VSSOP	PDIP	8-BUMP DSBGA	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169	225	111	220	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Supply Current	V_S = 1.5 V V_S = 5 V V_S = 12 V		50 100 150	150 250 400	µA
V_{CTRL}	Control Voltage	V_S = 1.5 V V_S = 5 V V_S = 12 V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V_{DIS}	Discharge Saturation Voltage	V_S = 1.5 V, I_{DIS} = 1 mA V_S = 5 V, I_{DIS} = 10 mA		75 150	150 300	mV
V_{OL}	Output Voltage (Low)	V_S = 1.5 V, I_O = 1 mA V_S = 5 V, I_O = 8 mA V_S = 12 V, I_O = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
V_{OH}	Output Voltage (High)	V_S = 1.5 V, I_O = −0.25 mA V_S = 5 V, I_O = −2 mA V_S = 12 V, I_O = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V_{TRIG}	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I_{TRIG}	Trigger Current	V_S = 5V		10		pA
V_{RES}	Reset Voltage	V_S = 1.5 V (2) V_S = 12 V	0.4 0.4	0.7 0.75	1.0 1.1	V
I_{RES}	Reset Current	V_S = 5 V		10		pA
I_{THRESH}	Threshold Current	V_S = 5 V		10		pA
I_{DIS}	Discharge Leakage	V_S = 12 V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5 V V_S = 5 V V_S = 12 V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
$\Delta t/\Delta V_S$	Timing Shift with Supply	V_S = 5V ± 1 V		0.3%		V
$\Delta t/\Delta T$	Timing Shift with Temperature	V_S = 5 V		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed, V_S = 12 V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5 V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5 V, Measure Delay from Trigger to Output		100		ns

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0 V or greater.

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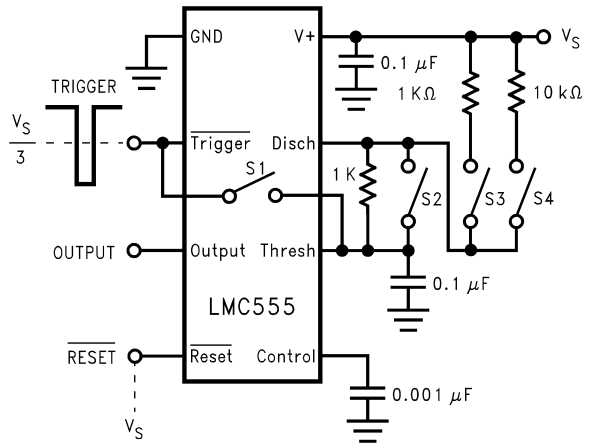
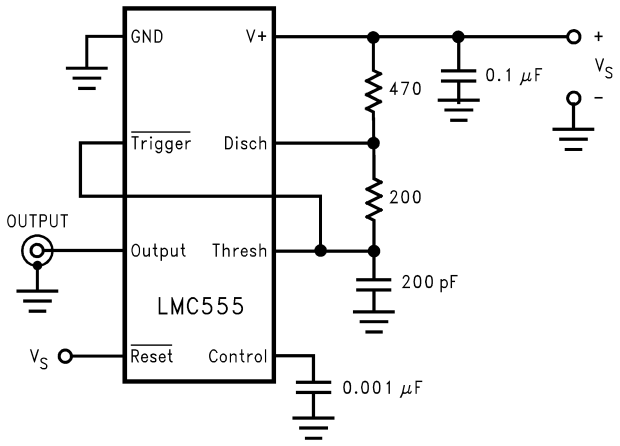
7 Parameter Measurement Information



For device pinout, see *Pin Configuration and Functions*.

Figure 1. Test Circuit



For device pinout, see *Pin Configuration and Functions*.

Figure 2. Maximum Frequency Test Circuit

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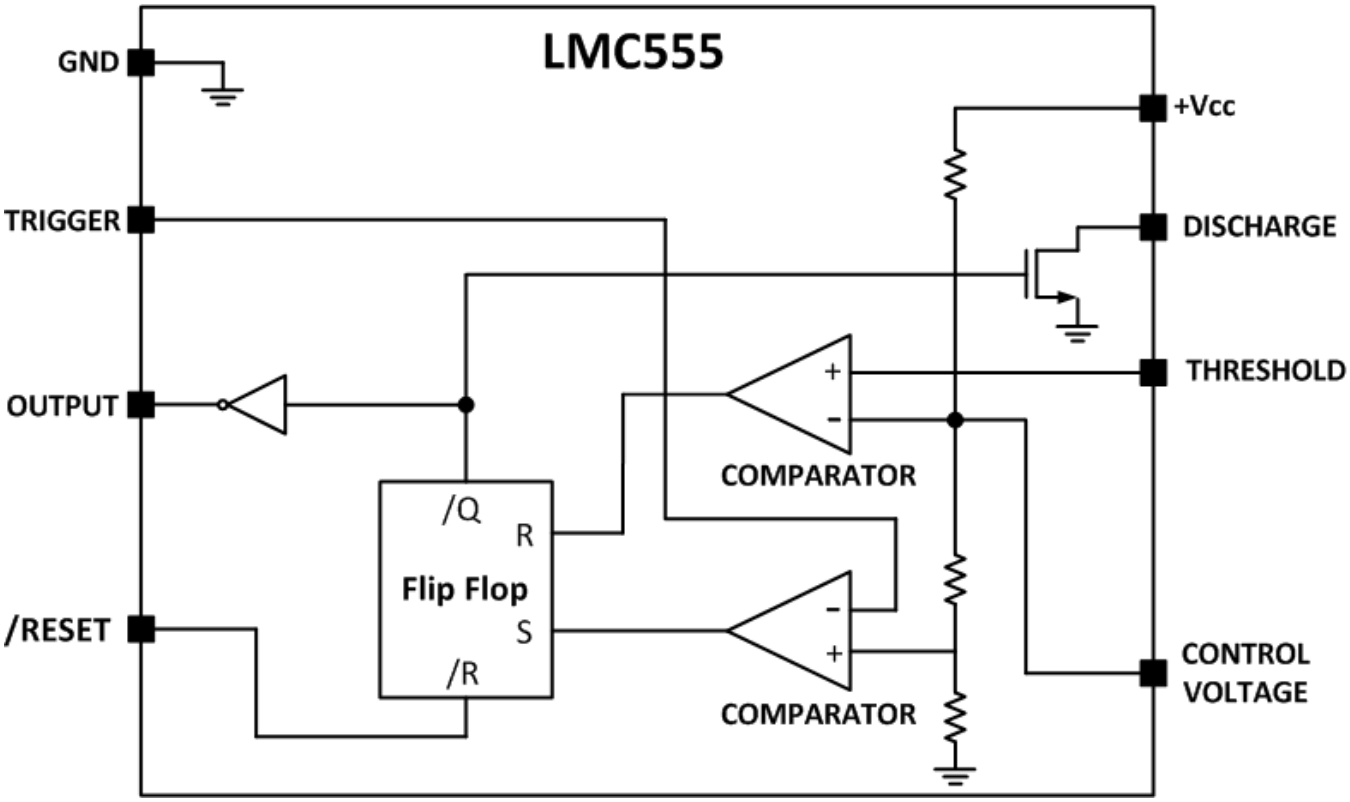
8 Detailed Description

8.1 Overview

The LMC555 is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard package (SOIC, VSSSOP, and PDIP) the LMC555 is also available in a chip-sized package (8-bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of TI's LMCMOS process extends both the frequency range and the low supply capability. The LMC555 is available in an 8-pin PDIP, SOIC, VSSOP, and 8-bump DSBGA package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low-Power Dissipation

The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation. A power dissipation of less than 0.2 mW can be achieved with a 1.5-V operating supply voltage and less than 1 mW with a 5-V operating supply voltage. The use of TI's LMCMOS process allows this low supply current and voltage capability. Reduced supply current spikes during output transitions and extremely low reset, trigger and threshold currents also provide low power dissipation advantages with the LMC555.

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Feature Description (continued)

8.3.2 Various Packages and Compatibility

There are various packages available for use of the LMC555. In addition to the standard package (8-pin SOIC, VSSOP, and PDIP, the LMC555 is also available in a chip-sized package (8-bump DSBGA). The PDIP, SOIC, and VSSOP packages for the LMC555 are pin-for-pin compatible with the 555 series of timers (NE555/SE555/LM555) allowing flexibility in design and unnecessary modifications to PCB schematics and layouts.

8.3.3 Operates in Both Astable and Monostable Mode

The LMC555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LMC555 timer acts as a “one-shot” pulse generator. The pulse begins when the LMC555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.
- Astable (free-running) mode: The LMC555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of RA, RB, and C.

8.4 Device Functional Modes

8.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 3). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 V_S to the $\overline{\text{Trigger}}$ terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

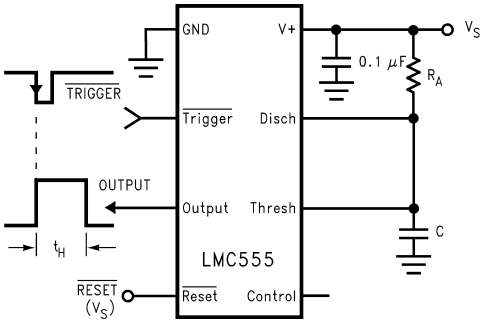

Figure 3. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of $t_H = 1.1\ R_AC$, which is also the time that the output stays high, at the end of which time the voltage equals 2/3 V_S. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 4 shows the waveforms generated in this mode of operation. Because the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

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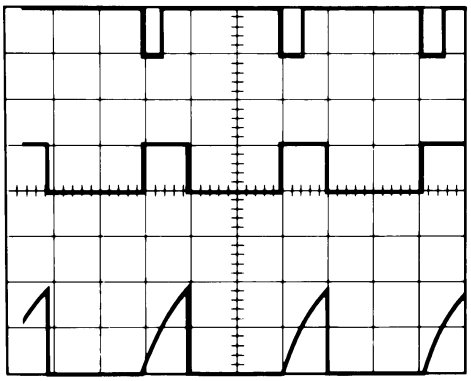
Device Functional Modes (continued)



V_{CC} = 5 V
TIME = 0.1 ms/Div.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 5 V/Div.
Middle Trace: Output 5 V/Div.
Bottom Trace: Capacitor Voltage 2 V/Div.

Figure 4. Monostable Waveforms

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired t_H. The minimum pulse width for the Trigger is 20 ns, and it is 400 ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to V_+ to avoid any possibility of false triggering. Figure 5 is a nomograph for easy determination of RC values for various time delays.

NOTE

In monstable operation, the trigger should be driven high before the end of timing cycle.

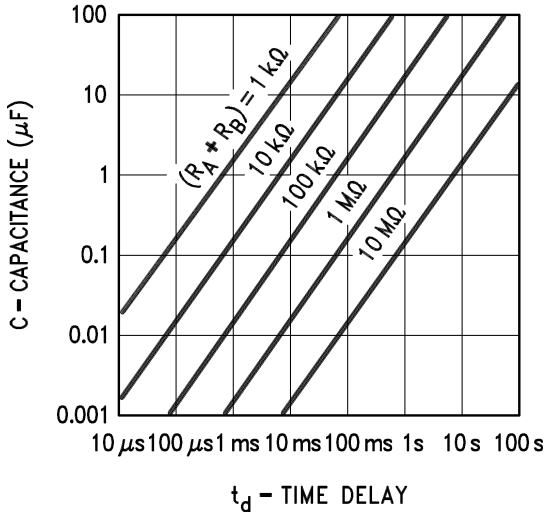


Figure 5. Time Delay

Device Functional Modes (continued)

8.4.2 Astable Operation

If the circuit is connected as shown in Figure 6 ($\overline{\text{Trigger}}$ and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

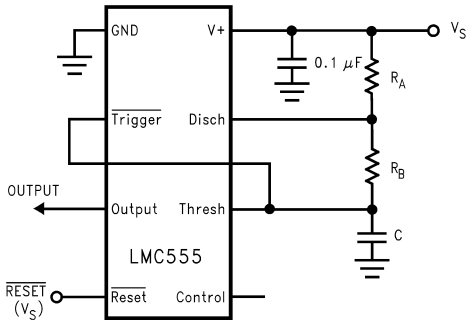
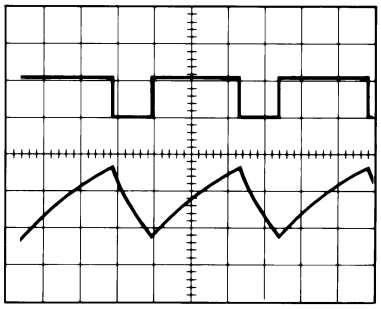


Figure 6. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V_S and 2/3 V_S. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 7 shows the waveform generated in this mode of operation.



V_{CC} = 5 V
TIME = 20 µs/Div.
R_A = 3.9 kΩ
R_B = 9 kΩ
C = 0.01 µF

Top Trace: Output 5 V/Div.
Bottom Trace: Capacitor Voltage 1 V/Div.

Figure 7. Astable Waveforms

The charge time (output high) is given by

$$t_1 = 0.693\ (R_A + R_B)C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

Figure 8 may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

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Device Functional Modes (continued)

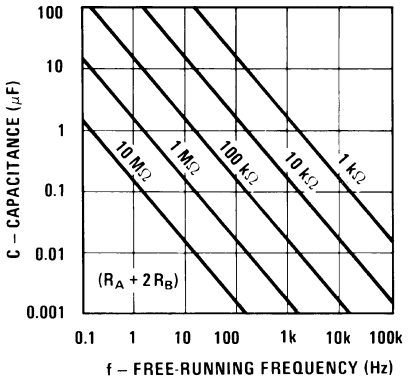

Figure 8. Free-Running Frequency

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMC555 timer can be used a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LMC555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

9.2 Typical Application

Figure 9 shows the schematic of the LM555 that flashes an LED in monostable mode.

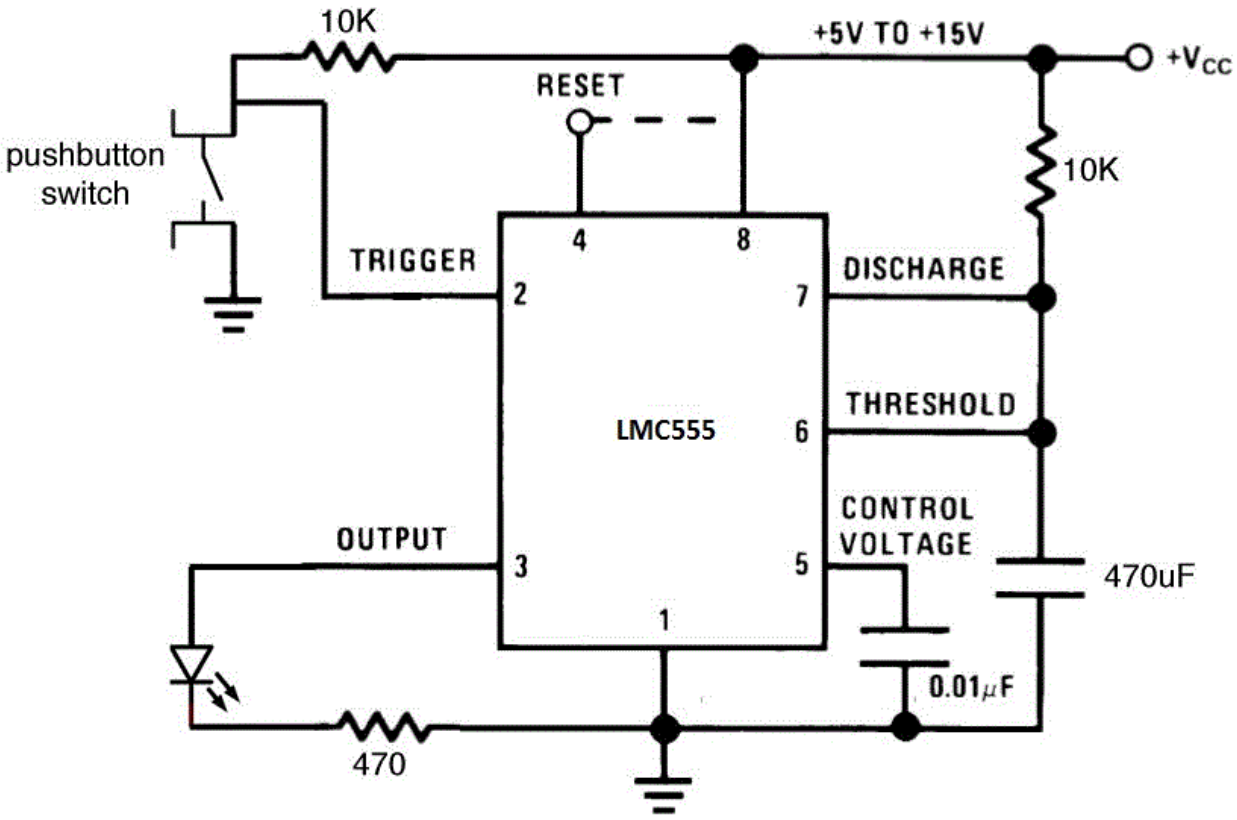

Figure 9. Schematic of Monostable Mode to Flash an LED

9.2.1 Design Requirements

The main design requirement for this application requires calculating the duration of time for which the output stays high. The duration of time is dependent on the R and C values (as shown in monostable figure) and can be calculated by: t= 1.1*R*C seconds.

$$t = 1.1 \times R \times C \quad (6)$$

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Typical Application (continued)

9.2.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5-second time delay was chosen for this application. By using the equation:

$$t = 1.1 \times R \times C \text{ seconds} \quad (7)$$

where

- RC equals 4.545

If R is chosen as 100 kΩ, C = 45.4 µF. The values of R = 100 kΩ and C = 47 µF was chosen based on standard values of resistors and capacitors.

A momentary push button switch connected to ground is connected to the trigger input with a 10-kΩ current limiting resistor pull up to the supply voltage. When the push button is pressed, the trigger pin goes to GND. An LED is connected to the output pin with a current limiting resistor in series from the output of the LMC555 to GND. The reset pin is not used and was connected to the supply voltage.

9.2.3 Application Curve

The data shown in Figure 10 was collected with the circuit used in the typical applications section. The LM555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Blue) – Capacitor voltage
- Middle Waveform (Purple) – Trigger
- Bottom Waveform (Green) – Output

As the trigger pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 seconds.

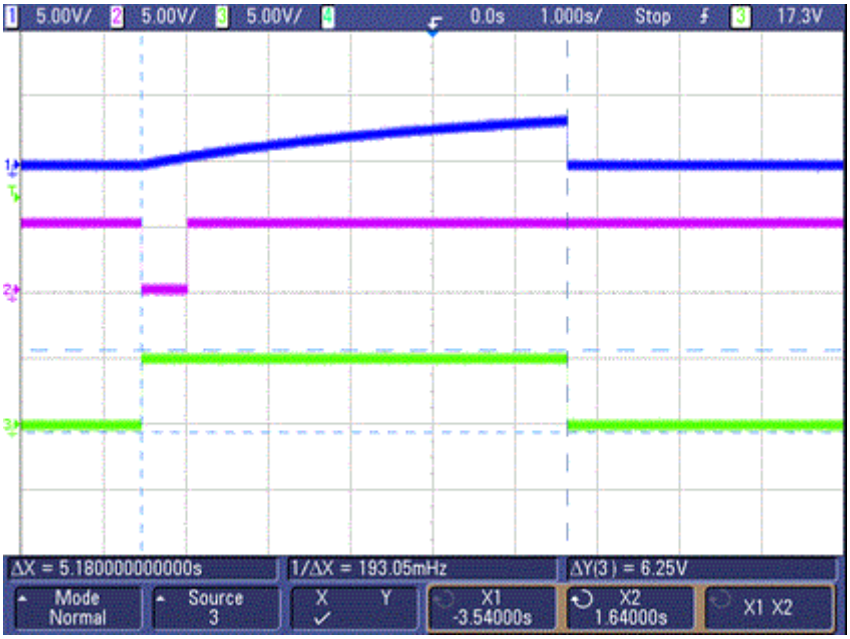

Figure 10. Trigger, Capacitor Voltage, and Output Waveforms in Monostable Mode

9.3 Frequency Divider

The monostable circuit of Figure 11 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 12 shows the waveforms generated in a divide by three circuit.

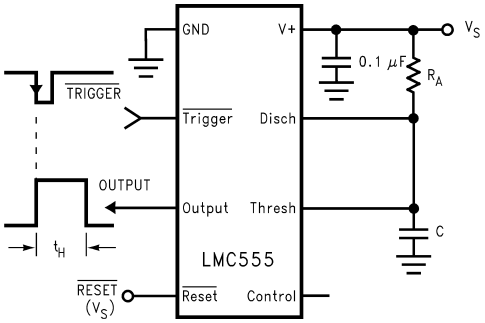

Figure 11. Monostable (One-Shot)

9.3.1 Design Requirements

Design a frequency divider by adjusting the length of the timing cycle.

9.3.2 Application Curve

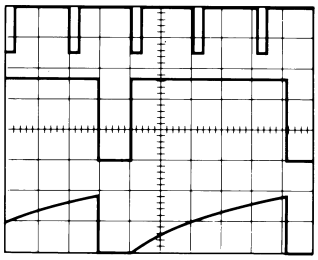

Figure 12. Frequency Divider Waveforms

9.4 Pulse Width Modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the control voltage terminal. Figure 13 shows the circuit, and in Figure 14 are some waveform examples.

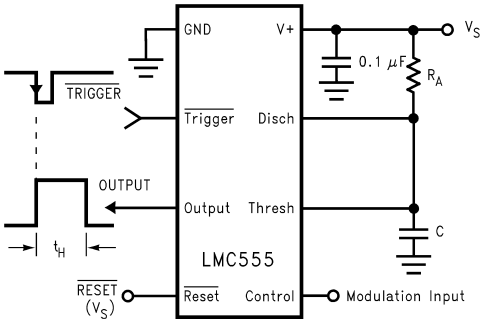

Figure 13. Pulse Width Modulator

9.4.1 Design Requirements

Modulator the output pulse width by the signal applied to the control voltage terminal.

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Pulse Width Modulator (continued)

9.4.2 Application Curve

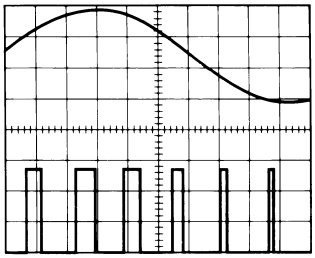

Figure 14. Pulse Width Modulator Waveforms

9.5 Pulse Position Modulator

This application uses the timer connected for astable operation, as in Figure 15, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 16 shows the waveforms generated for a triangle wave modulation signal.

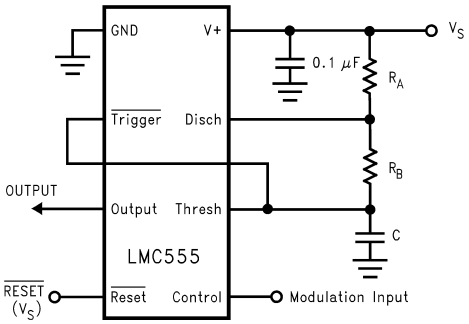

Figure 15. Pulse Position Modulator

9.5.1 Design Requirements

Using astable operation vary the pulse position with a modulating signal applied to the control voltage terminal.

9.5.2 Application Curve

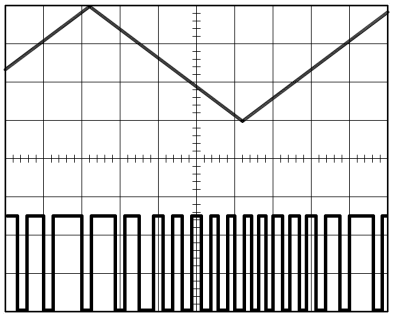

Figure 16. Pulse Position Modulator Waveforms

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9.6 50% Duty Cycle Oscillator

The frequency of oscillation is:

$f = 1/(1.4\ R_C C)$ (8)

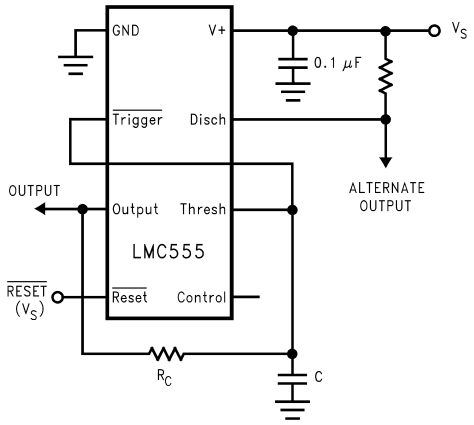

Figure 17. 50% Duty Cycle Oscillator

9.6.1 Design Requirements

An oscillator with a 50% duty cycle output.

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10 Power Supply Recommendations

The LM555 requires a voltage supply within 1.5 V to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 µF in parallel with 1-µF electrolytic. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

11 Layout

11.1 Layout Guidelines

Standard PCB rules apply to routing the LMC555. The 0.1 µF in parallel with a 1-µF electrolytic capacitor should be as close as possible to the LMC555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

11.2 Layout Example

The figure below is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01 µF bypass capacitor for control voltage pin
- C3 – 0.1 µF bypass ceramic capacitor
- C4 – 1-µF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

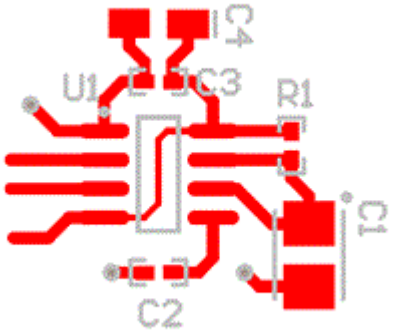

Figure 18. PCB Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC555CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC 555CM	
LMC555CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC 555CM	Samples
LMC555CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	ZC5	
LMC555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZC5	Samples
LMC555CMMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	ZC5	
LMC555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZC5	Samples
LMC555CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC 555CM	
LMC555CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC 555CM	Samples
LMC555CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LMC 555CN	Samples
LMC555CTP/NOPB	ACTIVE	DSBGA	YPB	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02	Samples
LMC555CTPX/NOPB	ACTIVE	DSBGA	YPB	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02	Samples
LMC555IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMC 555IM	Samples
LMC555IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMC 555IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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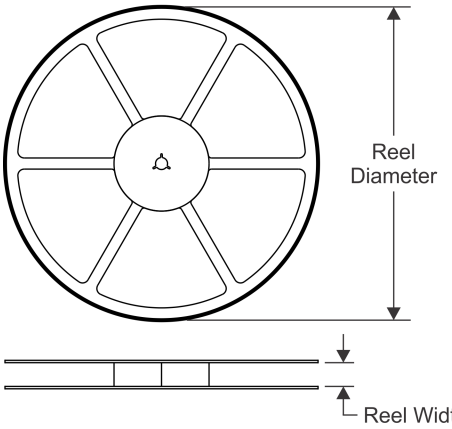
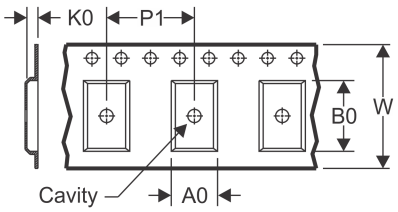
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

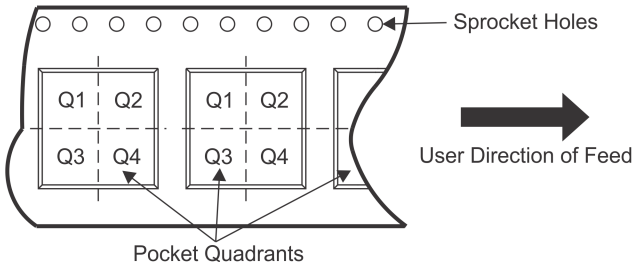


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

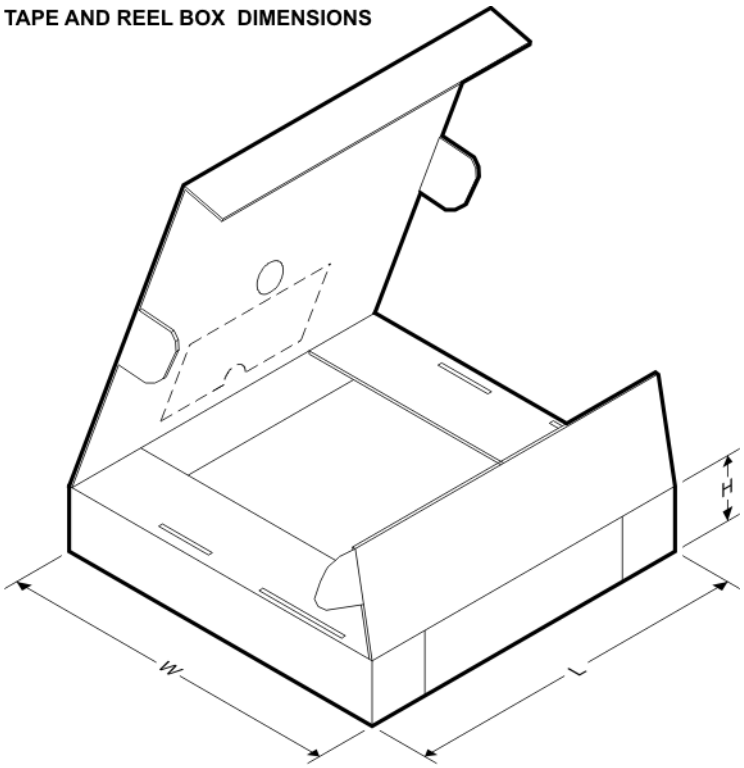
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

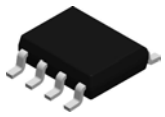
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC555CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC555CTP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC555CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC555CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC555CMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CTP/NOPB	DSBGA	YPB	8	250	210.0	185.0	35.0
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	210.0	185.0	35.0
LMC555IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

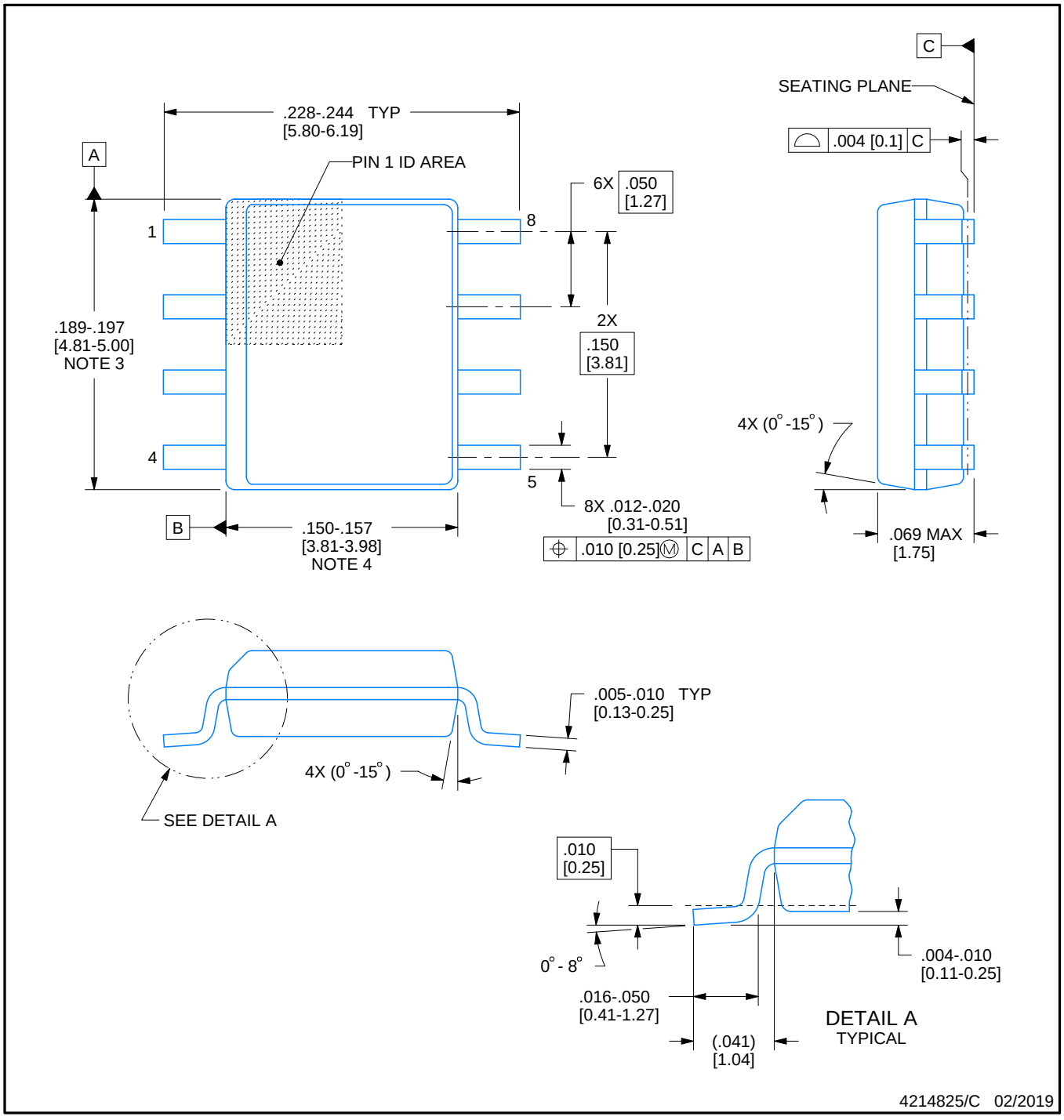


PACKAGE OUTLINE

D0008A

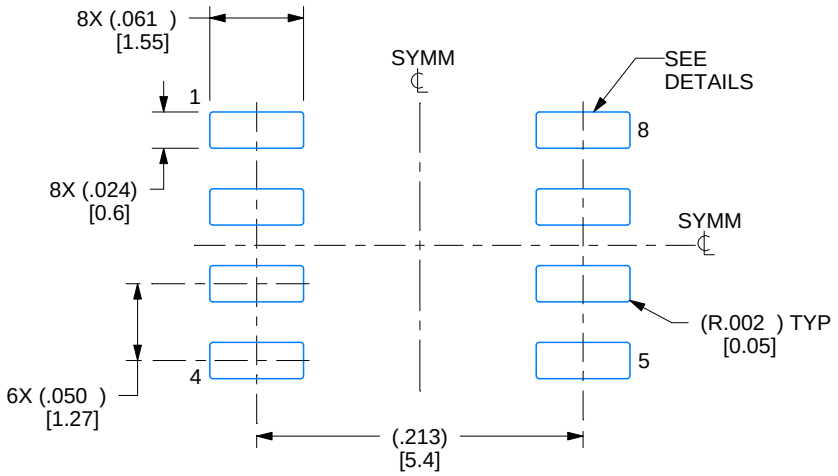
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

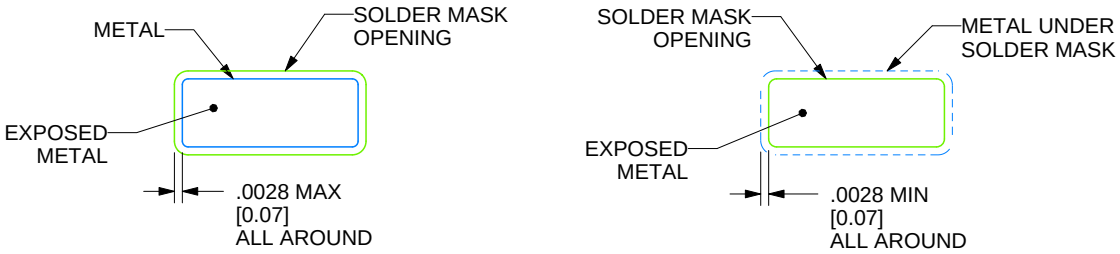


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

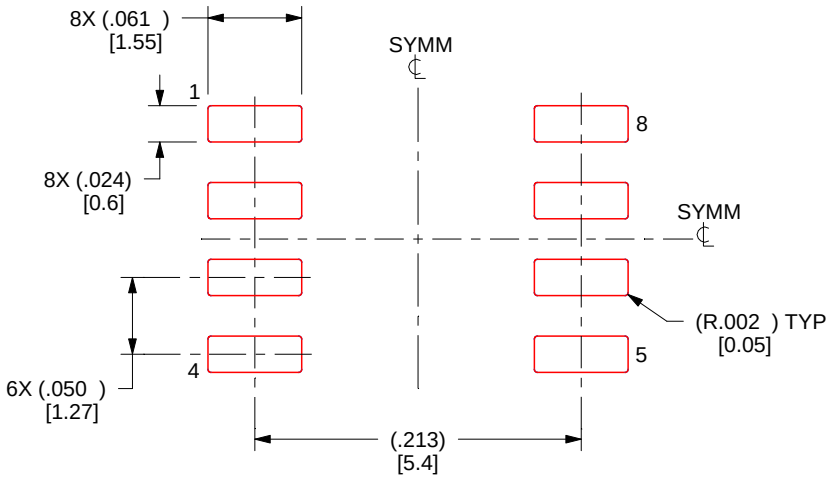
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



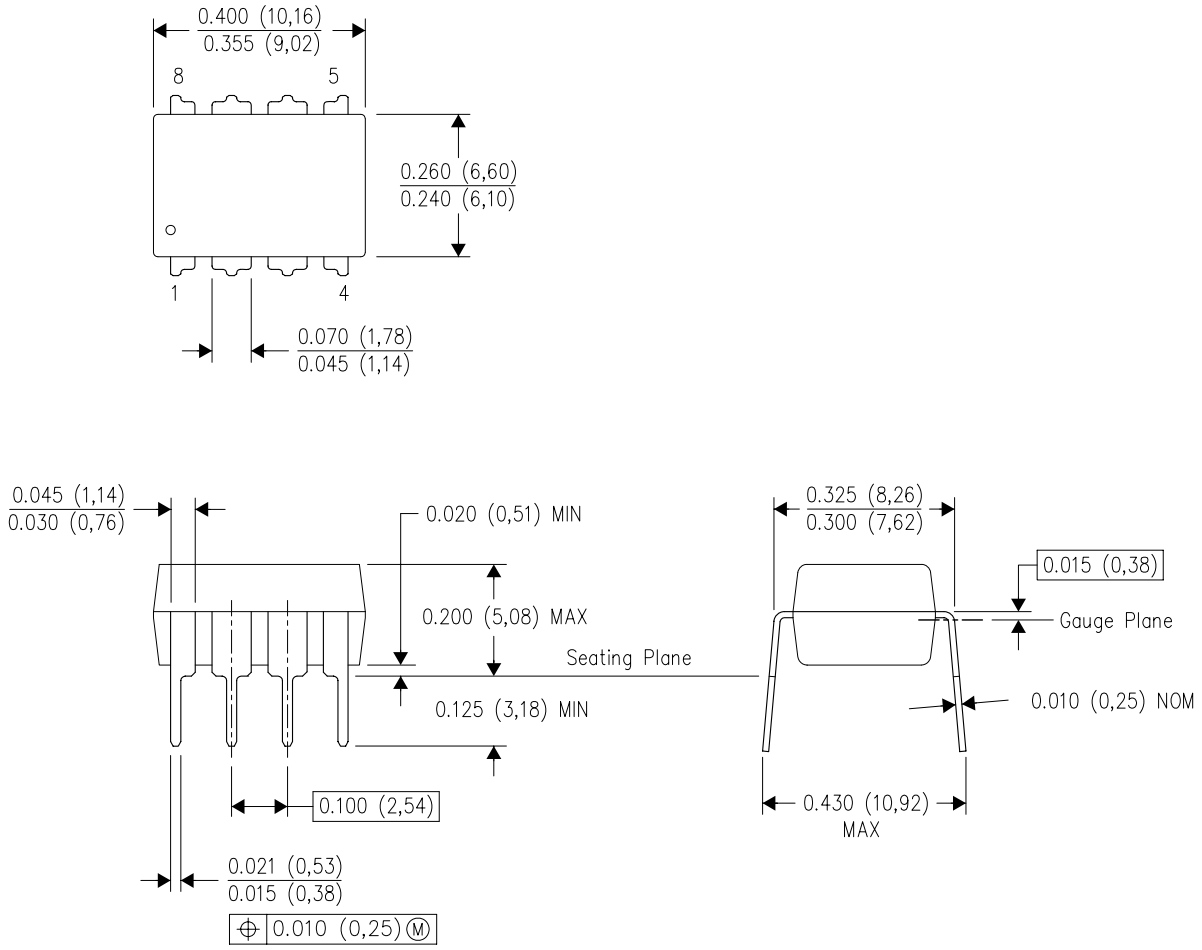
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

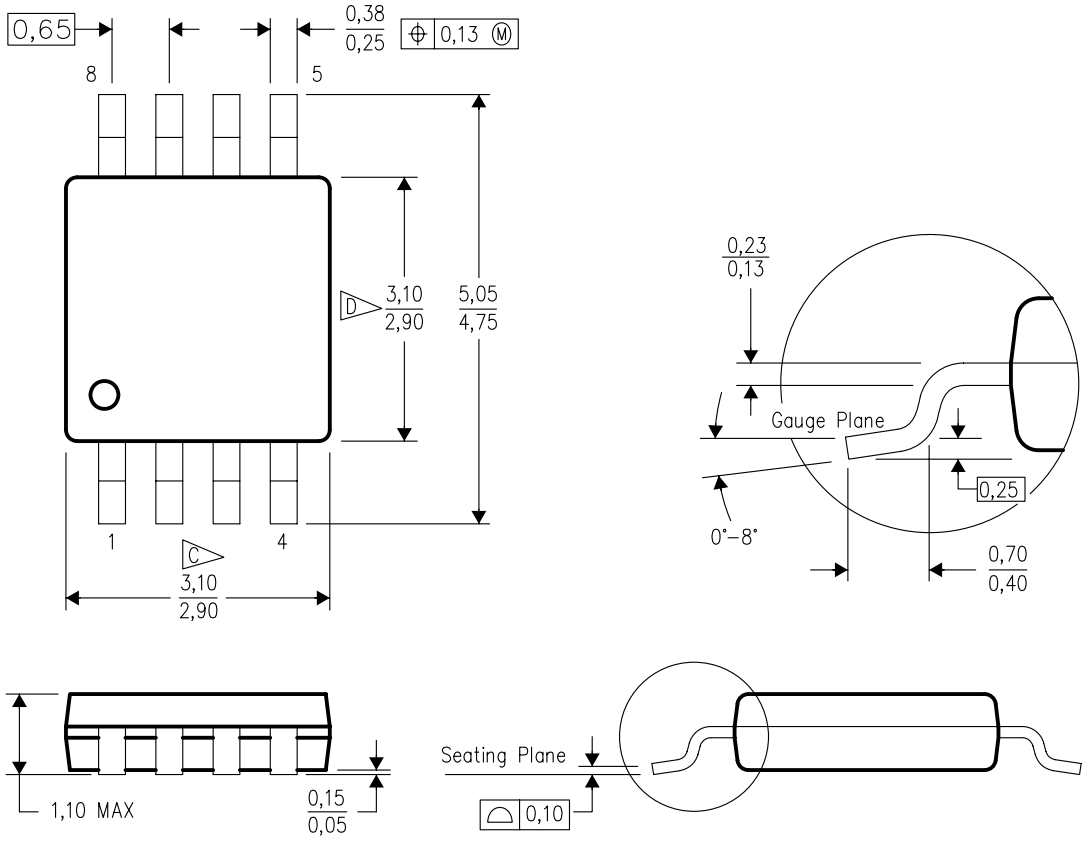
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

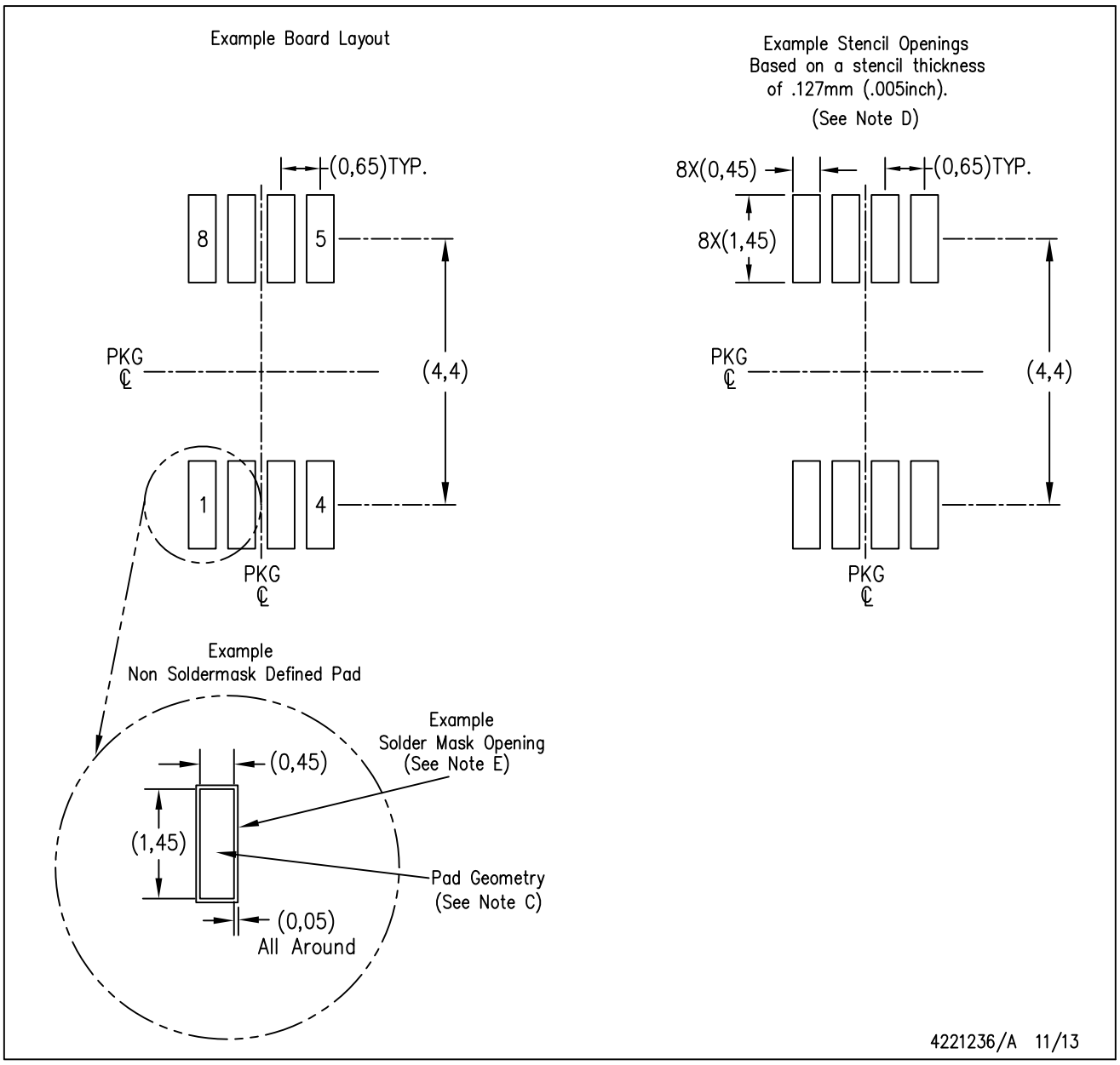
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



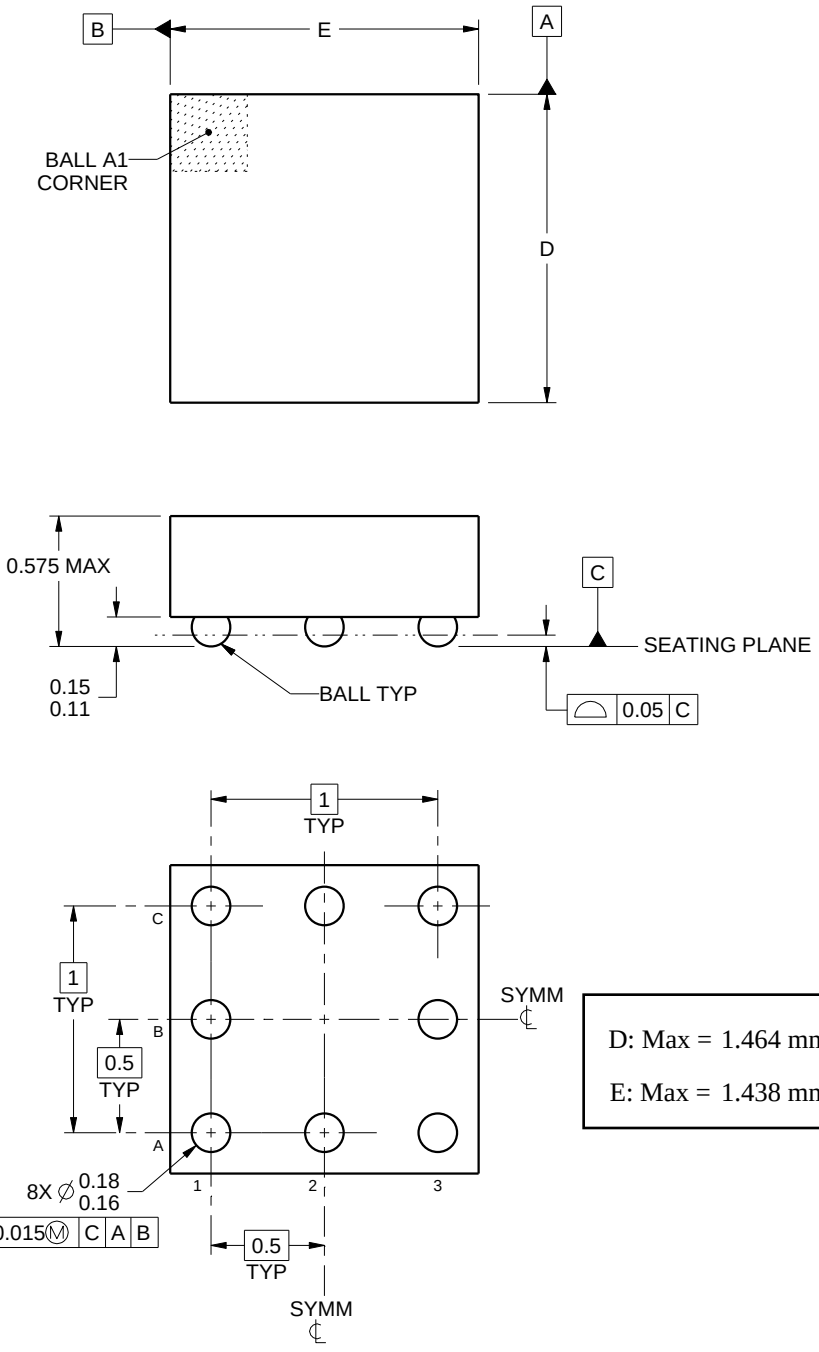
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

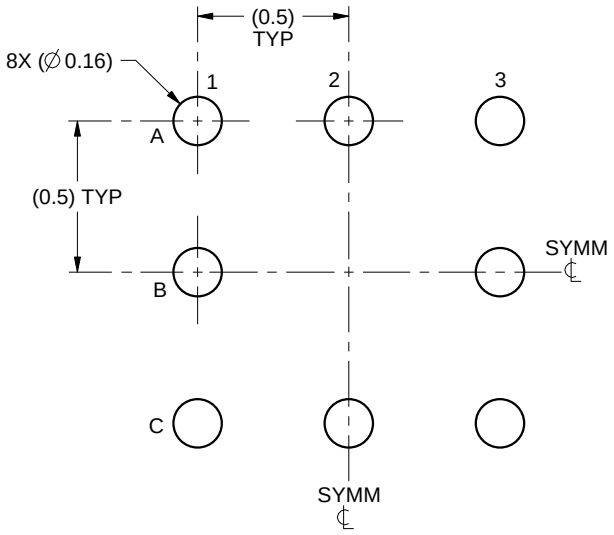
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

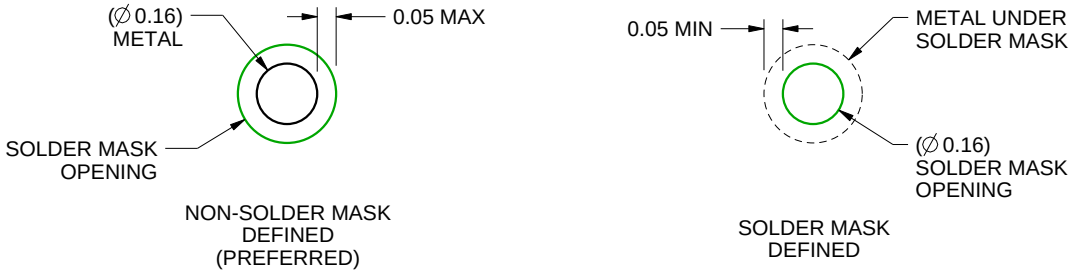
YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X

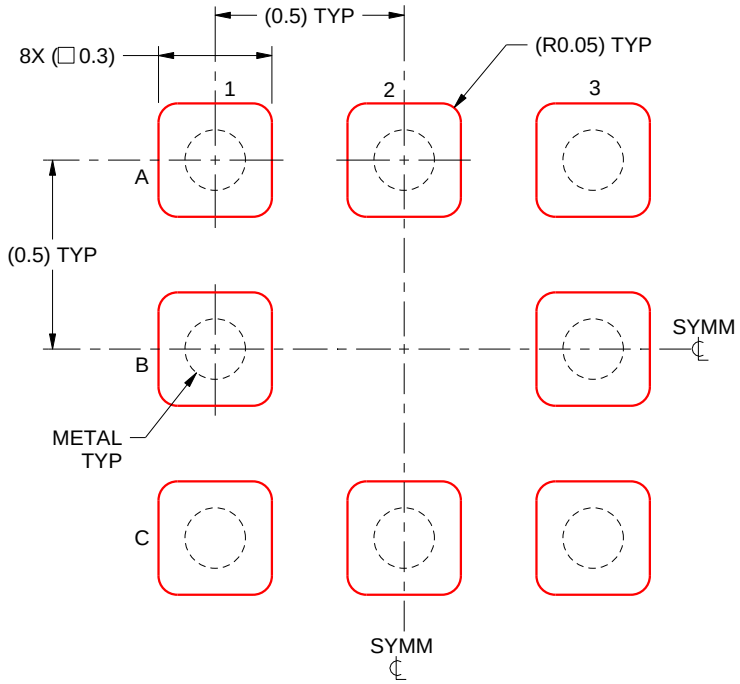


SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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