THE DATASHEET OF

TPS23851DCER

Quad IEEE 802.3at Power-Over-Ethernet PSE Controller

Check for Samples: TPS23851

FEATURES

- **INDUSTRY STANDARD PSE**
  - **Fully IEEE Std 802.3at-2009 Compliant**
  - **Four Independent PSE Ports**
    - **PD Detection and Classification**
    - **Current Limit Output Protection with Foldback for Reduced Cost FET**
    - **AC and DC Disconnect Detection**
  - **I²C™ Communication**
    - **4 Bit Address for 64-Port Systems**
  - **Flexible Operation Modes**
    - **Automatic**
    - **Semi Automatic**
    - **Processor Controlled**
  - **Pin Compatible with LTC4259A and MAX5952, MAX5945, MAX5935**
- **ENHANCED FEATURES**
  - ***Never Fooled* 4-Point Detection**
  - **Onboard Precision 110-Hz AC Disconnect Sine Wave Oscillator**
  - **I²C Watchdog for Failsafe Operation**
  - **Individual and Multiplexed Port Shutdown Modes**
  - **Per Port A/D Converters**
    - **14-Bit Resolution for Precision Measurements**
    - **Real-time Voltage Monitoring**
    - **Real-time Current Monitoring**
    - **Inherent Filtering**
  - **Extended -20°C to 125°C Temperature Operation**
  - **802.3at Type 2 Mode**
    - **High-Power Mode**
    - **Classification through Link Layer Discovery Protocol (LLDP)**
  - **Available in 36-lead SSOP Package**

APPLICATIONS

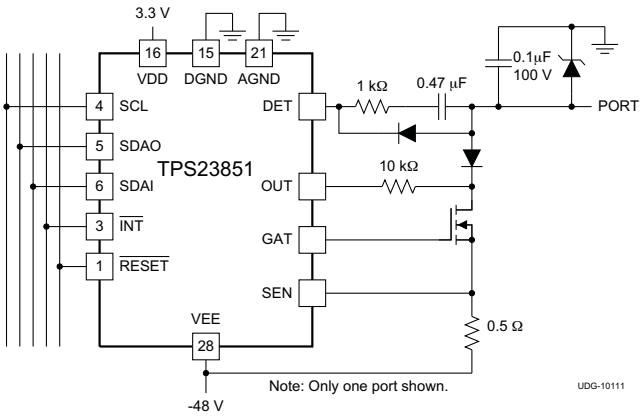
- **Ethernet Switches and Routers**

DESCRIPTION

The TPS23851 is a quad-power controller engineered to insert power onto Ethernet cable according to IEEE Std 802.3at-2009 (or 802.3at) for Power Sourcing Equipment (PSE). The PSE controller can detect Powered devices (PDs) that have a valid signature, determine the power requirements of the devices according to the classification, and apply power to the devices, limited per 802.3at. Based on an industry standard register set, the PSE controller is software compatible with other PSE controllers for basic functionality

Beyond the industry standard operation, the TPS23851 operates with enhanced features. Port current trip point can be set to all classification thresholds of IEEE Std 802.3-2005 (or 802.3af) and can be programmed up to more than 720 mA when used with a LLDP classification stack, complying with 802.3at. The TPS23851 supports AC and DC disconnection with a precision on-chip, 110-Hz oscillator for AC waveform generation. The PSE also contains four 14-bit A/D converters that constantly monitor voltage and current on each port. This information is available on the I²C bus for power management. The unique converter integrating topology used in the TPS23851 provides inherent filtering for a robust solution.

Typical Application



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

T_J	PACKAGE	ORDERING CODE	MARKING
-20°C to 125°C	DCE36 (SSOP)	TPS23851DCE	TPS23851

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

voltages are referenced to DGND (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Input voltage	VEE to AGND	-70	0.3	V
Input voltage	VDD	-0.3	3.6	
Voltage range	AGND	-1	1	
Voltage range	SDAI, SDAO (2), SCL, A0 (3), A1 (3), A2 (3), A3 (3), $\overline{SHDN1\text{-}4}$, $\overline{RESET}$, $\overline{INT}$ (2)	-0.3	3.6	
Output voltage	GATE1-4 to VEE (4)	-0.3	12	
Input voltage range	SEN1-4 to VEE	-0.3	3	
Input voltage range	OUT1-4 to VEE	-3	70	
Voltage range	DET1-4 to VEE (2)	-0.3	70	
Voltage range	TSTA, TSTB (2)	VEE	VDD	
Voltage slew rate	VEE		1	V/µs
Sinking current,	$\overline{INT}$, SDAO		20	mA
ESD – human body model			2	kV
ESD – charged device model			500	V
Operating junction temperature range	T_J	Internally limited		
Storage temperature	T_{ST}	-65	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply external voltage sources directly.
(3) A3-A0 can be directly tied to DGND but a resistor (at least 2 kΩ) must be used if pulled up. Do not tie directly to a positive voltage source.
(4) Application of voltage is not implied – these are internally driven pins.

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THERMAL INFORMATION

THERMAL METRIC[1]		TPS23851 DCE 36 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	52.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	25.1	
θ_{JB}	Junction-to-board thermal resistance[4]	29.0	
ψ_{JT}	Junction-to-top characterization parameter[5]	3.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	26.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

voltages are referenced to DGND (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VDD}		3	3.3	3.5	V
V_{VEE}	To AGND	-44	-48	-57	
V_{VEE}	Slew rate			1	V/µs
T_J	Operating junction temperature	-20		125	°C
T_A	Operating free-air temperature	-20		85	

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ELECTRICAL CHARACTERISTICS

Conditions are -20 ≤ TJ ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VEE} = -48 V, V_{DGND} = V_{AGND}, and all outputs are unloaded, unless otherwise noted. Positive currents are into pins. Current sense resistor = 0.5 Ω. Typical values are at 25°C. All voltages are with respect to DGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply						
I_{VDD}	VDD current consumption			2	5	mA
I_{VEE}	VEE current consumption			-7	-10	
Detection						
I_{DISC}	Detection current	First detection point, DET = 0 V	145	165	190	µA
		Second detection point, DET = 0 V	245	275	310	
V_{DETECT}	Open circuit detection voltage		-25	-18.11	-17	V
R_{REJ_LOW}	Rejected resistance low range		2.8		15	KΩ
R_{REJ_HI}	Rejected resistance high range		33		55	
R_{ACCEPT}	Accepted resistance range		19	25	26.5	
R_{SHORT}	Shorted port threshold				1.5	
R_{OPEN}	Open port threshold		55			
Classification						
V_{CLASS}	Classification voltage	At DET pin	-21	-18.5	-16.4	V
I_{CLASS_Lim}	Classification current limit	At 0 V	52.5	70	95	mA
Gate						
V_{GOH}	Gate drive voltage	$V_{GATEn-VEE}$, I_{GATE} = -1 µA	8		10.5	V
I_{GO-}	Gate sinking current with port short-circuit detected	$V_{GATEn-VEE}$ = 5 V	70	100	120	mA
I_{GO+}	Gate sourcing current	V_{GATEn} = V_{VEE}	0.05		1.5	
t_{D_off}	Gate turn off time with /SHDNn	From $\overline{SHDNn}$ to $V_{GATEn-VEE}$ < 1 V, SENn connected to VEE			900	µs
$t_{P_off_CMD}$	Gate turn off time from port off command	From port off command to $V_{GATEn-VEE}$ < 1 V, SENn connected to VEE			900	
$t_{P_off_RST}$	Gate turn off time with $\overline{RESET}$	From $\overline{RESET}$ low to $V_{GATEn-VEE}$ < 1V, SENn connected to VEE	1		5	
t_{P_didt}	Gate turn on and turn off di/dt control period	From port turn on/off command or from $\overline{SHDN}$ input		150		
OUT Pin Sense						
V_{PGT}	Power good threshold	Measured at V_{OUT}	1.5	2.13	3	V
	Resistance from OUT to AGND			2.5		MΩ
I_{OUT}	OUT pin bias current	V_{OUT} = 0 V	-6		5	µA
		-10 V > V_{OUT} > -30 V	-18		0	
		V_{OUT} = -48	-30	-20	-10	

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC Disconnect						
I_{ACDMAX}	Absolute magnitude of AC disconnect DET pin drive current	Port powered, $V_{VEE} < V_{DET} < V_{DGND}$, relative to VEE	-5		15	mA
I_{ACDMIN}	AC Disconnect DET pin drive current. Minimum current to remain connected.	Port powered	150	205	260	µA
V_{ACD}	Peak-to-peak DET pin output level	Port on, PD not present. Ports 1 – 4.	3.5	4	4.5	V
f_{sin}	sine wave frequency		100	110	125	Hz
A/D Converter						
T_{CONV}	Conversion time	All ranges, each port	15	20	27.5	ms
	Powered port voltage conversion scale factor and accuracy	OUT = -66 V	10800	11147	11400	Counts
		OUT = -44 V	7200	7432	7600	
	Powered port current conversion scale factor and accuracy	Port current = 770 mA	12288	12616	12944	
		Port current = 10 mA	100	163.8	220	
Input Supply UVLO						
V_{UVEE_F}	VEE UVLO falling threshold	VEUV threshold (supply event register) for port deassertion	25	31	34	V
V_{UVP_F}	VDD UVLO falling threshold	For port deassertion	1.9	2.3	2.6	
V_{DD_I2C}	Required VDD supply for I^2C operation		2.9			

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Port Current Sense						
V_{CUT}	I_{CUT} limit	OUT = VEE, ICUT(2:0) = 000b	175	187	200	mV
		OUT = VEE, ICUT(2:0) = 001b	45	55	65	
		OUT = VEE, ICUT(2:0) = 010b	90	102	115	
		OUT = VEE, ICUT(2:0) = 011b	175	187	200	
		OUT = VEE, ICUT(2:0) = 100b	350	377	400	
		OUT = VEE, ICUT(2:0) = 101b	276	296	316	
		OUT = VEE, ICUT(2:0) = 110b	318	343	365	
		OUT = VEE, ICUT(2:0) = 111b	385	408	430	
V_{LIM}	I_{LIM} limit	OUT = - 47 V	200		225	
		OUT = - 30 V	200		225	
		OUT = - 10 V	90		175	
V_{LIM2X}	I_{LIM} limit in 2X mode	OUT = - 47 V	409	431	452	
		OUT = - 40 V	409	431	452	
		OUT = - 10 V	150		300	
V_{short}	I_{short} threshold	Threshold for GATE to be less than 1 V, 2 µs after application of pulse	275	290	335	
$V_{short2X}$	I_{short} threshold in 2X mode		525	562	625	
I_{bias}	Sense pin bias current		-100		100	µA
I_{MIN}	DC disconnect threshold		2.5		5	mV

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ELECTRICAL CHARACTERISTICS (continued)

Conditions are -20 ≤ TJ ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VEE} = -48 V, V_{DGND} = V_{AGND}, and all outputs are unloaded, unless otherwise noted. Positive currents are into pins. Current sense resistor = 0.5 Ω. Typical values are at 25°C. All voltages are with respect to DGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timings						
t_{ICUT}	I_{CUT} time limit	TICUT = 00	50		70	ms
		TICUT = 01	25		35	
		TICUT = 10	100		140	
		TICUT = 11	200		280	
t_{START}	Maximum current limit duration in port start-up	TSTART = 00	50		70	
		TSTART = 01	25		35	
		TSTART = 10	100		140	
		TSTART = 11	200		280	
t_{DET}	Detection duration with 4-point discovery	Time to complete a detection	275		425	
t_{pdc}	Classification duration	Auto or semi-auto mode. From detection complete			50	
		Manual mode. From class command			50	
T_{pon}	Port power on delay	Auto mode from end of detection to port turn on			200	
		Manual mode from port turn on command to I_{GATE} = I_{GO+}			4	
t_{ed}	Error delay timing	Delay before next attempt to power a port following power removal due to error condition	750			
T_{RESET}	Reset time duration from $\overline{RESET}$ pin		3		6	µs
T_{RDG}	$\overline{RESET}$ input deglitch time		1		5	
t_{MPDO}	PD Maintain Power signature dropout time limit	TDIS = 00	300		400	ms
		TDIS = 01	75		100	
		TDIS = 10	150		200	
		TDIS = 11	600		800	
t_{SHDG}	$\overline{SHDNn}$ input deglitch time	$\overline{SHDNx}$ pin assertion threshold	1		5	µs
t_{POR}	device power-on reset delay				20	ms
Digital Interface						
V_{IH}	Digital input High		2.4			V
V_{IL}	Digital input Low				0.8	
V_{OL}	Digital output Low	at 3 mA			0.4	
		SDAO at 5 mA			0.7	
R_{pullup}	Pullup resistor to VDD	$\overline{RESET}$, A[3:0], /SHDN[4:1]	30	50	80	kΩ
$R_{pulldown}$	Pulldown resistor to DGND	AUTO pin	30	50	80	

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ELECTRICAL CHARACTERISTICS (continued)

Conditions are -20 ≤ TJ ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VEE} = -48 V, V_{DGND} = V_{AGND}, and all outputs are unloaded, unless otherwise noted. Positive currents are into pins. Current sense resistor = 0.5 Ω. Typical values are at 25°C. All voltages are with respect to DGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C Interface Timing Requirements at 0 ≤ T_J ≤ 100°C						
f_{SCL}	SCL clock frequency				400	kHz
		-20 ≤ T_J ≤ 100°C			100	
t_{LOW}	LOW period of the clock		1.3			µs
t_{HIGH}	HIGH period of the clock		0.6			
t_{fo}	SDAO output fall time	SDA, 2.3 V – 1.0 V, C_b = 10 pF, 10 kΩ pull-up to 3.3 V	21		250	ns
		SDA, 2.3 V – 1.0 V, C_b = 400 pF, 1.3 kΩ pull-up to 3.3 V	60		250	
$t_{SU,DAT}$	Data set-up time		200			
$t_{HD,DAT}$	Data hold time		150			
t_{rfSDA}	Input rise/fall times of SDAI		20		120	
t_r	Input rise time of SCL		20		300	
t_f	Input fall time of SCL		20		150	
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{HD,STA}$	Hold time after (repeated) start condition		0.6			
$t_{SU,STA}$	Repeated start condition set-up time		0.6			
$t_{SU,STO}$	Stop condition set-up time		0.6			
t_{FLT_INT}	Fault to $\overline{INT}$ assertion	Time to internally register an Interrupt fault		100		
t_{STOP_INT}	STOP to $\overline{INT}$ assertion			140		ns
t_{ARA_INT}	ARA to $\overline{INT}$ de-assertion				500	
Thermal Shutdown						
	Shutdown temperature	Temperature rising	143	154	161	°C
	Hysteresis			8		

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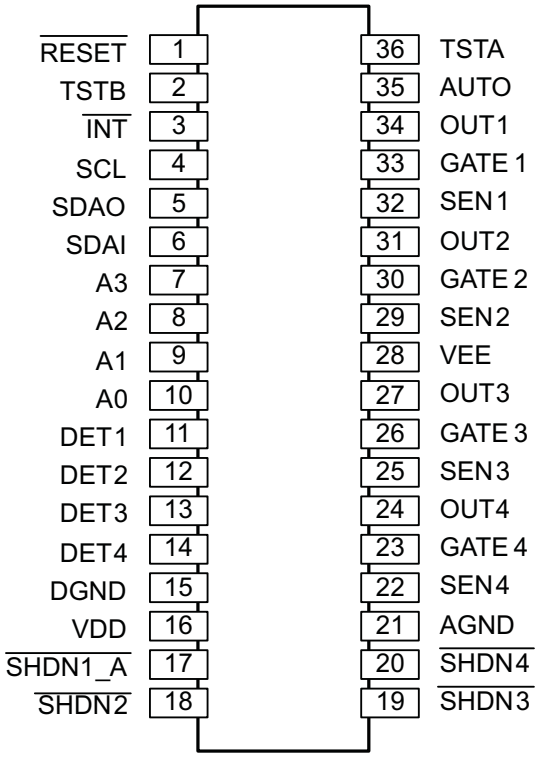
DEVICE INFORMATION

36-Pin DCE Package



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PIN FUNCTIONS

PIN	NAME	I/O	DESCRIPTION
1	$\overline{\text{RESET}}$	I	Reset input. When asserted low, the TPS23851 will reset. This pin is internally pulled up to VDD.
2	TSTB		Used for internal test modes only. Negative high voltage may appear if test mode is enabled. Leave this pin open.
36	TSTA		Used for internal test modes only. Negative high voltage may appear if test mode is enabled. Leave this pin open
3	$\overline{\text{INT}}$	O	Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This pin is updated between I^2C transactions. This output is open-drain.
4	SCL	I	Serial clock input for I^2C bus.
5	SDAO	O	Serial data output for I^2C bus. This pin can be connected to SDAI for non-isolated systems. This output is open-drain.
6	SDAI	I	Serial data input for I^2C bus. This pin can be connected to SDAO for non-isolated systems.
7	A3	I	I^2C A3-A0 Address lines. These pins are internally pulled up to VDD. Do not tie directly to a positive voltage source. (1)(2)
8	A2	I	
9	A1	I	
10	A0	I	
11, 12, 13, 14	DET1-4	I	Port 1-4 detect sense.
15	DGND		Digital ground.
16	VDD		Digital supply. Bypass VDD to DGND using 0.1 µF and 1 µF capacitors in parallel. Connect VDD to the 3.3V digital supply using a 10 Ω resistor.
17	$\overline{\text{SHDN1_A}}$	I	Port 1 manual shutdown input or Port 1-4 multiplexed shutdown. This pin is internally pulled up to VDD.
18,19,20	$\overline{\text{SHDN2-4}}$	I	Port 2-4 manual shutdown logic input. These pins are internally pulled up to VDD.
21	AGND		Analog ground.
32, 29, 25	SEN1-3	I	Port 1-3 current sense input. Connect to current sense resistor.
22	SEN4	I	Port 4 current sense input. Connect to current sense resistor.
33, 30, 26, 23	GAT1-4	O	Port 1-4 gate drive output.
34, 31, 27, 24	OUT1-4	I	Port 1-4 output voltage monitor. Connect to output port through a 10-kΩ resistor.
28	VEE		Analog supply. Bypass VEE to AGND using 0.1 µF and 1 µF capacitors in parallel.
35	AUTO	I	Mode select input. Asserting high on power-up puts the TPS23851 into auto mode. This pin is internally pulled down to DGND.

(1) Can be directly tied to DGND but a resistor (at least 2 kΩ) must be used if pulled up.
(2) A6, A5, A4 are factory set to 010.

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Detailed Pin Description

The following descriptions refer to the pinout and the functional block diagram.

$\overline{\text{RESET}}$: Reset input, active low. When asserted, the TPS23851 will reset, turning off all ports and forcing the registers to their power-up state. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. External RC network can be used to delay the turn on. There is also an internal power-on reset which is independent of the $\overline{\text{RESET}}$ input.

$\overline{\text{INT}}$: Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This pin is updated between I^2C transactions. This output is open-drain. Interrupt functional diagram is shown in Figure 31.

SDAO: Open-drain I^2C bus output data line requiring an external resistive pullup. The TPS23851 uses separate SDAO and SDAI lines to allow optoisolated I^2C interface. SDAO can be connected to SDAI for non-isolated systems.

SCL: Serial clock input for I^2C bus.

SDAI: Serial data input for I^2C bus. This pin can be connected to SDAO for non-isolated systems. Note that the data sent by the TPS23851 on SDAO must be mirrored on its SDAI line for correct operation. See Figure 35.

A3-A0: I^2C bus address inputs. Can be directly tied to DGND but a resistor (at least 2 kΩ) must be used if pulled up. These pins are internally pulled up to VDD. See the Pin Status Register for more details.

$\overline{\text{SHDN1_A}}$: Port 1 Manual Shutdown Input or Port 1-4 Multiplexed Shutdown, active low. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter.

When Multiplexed Shutdown is disabled, pulling low $\overline{\text{SHDN1_A}}$ turns off port 1, regardless of the state of registers except the Multiplexed Shutdown Configuration Register.

When Multiplexed Shutdown is Enabled, pulling low $\overline{\text{SHDN1_A}}$ turns off the ports selected in the Multiplexed Shutdown Configuration Register. This turn off action is triggered regardless of the state of registers except the Multiplexed Shutdown Configuration Register.

$\overline{\text{SHDN2-4}}$: Port 2-4 Manual Shutdown Logic Input, active low. These pins are internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. When Multiplexed Shutdown is disabled, pulling low $\overline{\text{SHDNn}}$ turns off port n, regardless of the state of registers except the Multiplexed Shutdown Configuration Register.

NOTE

If the Multiplexed Shutdown function is Enabled, the $\overline{\text{SHDN2}}$ to $\overline{\text{SHDN4}}$ inputs must be at logic High.

DET1-DET4: Port 1-4 detect sense.

Used during AC disconnect detection and powered device discovery. Connect to output port through a 1 kΩ in series with a 0.47 µF, both in parallel with a diode. AC disconnect consists in sensing the load impedance by injecting an AC voltage at DETn pin and measuring the resultant current through the same pin. If the impedance is higher than a defined threshold, the port will automatically be turned off. The DET pin sine wave output voltage typically has a 2.5-V offset above the VEE supply, with a 2 V peak-to-peak amplitude under a no load condition.

The TPS23851 uses an innovative 4-point technique in order to provide a reliable PD detection. The discovery is performed by sinking two different current levels via the DETn pin, while the PD voltage is measured from DGND to DET. The 4-point measurement provides the capability to avoid powering a capacitive or legacy load.

The resistor and capacitor are not needed if AC disconnect is not used. If the port is not used, the DETn pin can be floated or tied to VEE.

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GAT1-GAT4: Port 1-4 gate drive output used for external N channel MOSFET gate control. At port turn on, it is driven positive by a low current charge pump to turn the MOSFET on. Note that the MOSFET turn on is done with di/dt control, which means that an internal amplifier forces the load current to track an internally defined voltage ramp. GATn is pulled low whenever any of the input supplies are low or if an over-current timeout has occurred. GATn will also be pulled low if its port is turned off by use of manual shutdown inputs. Leave floating if unused.

For a robust design, a current foldback function limits the power dissipation of the MOSFET during low resistance load or a short circuit event. The foldback mechanism measures the port voltage across AGND and OUTn to reduce the current limit threshold from 100% at 18 V (28 V if in 2X mode) down to around 14% at a port voltage of 0 V.

When I_{CUT} threshold is exceeded while a port is on, a timer starts. During that time, linear current limiting makes sure the current will not exceed I_{LIM} combined with current foldback action. When the timer reaches its t_{ICUT} (or t_{START} if at port turn on) limit, the port shuts off. When the port current goes below I_{CUT}, while there is no foldback action, the counter counts down at a rate $1/16^{th}$ of the increment rate and it must reach a count of zero before the port can be turned on again.

The fast overload protection is for major faults like a direct short. This turns off the MOSFET in less than a microsecond, for a period of 100 µs, after which the gate is slowly turned back on with controlled di/dt. If the port is not used, tie SENn to VEE.

OUT1-OUT4: Port 1-4 output voltage monitor. Used to measure the port output voltage, for port voltage monitoring, port power good detection and foldback action. Should be connected to output port through a 10-kΩ resistor. There is an internal resistor between each OUTn pin and AGND. If the port n is not used, OUTn can be left floating or tied to AGND.

SEN1-4: Port 1-4 current sense input, relative to VEE. Monitors the external MOSFET current by use of a 0.5-Ω current sense resistor connected to VEE. Used by current foldback engine and also during classification. Can be used to perform load current monitoring via A/D conversion.

A classification is done while using the external MOSFET so that doing a classification on more than one port at same time is possible without overdissipation in the TPS23851.

For the DC disconnect function, there is an internal 2-µs analog filter on the SEN1-4 pins to provide glitch filtering.

SENn is a single ended measurement for all four ports and any voltage drop on the VEE path between the sense resistor and the VEE pin of TPS23851 can introduce errors, particularly during classification. Consequently, the PCB layout must be done in order to mitigate any such error, for example by using a copper plane, a star return point at the VEE pin for all four current sense resistors, or both. Connect to VEE if the port is unused.

NOTE

In order to meet clearance safety regulations, a fuse or an equivalent component should be inserted in series between the SEN4 pin and its corresponding current sense resistor.

AUTO: Auto mode input. A logic high state at POR means the TPS23851 will operate autonomously in auto mode even in the absence of a host controller. The state of that pin is measured only immediately following a Power-on-Reset or after the RESET input has been activated.

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TYPICAL CHARACTERISTICS

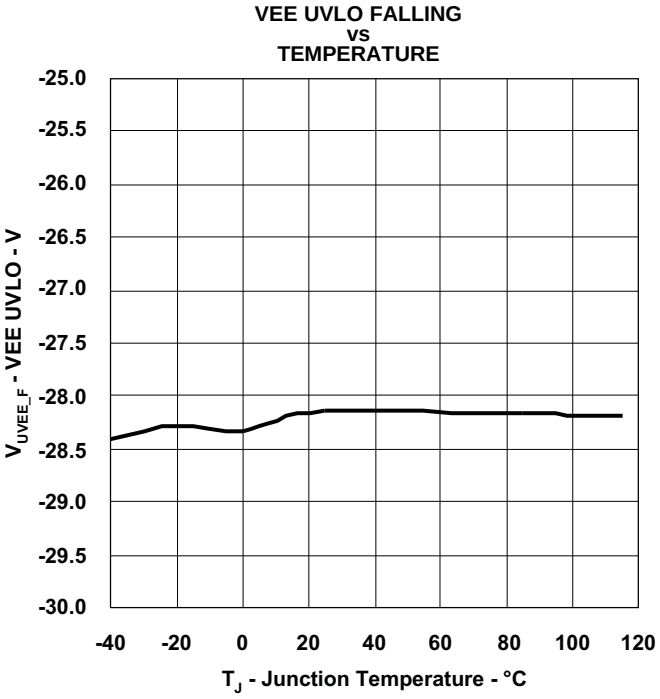

Figure 1.

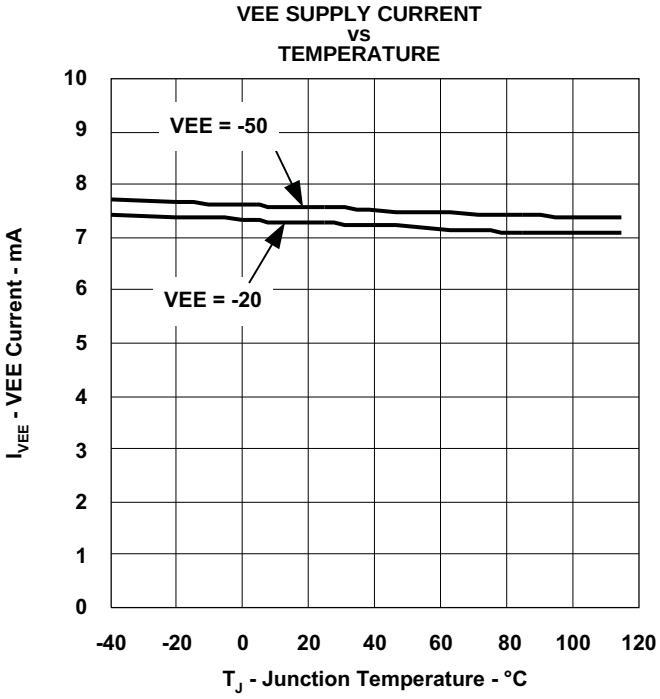

Figure 2.

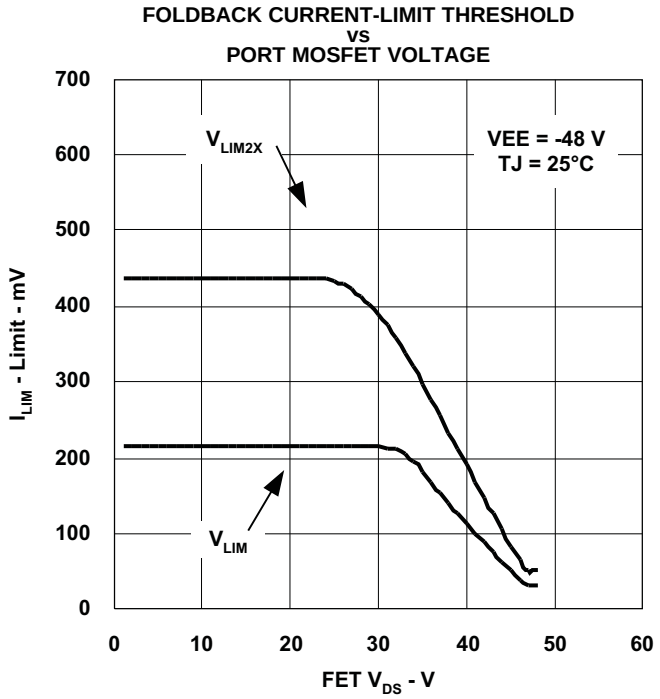

Figure 3.

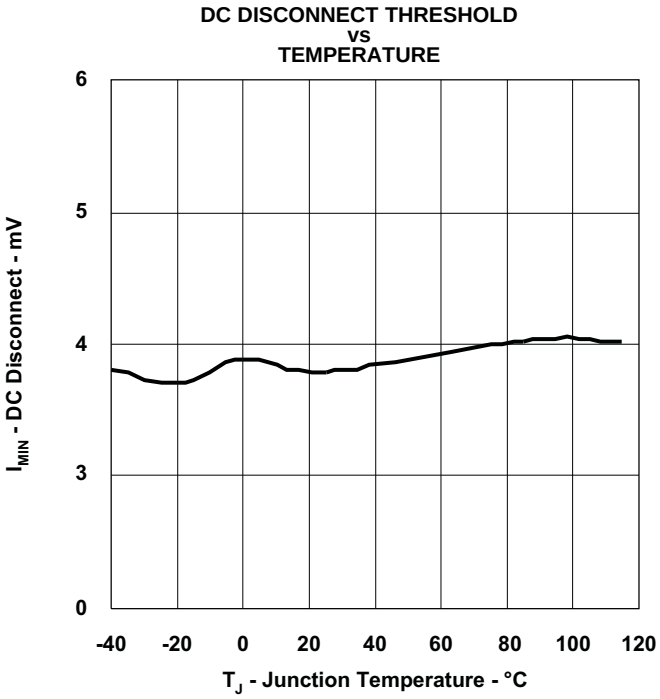

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

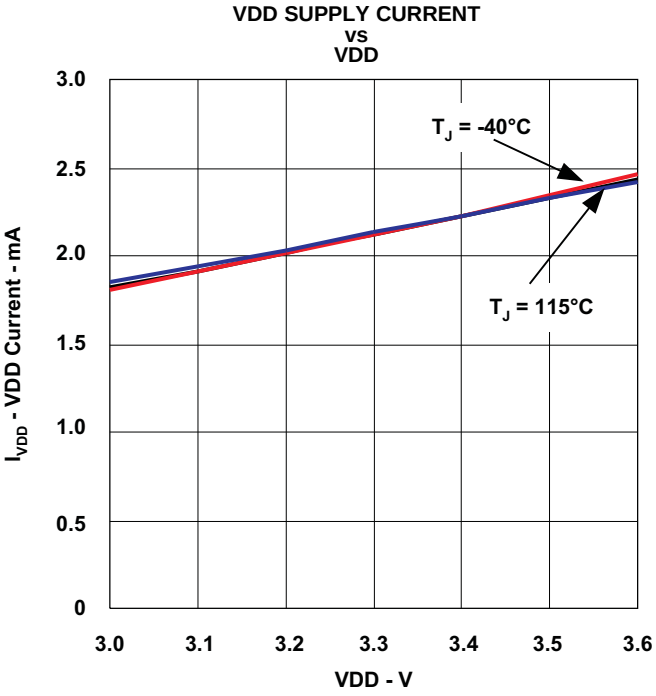

Figure 5.

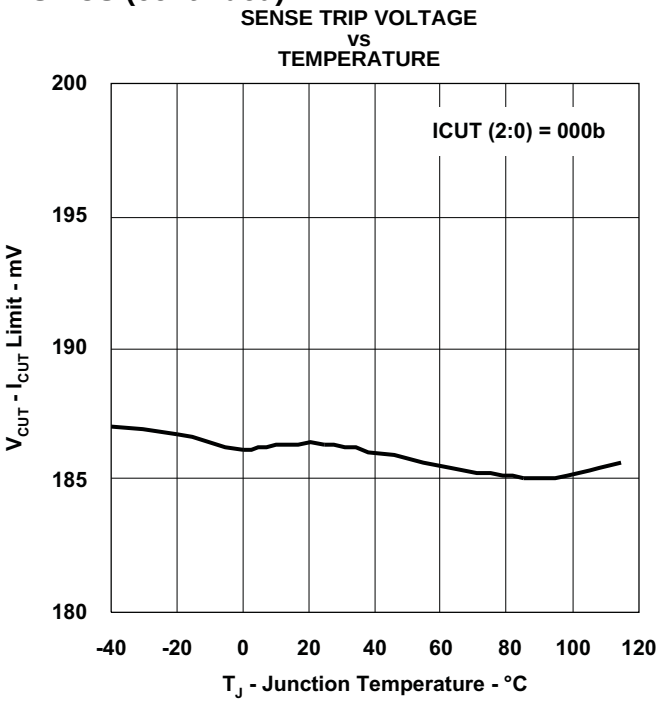

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

STARTUP WITH VALID PD (25 KΩ and 0.1 µF), CLASS 0

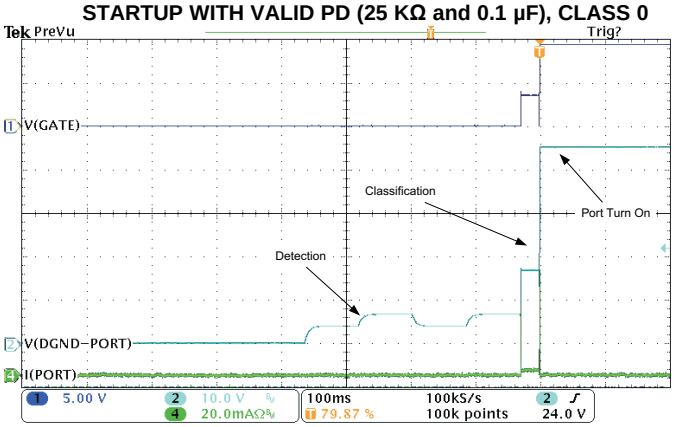

Figure 7.

STARTUP WITH VALID PD (25 KΩ and 0.1 µF), CLASS 1

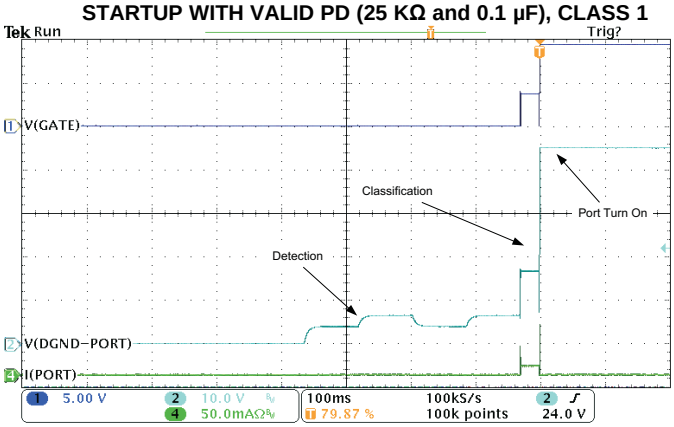

Figure 8.

STARTUP WITH VALID PD (25 KΩ and 0.1 µF), CLASS 2

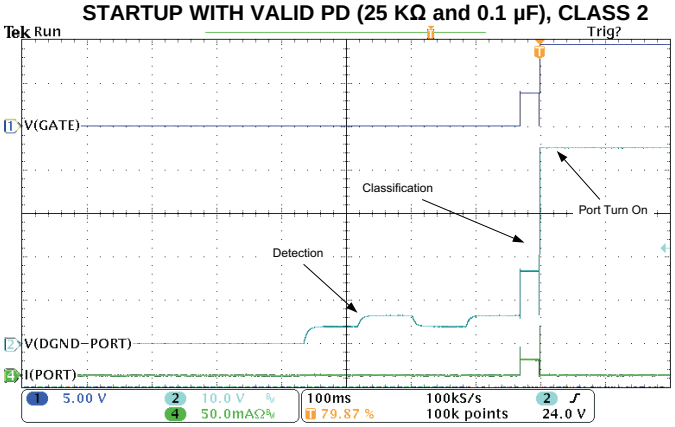

Figure 9.

STARTUP WITH VALID PD (25 KΩ and 0.1 µF), CLASS 3

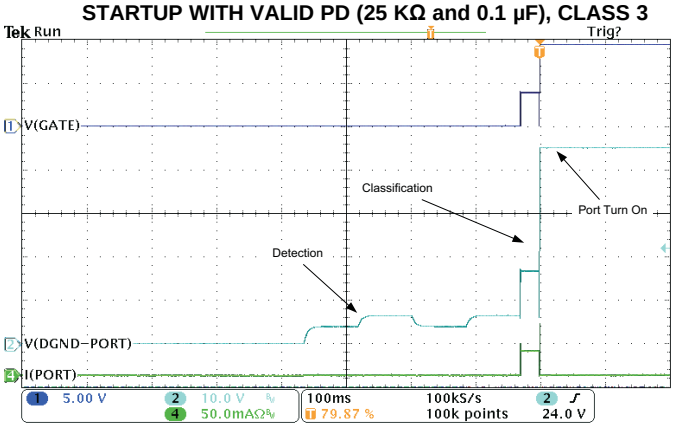

Figure 10.

STARTUP WITH VALID PD (25 KΩ and 0.1 µF), CLASS 4

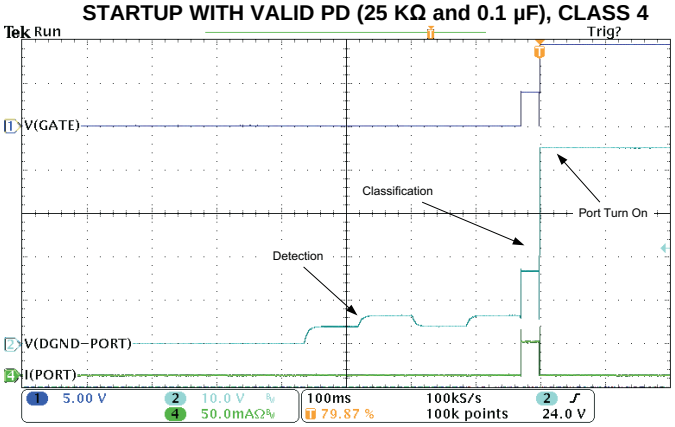

Figure 11.

DETECTION WITH INVALID PD (25 KΩ and 10 µF)

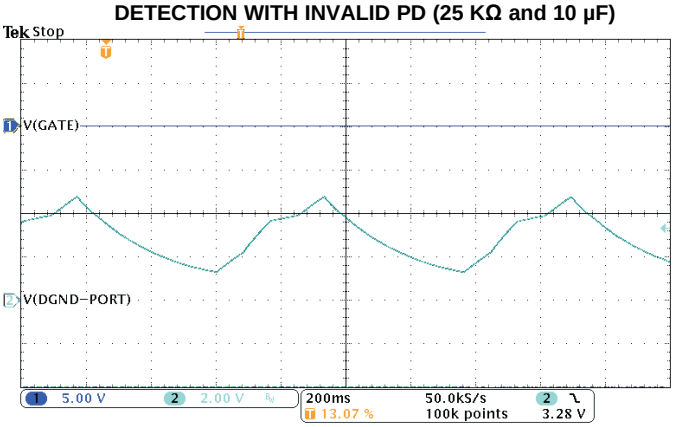

Figure 12.

TYPICAL CHARACTERISTICS (continued)

DETECTION WITH INVALID PD (15 KΩ and 0.1 µF)

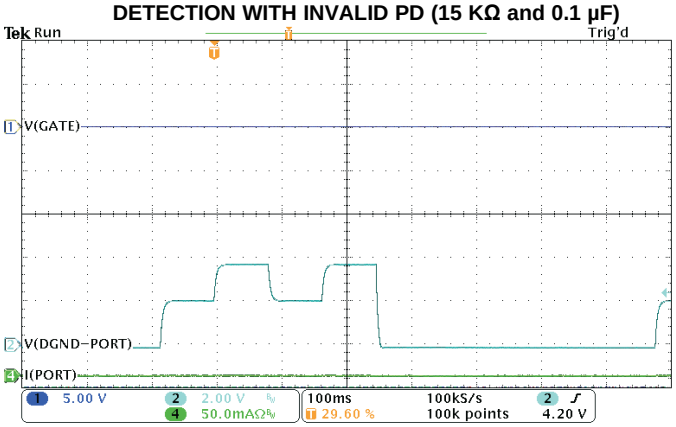

Figure 13.

DETECTION WITH INVALID PD (open circuit)

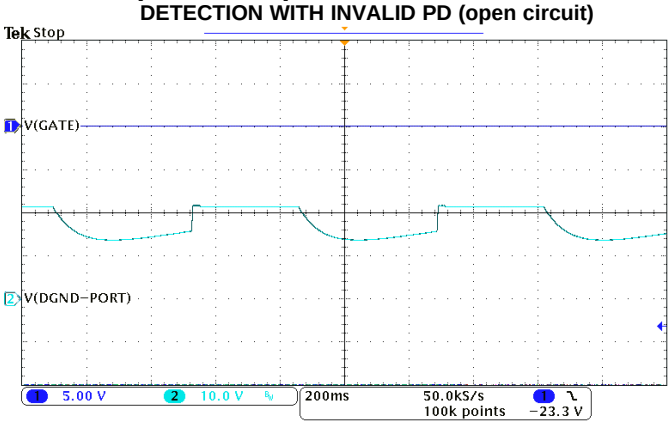

Figure 14.

RESPONSE TO PD REMOVAL, AC DISCONNECT ENABLED

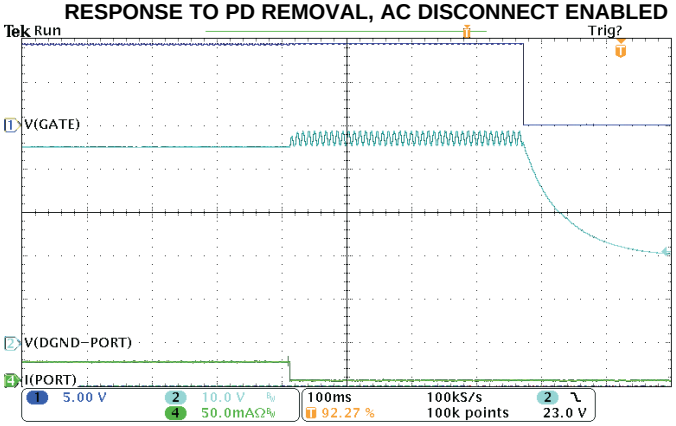

Figure 15.

RESPONSE TO 8-mA to 6-mA LOAD, DC DISCONNECT ENABLED

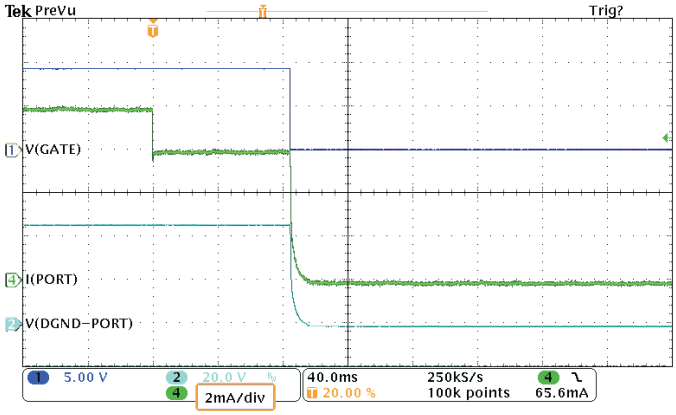

Figure 16.

RAPID RESPONSE TO A 1-Ω SHORT

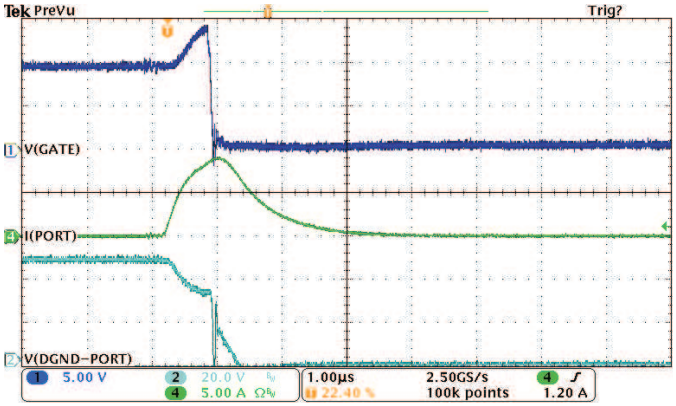

Figure 17.

RESPONSE TO A 50-Ω LOAD IN 803.2af MODE

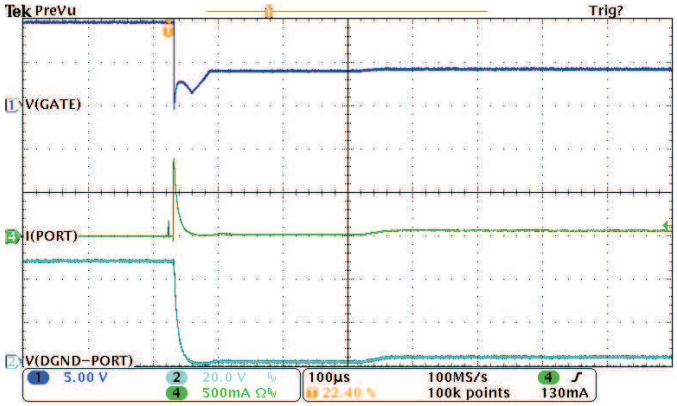

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

RESPONSE TO A 39-Ω LOAD IN HIGH-POWER MODE

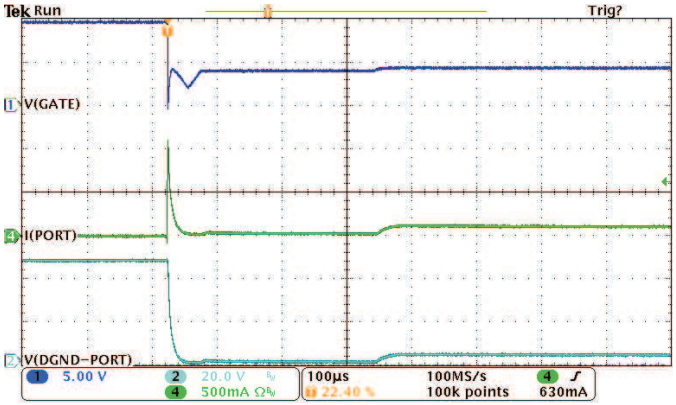

Figure 19.

OVERCURRENT RESTART DELAY

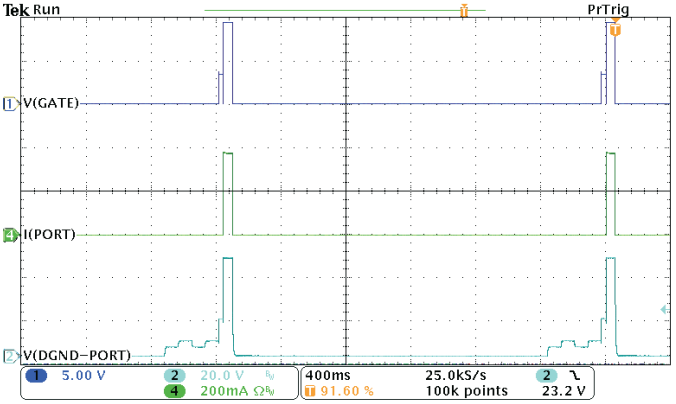

Figure 20.

Figure 21. OVERCURRENT RESTART DELAY WITH CURRENT LIMIT

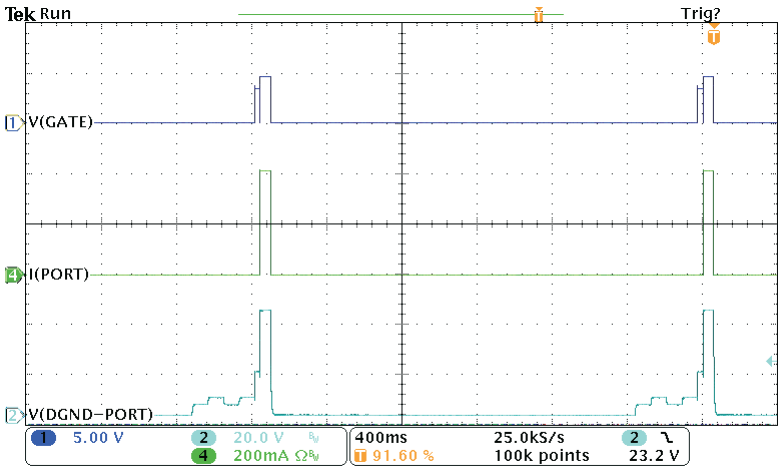

Figure 22.

TYPICAL CHARACTERISTICS (continued)

Block Diagrams

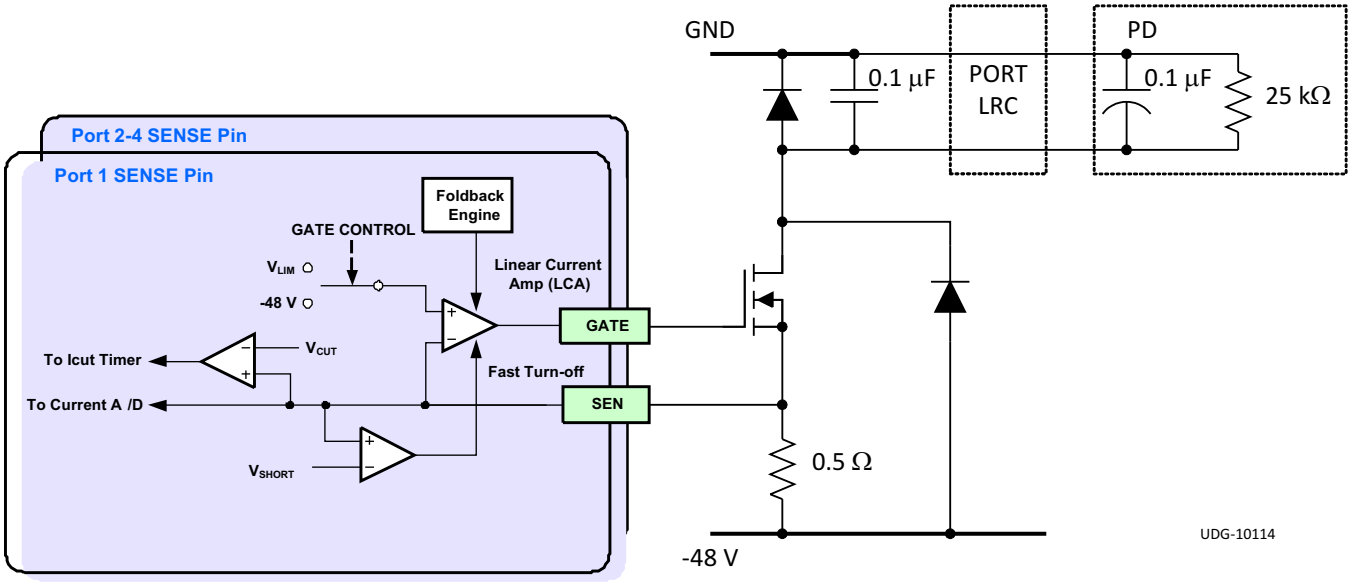

Figure 23. Port Current Sense Circuitry

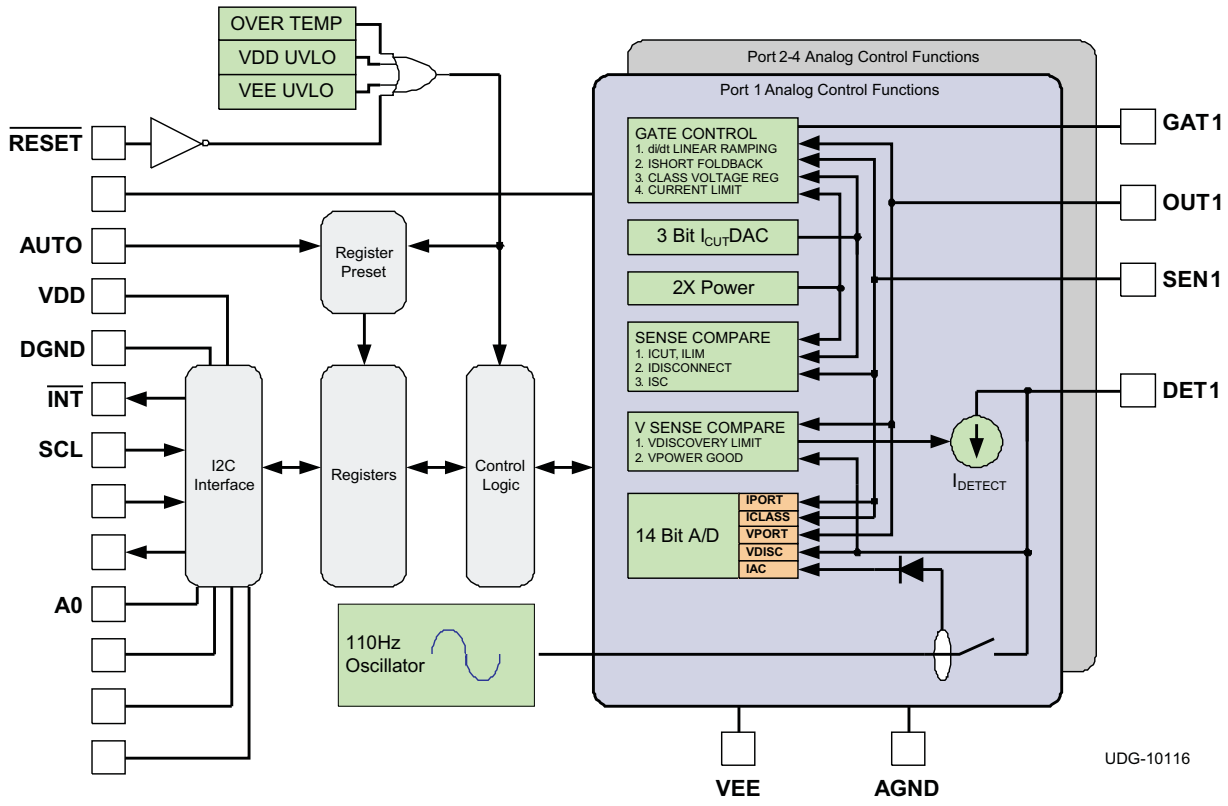

Figure 24. Block Diagram

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TYPICAL CHARACTERISTICS (continued)

Timing Diagrams

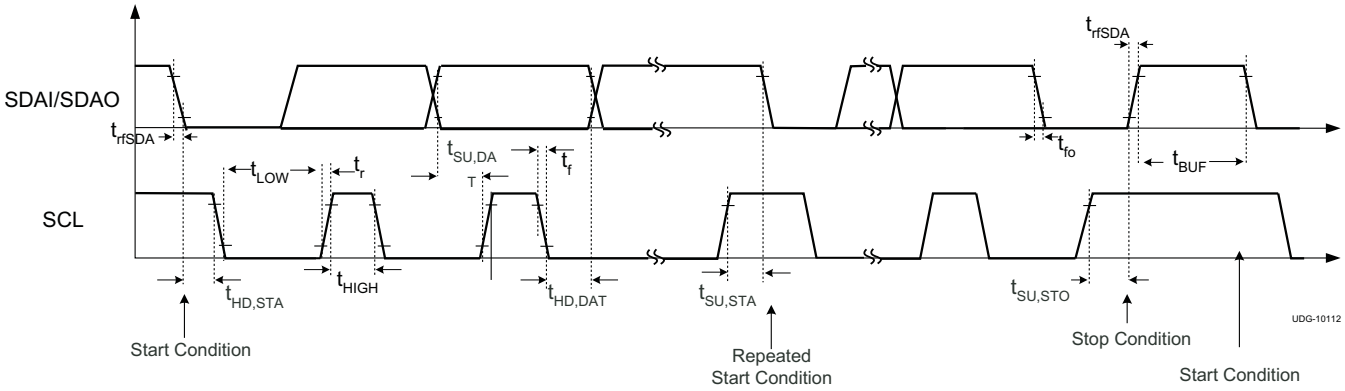

Figure 25. I^2C Timings

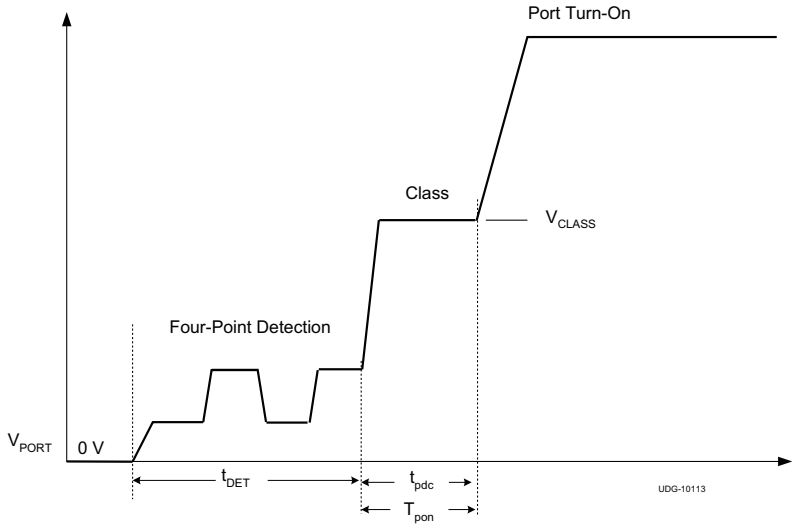

Figure 26. Detection, Classification and Turn On In Auto Mode

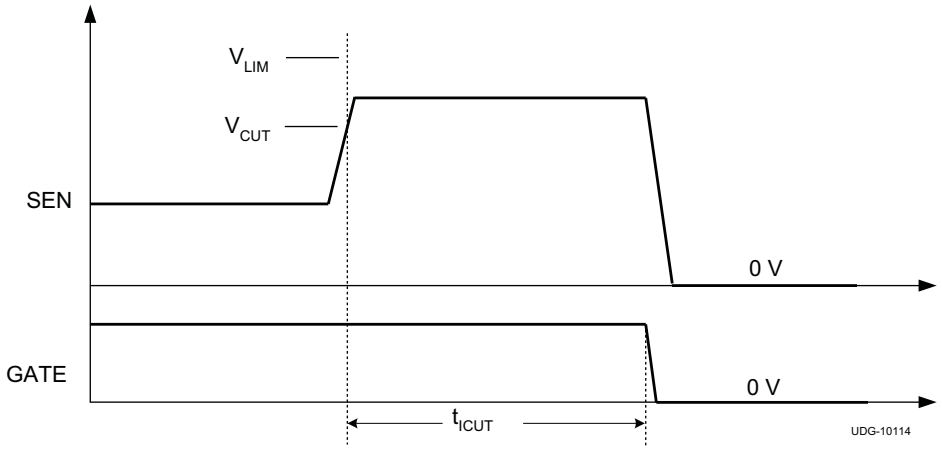

Figure 27. Overcurrent Fault Timing

DETAILED DESCRIPTION

A/D Converters

The TPS23851 features one 14-bit multi-slope integrating converter per port, for a total of four converters. Each converter is operated independently to perform measurements in any of the following modes: discovery, classification, port powered (current, voltage and AC disconnect).

The A/D converter type used in the TPS23851 differs from other similar types of converters in that it converts while the input signal is being sampled by the integrator, resulting in reduced conversion time and providing inherent filtering over the conversion period. The typical conversion time of this converter is 20 ms with 17.5-ms sampling window, providing significant rejection of noise at 50-Hz to 60-Hz line frequency.

NOTE

1. During AC disconnect measurement, the converter integration is synchronized with the sinewave generator for rejection of the excitation signal.
2. Note that during port powered mode, voltage conversions are interleaved with port current conversions. If AC disconnect is Enabled, DC current, DC voltage and AC current measurements are interleaved.

When a port is on, its voltage and current results are stored in the Port n Voltage and Port n Current Registers.

NOTE

The content of the Port #n Current and Voltage Registers is not updated when the port is off.

Any port reading should be qualified with the PGn bit of the Power Status Register (10h). If the port bit is a 1, then the reading should be accepted. If zero, the A/D reading should be considered corrupt as it may represent a port that experienced a power fault event or was disabled midway through a conversion.

Also, in port powered mode, the t_{START} timer must expire before any current or voltage A/D conversion can begin.

Each 14-bit result can be read via a 2-byte read cycle, as shown in Figure 5.

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I²C Serial Interface

The TPS23851 features a 3-wire I²C interface, using SDAI, SDAO and SCL. Each transmission includes a Start condition sent by the master, followed by the device address (7-bit) with R/W bit, a register address byte, then one or two data bytes, and a Stop condition. There is also an acknowledge bit sent by the recipient following each byte transmitted. Also, SDAI/SDAO is stable while SCL is high except during a Start or Stop condition. Figure 28 illustrates read and write operations through I²C interface. The 2 data bytes read operation is applicable to A/D conversion results. Note that the data sent by the TPS23851 on SDAO must be mirrored on its SDAI line for correct operation, as shown.

The TPS23851 features a quick access to the Interrupt Register through I²C bus. See Figure 28.

NOTE

This means that when a Stop Bit is received, the register pointer is automatically reset. This means that there must not be any Stop Bit before a Repeated Start Bit, as shown.

It is also possible to perform a write operation to many TPS23851 devices at same time. The slave address during this broadcast access is 0x30, as shown in the Pin Status Register description.

The TPS23851, using the $\overline{\text{INT}}$ line, supports the SMBALERT protocol.

When $\overline{\text{INT}}$ is asserted low, if the bus master controller sends the Alert response address, the TPS23851 responds providing its device address on the SDA line and releases the $\overline{\text{INT}}$ line. If there is a collision between two TPS23851 devices responding simultaneously, then the device with the lower address wins arbitration and responds first, by use of SDAI and SDAO lines.

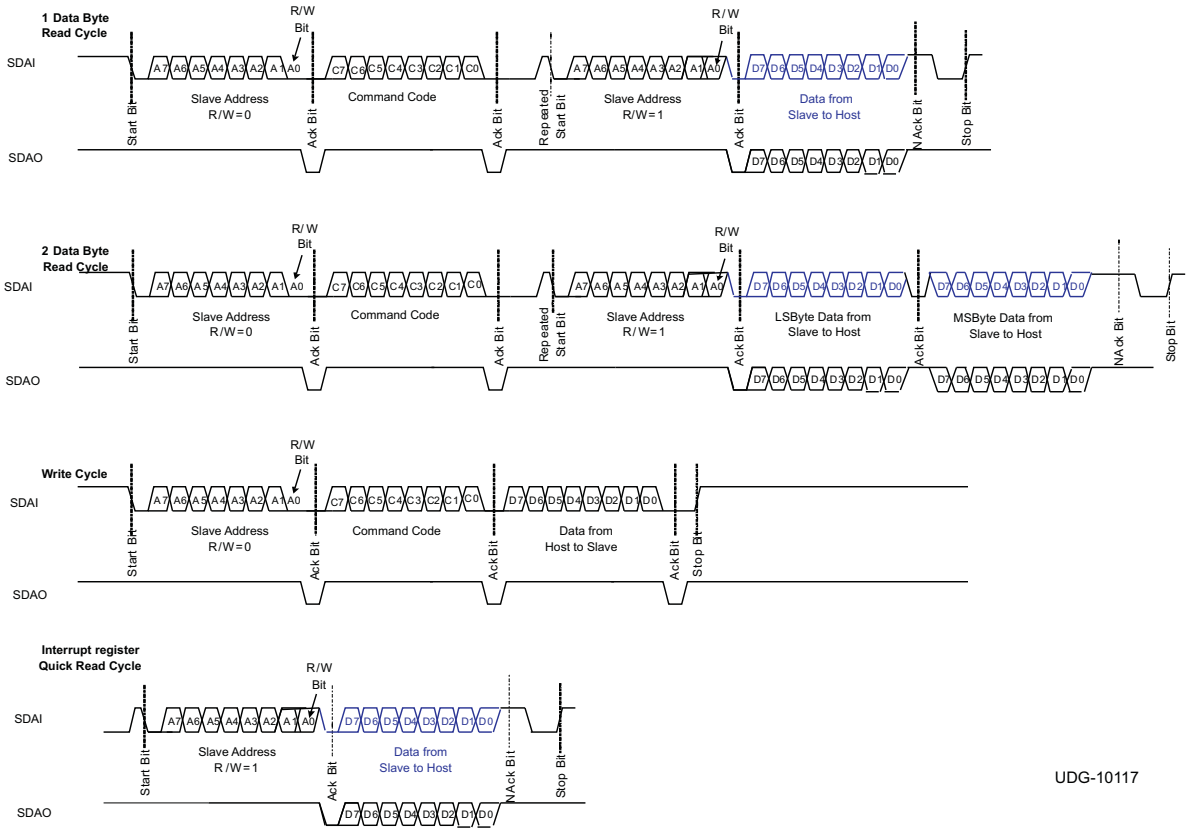

Figure 28. I²C/SMBus Interface Read And Write Protocol

Foldback and High Power Mode

For a robust design, a current foldback function limits the power dissipation of the MOSFET during low resistance load or a short circuit event. Using the TPS23851, it is possible to select one of two foldback profiles. The first one is for 802.3af applications, while the second one (2X mode) is for higher power applications as defined in the 802.3at standard. See Figure 29 and Figure 30.

The HPWn bit of the High Power and Sine Disable Register needs to be set to select the High Power Mode.

The linear foldback mechanism measures the port voltage across AGND and OUTn to reduce the current limit threshold from 100% at 18 V (28 V if in 2X mode) down to around 14% at a port voltage of 0 V.

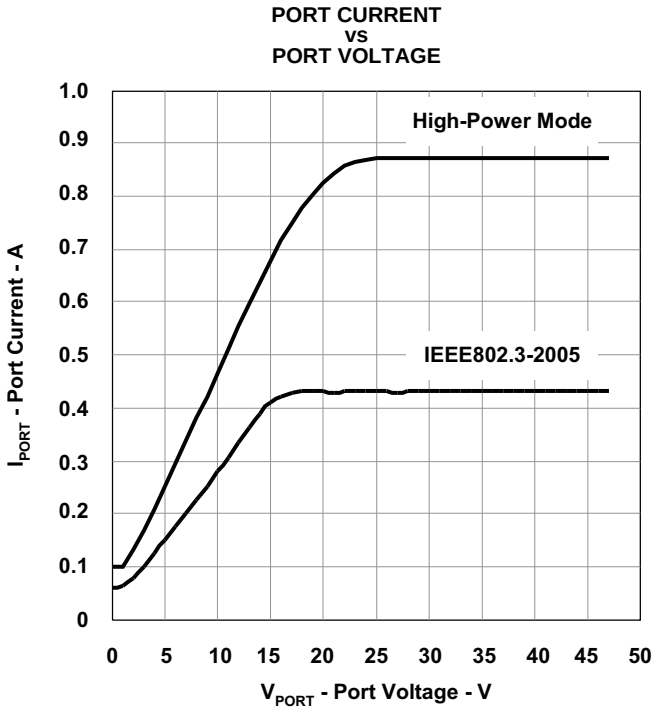

Figure 29. Output Current Foldback Function (In IEEE Std 802.3at-2009 Mode and High-Power Mode)

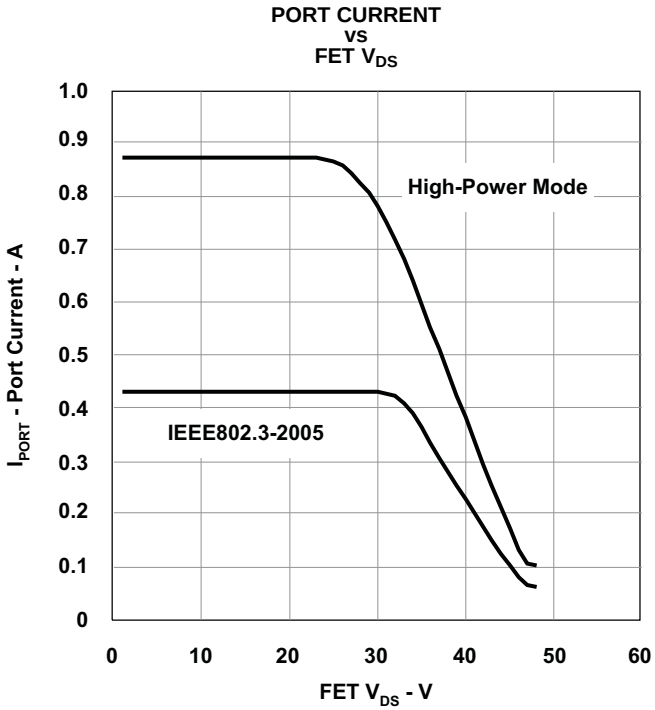

Figure 30. Output Current Foldback Function (With VEE = -48 V, in IEEE Std 802.3at-2009 Mode and High-Power Mode)

Inrush Control, ICUT Fault Control

During a port turn on, the port MOSFET is turned on with di/dt control, which means that an internal current limiting amplifier forces the load current to track an internally defined voltage ramp. The t_{START} fault timer is also started at port turn on. If at the end of t_{START} time period the port is still in current limit, the port shuts off and its STRTn fault bit is set (Start Event Register).

NOTE

During inrush period, the regular (1x) current foldback is used, regardless of the state of the HPWn bit in High Power and Sine Disable Register.

Once the t_{START} fault timer has expired without a fault, the t_{ICUT} timer becomes effective. It starts when I_{CUT} threshold is exceeded while a port is on. During that time, linear current limiting makes sure the current will not exceed I_{LIM} combined with current foldback action. When the timer reaches its t_{ICUT} limit, the port shuts off and its ICUTn bit is set (Fault Event Register). When the port current goes below I_{CUT}, while there is no foldback action, the counter counts down at a rate $1/16^{th}$ of the increment rate and it must reach a count of zero before the port can be turned on again.

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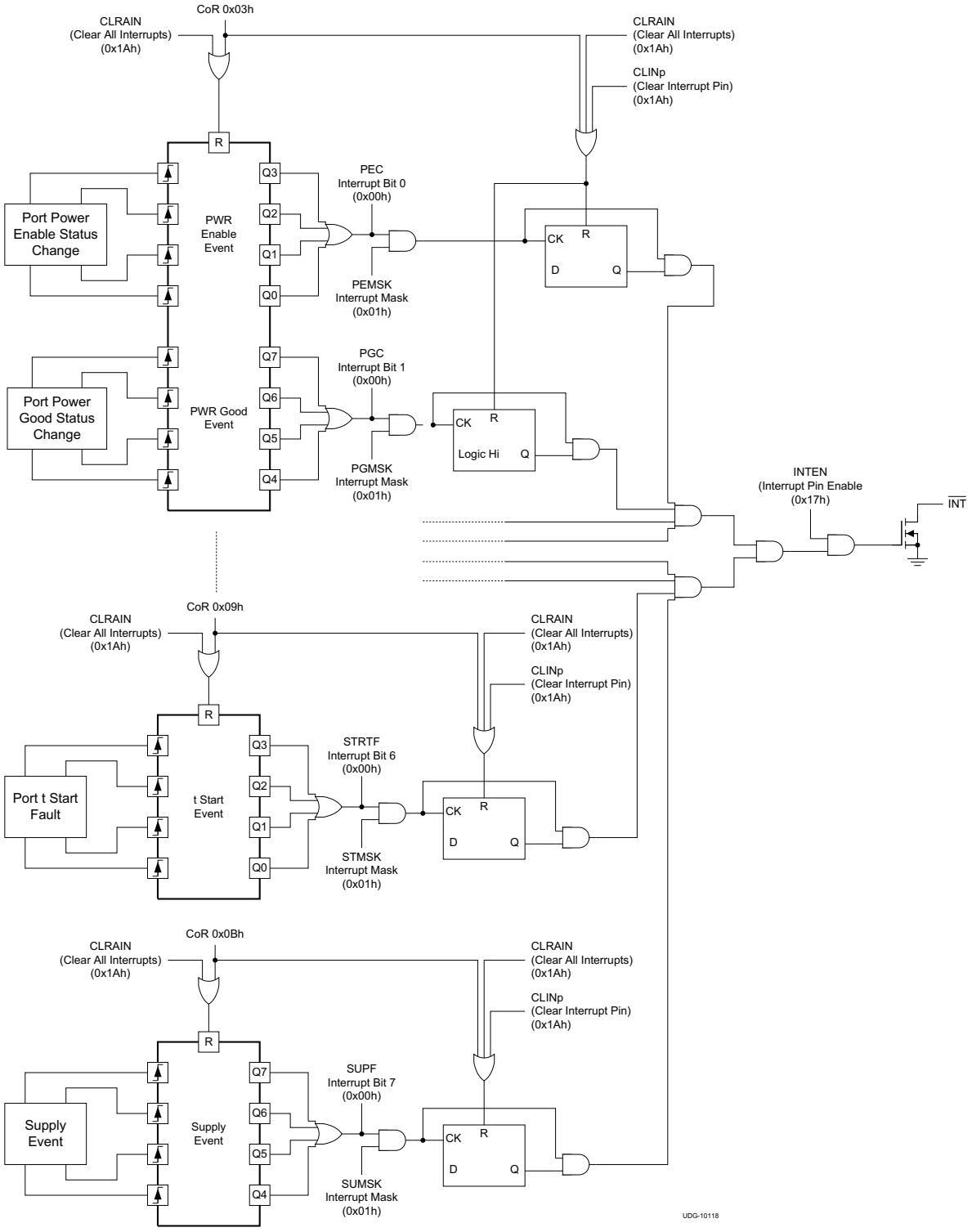

Figure 31. Interrupt Logic Functional Diagram

APPLICATION INFORMATION

Introduction to POE

Power-Over-Ethernet (POE) is a means of distributing power to Ethernet devices over the Ethernet cable using either data or spare pairs. POE eliminates the need for power supplies at the Ethernet device. Common applications of POE are security cameras, IP Phones and PDA chargers. The host or mid-span equipment that supplies power is the Power Source Equipment (PSE). The load at the Ethernet connector is the Powered device (PD). POE protocol between PSE and PD controlling power to the load is specified by IEEE Std 802.3at-2009.

Transformers are used at Ethernet host ports, mid-spans and hubs, to interface data to the cable. A DC voltage can be applied to the center tap of the transformer with no effect on the data signals. As in any power transmission line, a relatively high 48 V is used to keep current low, minimize the effect of IR drops in the line and preserve power to the load. Standard POE delivers approximately 13 W to the PD. Figure 35 shows the overview schematic of a POE port.

POE States Introduction

The PSE and PD operate under a three state protocol to complete the power connection. At initialization or when the port is disconnected, the PSE controller enters the detection state. In detection, the PD places a 25-kΩ signature resistor across the wire pair. The TPS23851 controller outputs a small current and checks the voltage to determine a valid PD signature. When a valid PD is found, the PSE controller enters the classification state to find out how much current the device requires. The PSE outputs a fixed 17.5 V and reads the current taken by the PD at this level. The current is converted to a device class. The PSE then enters the power on state. The PSE powers the port and continuously monitors the current supplied to the PD. See Figure 26.

The port remains on as long as the port load is less than I_{CUT}, which is the maximum current allowed. Once a port load is above I_{CUT} or is disconnected or faulted, the port is powered down.

Detection

To eliminate the possibility of false detection, the TPS23851 uses a TI proprietary 4-point detection method to determine the signature resistance of the PD device. False detection of a 25-kΩ signature can occur with 2-point detection type PSE's in noisy environments or if the load is highly capacitive.

Both detection 1 and detection 2 are merged into a single detection function which is repeated. Detection 1 applies I1 (165 µA) to a port, waits 80 ms and then measures the port voltage V1 with the integrating ADC. Detection 2 applies I2 (275 µA) to a port, waits 80 ms and measures the port voltage V2. The process is repeated a second time. Multiple comparisons and calculations are performed on all four measurement point combinations to eliminate the effects of a non-linear or hysteretic PD signature. The resulting port signature is then sorted into the appropriate category.

Classification

802.3af (or 802.3at Type 1) classification (class) is performed by supplying a voltage and sampling the resulting current. To eliminate the high power of a classification event from occurring in the power controller chip, the TPS23851 makes use of the external power FET for classification.

During classification, the voltage on the gate node of the external MOSFET is part of a linear control loop. The control loop applies the appropriate MOSFET drive to maintain a differential voltage between GND and OUT of 17.5 V. During classification the voltage across the sense resistor in the source of the MOSFET is measured and converted to a Class level within the TPS23851. If a load short occurs during classification the MOSFET gate voltage is quickly reduced to a linearly controlled, short circuit value for the duration of the class event.

Classification results may be read through the I^2C Detection Event and Port n Status Registers.

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Power On

Once the port has met the requirements of a valid POE load, the port is powered on.

Port Operating Modes

Each port may operate in one of four modes:

1. **Auto:** The port operates autonomously. It performs detection continuously until a valid PD is detected. Once a PD is found, classification is performed and the port is powered up as specified within its registers. Classification has no effect on the power-on step. When the AUTO pin is pulled high on power-up, the TPS23851 operates the four ports in auto mode. If the AUTO pin is pulled low, the operation is controlled by the system software through the I^2C interface. The power on setting of the AUTO pin can be changed at any time by the I^2C Operating Mode Registers. If the AUTO Mode is to be selected through I^2C while the AUTO pin voltage is low, additional registers also need to be changed accordingly. This includes the Interrupt Mask Register, Disconnect Enable Register, Detect/Class Enable Register.
2. **SemiAuto:** The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is not automatically turned on.
3. **Manual:** The port performs the functions indicated by its registers one time when Commanded. There is no automatic state change.
4. **Power Off:** The port is powered off and will not autonomously perform a detection, classification or power-on. In this mode, Status and Enable Bits for the associated port are reset.

Disconnect

Disconnect is the automated process of turning off power to the port. When the port is unloaded or at least falls below minimum load it is necessary to turn off power to the port and restart detection. Two methods of determining the port is below minimum load are AC disconnect and DC disconnect.

DC Disconnect

In DC disconnect, the voltage across the sense resistors is measured. When enabled, the DC disconnect function monitors the sense resistor voltage of a powered port to verify the port is drawing at least the minimum current to remain active. The T_{DIS} timer will count up whenever the port current is below a 7.5-mA threshold. If a timeout occurs, the port will be shut down and the corresponding disconnect bit in the Fault Event Register will be set. The T_{DIS} counter is reset each time the current goes continuously higher than the disconnect threshold for 17% of T_{MPDO}.

The timer will start counting from the beginning if an undercurrent condition occurs again. An internal 2-µs analog filter on the SENSE pin provides glitch filtering. The T_{DIS} duration is set by the T_{DIS} Bits of the Timing Configuration Register (0x16).

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AC Disconnect

The TPS23851 can detect a PD disconnect using AC or DC measurement.

AC disconnect consists in sensing the load impedance by injecting an AC voltage (110-Hz sinewave) at DETn pin and measuring the resultant current through the same pin. If the impedance is higher than a defined threshold, a timer (T_{DIS}) is started and if a time-out occurs the port is turned off.

Also, the corresponding disconnect bit (DISFn) in the Fault Event Register is set accordingly. The T_{DIS} counter is reset each time the impedance goes lower than the disconnect threshold.

Referring to Figure 32, each DETn pin is connected to its output port through a 1 kΩ in series with a 0.47 µF, both in parallel with a low leakage diode. The AC disconnect technique requires a diode to be inserted in series with the power MOSFET as shown in Figure 32. This diode must be a S1B or equivalent. Also, the capacitance across the port on PSE is critical for accurate detection and must be close to 0.1 µF. Also consider that ceramic capacitors are strongly dependent on DC bias voltage, capacitance going down substantially at higher voltage. For these reasons, using X7R type with 100-V rating or equivalent is required.

The A/D converter is used to perform AC disconnect detection. A port's AC disconnect current is measured as the DC equivalent of the full-wave rectified AC current that circulates in and out of the DETn pin.

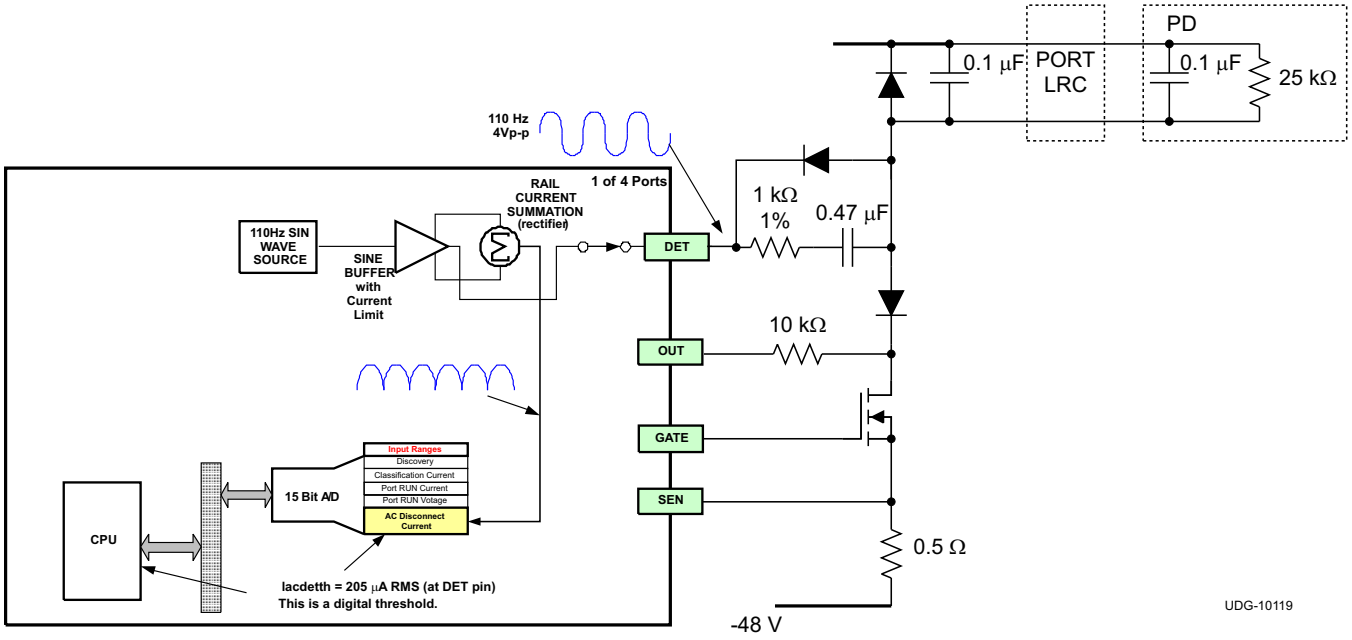

Figure 32. AC Disconnect Block Diagram

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I²C Timing While Using Isolators

The data communications used by TPS23851 is I²C fast mode to a maximum of 400 kHz. Repeated start is supported; there may not be a Stop bit before a repeated Start. Clock stretching is not supported. The TPS23851 is always a slave device. One of sixteen devices may be selected by a hex digit. Starting address is 20h.

Because of the high voltage for POE and the low-voltage computer communication systems, it is good practice to use isolation on I²C signals. Texas Instruments ISO724X galvanic isolation is recommended because of their 20-ns propagation delay and 2-ns rise and fall times.

Optical isolation may be used but careful device selection is needed to maintain proper transmission timing. The master provides SCLK for the slave devices. The TPS23851 respond with SDAO which is aligned to an SCLK delayed from the master by the isolators. The master receives SDAO after an isolation propagation delay time relative to the TPS23851 SDAO. With slower isolation devices it becomes difficult to maintain I²C setup and hold times over DATA, ACK, START and STOP conditions. An opto-isolator with less than 200-ns total propagation delay is required.

Other factors can have an effect on the propagation delay. For opto-isolation, set the input bias current to meet the desired propagation delay for the maximum forward current of the diode using the minimum input voltage. Then check the maximum power of the diode is not violated for minimum V_F and maximum supply voltage conditions.

The output side of the opto-isolator has a secondary delay because the signal rise/fall time is effected by the output pull-up resistor. The range of values for the output resistor used with an opto-isolator may be listed in its datasheet. Many factors including test result are needed to determine the best choice. The lower values are bounded by the maximum power dissipation of the device and managing the V_{OL}. As the output resistor value increases, the rise and fall time of the signal increase. The total propagation delay of the device is also increased. In this example the resistor range is 350 Ω to 4000 Ω. Signal rise and fall time with a 1-kΩ resistor is about 60 ns and is nearly 300 ns for 4 kΩ. Similarly, the propagation delay with a 1-kΩ resistor is about 50 ns and is about 85 ns for 1 kΩ. Based on other system conditions such as nominal voltage and temperature, a 2-kΩ output resistor is selected for test.

TPS23851 uses separate SDAI and SDAO lines to allow isolated I²C interface. SDAI can be connected to SDAO for non-isolated systems. Isolated or not, the SDAO must be mirrored on its SDAI for correct I²C operation. SDAO and SDAI are usually ORed on the I²C host side to become SDA, the single wire I²C host data signal. The I²C data integrity is best when the SDAI signal to TPS23851 has edges faster than 120 ns. The SDAO signal is an open drain output. It is rated for 5-mA output to meet a 0.7-V maximum V_{OL} The SDAO signal can sink higher current at increased V_{OL}. V_{OL} is not critical for receivers that do not have threshold inputs, the usual case for opto-isolators

Figure 33 shows the open drain output at SDAO with equivalent series impedance 78 Ω to 118 Ω.

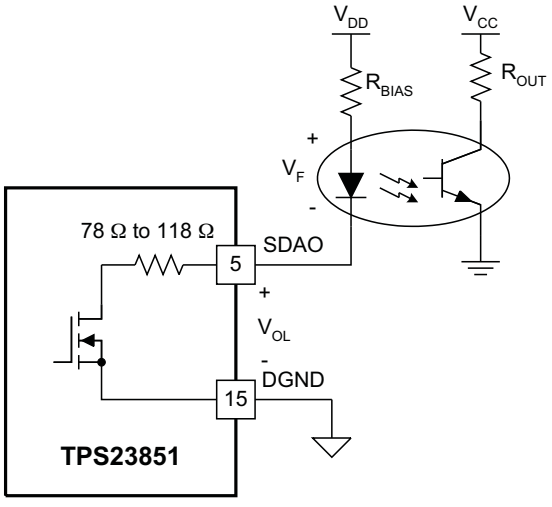

Figure 33. I²C Optocoupler Interface

Biasing Opto-Isolators

A worst case design for opto-isolators ensures operation over input voltage and temperature range. The following design example can be applied to any opto or system specifications. This example uses HCPL0631.

The bias on the isolator should meet minimum current specifications when the input voltage is minimum (3.0 V) and the temperature is high (85ºC). The bias is then checked when the the applied voltage is high (3.5 V) and the temperature is minimum (-20°C). The result is that the maximum forward current is within isolator specifications. Different vendors HCPL-0631 datasheets show minimum I_F from 5 mA to 6.7 mA. Allowing for specifiations and aging of the isolator, choose 6.3-mA minimum current. Next, use the isolator datasheet graphs to determine V_F at -20°C as 1.46 V and V_F at 85°C as 1.67 V.

NOTE

The Vf goes down at high temperature, while the Rdson of SDAO FET goes up, so that a worst case 1.67V at high temperature is a good assumption.

Minimum bias, low input voltage.

$$V_{SDAO} = 6.3\,mA \times 118\,\Omega = 0.74\,V \quad (1)$$

$$V_R = V_{DD} - V_{SDAO} - V_F = 3.0 - 0.74 - 1.67 = 0.59\,V \quad (2)$$

$$\frac{V_R}{V_F} = \frac{0.59\,V}{0.0063} = 93.6\,\Omega, \text{ use } 95.3\,\Omega \quad (3)$$

After setting low voltage bias, check for safe high voltage bias.

$$V = V_{DD} - V_F = 3.5\,V - 1.47\,V = 2.03\,V \quad (4)$$

$$I_F = \frac{V}{(R_{BIAS} + R_{SDAO})} = \frac{2.03}{(95.3 + 78)} = 11.7\,mA \quad (5)$$

Isolator data sheet specs 15 mA max.

I²C Watchdog

An I²C Watchdog time is available on the Texas Instruments TPS23851 device. When enabled, the timer will monitor the I²C, SCL line for clock edges. A timeout of the watchdog will reset the I²C interface along with any active ports. This feature provides protection in the event of rogue system software or I²C bus hang-up by slave devices. In the latter case, if a slave is attempting to send a data bit of “0” when the master stops sending clocks, then the slave could get stuck driving the data line low indefinitely. Since the data line is being driven low, the master cannot send a STOP to clean up the bus. Activating the I²C watchdog feature of the TPS23851 would clear this deadlocked condition. If the timer of 2 seconds expires, the ports will latch off and WD Status bit will be set. WD Status can only be cleared by a reset or writing a 0 to the WDS status bit location. The 4-bit watchdog disable field will shutdown this feature when a code of 1011b is loaded. This field is preset to 1011b whenever the TPS23851 is initially powered. The Watchdog Timer is divided from the main 7.4-MHz clock. Also see the I²C Watchdog Register for more details on the subject.

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Port Output Construction and Component Selection

Port output components can be seen in the applications schematic lower left, Figure 35. The output port has a TVS (D1) for protection against voltage transients. TheTVS shown was selected for 68-V breakdown, uni-directional, 600 W with less than 5-µA leakage. A 0.1 µF, X7R capacitor (C9) rated at 100 V provides minimal filtering and stability to the output.

The series RC (R7, C10) with parallel diode (D2) and Diode D3 are needed for AC disconnect only. These components are described in the AC disconnect section. If DC disconnect is used, they are omitted. MOSFET, Q2 is the port power switch controlled by the TPS23851. The MOSFET is used to power to the port connected device and also during classification.

TPS23851 reads the voltage at sense resistors (R13 and R14) to determine the port current. Port current is measured as the voltage drop across the external 0.5-Ω sense resistor. Two 1-Ω resistors wired in parallel are recommended. Two resistors improve the overall resistor tolerance and spread out the heat dissipation minimizing the effects of self heating.

Layout

Sense readback should be wired in a Kelvin connection to the sense resistors. It is important to read voltage directly across the sense resistor to get a true measure of the current to the port load. Do not use other sense or GND points that may be electrical equivalents to these signals in the design layout tool. Read errors will occur because of stray current from other sources. Similarly, care must be taken to keep the flow of port current direct from the power source, through the pass FET to the sense resistors and to the return . This will minimize crosstalk between port loads and provide accurate current sense.

Accurate current readings are essential because they are used for sensitive measurements such as DC disconnect, classification, port loading and output faults.

NOTE

For more details on TPS23851 layout recommendations, see TI document SLUU451.

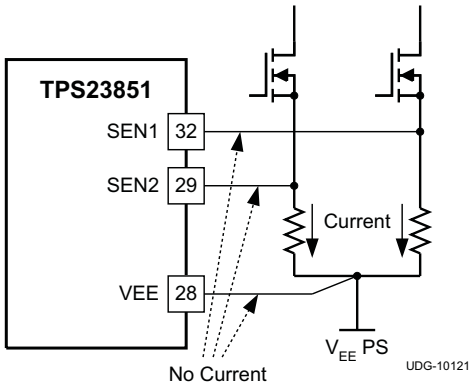

Figure 34. Current Sensing Resistor Layout

MOSFET Selection

MOSFET selection is based on a number of key parameters listed in the MOSFET datasheet. An N-channel MOSFET is used. The IRFM120A or equivalent is recommended.

- **V_{DS}:** The system voltage is 48 V and could operate as high as 53V. There must be some allowance for transients in inductive cables. Use 100-V parts as a good safety factor for 48-V systems.
- **$R_{DS(on)}$:** The on resistance of the MOSFET determines the power to be dissipated at a given load. The commonly used parts have about a 0.2-Ω on resistance
- **ID:** The current capability of the device, while important, is not sufficient for device selection. The maximum safe operating area curve gives the drain current (ID) vs drain-to-source voltage (VDS) curve. This is usually a family of curves for an on time duration. This data is given for 25°C. It must therefore be de-rated by the thermal response for pulse duration.

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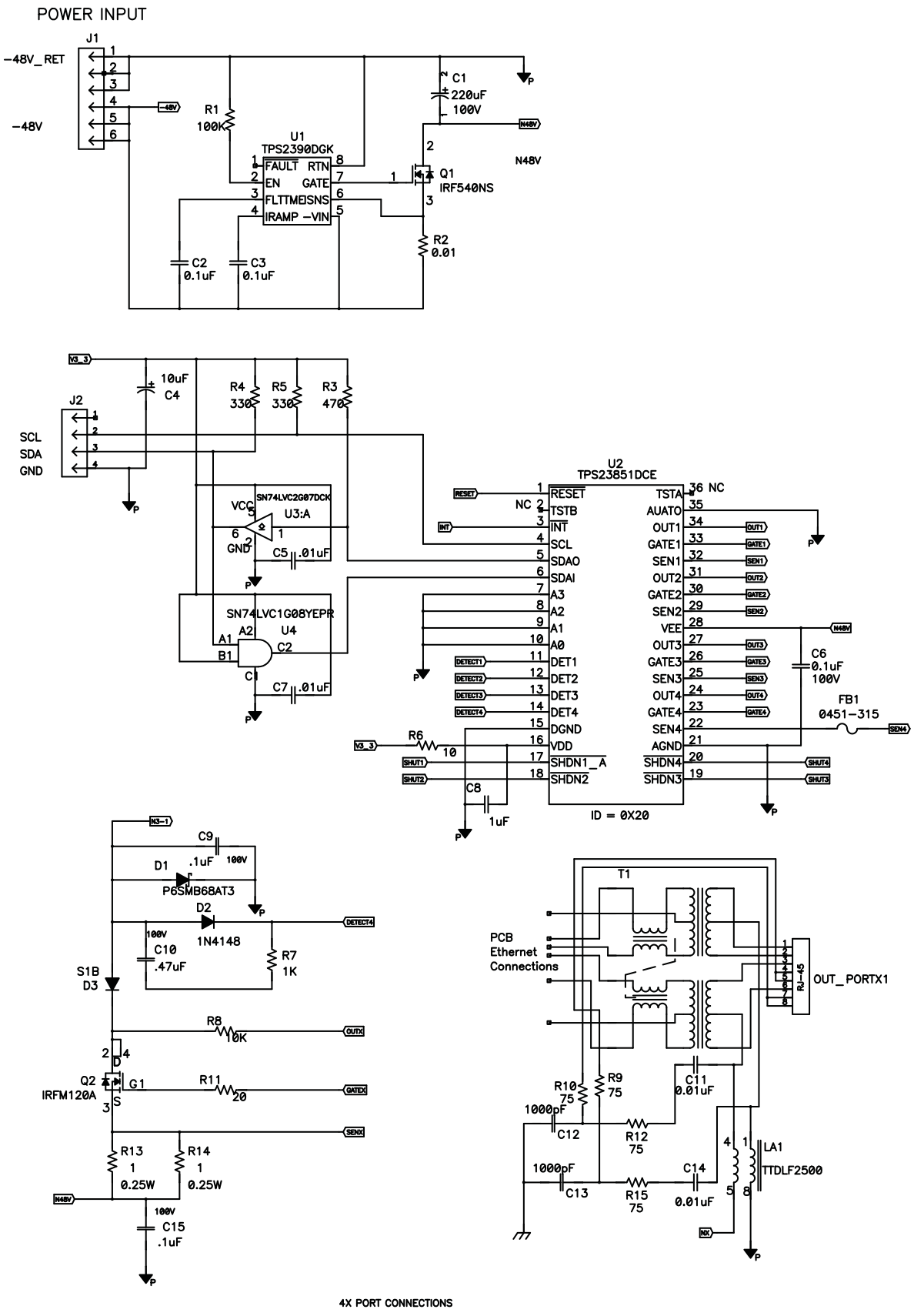

Figure 35. TPS23851 Application Schematic With AC Disconnect Detection

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Table 1. Summary of Main Registers (1)

CMD CODE	REGISTER OR COMMAND NAME	R/W	DATA BYTE	RST State	BITS DESCRIPTION							
00h	Interrupt	RO	1	1000,0000b	SUPF	STRTF	ICUTF	CLASC	DETC	DISF	PGC	PEC
01h	Interrupt mask	R/W	1	1AA0,0A00b	SUMSK	STMSK	ICMSK	CLMSK	DEMSK	DIMSK	PGMSK	PEMSK
02h	Power status	RO	1	0000,0000b	Power Good status change				Power Enable status change			
03h		CoR	1		PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
04h	Detection status	RO	1	0000,0000b	Classification occured				Detection occurred			
05h		CoR	1		CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
06h	Fault status	RO	1	0000,0000b	Disconnect occurred				ICUT fault occurred			
07h		CoR	1		DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
08h	Start status	RO	1	0000,0000b					START fault occurred			
09h		CoR	1		-	-	-	-	STRT4	STRT3	STRT2	STRT1
0Ah	Supply event	RO	1	0010,0010b	TSD	-	VDUV	VEUV	-	-	OSCF	-
0Bh		CoR	1									
0Ch	Port 1 status	RO	1	0000,0000b	-	CLASS Port 1			-	DETECT Port 1		
0Dh	Port 2 status	RO	1	0000,0000b	-	CLASS Port 2			-	DETECT Port 2		
0Eh	Port 3 status	RO	1	0000,0000b	-	CLASS Port 3			-	DETECT Port 3		
0Fh	Port 4 status	RO	1	0000,0000b	-	CLASS Port 4			-	DETECT Port 4		
10h	Power status	RO	1	0000,0000b	PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
11h	Pin status	RO	1	00,A[3:0],0,A	-	-	SLA3	SLA2	SLA1	SLA0	-	AUTO
12h	Operating mode	R/W	1	AAAA,AAAAb	Port 4 Mode		Port 3 Mode		Port 2 Mode		Port 1 Mode	
13h	Disconnect enable	R/W	1	AAAA,0000b	ACDE4	ACDE3	ACDE2	ACDE1	DCDE4	DCDE3	DCDE2	DCDE1
14h	Detect/class enable	R/W	1	AAAA,AAAAb	CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
16h	Timing configuration	R/W	1	0000,0000b	-		TSTART		TICUT		TDIS	
17h	General mask	R/W	1	1010,0000b	INTEN	-	OSCMSK	-	-	-	-	-
18h	Detect/class restart	WO	1	0000,0000b	RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1
19h	Power enable	WO	1	0000,0000b	POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	POWN1
1Ah	Reset	WO	1	0000,0000b	CLRAIN	CLINP	-	RESAL	RESP4	RESP3	RESP2	RESP1
1Bh	ID	RO	1	Mf[4:0],IC[2:0]	MFR ID				IC Version			
2Ah	ICUT21 configuration	R/W	1	0000,0000b	-	ICUT Port 2			-	ICUT Port 1		
2Bh	ICUT43 configuration	R/W	1	0000,0000b	-	ICUT Port 4			-	ICUT Port 3		

(1) A = Auto pin logical value at POR

Table 1. Summary of Main Registers (1) (continued)

CMD CODE	REGISTER OR COMMAND NAME	R/W	DATA BYTE	RST State	BITS DESCRIPTION							
30h	Port 1 current	RO	2	0000,0000b	Port 1 Current: LSByte							
31h		RO		0000,0000b	-	AC1	Port 1 Current: MSByte (bits 13 to 8)					
32h	Port 1 voltage	RO	2	0000,0000b	Port 1 Voltage: LSByte							
33h		RO		0000,0000b	-	-	Port 1 Voltage: MSByte (bits 13 to 8)					
34h	Port 2 current	RO	2	0000,0000b	Port 2 Current: LSByte							
35h		RO		0000,0000b	-	AC2	Port 2 Current: MSByte (bits 13 to 8)					
36h	Port 2 voltage	RO	2	0000,0000b	Port 2 Voltage: LSByte							
37h		RO		0000,0000b	-	-	Port 2 Voltage: MSByte (bits 13 to 8)					
38h	Port 3 current	RO	2	0000,0000b	Port 3 current: LSByte							
39h		RO		0000,0000b	-	AC3	Port 3 Current: MSByte (bits 13 to 8)					
3Ah	Port 3 voltage	RO	2	0000,0000b	Port 3 Voltage: LSByte							
3Bh		RO		0000,0000b	-	-	Port 3 Voltage: MSByte (bits 13 to 8)					
3Ch	Port 4 current	RO	2	0000,0000b	Port 4 current: LSByte							
3Dh		RO		0000,0000b	-	AC4	Port 4 Current: MSByte (bits 13 to 8)					
3Eh	Port 4 voltage	RO	2	0000,0000b	Port 4 Voltage: LSByte							
3Fh		RO		0000,0000b	-	-	Port 4 Voltage: MSByte (bits 13 to 8)					
40h	High power and sine disable	R/W	1	0000,0000b	HPW4	HPW3	HPW2	HPW1	SNDI	-	-	-
41h	Firmware revision	RO	1	0000,0RRRb	Firmware Revision							
42h	I^2C watchdog	R/W	1	0001,0110b				Watchdog Disable				WDS
43h	device ID	R/W	1	1010,0,sr[2:0]	Device ID number					Silicon Revision number		

Table 2. Special Function Registers

CMD CODE	REGISTER OR COMMAND NAME	R/W	DATA BYTES	RST STATE	BITS DESCRIPTION							
1Dh	Test enable	R/W	1	0000,0000b	Unlock code							
22h	Multiplexed shutdown configuration	R/W	1	0000,0000b	-			MUX shutdown config				
					-	-	-	MSE	MSE4	MSE3	MSE2	MSE1

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Interrupt Register
Command = 00h With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SUPF	STRTF	ICUTF	CLASC	DETC	DISF	PGC	PEC
RESET OR POR VALUE	1	0	0	0	0	0	0	0

Bit Descriptions

Active high, each bit corresponds to a particular event that occurred.

Each bit can be individually reset by doing a read at the corresponding event register address, or by setting bit 7 of Reset Register.

Any active bit of Interrupt Register will activate the $\overline{INT}$ output if its corresponding Mask bit in Interrupt Mask Register (01h) is set, as well as the INTEN bit in the General Mask Register.

SUPF: Indicates that a Supply Event Fault occurred.

SUPF = TSD || VDUV || VEUV || OSCF

- 1 = At least one Supply Event Fault occurred
- 0 = No such event occurred

STRTF: Indicates that a t_{START} fault occurred on at least one port.

STRTF = STRT1 || STRT2 || STRT3 || STRT4

- 1 = t_{START} fault occurred for at least one port
- 0 = No t_{START} fault occurred

ICUTF: Indicates that a t_{ICUT} fault occurred on at least one port.

ICUTF = ICUT1 || ICUT2 || ICUT3 || ICUT4

- 1 = t_{ICUT} fault occurred for at least one port
- 0 = No t_{ICUT} fault occurred

CLASC: Indicates that at least one classification cycle occurred on at least one port.

CLASC = CLSC1 || CLSC2 || CLSC3 || CLSC4

- 1 = At least one classification cycle occurred for at least one port
- 0 = No classification cycle occurred

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DETC: Indicates that at least one detection cycle occurred on at least one port.

DETC = DETC1 || DETC2 || DETC3 || DETC4

- 1 = At least one detection cycle occurred for at least one port
- 0 = No detection cycle occurred

DISF: Indicates that a disconnect event occurred on at least one port.

DISF = DISF1 || DISF2 || DISF3 || DISF4

- 1 = Disconnect event occurred for at least one port
- 0 = No disconnect event occurred

PGC: Indicates that a power good status change occurred on at least one port.

PGC = PGC1 || PGC2 || PGC3 || PGC4

- 1 = Power good status change occurred on at least one port
- 0 = No power good status change occurred

PEC: Indicates that a power enable status change occurred on at least one port.

PEC = PEC1 || PEC2 || PEC3 || PEC4

- 1 = Power enable status change occurred on at least one port
- 0 = No power enable status change occurred

NOTE

The register pointer is always reset after a Stop Bit on I^2C bus. This allows a quick access to the interrupt register through I^2C bus.

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Interrupt Mask Register
Command = 01h with 1 Data Byte, Read/Write(1)

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SUMSK	STMSK	ICMSK	CLMSK	DEMSK	DIMSK	PGMSK	PEMSK
RESET OR POR VALUE	1	A	A	0	0	A	0	0

(1) A = Auto pin logical value at POR

Bit Descriptions

Each bit corresponds to a particular event or fault as defined in the Interrupt Register.

Writing a 0 into a bit will mask the corresponding event/fault from activating the $\overline{INT}$ output.

NOTE

1. The bits of the Interrupt Register always change state according to events or faults, regardless of the state of the state of the Interrupt Mask Register.
2. The INTEN bit of the General Mask Register must also be set in order to allow an event to activate the $\overline{INT}$ output.

SUMSK: Supply Event Fault mask bit.
- 1 = Supply event fault will activate the $\overline{INT}$ output.
- 0 = Supply event fault will have no impact on $\overline{INT}$ output.

STMSK: t_{START} fault mask bit.
- 1 = t_{START} fault will activate the $\overline{INT}$ output.
- 0 = t_{START} fault will have no impact on $\overline{INT}$ output.

ICMSK: t_{ICUT} fault mask bit.
- 1 = t_{ICUT} fault occurrence will activate the $\overline{INT}$ output.
- 0 = t_{ICUT} fault occurrence will have no impact on $\overline{INT}$ output.

CLMSK: Classification cycle mask bit.
- 1 = Classification cycle occurrence will activate the $\overline{INT}$ output.
- 0 = Classification cycle occurrence will have no impact on $\overline{INT}$ output

DEMSK: Detection cycle mask bit.
- 1 = Detection cycle occurrence will activate the $\overline{INT}$ output.
- 0 = Detection cycle occurrence will have no impact on $\overline{INT}$ output.

DIMSK: Disconnect event mask bit.
- 1 = Disconnect event occurrence will activate the $\overline{INT}$ output.
- 0 = Disconnect event occurrence will have no impact on $\overline{INT}$ output.

PGMSK: Power good status change mask bit.
- 1 = Power-good status change will activate the $\overline{INT}$ output.
- 0 = Power-good status change will have no impact on $\overline{INT}$ output.

PEMSK: Power Enable status change mask bit.
- 1 = Power enable status change will activate the $\overline{INT}$ output.
- 0 = Power enable status change will have no impact on $\overline{INT}$ output.

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Power Event Register
Command = 02h with 1 Data Byte, Read Only
Command = 03h With 1 Data Byte, Clear On Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual port.

A read at each location (02h or 03h) returns the same register data with the exception that the Clear on Read Command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear on Read will release the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

PGC4-PGC1: Indicates that a power-good status change occurred.

- 1 = Power-good status change occurred
- 0 = No power good status change occurred

PEC4-PEC1: Indicates that a power enable status change occurred.

- 1 = Power enable status change occurred
- 0 = No power enable status change occurred

Detection Event Register
Command = 04h With 1 Data Byte, Read Only
Command = 05h With 1 Data Byte, Clear On Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Active high, each bit corresponds to a particular event that occurred.

Each bit xxxx1-4 represents an individual port.

A read at each location (04h or 05h) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear on Read will release the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

CLSC4- CLSC1: Indicates that at least one classification cycle occurred.

- 1 = At least one classification cycle occurred
- 0 = No classification cycle occurred

DETC4-DETC1: Indicates that at least one detection cycle occurred.

- 1 = At least one detection cycle occurred
- 0 = No detection cycle occurred

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Fault Event Register
Command = 06h With 1 Data Byte, Read Only
Command = 07h With 1 Data Byte, Clear On Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Active high, each bit corresponds to a particular event that occurred.

Each bit xxxx1-4 represents an individual port.

A read at each location (06h or 07h) returns the same register data with the exception that the Clear on Read Command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear on Read will release the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

DISF4-DISF1: Indicates that a disconnect event occurred.

- 1 = Disconnect event occurred
- 0 = No disconnect event occurred

ICUT4-ICUT1: Indicates that a t_{ICUT} fault occurred.

- 1 = t_{ICUT} fault occurred
- 0 = No t_{ICUT} fault occurred

Start Event Register
Command = 08h with 1 Data Byte, Read Only
Command = 09h With 1 Data Byte, Clear On Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	-	-	STRT4	STRT3	STRT2	STRT1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Active high, each D3-D0 bit corresponds to a particular event that occurred.

Each bit xxxx1-4 represents an individual port. Bits D7-D4 are reserved for future use.

A read at each location (08h or 09h) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear on Read will release the $\overline{INT}$ pin.

Any active bit will have an impact on the INTERRUPT register as indicated in the INTERRUPT register description.

STRT4-STRT1: Indicates that a tSTART Fault occurred.

- 1 = t_{START} fault occurred
- 0 = No t_{START} fault occurred

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Supply Event Register
Command = 0Ah with 1 Data Byte, Read Only
Command = 0Bh With 1 Data Byte, Clear On Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TSD	-	VDUV	VEUV	-	-	OSCF	-
POR VALUE IF VDD COMES UP FIRST	0	0	1	1	0	0	1	0
POR VALUE IF VEE COMES UP FIRST	0	0	1	0	0	0	1	0

Bit Descriptions

Active high, each bit corresponds to a particular event that occurred.

Bits D6, D3, D2 and D0 are reserved for future use.

A read at each location (0Ah or 0Bh) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear on Read will release the $\overline{INT}$ pin.

Any active bit will have an impact on Interrupt Register as indicated in the Interrupt Register description.

TSD: Indicates that a thermal shutdown occurred.
- 1 = Thermal shutdown occurred
- 0 = No thermal shutdown occurred

VDUV: Indicates that a VDD UVLO occurred. This means that a power-on reset occurred.
- 1 = VDD UVLO occurred
- 0 = No VDD UVLO occurred

VEUV: Indicates that a VEE UVLO occurred while VDD was maintained higher than its UVLO threshold.
- 1 = VEE UVLO occurred
- 0 = No VEE UVLO occurred

OSCF: Indicates that an invalid AC disconnect oscillator condition occurred.
- 1 = Invalid AC disconnect oscillator condition occurred
- 0 = No invalid AC disconnect oscillator condition occurred

NOTE

1. If the $\overline{RESET}$ input is pulled low during normal operation, the OSCF bit will be set while the VEUV will be set if VEE is below its UVLO threshold. There is no impact on VDUV since VDD is maintained.
2. When VEE UVLO condition occurs while ports are ON, these ports are turned off and the Power Status and Power Event Registers are updated accordingly.

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Port 1 Status Register
Command = 0Ch With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	CLASS P1			-	DETECT P1		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 2 Status Register
Command = 0Dh With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	CLASS P2			-	DETECT P2		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 3 Status Register
Command = 0Eh With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	CLASS P3			-	DETECT P3		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 4 Status Register
Command = 0Fh With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	CLASS P4			-	DETECT P4		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

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Bit Descriptions:

Represents the most recent classification and detection results for port n. These bits are cleared when port n is turned off.

CLASS Pn: Most recent classification result on Port n.

The selection is as following:

Table 3. Classification Result On Port n

CLASS Pn			CLASS STATUS
0	0	0	unknown
0	0	1	Class 1
0	1	0	Class 2
0	1	1	Class 3
1	0	0	Class 4
1	0	1	Reserved – read as Class 0
1	1	0	Class 0
1	1	1	Overcurrent

DETECT Pn: Most recent detection result on port n.

The selection is as following:

Table 4. Detection Result On Port n(1)

DETECT Pn			DETECT STATUS
0	0	0	unknown
0	0	1	Short-circuit (< 150 Ω)
0	1	0	Reserved
0	1	1	Too Low
1	0	0	Valid
1	0	1	Too High
1	1	0	Open Circuit
1	1	1	Reserved

(1) Code 000 is shown as “Unknown” which is the code to indicate that the PSE controller has never has never inspected the port since the last reset. Once a least one detection cycle has completed, the result will never occur again.

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Power Status Register
Command = 10h With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Each bit represents the actual power status of a port.

Each bit xx1-4 represents an individual port.

PG4-PG1: Each bit, when at 1, indicates that the port is on and that the voltage at OUTn pin has gone below the power good threshold during the port turn on.

These bits are latched high once the turn on is complete and can only be cleared when the port is turned off or at reset/POR.

- 1 = Power is good
- 0 = Power is not good

PE4-PE1: Each bit indicates the ON/OFF state of the corresponding port. Each bit is set to 1 when the PSE controller is attempting to supply power to the port. The bit remains at 1 for all conditions while power is applied, regardless of the actual port voltage or if some other functions, such as foldback, is limiting power to the port.

PEx is zero when the PSE is not trying to power the port, regardless of the port voltage. For example if power is being removed but the port has not fully discharged the status will report 0 as the PSE is not trying to power the port.

- 1 = Port is on
- 0 = Port is off

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Pin Status Register
Command = 11h With 1 Data Byte, Read Only(1)

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	SLA3	SLA2	SLA1	SLA0	-	AUTO
RESET OR POR VALUE	0	0	A3 pin	A2 pin	A1 pin	A0 pin	-	A

(1) A = Auto pin logical value at POR.

Bit Descriptions

AUTO: State of the AUTO pin.

- 1 = AUTO is high
- 0 = AUTO is low

The logic state of the AUTO pin at POR determines the preset state for multiple registers of the TPS23851. After POR is complete, the state of the AUTO pin is reflected in bit D0 of the Pin Status Register only. In some applications, this behavior enables the AUTO pin to be used as a discrete input after POR.

SLA3-SLA0: State of A3-A0 pins representing the I^2C slave address.

Table 5. A3-A0 Pins Representing the I^2C Slave Address

DESCRIPTION	BINARY device ADDRESS							ADDRESS PINS			
	6	5	4	3	2	1	0	A3	A2	A1	A0
BROADCAST ACCESS	0	1	1	0	0	0	0	X	X	X	X
ALERT RESPONSE	0	0	0	1	1	0	0	X	X	X	X
SLAVE 0	0	1	0	0	0	0	0	GND	GND	GND	GND
SLAVE 1	0	1	0	0	0	0	1	GND	GND	GND	HIGH
SLAVE 2	0	1	0	0	0	1	0	GND	GND	HIGH	GND
SLAVE 3	0	1	0	0	0	1	1	GND	GND	HIGH	HIGH
SLAVE 4	0	1	0	0	1	0	0	GND	HIGH	GND	GND
SLAVE 5	0	1	0	0	1	0	1	GND	HIGH	GND	HIGH
SLAVE 6	0	1	0	0	1	1	0	GND	HIGH	HIGH	GND
SLAVE 7	0	1	0	0	1	1	1	GND	HIGH	HIGH	HIGH
SLAVE 8	0	1	0	1	0	0	0	HIGH	GND	GND	GND
SLAVE 9	0	1	0	1	0	0	1	HIGH	GND	GND	HIGH
SLAVE 10	0	1	0	1	0	1	0	HIGH	GND	HIGH	GND
SLAVE 11	0	1	0	1	0	1	1	HIGH	GND	HIGH	HIGH
SLAVE 12	0	1	0	1	1	0	0	HIGH	HIGH	GND	GND
SLAVE 13	0	1	0	1	1	0	1	HIGH	HIGH	GND	HIGH
SLAVE 14	0	1	0	1	1	1	0	HIGH	HIGH	HIGH	GND
SLAVE 15	0	1	0	1	1	1	1	HIGH	HIGH	HIGH	HIGH

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Operating Mode Register
Command = 12h With 1 Data Byte, R/W(1)

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	P4M1	P4M0	P3M1	P3M0	P2M1	P2M0	P1M1	P1M0
RESET OR POR VALUE	A	A	A	A	A	A	A	A

(1) A = Auto pin logical value at POR.

Bit Descriptions

Each pair of bits configures the operating mode per port.

The selection is as following:

Table 6. Bits Configuration

M1	M0	OPERATING MODE
0	0	OFF
0	1	Manual
1	0	Semi Auto
1	1	Auto

In OFF Mode, the port is OFF and there is no detection nor classification. In Manual Mode, there is no automatic state change. In Semi Auto Mode, detection and class are automated but not the port power on, while in Auto Mode all three are automated.

Disconnect Enable Register
Command = 13h With 1 Data Byte, R/W(1)

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ACDE4	ACDE3	ACDE2	ACDE1	DCDE4	DCDE3	DCDE2	DCDE1
RESET OR POR VALUE	A	A	A	A	0	0	0	0

(1) A = Auto pin logical value at POR.

Bit Descriptions

Defines the disconnect detection mechanism for each port.

ACDE4-ACDE1: AC disconnect enable. AC disconnect consists in sensing the load impedance by injecting an AC voltage and measuring the resultant current. If the impedance is higher than a defined threshold, a timer (T_{DIS}) is started and if a timeout occurs the port is turned off. Also, the corresponding disconnect bit (DISFn) in the Fault Event Register is set accordingly. The T_{DIS} counter is reset each time the impedance goes lower than the disconnect threshold.

NOTE

The A/D converter is used to perform AC disconnect detection.

DCDE4-DCDE1: DC disconnect enable. DC disconnect consists in measuring the port DC current at SENn, starting a timer (T_{DIS}) if this current is below a threshold and turning the port off if a timeout occurs. Also, the corresponding disconnect bit (DISFn) in the Fault Event Register is set accordingly. The T_{DIS} counter is reset each time the current goes continuously higher than the disconnect threshold for 17% of T_{MPDO}.

NOTE

DC disconnect detection is performed by use of an analog comparator.

Look at the Timing Configuration Register for more details on how to define the T_{DIS} time period.

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Detect/Class Enable Register Command = 14h With 1 Data Byte, R/W(1)

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
RESET OR POR VALUE	A	A	A	A	A	A	A	A

(1) A = Auto pin logical value at POR.

Bit Descriptions

Detection and classification enable for each port.

When in Manual Mode, setting a bit means that only one cycle (detection or classification) is performed for the corresponding port. The bit is automatically cleared when the cycle has been completed.

NOTE

1. Similar result can be obtained by writing to the Detect/Class Restart Register.
2. A classification is done while using the external MOSFET so that doing a classification on more than one port at same time is possible without overdissipation in the TPS23851.

CLE4-CLE1: Classification enable bits.

DETE4-DETE1: Detection enable bits.

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Timing Configuration Register
Command = 16h With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	TSTART		TICUT		TDIS	
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

These bits define the timing configuration for all four ports.

TSTART: START fault timing, which is the maximum allowed overcurrent time during inrush.

The selection is as following:

Table 7. TSTART: Start fault timing

TSTART		NOMINAL T_{START} (ms)
0	0	60
0	1	30
1	0	120
1	1	240

TICUT: I_{CUT} fault timing, which is the overcurrent time duration before port turn off.

This timer is active and increments to the settings defined below after expiration of the T_{START} time window and when the port current meets or exceeds I_{CUT}. If the I_{CUT} counter is allowed to reach the programmed time-out duration specified below, the port will be powered off. The counter continues to operate when the port is off (counting down) and the port can not be turned-on until the counter has reached a count of zero. When the port current is below I_{CUT}, while there is no foldback action, the same counter decrements at a rate $1/16^{th}$ of the increment rate. The counter does not decrement below zero.

The selection is as following:

Table 8. TICUT: ICUT Fault Timing

TICUT		NOMINAL T_{ICUT} (ms)
0	0	60
0	1	30
1	0	120
1	1	240

TDIS: Disconnect delay, which is the time to turn off a port once there is a disconnect condition, and if at least one of the two disconnect detect methods has been enabled.

The selection is as following:

Table 9. TDIS: Disconnect Delay

TDIS		NOMINAL T_{DIS} (ms)
0	0	360
0	1	90
1	0	180
1	1	720

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General Mask Register
Command = 17h With 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	INTEN	-	OSCMSK	-	-	-	-	-
RESET OR POR VALUE	1	-	1	-	-	-	-	-

Bit Descriptions

INTEN: $\overline{\text{INT}}$ pin mask bit. Writing a 0 will mask any bit of Interrupt Register from activating the $\overline{\text{INT}}$ output, whatever the state of the Interrupt Mask Register. Note that activating INTEN has no impact on the event registers.

- 1 = Any unmasked bit of Interrupt Registercan activate the $\overline{\text{INT}}$ output
- 0 = $\overline{\text{INT}}$ output cannot be activated

OSCMSK: AC disconnect oscillator mask bit. If cleared, an oscillator failure will not set the OSCF bit of the Supply Event Register.

- 1 = An invalid oscillator condition will set the OSCF bit of Supply Event Register
- 0 = OSCF bit of Supply Event Register will stay low whatever the condition of the oscillator

Detect/Class Restart Register
Command = 18h With 1 Data Byte, Write only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Each bit corresponds to a particular event per port.

Each event can be individually triggered by writing a “1” at that bit location, while writing a “0” does not change anything for that event.

In Manual mode, a single event will be triggered while in Auto or Semiauto mode, it sets the corresponding bit in the Detect/Class Enable Register.

A Read operation will return 00h.

NOTE

A classification is done while using the external MOSFET so that doing a classification on all ports at same time is allowed.

RCL4-RCL1: Restart classification bits.

DETE4-DETE1: Restart detection bits.

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Power Enable Register
Command = 19h With 1 Data Byte, Write Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	PWON1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Used to force an immediate port(s) turn on or turn off in any mode except Shutdown Mode, regardless of the classification and detection status.

Writing a “1” at that PWONn bit location turns ON the corresponding port, while writing a “1” at POFFn location turns it off.

NOTE

1. Writing a “1” at POFFn and PWONn of same port during the same write operation turns the port off.
2. t_{ICUT}, t_{START} and disconnect events are prioritary over the power on command. During t_{ICUT} or t_{START} cool down cycle, any port turn on using Power Enable Command will be ignored and the port will be kept off.

Turning OFF a port with this command also clears the corresponding bits in Detection Event Register (CLSCn, DETCn), Fault Event Register (DISFn, ICUTn), Start Event Register (STRTn), Port n Status Register (Class Pn, Detect Pn) and Detect/Class Enable Register (CLEn, DETEn).

The corresponding PGCn and PECn Bits of Power Event Register will also be set if there is a change.

NOTE

Note that following a port turn off, it is required to wait at least 2 ms before enabling detection or classification for this port.

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Reset Register
Command = 1Ah With 1 Data Byte, Write Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLRAIN	CLINP	-	RESAL	RESP4	RESP3	RESP2	RESP1
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Writing a “1” at a bit location triggers an event while a “0” has no impact.

CLRAIN: Clear all interrupts bit. Writing a “1” to CLRAIN clears all event registers and all bits in the Interrupt Register. It also releases the $\overline{\text{INT}}$ pin.

CLINP: When set, it releases the $\overline{\text{INT}}$ pin without any impact on the Event Registers nor on the Interrupt Register.

RESAL: Reset all bits when RESAL is set. Results in a state equivalent to a power-up reset, including a reread of the Auto pin. Note that the VDUV and VEUV Bits (Supply Event Register) follow the state of VDD and VEE supply rails. Also OSCF (Supply Event Register) will become set regardless of its prior state.

RESP4-RESP1: Reset Port Bits. Used to force an immediate port(s) turn off in any mode, by writing a “1” at the corresponding RESPn bit location(s).

Turning OFF a port with this command also clears the corresponding bits in Detection Event Register (CLSCn, DETCn), Fault EVENT Register (DISFn, ICUTn), Start Event Register (STRTn), Port n Status Register (Class Pn, Detect Pn) and DEtect/Class Enable Register (CLEn, DETEn).

The corresponding PGCn and PECn Bits of POWER EVENT register will also be set if there is a change.

NOTE

Following a port reset or Reset all, it is required to wait at least 2 ms before enabling detection or classification for this port.

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ID Register
Command = 1Bh With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	MFR ID					ICV		

Bit Descriptions

MFR ID: Manufacture Identification number (0110)

ICV: Device version number (100)

ICUT21 Configuration Register
Command = 2Ah With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	ICUT P2			-	ICUT P1		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

ICUT43 Configuration Register
Command = 2Bh With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	ICUT P4			-	ICUT P3		
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Defines the I_{CUT} threshold as following:

Table 10. ICUT Threshold

ICUT Pn			I_{CUT} (mA) if 0.5 Ω R_{SENSE}
0	0	0	374
0	0	1	110
0	1	0	204
0	1	1	374
1	0	0	754 (1)
1	0	1	592 (1)
1	1	0	686 (1)
1	1	1	816 (1)

(1) If ICUT Pn is defined from 100 to 111 inclusively, the port 2X mode bit of High Power and Sine Disable Register must be set, in order to make sure that $I_{LIM} > I_{CUT}$. If I_{LIM} is programmed lower than I_{CUT} , the I_{CUT} will not be activated in certain fault situations and damage to the power MOSFET or the load will likely occur.

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Port 1 Current Register
Command = 30h With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	I1_7	I1_6	I1_5	I1_4	I1_3	I1_2	I1_1	I1_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	I1_13	I1_12	I1_11	I1_10	I1_9	I1_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 2 Current Register
Command = 34h With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	I2_7	I2_6	I2_5	I2_4	I2_3	I2_2	I2_1	I2_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	I2_13	I2_12	I2_11	I2_10	I2_9	I2_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

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Port 3 Current Register
Command = 38h With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	I3_7	I3_6	I3_5	I3_4	I3_3	I3_2	I3_1	I3_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	I3_13	I3_12	I3_11	I3_10	I3_9	I3_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 4 Current Register
Command = 3Ch With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	I4_7	I4_6	I4_5	I4_4	I4_3	I4_2	I4_1	I4_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	I4_13	I4_12	I4_11	I4_10	I4_9	I4_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Data conversion result. The I^2C data transmission is a 2-byte transfer.

NOTE

The conversion is done using a TI proprietary multi-slope integrating converter.

In_13- In_0: 14-bit data conversion result of current for port n. The result varies depending on the operating mode.

The equation defining the current measured is:

$$I = N \times I_{STEP} \quad (6)$$

Where I_{STEP} is defined below as well as the full scale value, according to the operating mode:

Table 11. ISTEP Definition(1)

MODE	FULL SCALE VALUE	ISTEP_14 BITS
Port Powered	1 A (with 0.5 Ω R_{SENSE})	61.035 µA
Classification	100 mA (with 0.5 Ω R_{SENSE})	6.1035 µA

(1) The content of the Port n Current Register is not updated when the port is off.

Any port reading should be qualified with the PGn bit of the Power Status Register (10h). If the port bit is a 1, then the reading should be accepted. If zero, the A/D reading should be considered corrupt as it may represent a port that experienced a power fault event or was disabled midway through a conversion.

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Port 1 Voltage Register
Command = 32h With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	V1_7	V1_6	V1_5	V1_4	V1_3	V1_2	V1_1	V1_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	V1_13	V1_12	V1_11	V1_10	V1_9	V1_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 2 Voltage Register
Command = 36h With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	V2_7	V2_6	V2_5	V2_4	V2_3	V2_2	V2_1	V2_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	V2_13	V2_12	V2_11	V2_10	V2_9	V2_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

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Port 3 Voltage Register
Command = 3Ah With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	V3_7	V3_6	V3_5	V3_4	V3_3	V3_2	V3_1	V3_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	V3_13	V3_12	V3_11	V3_10	V3_9	V3_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Port 4 Voltage Register
Command = 3Eh With 2 Data Byte (LSByte first, MSByte second), Read Only

LSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	V4_7	V4_6	V4_5	V4_4	V4_3	V4_2	V4_1	V4_0
RESET OR POR VALUE	0	0	0	0	0	0	0	0
MSB								
BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	-	V4_13	V4_12	V4_11	V4_10	V4_9	V4_8
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Data conversion result. The I^2C data transmission is a 2-byte transfer.

Vn_13- Vn_0: 14-bit data conversion result of voltage for port n.

The equation defining the current measured is:

$$V = N \times V_{STEP} \quad (7)$$

Where V_{STEP} is defined below as well as the full scale value:

Table 12. VSTEP Definition(1)(2)

MODE	FULL SCALE VALUE	V_{STEP} 14 BITS
Port Powered	97 V	5.920 mV

(1) A powered port voltage measurement is made between OUTn and AGND.
(2) The content of the Port n Voltage Register is not updated when the port is off.

Any port reading should be qualified with the PGn bit of the Power Status Register (10h). If the port bit is a 1, then the reading should be accepted. If zero, the A/D reading should be considered corrupt as it may represent a port that experienced a power fault event or was disabled midway through a conversion.

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High Power and Sine Disable Register Command = 40h With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	HPW4	HPW3	HPW2	HPW1	SNDI	-	-	-
RESET OR POR VALUE	0	0	0	0	0	-	-	-

Bit Descriptions

HPW4- HPW1: When set, this activates the high power (2X) mode for a port which increases its I_{LIM} and I_{SHORT} levels to around two times its normal settings. In any of these modes, the I_{CUT} timer still starts when the I_{CUT} threshold is exceeded.

NOTE

1. If I_{CUT} Pn (see ICUTxx Configuration Register) is defined from 100 to 111 inclusively, the port 2X mode bit of High Power and Sine Disable Register must be set, in order to make sure that $I_{LIM} > I_{CUT}$. If I_{LIM} is programmed lower than I_{CUT} , the I_{CUT} will not be activated in certain fault situations and damage to the power MOSFET or the load will likely occur.
2. A linear foldback mechanism measures the port voltage across AGND and OUTn to reduce the current limit threshold from 100% at 18 V (28 V if in 2X mode) down to around 14% at a port voltage of 0 V.

SNDI: When set, this deactivates the internal sinewave generator used for AC disconnect function. If AC disconnect is used, this bit should always be maintained to 0.

NOTE

Manually setting and resetting SNDI clears the OSCF bit of the Supply Event Register.

Firmware Revision Register Command = 41h With 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	-	-	-	FRV		

Bit Descriptions

FRV: Firmware revision number

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I²C Watchdog Register
Command = 42h With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	-	IWDD3	IWDD2	IWDD1	IWDD0	WDS
RESET OR POR VALUE	-	-	-	1	0	1	1	0

Bit Descriptions

The I²C watchdog timer monitors the I²C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on SCL input. If the watchdog timer expires, all ports will be turned off and WDS bit will be set. The nominal watchdog time-out period is 2 seconds.

IWD3- IWD0: I²C watchdog disable. When equal to 1011b, the watchdog is masked. Otherwise, it is umasked and the watchdog is operational.

WDS: I²C Watchdog Timer Status, valid even if the watchdog is masked. When set, it means that the watchdog timer has expired without any activity on I²C clock line. Writing 0 at WDS location clears it. Note that when the watchdog timer expires, all ports are also turned off.

Device ID Register
Command = 43h With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID			-	-	SR		

Bit Descriptions

DID: device ID number (101)

SR: Silicon revision number

NOTE

This is a R/W register. The initial state after power up can be modified by writing to this register.

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Test Enable Register
Command = 1Dh With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	UNLOCK CODE							
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Unlock Code: Gives access to the Multiplexed Shutdown Configuration Register.

BCh = Unlocks the access to Multiplexed Shutdown Configuration Register Any value else than

BCh = Locks the access to Multiplexed Shutdown Configuration Register.

NOTE

1. At power up, the Multiplexed Shutdown Configuration Register is locked. Unlocking the access to this register also gives access to special test modes registers as well as the internal microprocessor's working memory which must not be used in the application. In order to prevent any accidental write operation, it is highly recommended to keep the Multiplexed Shutdown Configuration Register locked in any circumstance except during the time when it needs to be reconfigured. Once the multiplexed shutdown has been reconfigured, it is highly recommended to lock the access to it by writing any value else than BCh in the Test Enable Register.
2. Once the lock code has been written once into the Test Enable Register, the procedure to reprogram the Multiplexed Shutdown Configuration Register is:
   - Write BCh into Test Enable Register: unlock code
   - The I^2C device address becomes 20h until the next lock code
   - Write the configuration byte in Multiplexed Shutdown Configuration Register
   - Write 00h into Test Enable Register: lock code, still with device address equal to 20h
   - After that operation, the I^2C device address stops being equal to 20h and becomes again defined using the address pins, as described in the Pin Status Register

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Multiplexed Shutdown Configuration Register Command = 22h With 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	-	MSE	MSE4	MSE3	MSE2	MSE1
RESET OR POR VALUE	-	-	-	0	0	0	0	0

Bit Descriptions

Used to quickly turn off ports using the $\overline{\text{SHDN1_A}}$ pin.

MSE: Multiplexed Shutdown Enable bit. Used to quickly turn off ports using the $\overline{\text{SHDN1_A}}$ pin.

- 1 = $\overline{\text{SHDN1_A}}$ pin can quickly turn off active port(s) having the corresponding bit(s) in Multiplexed Shutdown Configuration Register being set.
- 0 = $\overline{\text{SHDN1_A}}$ pin has no impact on the status of output ports 2 to 4. The pin can turn off port 1 only.

NOTE

If the Multiplexed Shutdown Function is enabled, the $\overline{\text{SHDN2}}$ to $\overline{\text{SHDN4}}$ inputs must be at logic high.

MSE1-4: Used to quickly turn off ports using the $\overline{\text{SHDN1_A}}$ pin, if MSE bit of Multiplexed Shutdown Enable Register is set. Each bit corresponds to one particular port. If MSE bit of Multiplexed Shutdown Enable Register is set:

- 1 = $\overline{\text{SHDN1_A}}$ going low pin will quickly turn off the port.
- 0 = $\overline{\text{SHDN1_A}}$ pin has no impact on the port.

NOTE

In order to have access to the Multiplexed Shutdown Configuration Register, refer to the Test Enable Register.

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REVISION HISTORY

Changes from Original (September 2010) to Revision A **Page**

- Added Slew rate to the RECOMMENDED OPERATING CONDITIONS table 3
- Changed the DESCRIPTION of Pin 16 (VDD) 10
- Changed the DESCRIPTION of Pins 32, 29, 25 (SEN1-3) 10
- Changed the DESCRIPTION of Pin 22 (SEN4) 10
- Changed the DESCRIPTION of Pins 33, 30, 26, 23 (GAT1-4) 10
- Changed the DESCRIPTION of Pins 34, 31, 27, 24 (OUT1-4) 10
- Changed the DESCRIPTION of Pin 28 (VEE) 10
- Changed Figure 14 15
- Changed 1 µF to 0.1 µF in Figure 23 18
- Changed 1 µF to 0.1 µF in Figure 32 26

Changes from Revision A (May 2013) to Revision B **Page**

- Changed t_{ED} - Error delay timing From: MAX = 750 ms To: MIN = 750 ms 7

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23851DCE	LIFEBUY	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 125	TPS23851	
TPS23851DCER	LIFEBUY	SSOP	DCE	36	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 125	TPS23851	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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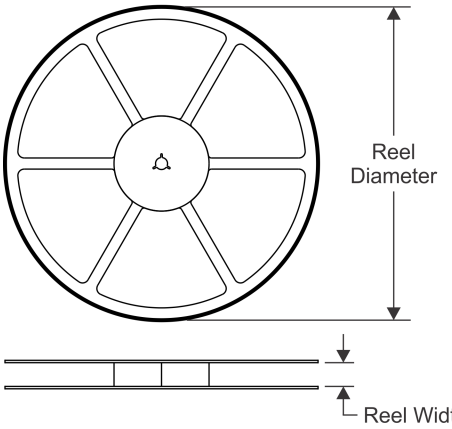
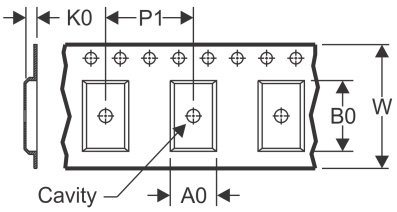
REEL DIMENSIONS

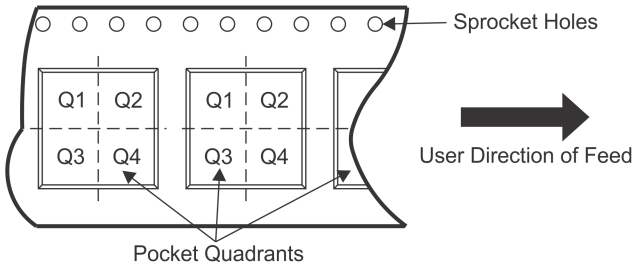


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

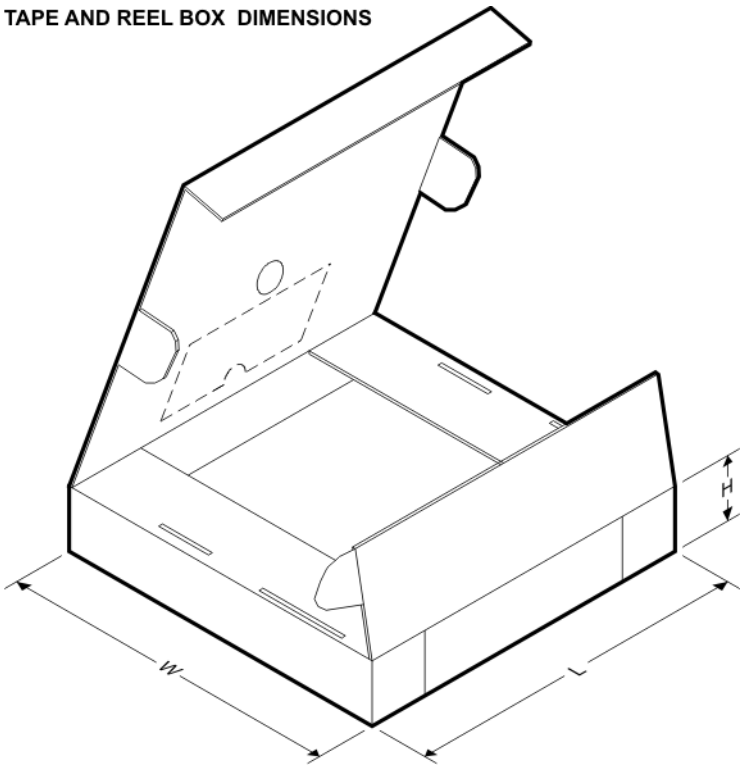
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23851DCER	SSOP	DCE	36	1000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



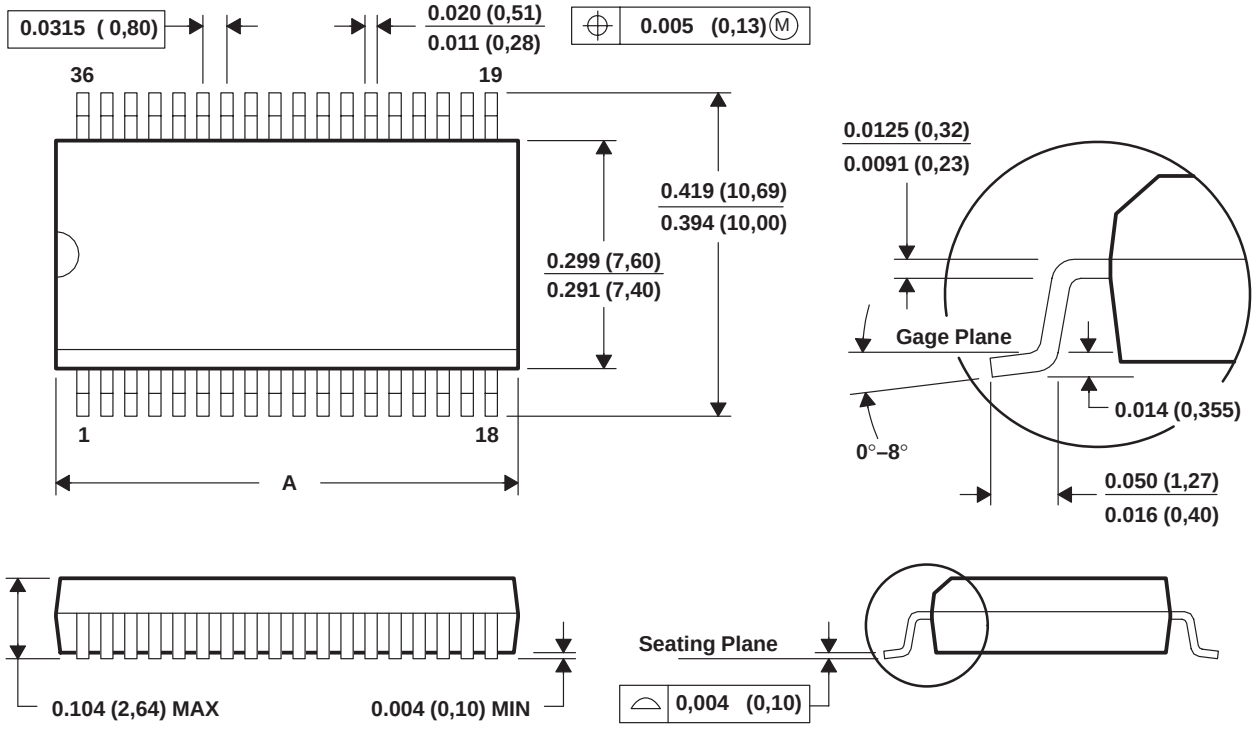
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23851DCER	SSOP	DCE	36	1000	367.0	367.0	45.0

DCE (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

36 PINS SHOWN



DIM \ PINS **	36	44
A MAX	0.613 (15,57)	0.713 (18,11)
A MIN	0.598 (15,20)	0.697 (17,70)

4201503/A 09/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

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