WM8998

High Performance Audio Hub CODEC

DESCRIPTION

The WM8998 is a highly-integrated low-power audio hub CODEC for smartphones, tablets and other portable audio devices. It is optimised for use in multimedia devices where the audio processing requirements are implemented on the host applications processor.

The WM8998 digital core combines fixed-function signal processing blocks with a fully-flexible, all-digital audio mixing and routing engine, for extensive use-case flexibility. Signal processing blocks include filters, EQ, dynamics processors and sample rate converters.

A SLIMbus® interface supports multi-channel audio paths and host control register access. Multiple sample rates are supported concurrently via the SLIMbus interface. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice call handover.

The stereo headphone driver provides ground-referenced outputs, with noise levels as low as $1\mu V_{RMS}$ for hi-fi quality line or headphone output. The CODEC also features a stereo line output, stereo 2W Class-D speaker outputs, a dedicated BTL earpiece output, PDM for external speaker amplifiers, and an IEC-60958-3 compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class-D speaker output, or via an external driver on the PDM output interface. All inputs, outputs and system interfaces can function concurrently.

The WM8998 supports up to six analogue mic/line inputs, and up to three PDM digital inputs. The input multiplexers support up to three signal paths. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM8998 power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power 'Sleep' is supported, with configurable wake-up events. The WM8998 is powered from a 1.8V external supply. A separate supply is required for the Class D speaker drivers (typically direct connection to 4.2V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The WM8998 is configured using the I2C or SLIMbus interfaces. The fully-differential internal analogue architecture, minimal analogue signal paths and on-chip RF noise filters ensure a very high degree of noise immunity.

FEATURES

- Hi-Fi audio hub CODEC for mobile applications
- Digital audio processing core
  - Fully flexible digital signal routing and mixing
  - Wind noise, sidetone and other programmable filters
  - Dynamic Range Control (compressor, limiter)
  - Fully parametric EQs
  - Low-pass / High-pass filters
- Multi-channel asynchronous sample rate conversion
- Integrated multi-channel 24-bit hi-fi audio hub CODEC
  - 3 ADCs, 96dB SNR microphone input (48kHz)
  - 7 DACs, 122dB SNR headphone playback (48kHz)
- Audio inputs
  - Up to 6 analogue or 3 digital microphone inputs
  - Single-ended or differential mic/line inputs
- Stereo headphone output driver
  - 28mW into 32Ω load at 0.1% THD+N
  - 6.9mW typical headphone playback power consumption
  - Pop suppression functions
  - $1\mu V_{RMS}$ noise floor (A-weighted)
- Ground-referenced line output driver
  - Stereo single-ended or Mono differential configuration
- Mono BTL earpiece output driver
  - 100mW into 32Ω BTL load at 5% THD+N
- Stereo (2 x 2W) Class D speaker output drivers
  - Direct drive of external haptics vibe actuators
- Two-channel digital speaker (PDM) output interface
- IEC-60958-3 compatible S/PDIF transmitter
- SLIMbus audio and control interface
- 3 full digital audio interfaces
  - Standard sample rates from 8kHz up to 192kHz
  - TDM support on all AIFs
  - 6 channel input and output on AIF1 and AIF2
- Flexible clocking, derived from MCLKn, BCLKn or SLIMbus
- 2 low-power FLLs support reference clocks down to 32kHz
- Advanced accessory detection functions
  - Low-power standby mode and configurable wake-up
- Configurable functions on 5 GPIO pins
- Integrated LDO regulators and charge pumps
- Support for single 1.8V supply operation
- Small W-CSP package, 0.4mm pitch

APPLICATIONS

- Smartphones and Multimedia handsets
- Tablets and Mobile Internet Devices (MID)

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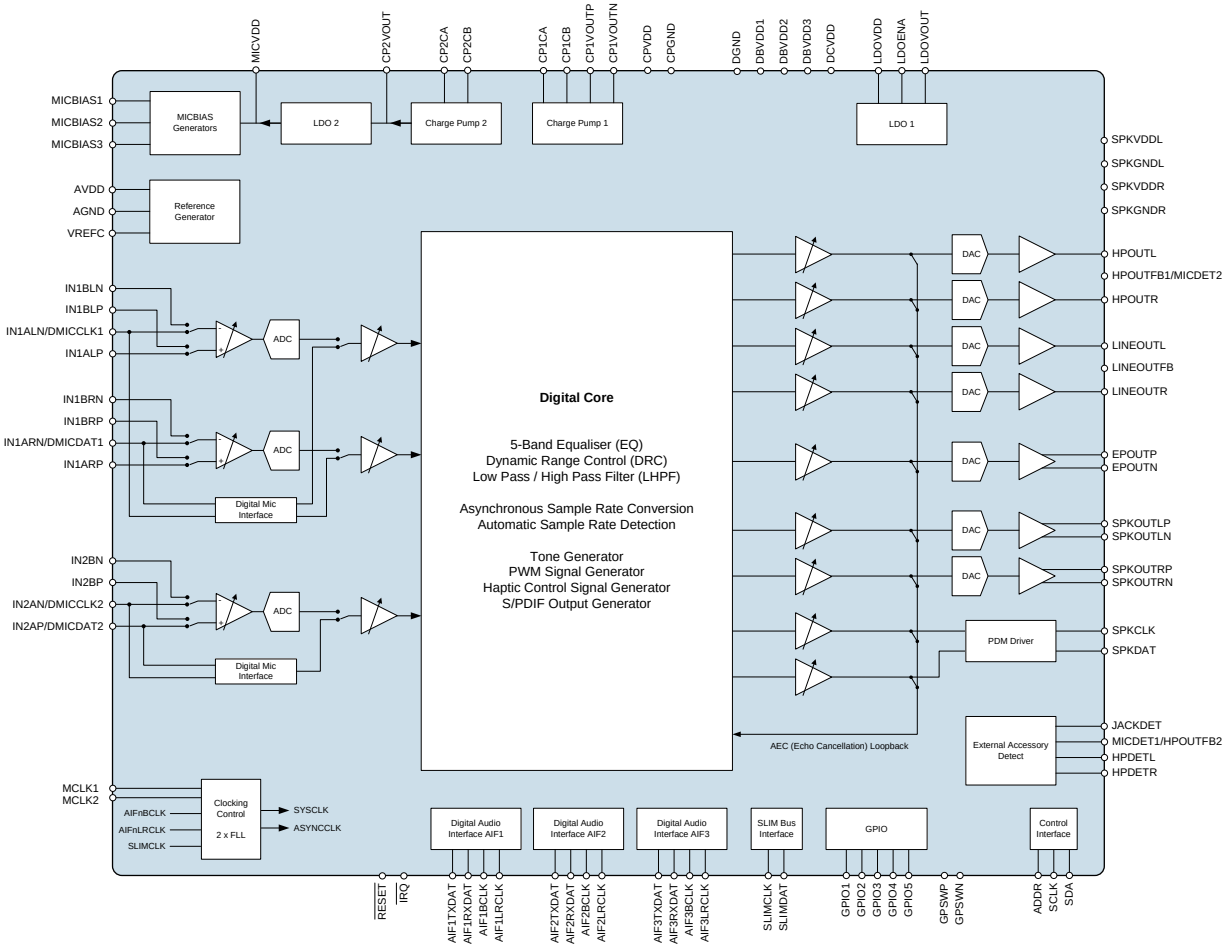
BLOCK DIAGRAM



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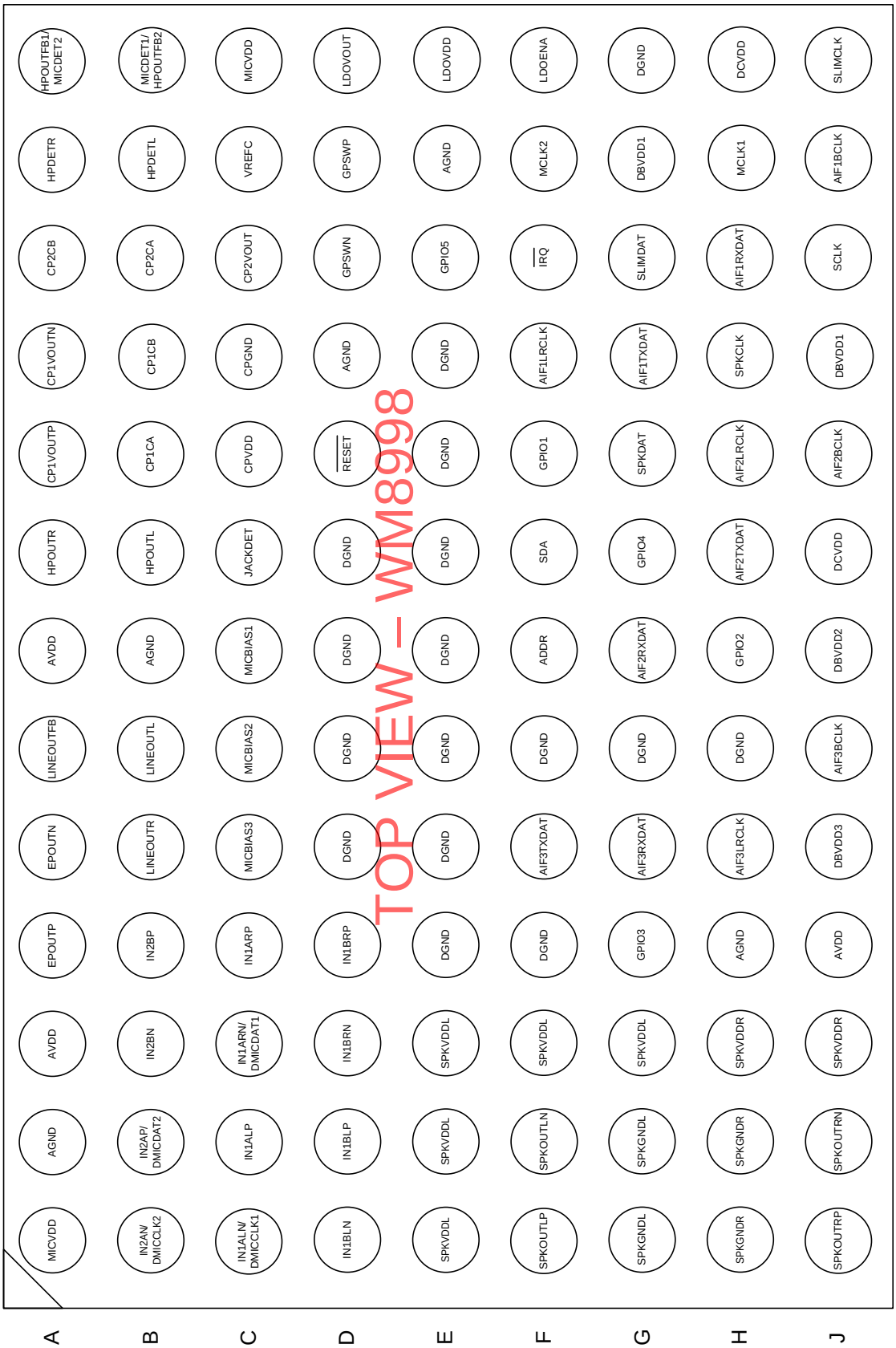
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8998ECS/R	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 7000

PIN DESCRIPTION

A description of each pin on the WM8998 is provided below.
Note that a table detailing the associated power domain for every digital input / digital output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
F7	ADDR	Digital Input	Control interface (I2C) address select
A2, B7, D10, E12, H4	AGND	Supply	Analogue ground (Return path for AVDD)
J12	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
F10	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
H11	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
G10	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
J9	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
H9	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
G7	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
H8	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
J6	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
H5	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
G5	AIF3RXDAT	Digital Input	Audio interface 3 RXdigital audio data
F5	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
A3, A7, J4	AVDD	Supply	Analogue supply
B9	CP1CA	Analogue Output	Charge pump 1 fly-back capacitor pin
B10	CP1CB	Analogue Output	Charge pump 1 fly-back capacitor pin
A10	CP1VOUTN	Analogue Output	Charge pump 1 negative output decoupling pin
A9	CP1VOUTP	Analogue Output	Charge pump 1 positive output decoupling pin
B11	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
A11	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
C11	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
C10	CPGND	Supply	Charge pump 1 & 2 ground (Return path for CPVDD)
C9	CPVDD	Supply	Supply for Charge Pump 1 & 2
G12, J10	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
J7	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2, GPIO2, GPIO4)
J5	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3, GPIO3)
H13, J8	DCVDD	Supply	Digital core supply
D5, D6, D7, D8, E4, E5, E6, E7, E8, E9, E10, F4, F6, G6, G13, H6	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3)
A5	EPOUTN	Analogue Output	Earpiece negative output
A4	EPOUTP	Analogue Output	Earpiece positive output

PIN NO	NAME	TYPE	DESCRIPTION
F9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
H7	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
G4	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output configuration is selectable CMOS or Open Drain.
G8	GPIO4	Digital Input / Output	General Purpose pin GPIO4. The output configuration is selectable CMOS or Open Drain.
E11	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output configuration is selectable CMOS or Open Drain.
D11	GPSWN	Analogue Output	General Purpose analogue switch contact (negative)
D12	GPSWP	Analogue Input	General Purpose analogue switch contact (positive)
B12	HPDETL	Analogue Input	Headphone left (HPOUTL) sense input
A12	HPDETR	Analogue Input	Headphone right (HPOUTR) sense input
A13	HPOUTFB1/ MICDET2	Analogue Input	HPOUTL and HPOUTR ground feedback pin 1/ Microphone & accessory sense input 2
B8	HPOUTL	Analogue Output	Left headphone output
A8	HPOUTR	Analogue Output	Right headphone output
C1	IN1ALN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 1
C2	IN1ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
C3	IN1ARN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 1
C4	IN1ARP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
B1	IN2AN/ DMICCLK2	Analogue Input / Digital Output	Negative differential Mic/Line input / Digital MIC clock output 2
B2	IN2AP/ DMICDAT2	Analogue Input / Digital Input	Single-ended Mic/Line input / Positive differential Mic/Line input/ Digital MIC data input 2
D1	IN1BLN	Analogue Input	Left channel negative differential Mic/Line input
D2	IN1BLP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D3	IN1BRN	Analogue input	Right channel negative differential Mic/Line input
D4	IN1BRP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
B3	IN2BN	Analogue Input	Negative differential Mic/Line input
B4	IN2BP	Analogue Input	Single-ended Mic/Line input / Positive differential Mic/Line input
F11	$\overline{\text{IRQ}}$	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
C8	JACKDET	Analogue Input	Jack detect input
F13	LDOENA	Digital Input	Enable pin for LDO1 (generates DCVDD supply). Logic 1 input enables LDO1. If using external DCVDD supply, then LDO1 is not used, and LDOENA must be held at logic 0.
E13	LDOVDD	Supply	Supply for LDO1
D13	LDOVOUT	Analogue Output	LDO1 output. If using external DCVDD, then LDOVOUT must be left floating.
A6	LINEOUTFB	Analogue Input	LINEOUTL and LINEOUTR ground loop noise rejection feedback
B6	LINEOUTL	Analogue Output	Left line output
B5	LINEOUTR	Analogue Output	Right line output
H12	MCLK1	Digital Input	Master clock 1
F12	MCLK2	Digital Input	Master clock 2
C7	MICBIAS1	Analogue Output	Microphone bias 1

PIN NO	NAME	TYPE	DESCRIPTION
C6	MICBIAS2	Analogue Output	Microphone bias 2
C5	MICBIAS3	Analogue Output	Microphone bias 3
B13	MICDET1/ HPOUTFB2	Analogue Input	Microphone & accessory sense input 1/ HPOUTL and HPOUTR ground feedback pin 2
A1, C13	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by WM8998). (Can also be used as reference/supply for external microphones.)
D9	$\overline{\text{RESET}}$	Digital Input	Digital Reset input (active low)
J11	SCLK	Digital Input	Control interface (I2C) clock input
F8	SDA	Digital Input / Output	Control interface (I2C) data input and output The output function is implemented as an Open Drain circuit.
J13	SLIMCLK	Digital Input	SLIMBus Clock input
G11	SLIMDAT	Digital Input / Output	SLIMBus Data input / output
H10	SPKCLK	Digital Output	Digital speaker (PDM) clock output
G9	SPKDAT	Digital Output	Digital speaker (PDM) data output
G1, G2	SPKGNDL	Supply	Left speaker driver ground (Return path for SPKVDDL)
H1, H2	SPKGNDR	Supply	Right speaker driver ground (Return path for SPKVDDR)
F2	SPKOUTLN	Analogue Output	Left speaker negative output
F1	SPKOUTLP	Analogue Output	Left speaker positive output
J2	SPKOUTRN	Analogue Output	Right speaker negative output
J1	SPKOUTRP	Analogue Output	Right speaker positive output
E1, E2, E3, F3, G3	SPKVDDL	Supply	Left speaker driver supply
H3, J3	SPKVDDR	Supply	Right speaker driver supply
C12	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
F7	ADDR	DBVDD1	DGND
J12	AIF1BCLK	DBVDD1	DGND
F10	AIF1LRCLK	DBVDD1	DGND
H11	AIF1RXDAT	DBVDD1	DGND
G10	AIF1TXDAT	DBVDD1	DGND
J9	AIF2BCLK	DBVDD2	DGND
H9	AIF2LRCLK	DBVDD2	DGND
G7	AIF2RXDAT	DBVDD2	DGND
H8	AIF2TXDAT	DBVDD2	DGND
J6	AIF3BCLK	DBVDD3	DGND
H5	AIF3LRCLK	DBVDD3	DGND
G5	AIF3RXDAT	DBVDD3	DGND
F5	AIF3TXDAT	DBVDD3	DGND
F9	GPIO1	DBVDD1	DGND
H7	GPIO2	DBVDD2	DGND
G4	GPIO3	DBVDD3	DGND
G8	GPIO4	DBVDD2	DGND
E11	GPIO5	DBVDD1	DGND
C1	IN1ALN/ DMICCLK1	(when DMICCLK1 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
C3	IN1ARN/ DMICDAT1	(when DMICDAT1 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
B1	IN2AN/ DMICCLK2	(when DMICCLK2 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
B2	IN2AP/ DMICDAT2	(when DMICDAT2 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
F11	$\overline{\text{IRQ}}$	DBVDD1	DGND
F13	LDOENA	DBVDD1	DGND
H12	MCLK1	DBVDD1	DGND
F12	MCLK2	DBVDD1	DGND
D9	$\overline{\text{RESET}}$	DBVDD1	DGND
J11	SCLK	DBVDD1	DGND
F8	SDA	DBVDD1	DGND
J13	SLIMCLK	DBVDD1	DGND
G11	SLIMDAT	DBVDD1	DGND
H10	SPKCLK	DBVDD1	DGND
G9	SPKDAT	DBVDD1	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (LDOVDD, AVDD, DCVDD, CPVDD)	-0.3V	+2.0V
Supply voltages (DBVDD1, DBVDD2, DBVDD3)	-0.3V	+4.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	+6.0V
Voltage range digital inputs (DBVDD1 domain)	AGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	AGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	AGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDATn)	AGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN1A*, IN1B*, IN2A*, MICDETn, HPOUTFBn, LINEOUTFB)	AGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN2B*)	AGND - 3.3V	MICVDD + 0.3V
Voltage range analogue inputs (JACKDET, HPDETL, HPDETR)	CP1VOUTN - 0.3V	AVDD + 0.3V
Voltage range analogue inputs (GPSWP, GPSWN)	AGND - 0.3V	MICVDD + 0.3V
Ground (DGND, CPGND, SPKGNDL, SPKGNDR)	AGND - 0.3V	AGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. DCVDD must not be powered if AVDD is not present.
2. CP1VOUT2N is an internal supply, generated by the WM8998 Charge Pump (CP1). The CP1VOUT2N voltage may vary between AGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 2, 3, 4, 5	DCVDD (≤24.576MHz clocking)	1.14	1.2	1.9	V
	DCVDD (>24.576MHz clocking)	1.71	1.8	1.9	
Digital supply range (I/O)	DBVDD1	1.7		1.9	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.7		3.47	V
LDO supply range	LDOVDD	1.7	1.8	1.9	V
Charge Pump supply range	CPVDD	1.7	1.8	1.9	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range See note 2	AVDD	1.7	1.8	1.9	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDL, SPKGNDR		0		V
Power supply rise time See notes 7, 8, 9, 10	DCVDD	10		2000	µs
	All other supplies	1			
Operating temperature range	T_A	-40		85	°C

Notes:

3. The grounds must always be within 0.3V of AGND.
4. AVDD must be supplied before DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
5. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.
6. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
7. Under default conditions, digital core clocking rates above 24.576MHz are inhibited. The register-controlled clocking limit should only be raised when the applicable DCVDD voltage is present.
8. An internal Charge Pump and LDO (powered by CPVDD) provide the microphone bias supply; the MICVDD pin should not be connected to an external supply.
9. DCVDD minimum rise time does not apply when this is powered using the internal LDO.
10. If DCVDD is supplied externally, and the rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
11. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
12. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 6dB PGA gain		0.5 -6		V_{RMS} dBV
		Differential PGA input, 0dB PGA gain		1 0		V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B)						
Input resistance	R_{IN}	Differential input, All PGA gain settings		24		kΩ
		Single-ended input, 0dB PGA gain		16		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Note:

The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Output Driver (HPOUTL, HPOUTR)						
Load resistance, Single-ended output mode		Charge Pump Normal mode (default)	15			Ω
		Charge Pump Low Impedance mode	6			
Load resistance, Differential (BTL) output mode		Charge Pump Normal mode (default)	30			Ω
		Charge Pump Low Impedance mode	15			
Load resistance		Device survival with load applied indefinitely	0.1			Ω
Load capacitance		Direct connection, Single-ended mode			500	pF
		Direct connection, Differential (BTL) mode			250	
		Connection via 16Ω series resistor			2	nF
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Note - to support HPOUT loads less than 15Ω, (or less than 30Ω BTL), the Charge Pump (CP1) must be configured for low impedance operation, as described in the “Output Signal Path” section.						
Line Output Driver (LINEOUTL, LINEOUTR)						
Load resistance		Normal operation	600			Ω
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection, Single-ended mode			500	pF
		Direct connection, Differential (BTL) mode			250	
		Connection via 16Ω series resistor			2	nF
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Earpiece Output Driver (EPOUTP+EPOUTN)						
Load resistance		Charge Pump Normal mode (default)	30			Ω
		Charge Pump Low Impedance mode	15			
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection (BTL)			250	pF
		Connection via 16Ω series resistor			2	nF
DC offset at Load				0.1		mV
Note - to support EPOUT loads less than 30Ω, the Charge Pump (CP1) must be configured for low impedance operation, as described in the “Output Signal Path” section.						

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
DC offset at Load				5		mV
SPKVDD leakage current				1		µA
Digital Speaker Output (SPKDAT)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Note:

The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B) to ADC (Differential Input Mode, INn_SRC = x0)						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)	87	96		dB
		Normal mode (INn_OSR = 0)		93		
Total Harmonic Distortion	THD	-1dBV input		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBV input		-88	-79	dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB		65		dB
		PGA gain = 0dB		70		
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV(peak-peak) 10kHz		65		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		95		dB
		100mV(peak-peak) 10kHz		95		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B) to ADC (Single-Ended Input Mode, INn_SRC = x1) PGA Gain = +6dB unless otherwise stated.						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)	86	94		dB
		Normal mode (INn_OSR = 0)		92		
Total Harmonic Distortion	THD	-7dBV input		-82		dB
Total Harmonic Distortion Plus Noise	THD+N	-7dBV input		-81	-71	dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		4.6		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV(peak-peak) 10kHz		50		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV(peak-peak) 10kHz		70		
DAC to Headphone Output (HPOUTL, HPOUTR; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		28		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		122		dB
Total Harmonic Distortion	THD	P_O = 20mW		-86		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-84		dB
Total Harmonic Distortion	THD	P_O = 5mW		-89		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-85		dB
Channel separation (Left/Right)		P_O = 20mW		110		dB
Output noise floor		A-weighted		1		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		
DAC to Headphone Output (HPOUTL, HPOUTR; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		34		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	P_O = 20mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-76		dB
Total Harmonic Distortion	THD	P_O = 5mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-77	-67	dB
Channel separation (Left/Right)		P_O = 20mW		110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (HPOUTL, HPOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	0dBFS input		-89		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-88	-73	dB
Channel separation (Left/Right)				110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		
DAC to Line Output (LINEOUTL, LINEOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	0dBFS input		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-89	-73	dB
Channel separation (Left/Right)				110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		127		dB
		100mV (peak-peak) 10kHz		90		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		85		
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		83		mW
		5% THD+N		100		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms	118	127		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-85		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-83	-73	dB
Output noise floor		A-weighted		1	2.5	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		113		dB
		100mV (peak-peak) 10kHz		115		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		100		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 16Ω BTL)						
Maximum output power	P_O	0.1% THD+N		83		mW
		10% THD+N		110		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms		127		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor		A-weighted		1		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		113		dB
		100mV (peak-peak) 10kHz		115		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		100		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.37		W
		SPKVDD = 4.2V, 1% THD+N		0.97		
		SPKVDD = 3.6V, 1% THD+N		0.71		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3Vrms	90	100		dB
Total Harmonic Distortion	THD	P_O = 0.7W		-74		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.7W		-73		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-74		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-73	-57	dB
Channel separation (Left/Right)		P_O = 0.5W		95		dB
Output noise floor		A-weighted		30	95	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		80		dB
		100mV (peak-peak) 10kHz		70		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.4		W
		SPKVDD = 4.2V, 1% THD+N		1.69		
		SPKVDD = 3.6V, 1% THD+N		1.24		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3Vrms		100		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-61		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 1.0W		-60		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-64		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-63		dB
Channel separation (Left/Right)		P_O = 0.5W		85		dB
Output noise floor		A-weighted		30		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		80		dB
		100mV (peak-peak) 10kHz		70		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn) **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3. See "Pin Description" for the domain applicable to each pin.** **See "Recommended Operating Conditions" for the valid operating voltage range of each DBVDDn domain.**						
Input HIGH Level	V_{IH}	V_{DBVDDn} =1.8V ±10%	0.65 × V_{DBVDDn}			V
		V_{DBVDDn} =3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDDn} =1.8V ±10%			0.35 × V_{DBVDDn}	V
		V_{DBVDDn} =3.3V ±10%			0.3 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDDn}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDDn}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
Pull-up resistance (where applicable)			42	49	56	kΩ
Pull-down resistance (where applicable)			80	105	130	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
SLIMbus Digital Input / Output (SLIMCLK and SLIMDAT) **1.8V I/O Signalling (ie. 1.65V ≤ DBVDD1 ≤1.95V)**						
Input HIGH Level	V_{IH}		0.65 × V_{DBVDD1}			V
Input LOW Level	V_{IL}				0.35 × V_{DBVDD1}	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDD1}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDD1}	V
Pin capacitance					5	pF
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			26.5	MHz
General Purpose Switch The GPSWP pin should be positive-biased with respect to GPSWN. The GPSWN pin voltage must not exceed GPSWP + 0.3V.						
Switch resistance	$R_{DS(ON)}$	Switch closed, I=1mA		40		Ω
Switch resistance	$R_{DS(OFF)}$	Switch open		100		MΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIASn}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		50		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		4		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		95		dB
		100mV (peak-peak) 10kHz		65		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		5		kΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External Accessory Detect						
Load impedance detection range Detection via HPDETL pin (ACCDET_MODE=001) or HPDETR pin (ACCDET_MODE=010)		HP_IMPEDANCE_ RANGE=00	4		30	Ω
		HP_IMPEDANCE_ RANGE=01	8		100	
		HP_IMPEDANCE_ RANGE=10	100		1000	
		HP_IMPEDANCE_ RANGE=11	1000		10000	
Load impedance detection range Detection via the MICDET1 or MICDET2 pin (ACCDET_MODE=100)			400		6000	Ω
Load impedance detection accuracy (ACCDET_MODE=001, 010 or 100)			-30		+30	%
Load impedance detection range Detection via the MICDET1 or MICDET2 pin (ACCDET_MODE=000). 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn. See “Applications Information” for recommended external components when a typical microphone is present.		for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	17		21	
		for MICD_LVL[2] = 1	36		44	
		for MICD_LVL[3] = 1	62		88	
		for MICD_LVL[4] = 1	115		160	
		for MICD_LVL[5] = 1	207		381	
		for MICD_LVL[8] = 1	475		30000	
Jack Detection input threshold voltage (JACKDET)	$V_{JACKDET}$	Jack insertion		0.5 x AVDD		V
		Jack removal		0.85 x AVDD		
Jack Detect pull-up resistance			0.65	1	1.3	MΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICVDD Charge Pump and Regulator (CP2 and LDO2)						
Output voltage	V_{MICVDD}		1.7	2.7	3.3	V
Programmable output voltage step size				50		mV
Maximum output current				8		mA
Start-up time		4.7µF on MICVDD, $I_{MICBIASn}$ = 1mA		4.5		ms
Frequency Locked Loop (FLL1, FLL2)						
Output frequency		Normal operation, input reference supplied	13		50	MHz
		Free-running mode, no reference supplied		30		
Lock Time		F_{REF} = 32kHz, F_{OUT} = 24.576MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 24.576MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}	V_{AVDD} rising			0.96	V
		V_{AVDD} falling	0.54			
DCVDD Reset Threshold	V_{DCVDD}	V_{DCVDD} rising			1.03	V
		V_{DCVDD} falling	0.48			
DBVDD1 Reset Threshold	V_{DBVDD1}	V_{DBVDD1} rising			0.96	V
		V_{DBVDD1} falling	0.54			
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the WM8998 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass ‘brick-wall’ filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise.

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance	Θ_{JA}		33.8		°C/W
Junction-to-board thermal resistance	Θ_{JB}		10.5		°C/W
Junction-to-case thermal resistance	Θ_{JC}		0.7		°C/W
Junction-to-board thermal characterisation parameter	Ψ_{JB}		9.4		°C/W
Junction-to-top thermal characterisation parameter	Ψ_{JT}		0.01		°C/W

Notes:

1. The Thermal Characteristics data is based on simulated test results, with reference to JEDEC JESD51 standards.
2. The thermal resistance (Θ) parameters describe the thermal behaviour in a standardised measurement environment.
3. The thermal characterisation (Ψ) parameters describe the thermal behaviour in the environment of a typical application.

TYPICAL PERFORMANCE

TYPICAL POWER CONSUMPTION

Typical power consumption data is provided below for a number of different operating conditions.

Test Conditions:
DCVDD = 1.2V, DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
SPKVDDL = SPKVDDR = 4.2V, T_A = +25ºC.

OPERATING MODE	TEST CONDITIONS	SUPPLY CURRENT (1.2V)	SUPPLY CURRENT (1.8V)	SUPPLY CURRENT (4.2V)	TOTAL POWER
Music Playback to Headphone					
AIF1 to DAC to HPOUT (stereo) SYSCLK=11.2896MHz, (direct MCLK input, FLL disabled) fs=44.1kHz, 24-bit I2S, Slave mode Load = 32Ω	Quiescent	2.42mA	2.20mA	0.00mA	6.86mW
	1kHz sine wave, P_O=10mW	2.61mA	36.73mA	0.00mA	66.25mW
Music Playback to Line Output					
AIF1 to DAC to LINEOUT (stereo) SYSCLK=24.576MHz, (direct MCLK input, FLL disabled) fs=48kHz, 24-bit I2S, Slave mode Load = 10kΩ, 50pF	Quiescent	2.78mA	2.01mA	0.00mA	6.96mW
Music Playback to Earpiece					
AIF1 to DAC to EPOUT SYSCLK=24.576MHz, (direct MCLK input, FLL disabled) fs=48kHz, 24-bit I2S, Slave mode Load = 32Ω, BTL	Quiescent	1.97mA	1.27mA	0.00mA	4.65mW
	1kHz sine wave, P_O=30mW	2.05mA	57.52mA	0.00mA	106.0mW
Music Playback to Speaker					
AIF1 to DAC to SPKOUT (stereo) SYSCLK=24.576MHz, (direct MCLK input, FLL disabled) fs=48kHz, 24-bit I2S, Slave mode Load = 8Ω, 22µH, BTL	Quiescent	2.58mA	2.72mA	3.48mA	22.58mW
	1kHz sine wave, P_O=700mW	2.62mA	2.77mA	412mA	1738mW
Full Duplex Voice Call					
Analogue Mic to ADC to AIF1 (out) AIF1 (in) to DAC to EPOUT (mono) SYSCLK=24.576MHz, (direct MCLK input, FLL disabled) fs=8kHz, 16-bit I2S, Slave mode MICVDD=3.0V (powered from LDO2), MICBIAS=1.8V (regulator mode) Earpiece load = 32Ω, BTL Power dissipated in the microphone is not included.	Quiescent	1.84mA	3.09mA	0.00mA	7.78mW
Stereo Line Record					
Analogue Line to ADC to AIF1 SYSCLK=11.2896MHz, (direct MCLK input, FLL disabled) fs=44.1kHz, 24-bit I2S, Slave mode MICVDD=1.8V (CP2/LDO2 bypass)	1kHz sine wave, -1dBFS out	1.18mA	1.68mA	0.00mA	4.44mW
Sleep Mode					
Accessory detect enabled (JD1_ENA=1)		0.000mA	0.013mA	0.000mA	0.024mW

TYPICAL SIGNAL LATENCY

OPERATING MODE	TEST CONDITIONS			LATENCY
	INPUT	OUTPUT	DIGITAL CORE	
AIF to DAC Stereo Path				
Digital input (AIFn) to analogue output (HPOUT). Signal is routed via the digital core ASRC function in the asynchronous test cases only.	fs = 48kHz	fs = 48kHz	Synchronous	378µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	410µs
	fs = 16kHz	fs = 16kHz	Synchronous	592µs
	fs = 8kHz	fs = 8kHz	Synchronous	1148µs
	fs = 8kHz	fs = 44.1kHz	Asynchronous	1730µs
	fs = 16kHz	fs = 44.1kHz	Asynchronous	1096µs
ADC to AIF Stereo Path				
Analogue input (INn) to digital output (AIFn). Input path High Pass Filter (HPF) enabled. Signal is routed via the digital core ASRC function in the asynchronous test cases only.	fs = 48kHz	fs = 48kHz	Synchronous	170µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	199µs
	fs = 16kHz	fs = 16kHz	Synchronous	557µs
	fs = 8kHz	fs = 8kHz	Synchronous	1087µs
	fs = 44.1kHz	fs = 8kHz	Asynchronous	1181µs
	fs = 44.1kHz	fs = 16kHz	Asynchronous	644µs

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK & FREQUENCY LOCKED LOOP (FLL)

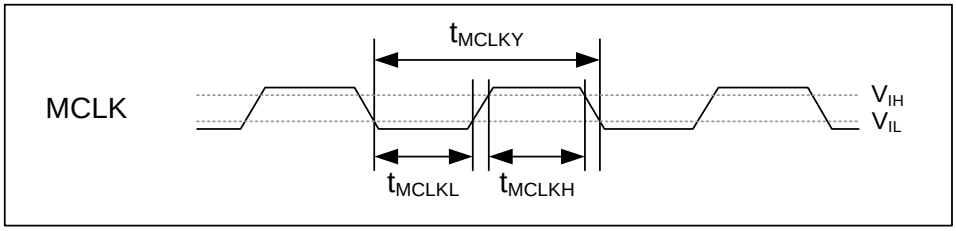


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1, MCLK2)					
MCLK frequency	MCLK as input to FLL, FLLn_REFCLK_DIV=00			13.5	MHz
	MCLK as input to FLL, FLLn_REFCLK_DIV=01			27	
	MCLK as input to FLL, FLLn_REFCLK_DIV=10 or 11			40	
	MCLK as direct SYSCLK or ASYNCCLK source			25	
MCLK duty cycle	MCLK as input to FLL	80:20		20:80	%
	MCLK as direct SYSCLK or ASYNCCLK source	60:40		40:60	
MCLK2 frequency	Sleep Mode			32.768	kHz
Frequency Locked Loops (FLL1, FLL2)					
FLL input frequency	FLLn_REFCLK_DIV=00	0.032		13.5	MHz
	FLLn_REFCLK_DIV=01	0.064		27	
	FLLn_REFCLK_DIV=10	0.128		40	
	FLLn_REFCLK_DIV=11	0.256		40	
FLL synchroniser input frequency	FLLn_SYNCCLK_DIV=00	0.032		13.5	MHz
	FLLn_SYNCCLK_DIV=01	0.064		27	
	FLLn_SYNCCLK_DIV=10	0.128		40	
	FLLn_SYNCCLK_DIV=11	0.256		40	

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Clocking					
SYSCLK frequency	SYSCLK_FREQ=000, SYSCLK_FRAC=0	-1%	6.144	+1%	MHz
	SYSCLK_FREQ=000, SYSCLK_FRAC=1	-1%	5.6448	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=0	-1%	12.288	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=1	-1%	11.2896	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=0	-1%	24.576	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=1	-1%	22.5792	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=0	-1%	49.152	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=1	-1%	45.1584	+1%	
ASYNCCLK frequency	ASYNC_CLK_FREQ=000	-1%	6.144	+1%	MHz
		-1%	5.6448	+1%	
	ASYNC_CLK_FREQ=001	-1%	12.288	+1%	
		-1%	11.2896	+1%	
	ASYNC_CLK_FREQ=010	-1%	24.576	+1%	
		-1%	22.5792	+1%	
	ASYNC_CLK_FREQ=011	-1%	49.152	+1%	
		-1%	45.1584	+1%	

Note:

When MCLK1 or MCLK2 is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

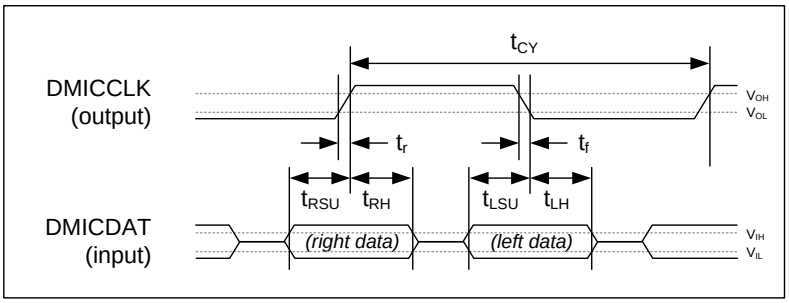


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLKn cycle time	t_{CY}	320	326	716	ns
DMICCLKn duty cycle		45		55	%
DMICCLKn rise/fall time (25pF load, 1.8V supply - see note)	t_r, t_f	5		30	ns
DMICDATn (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDATn (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDATn (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDATn (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

Notes:

DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}.

The applicable supply is selected using the INn_DMIC_SUP registers.

DIGITAL SPEAKER (PDM) INTERFACE TIMING

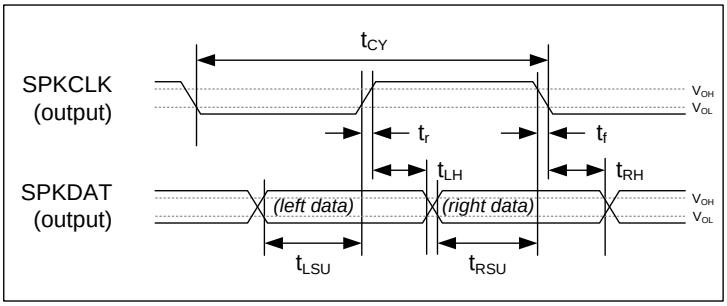


Figure 3 Digital Speaker (PDM) Interface Timing - Mode A

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLKn cycle time	t_{CY}	160	163	358	ns
SPKCLKn duty cycle		45		55	%
SPKCLKn rise/fall time (25pF load)	t_r, t_f	5		30	ns
SPKDATn set-up time to SPKCLKn rising edge (Left channel)	t_{LSU}	30			ns
SPKDATn hold time from SPKCLKn rising edge (Left channel)	t_{LH}	30			ns
SPKDATn set-up time to SPKCLKn falling edge (Right channel)	t_{RSU}	30			ns
SPKDATn hold time from SPKCLKn falling edge (Right channel)	t_{RH}	30			ns

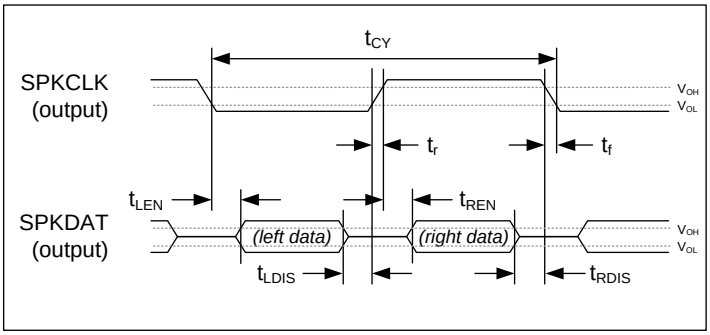


Figure 4 Digital Speaker (PDM) Interface Timing - Mode B

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLKn cycle time	t_{CY}	160	163	358	ns
SPKCLKn duty cycle		45		55	%
SPKCLKn rise/fall time (25pF load)	t_r, t_f	5		30	ns
SPKDATn enable from SPKCLK rising edge (Right channel)	t_{REN}			15	ns
SPKDATn disable to SPKCLK falling edge (Right channel)	t_{RDIS}			5	ns
SPKDATn enable from SPKCLK falling edge (Left channel)	t_{LEN}			15	ns
SPKDATn disable to SPKCLK rising edge (Left channel)	t_{LDIS}			5	ns

DIGITAL AUDIO INTERFACE - MASTER MODE

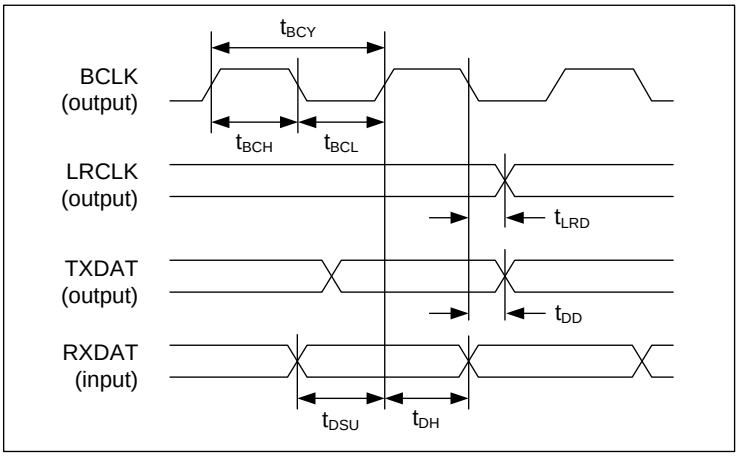


Figure 5 Audio Interface Timing - Master Mode

Note that BCLK and LRCLK outputs can be inverted if required; Figure 5 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

C_{LOAD} = 15pF to 25pF (output pins). BCLK slew (10% to 90%) = 3.7ns to 5.6ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
AIFnBCLK cycle time	t_{BCY}	80			ns
AIFnLRCLK propagation delay from BCLK falling edge	t_{LRD}	0		12	ns
AIFnTXDAT propagation delay from BCLK falling edge	t_{DD}	0		12	ns
AIFnRXDAT setup time to BCLK rising edge	t_{DSU}	7			ns
AIFnRXDAT hold time from BCLK rising edge	t_{DH}	5			ns

Note:

The descriptions above assume non-inverted polarity of AIFnBCLK.

DIGITAL AUDIO INTERFACE - SLAVE MODE

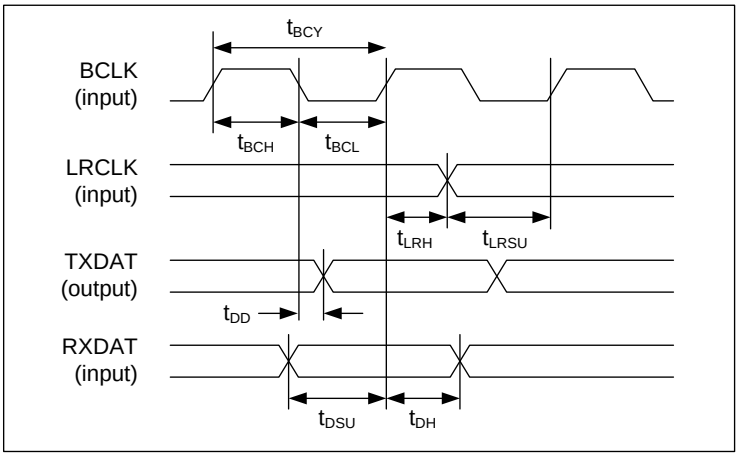


Figure 6 Audio Interface Timing - Slave Mode

Note that BCLK and LRCLK inputs can be inverted if required; Figure 6 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
AIFnBCLK cycle time	t_{BCY}	80			ns
AIFnBCLK pulse width high	t_{BCH}	12			ns
AIFnBCLK pulse width low	t_{BCL}	12			ns
AIFnLRCLK set-up time to BCLK rising edge	t_{LRSU}	7			ns
AIFnLRCLK hold time from BCLK rising edge	t_{LRH}	5			ns
AIFnRXDAT hold time from BCLK rising edge	t_{DH}	5			ns
AIFnTXDAT propagation delay from BCLK falling edge	t_{DD}	0		12	ns
AIFnRXDAT set-up time to BCLK rising edge	t_{DSU}	7			ns

Notes:

The descriptions above assume non-inverted polarity of AIFnBCLK.

When AIFnBCLK or AIFnLRCLK is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

DIGITAL AUDIO INTERFACE - TDM MODE

When TDM operation is used on the AIFnTXDAT pins, it is important that two devices do not attempt to drive the AIFnTXDAT pin simultaneously. To support this requirement, the AIFnTXDAT pins can be configured to be tri-stated when not outputting data.

The timing of the AIFnTXDAT tri-stating at the start and end of the data transmission is described in Figure 7 below.

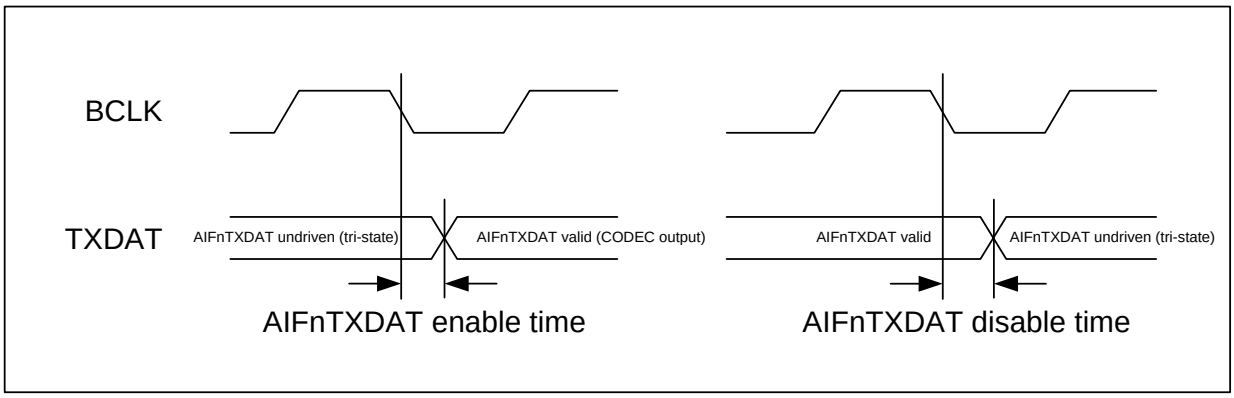


Figure 7 Audio Interface Timing - TDM Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	MIN	TYP	MAX	UNIT
TDM Timing - Master Mode				
AIFnTXDAT enable time from BCLK falling edge	0			ns
AIFnTXDAT disable time from BCLK falling edge			15	ns
TDM Timing - Slave Mode				
AIFnTXDAT enable time from BCLK falling edge	5			ns
AIFnTXDAT disable time from BCLK falling edge			32	ns

CONTROL INTERFACE TIMING

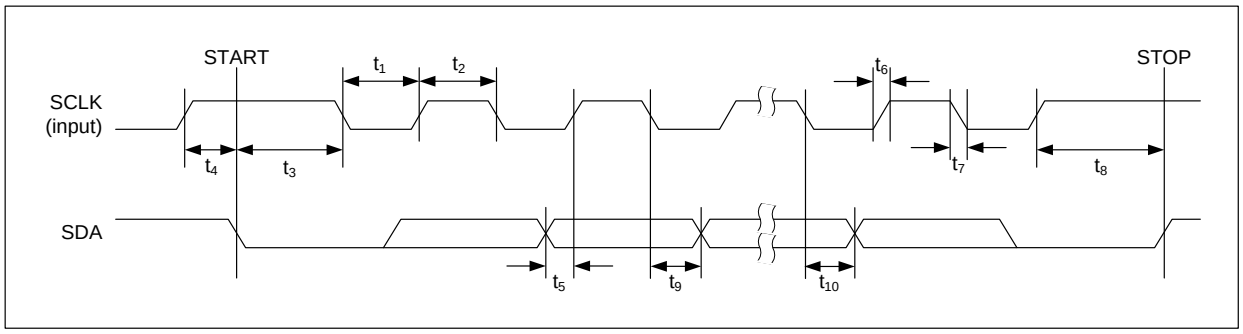


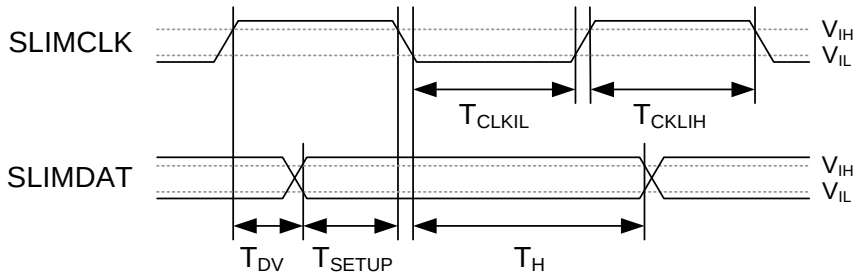
Figure 8 Control Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				1000	kHz
SCLK Low Pulse-Width	t_1	500			ns
SCLK High Pulse-Width	t_2	260			ns
Hold Time (Start Condition)	t_3	260			ns
Setup Time (Start Condition)	t_4	260			ns
SDA, SCLK Rise Time (20% to 80%)	t_6			120	ns
SDA, SCLK Fall Time (80% to 20%)	t_7			120	ns
Setup Time (Stop Condition)	t_8	260			ns
SDA Setup Time (data input)	t_5	50			ns
SDA Hold Time (data input)	t_9	0			ns
SDA Valid Time (data/ACK output)	t_{10}			450	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		50	ns

SLIMBUS INTERFACE TIMING



V_{IL}, V_{IH} are the 35%/65% levels of the respective inputs.
The SLIMDAT output delay (T_{DV}) is with respect to the input pads of all receiving devices.

Figure 9 SLIMbus Interface Timing

The signal timing information shown in Figure 9 describe the timing requirements of the SLIMbus interface as a whole, not just the WM8998 device. Accordingly, the following should be noted:

- T_{DV} is the propagation delay from the rising SLIMCLK edge (at WM8998 input) to the SLIMDAT output being achieved at the input to all devices across the bus.
- T_{SETUP} is the set-up time for SLIMDAT input (at WM8998), relative to the falling SLIMCLK edge (at WM8998).
- T_H is the hold time for SLIMDAT input (at WM8998) relative to the falling SLIMCLK edge (at WM8998).

For more details of the interface timing, refer to the MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus).

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SLIMCLK Input						
SLIMCLK cycle time			35			ns
SLIMCLK pulse width high		T_{CLKIH}	13			ns
SLIMCLK pulse width low		T_{CLKIL}	13			ns
SLIMDAT Input						
SLIMDAT setup time to SLIMCLK falling edge		T_{SETUP}	3.5			ns
SLIMDAT hold time from SLIMCLK falling edge		T_H	2			ns
SLIMDAT Output						
SLIMDAT time for data output valid (wrt SLIMCLK rising edge)	C_{LOAD} = 15pF, V_{DBVDD1} = 1.62V	T_{DV}		6.7	8.6	ns
	C_{LOAD} = 35pF, V_{DBVDD1} = 1.62V			9.8	12.5	
SLIMDAT slew rate (20% to 80%)	C_{LOAD} = 15pF	SR_{DATA}			0.54 x V_{DBVDD1}	V/ns
	C_{LOAD} = 35pF				0.34 x V_{DBVDD1}	
Other Parameters						
Driver disable time		T_{DD}			6	ns
Bus holder output impedance	0.1 x V_{DBVDD1} < V < 0.9 x V_{DBVDD1}	R_{DATAS}	18		50	kΩ

DEVICE DESCRIPTION

INTRODUCTION

The WM8998 is a highly integrated low-power audio hub CODEC for mobile telephony and portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It is optimised for the needs of tablet devices and multimedia phones using SLIMbus application processors.

The WM8998 digital core provides configurable capability for signal processing algorithms, including parametric equalisation (EQ) and dynamic range control (DRC). Highly flexible digital mixing, including stereo full-duplex asynchronous sample rate conversion, provides use-case flexibility across a broad range of system architectures. A signal generator for controlling haptics vibe actuators is included.

The WM8998 provides multiple digital audio interfaces, including SLIMbus, in order to provide independent and fully asynchronous connections to different processors (eg. application processor, baseband processor and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Two integrated Frequency Locked Loop (FLL) circuits provide additional flexibility.

Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications. Configurable 'Wake-Up' actions can be associated with the low-power standby (Sleep) mode.

Versatile GPIO functionality is provided, and support for external accessory / push-button detection inputs. Comprehensive Interrupt (IRQ) logic and status readback are also provided.

HI-FI AUDIO CODEC

The WM8998 is a high-performance low-power audio CODEC which uses a simple analogue architecture. Input path multiplexers select from up to 6 analogue mic/line and 3 digital microphone inputs; combinations of up to 3 inputs can be supported. 7 DACs are incorporated, providing a dedicated DAC for each output channel.

The analogue outputs comprise a 28mW (122dB SNR) stereo headphone amplifier with ground-referenced output, a flexible (single-ended or differential) line output, a 100mW differential (BTL) earpiece driver, and a Class D stereo speaker driver capable of delivering 2W per channel into a 4Ω load. Six analogue inputs are provided, each supporting single-ended or differential input modes. In differential mode, the input path SNR is 96dB. Up to 3 analogue or digital input paths can be supported at one time.

The audio CODEC is controlled directly via register access. The simple analogue architecture, combined with the integrated tone generator, enables simple device configuration and testing, minimising debug time and reducing software effort.

The WM8998 output drivers are designed to support as many different system architectures as possible. Each output has a dedicated DAC which allows mixing, equalisation, filtering, gain and other audio processing to be configured independently for each channel. This allows each signal path to be individually tailored for the load characteristics. All outputs have integrated pop and click suppression features.

The headphone, line and earpiece output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections.

The Class D speaker drivers deliver excellent power efficiency. High PSRR, low leakage and optimised supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimised across a wide variety of voice communication and multimedia playback use cases.

The WM8998 is cost-optimised for a wide range of mobile phone applications, and features two channels of Class D power amplification. For applications requiring more than two channels of power amplification (or when using the integrated Class D path to drive a haptics actuator), the PDM output channels can be used to drive two external PDM-input speaker drivers. In applications where stereo loudspeakers are physically widely separated, the PDM outputs can ease layout and EMC by avoiding the need to run the Class-D speaker outputs over long distances and interconnects.

DIGITAL AUDIO CORE

The WM8998 uses a core architecture based on all-digital signal routing, making digital audio effects available on all signal paths, regardless of whether the source data input is analogue or digital. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, whilst also supporting a variety of sample rates concurrently. This helps support many new audio use-cases. Soft mute and un-mute control allows smooth transitions between use-cases without interrupting existing audio streams elsewhere.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The WM8998 performs stereo full-duplex asynchronous sample rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample rate detection is provided, enabling seamless wideband/narrowband voice call handover.

Dynamic Range Controller (DRC) functions are available for optimising audio signal levels. In playback modes, the DRC can be used to maximise loudness, while limiting the signal level to avoid distortion, clipping or battery droop, in particular for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The 5-band parametric equaliser (EQ) functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications such as removal of wind and other low-frequency noise.

DIGITAL INTERFACES

Three serial digital audio interfaces (AIFs) each support PCM, TDM and I2S data formats for compatibility with most industry-standard chipsets. AIF1 and AIF2 support six input/output channels each; AIF3 supports two input/output channels. Bidirectional operation at sample rates up to 192kHz is supported.

Three digital PDM input channels are available (one stereo, and one mono interface); these are typically used for digital microphones, powered from the integrated MICBIAS power supply regulators. Two PDM output channels are also available (one stereo interface); these are typically used for external power amplifiers. Embedded mute codes provide a control mechanism for external PDM-input devices.

The WM8998 features a MIPI-compliant SLIMbus interface, providing 4 input, and 6 output channels of audio support. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the WM8998 control registers.

An IEC-60958-3 compatible S/PDIF transmitter is incorporated, enabling stereo S/PDIF output on a GPIO pin. Standard S/PDIF sample rates of 32kHz up to 192kHz are all supported.

The WM8998 is equipped with an I2C slave port (at up to 1MHz). Full access to the register map is also provided via the SLIMbus port.

OTHER FEATURES

The WM8998 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

Two Pulse Width Modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.

The WM8998 provides 5 GPIO pins, supporting selectable input/output functions for interfacing, detection of external hardware, and to provide logic outputs to other devices. Comprehensive Interrupt (IRQ) functionality is also provided for monitoring internal and external event conditions.

A signal generator for controlling haptics devices is included, compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices. The haptics signal generator is highly configurable, and can execute programmable drive event profiles, including reverse drive control. An external vibe actuator can be driven directly by the Class D speaker output.

The WM8998 can be powered from a 1.8V external supply. A separate supply (4.2V) is typically required for the Class D speaker driver. Integrated Charge Pump and LDO Regulators circuits are used to generate supply rails for internal functions and to support powering or biasing of external microphones.

A smart accessory interface is included, supporting most standard 3.5mm accessories. Jack detection, accessory sensing and impedance measurement is provided, for external accessory and push-button detection. Accessory detection can be used as a 'Wake-Up' trigger from low-power standby. Microphone activity detection with interrupt is also available.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the SLIMbus interface, or the audio interfaces (configured in Slave mode), can be used to provide a clock reference. Two integrated Frequency Locked Loop (FLL) circuits provide support for a wide range of clocking configurations, including the use of a 32kHz input clock reference.

INPUT SIGNAL PATH

The WM8998 has six highly flexible input channels. Selectable combinations of analogue (mic or line) and digital inputs are multiplexed into three input signal paths.

The analogue input paths support single-ended and differential modes, programmable gain control and are digitised using a high performance 24-bit sigma-delta ADC.

The digital input paths interface directly with up to three external digital microphones; two separate interfaces are provided (stereo and mono respectively), with an independent clock output for each. Digital delay can be applied to any of the digital input paths; this can be used for phase adjustment of any digital input, including directional control of multiple microphones.

Three microphone bias (MICBIAS) generators are available, which provide a low noise reference for biasing electret condenser microphones (ECMs) or for use as a low noise supply for MEMS microphones and digital microphones.

Digital volume control is available on all inputs (analogue and digital), with programmable ramp control for smooth, glitch-free operation.

The input signal paths and control registers are illustrated in Figure 10.

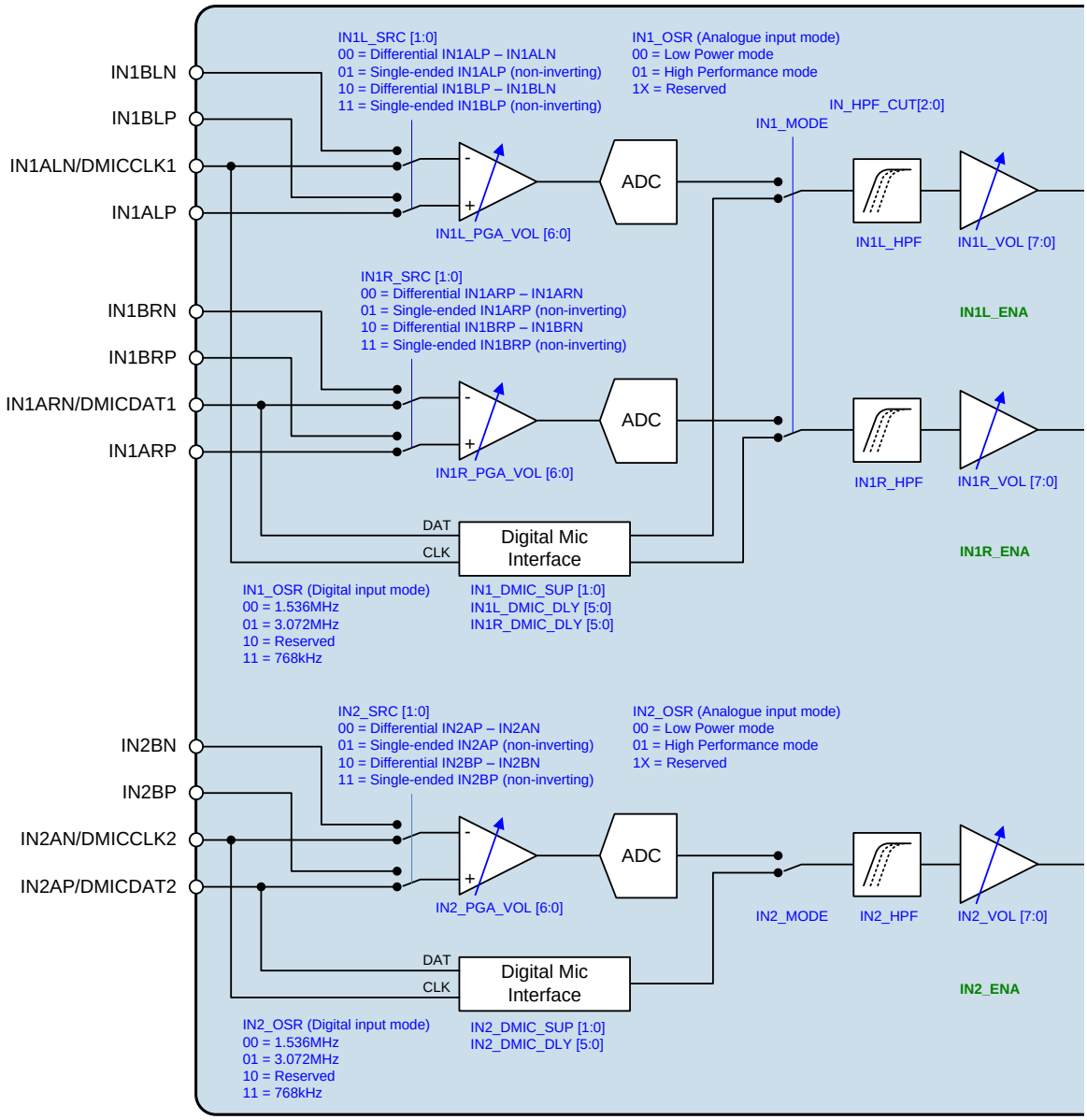


Figure 10 Input Signal Paths

ANALOGUE MICROPHONE INPUT

Up to six analogue microphones can be connected to the WM8998, either in single-ended or differential mode. The applicable mode, and input pin selection, is controlled using the IN*nx*_SRC registers, as described later.

The WM8998 includes external accessory detection circuits, which can detect the presence of a microphone, and the status of a hookswitch or other push-buttons. When using this function, it is recommended to use the IN2B analogue microphone input paths, to ensure best immunity to electrical transients arising from the push-buttons.

For single-ended input, the microphone signal is connected to the non-inverting input of the PGAs (IN*n*LP, IN*n*RP, or IN*n*P). The inverting inputs of the PGAs are connected to an internal reference in this configuration.

For differential input, the non-inverted microphone signal is connected to the non-inverting input of the PGAs (IN*n*LP, IN*n*RP, or IN*n*P), whilst the inverted (or 'noisy ground') signal is connected to the inverting input pins (IN*n*LN, IN*n*RN, or IN*n*N).

The gain of the input PGAs is controlled via register settings, as defined in Table 4. Note that the input impedance of the analogue input paths is fixed across all PGA gain settings.

The Electret Condenser Microphone (ECM) analogue input configurations are illustrated in Figure 11 and Figure 12. The integrated MICBIAS generators provide a low noise reference for biasing the ECMs.

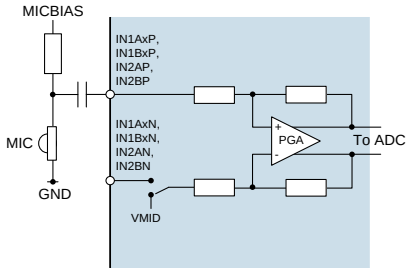


Figure 11 Single-Ended ECM Input

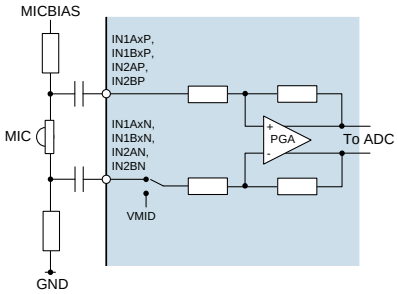


Figure 12 Differential ECM Input

Analogue MEMS microphones can be connected to the WM8998 in a similar manner to the ECM configurations described above; typical configurations are illustrated in Figure 13 and Figure 14. In this configuration, the integrated MICBIAS generators provide a low-noise power supply for the microphones.

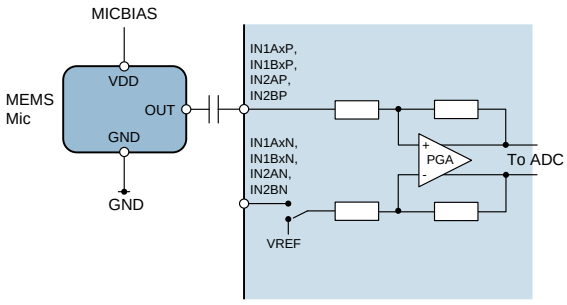


Figure 13 Single-Ended MEMS Input

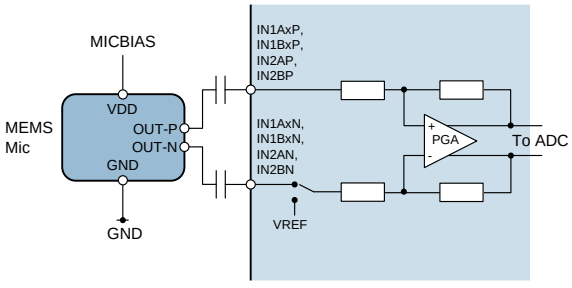


Figure 14 Differential MEMS Input

Note that the MICVDD pin can also be used (instead of MICBIASn) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

ANALOGUE LINE INPUT

Line inputs can be connected to the WM8998 in a similar manner to the microphone inputs described above. Single-ended and differential modes are supported on each of the six analogue input paths.

The applicable mode (single-ended or differential) is selected using the IN*nx*_SRC registers, as described later.

The analogue line input configurations are illustrated in Figure 15 and Figure 16. Note that the microphone bias (MICBIAS) is not used for line input connections.

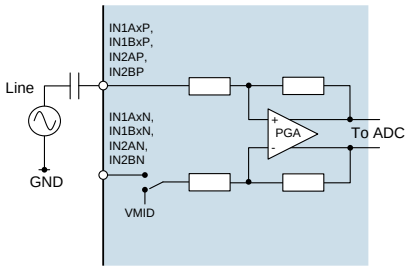


Figure 15 Single-Ended Line Input

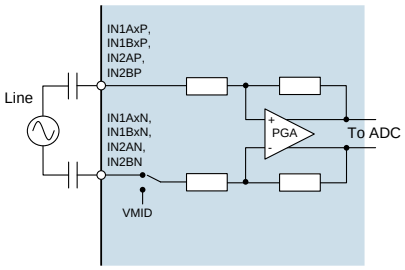


Figure 16 Differential Line Input

DIGITAL MICROPHONE INPUT

Up to three digital microphones can be connected to the WM8998. The digital microphone mode is selected using the IN*n*_MODE registers, as described later. Note that the IN1_MODE setting is applicable to a stereo pair of inputs; the Left and Right channels of any stereo pair of inputs are always in the same mode.

In digital microphone mode, audio data is input on the DMICDAT1 or DMICDAT2 pins. The DMICDAT1 pin carries two multiplexed channels of audio data; the DMICDAT2 pin supports a single channel of audio data. These interfaces are clocked using the respective DMICCLK1 or DMICCLK2 pin.

When digital microphone input is enabled, the WM8998 outputs a clock signal on the applicable DMICCLK*n* pin(s). The DMICCLK*n* frequency is controlled by the respective IN*n*_OSR register, as described in Table 1. See Table 3 for details of the IN*n*_OSR registers.

Note that, if the 768kHz DMICCLKn frequency is selected for one or more of the digital microphone input paths, then the Input Path sample rate (all input paths) is valid in the range 8kHz to 16kHz only.

Note that the DMICCLK*n* frequencies noted in Table 1 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the DMICCLK*n* frequencies will be scaled accordingly.

CONDITION	DMICCLKn FREQUENCY	SIGNAL PASSBAND
IN*n*_OSR = 00	1.536MHz	up to 20kHz
IN*n*_OSR = 01	3.072MHz	up to 20kHz
IN*n*_OSR = 11	768kHz	up to 8kHz

Table 1 DMICCLK Frequency

The voltage reference for each digital microphone interface is selectable, using the IN*n*_DMIC_SUP registers. Each interface may be referenced to MICVDD, or to the MICBIAS1, MICBIAS2 or MICBIAS3 levels.

A stereo pair of digital microphones is connected as illustrated in Figure 17. In this configuration, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The WM8998 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting.

The DMICDAT2 pin supports mono input on the Left interface channel only. The DMIC2 microphone

ust be configured to ensure that it transmits a data bit when DMICCLK is high.

Note that the WM8998 provides integrated pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices.

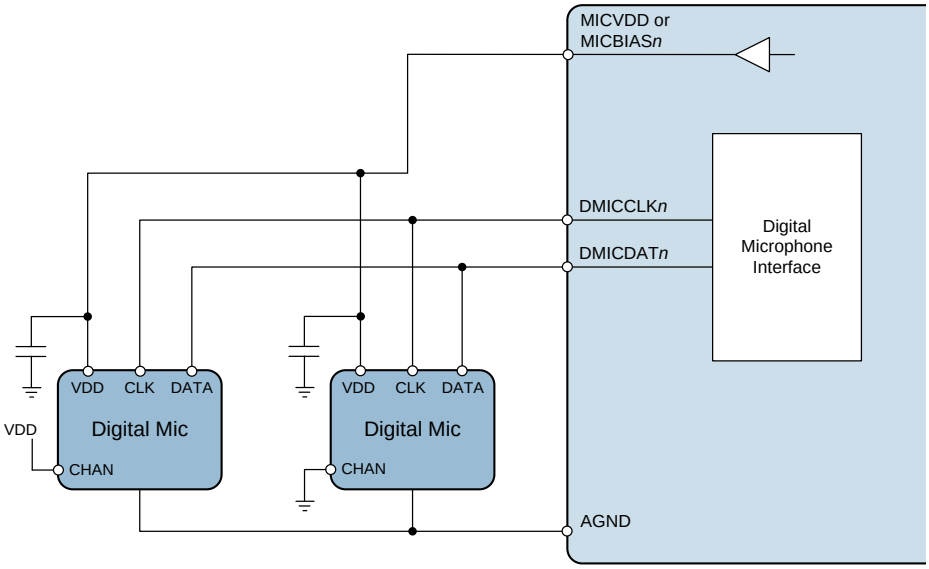


Figure 17 Digital Microphone Input

Two digital microphone channels are interleaved on DMICDAT*n*. The digital microphone interface timing is illustrated in Figure 18. Each microphone must tri-state its data output when the other microphone is transmitting.

The DMICDAT2 pin supports mono input on the Left interface channel only. The DMIC2 microphone ust be configured to ensure that it transmits a data bit when DMICCLK is high.

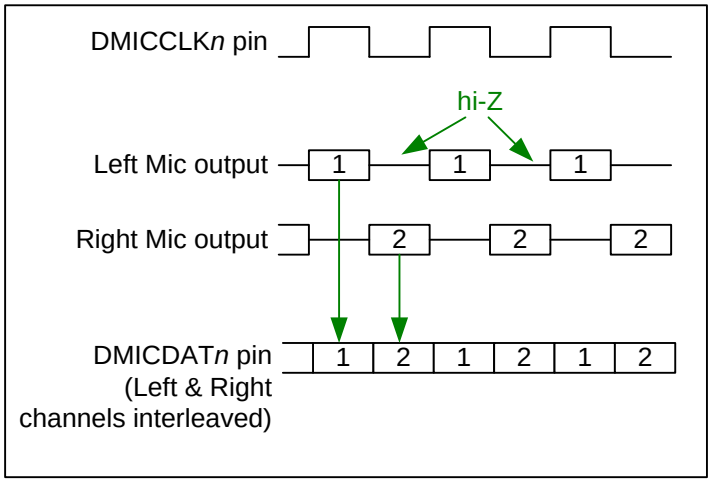


Figure 18 Digital Microphone Interface Timing

When digital microphone input is enabled, the WM8998 outputs a clock signal on the applicable DMICCLK pin(s). The DMICCLK frequency is selectable, as described in Table 1.

Note that SYSCLK must be present and enabled when using the Digital Microphone inputs; see “Clocking and Sample Rates” for details of SYSCLK and the associated register control fields.

INPUT SIGNAL PATH ENABLE

The input signal paths are enabled using the register bits described in Table 2. The respective bit(s) must be enabled for analogue or digital input on the respective input path(s).

The input signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The input signal path mute functions are controlled using the register bits described in Table 4.

The MICVDD power domain must be enabled when using the analogue input signal path(s). This power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See "Charge Pumps, Regulators and Voltage Reference" for details of these circuits.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK and 32kHz clock may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks.

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the input signal paths and associated ADCs. If an attempt is made to enable an input signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The status bits in Register R769 indicate the status of each of the input signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which input signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) Input Enables	3	IN2_ENA	0	Input Path 2 Enable 0 = Disabled 1 = Enabled
	1	IN1L_ENA	0	Input Path 1 (Left) Enable 0 = Disabled 1 = Enabled
	0	IN1R_ENA	0	Input Path 1 (Right) Enable 0 = Disabled 1 = Enabled
R769 (0301h) Input Enables Status	3	IN2_ENA_STS	0	Input Path 2 Enable Status 0 = Disabled 1 = Enabled
	1	IN1L_ENA_STS	0	Input Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	IN1R_ENA_STS	0	Input Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 2 Input Signal Path Enable

INPUT SIGNAL PATH SAMPLE RATE CONTROL

The input signal paths may be selected as input to the digital mixers or signal processing functions within the WM8998 digital core. The sample rate for the input signal paths is configured using the IN_RATE register - see Table 19 within the “Digital Core” section.

Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

INPUT SIGNAL PATH CONFIGURATION

The WM8998 supports six input channels. Selectable combinations of analogue (mic or line) and digital inputs are multiplexed into three input signal paths.

The input signal path configuration is selected using the IN*n*_MODE and IN*n*x_SRC registers (where ‘n’ identifies the associated input, and ‘x’ identifies the left/right channel, where applicable). The external circuit configurations are illustrated on the previous pages.

A configurable high pass filter (HPF) is provided on the left and right channels of each input path. The applicable cut-off frequency is selected using the IN_HPF_CUT register. The filter can be enabled on each path independently using the IN1L_HPF, IN1R_HPF and IN2_HPF bits.

The analogue input signal paths (single-ended or differential) each incorporate a PGA to provide gain in the range 0dB to +31dB in 1dB steps. Note that these PGAs do not provide pop suppression functions; it is recommended that the gain should not be adjusted whilst the respective signal path is enabled.

The analogue input PGA gain is controlled using the IN1L_PGA_VOL, IN1R_PGA_VOL and IN2_PGA_VOL registers.

When the input signal path is configured for digital microphone input, the voltage reference for the associated input/output pins is selectable using the IN*n*_DMIC_SUP registers - each interface may be referenced to MICVDD, or to the MICBIAS1, MICBIAS2 or MICBIAS3 levels.

When the input signal path is configured for digital microphone input, the respective DMICCLKn frequency can be configured using the INn_OSR register bits.

A digital delay may be applied to any of the digital microphone input channels. This feature can be used for phase adjustment of any digital input, including directional control of multiple microphones. The delay is controlled using the IN1L_DMIC_DLY, IN1R_DMIC_DLY and IN2_DMIC_DLY registers.

The MICVDD voltage is generated by an internal Charge Pump and LDO Regulator. The MICBIAS1, MICBIAS2 and MICBIAS3 outputs are derived from MICVDD - see “Charge Pumps, Regulators and Voltage Reference”.

Under default register conditions, the input signal paths are configured for highest performance. This can be adjusted using the IN*n*_OSR registers, which provide control of the DMICCLK*n* frequency and the ADC oversample rate.

The input signal paths are configured using the register bits described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R780 (030Ch) HPF Control	2:0	IN_HPF_CUT [2:0]	010	Input Path HPF Select Controls the cut-off frequency of the input path HPF circuits. 000 = 2.5Hz 001 = 5Hz 010 = 10Hz 011 = 20Hz 100 = 40Hz All other codes are Reserved
R784 (0310h) IN1L Control	15	IN1L_HPF	0	Input Path 1 (Left) HPF Enable 0 = Disabled 1 = Enabled
	14:13	IN1_OSR [1:0]	01	Input Path 1 DMIC Oversample Rate When analogue input is selected (IN1_MODE=0), this bit controls the performance mode 00 = Low Power mode 01 = High Performance mode 1X = Reserved When digital microphone input is selected (IN1_MODE=1), this field controls the sample rate as below: 00 = 1.536MHz 01 = 3.072MHz 10 = Reserved 11 = 768kHz When IN1_OSR=11, the Input Path sample rate (for all input paths) must be in the range 8kHz to 16kHz.
	12:11	IN1_DMIC_SUP [1:0]	00	Input Path 1 DMIC Reference Select (Sets the DMICDAT1 and DMICCLK1 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	10	IN1_MODE	0	Input Path 1 Mode 0 = Analogue input 1 = Digital input
	7:1	IN1L_PGA_VOL [6:0]	40h	Input Path 1 (Left) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R785 (0311h) ADC Digital Volume 1L	14:13	IN1L_SRC [1:0]	00	Input Path 1 (Left) Source 00 = Differential (IN1ALP - IN1ALN) 01 = Single-ended (IN1ALP) 10 = Differential (IN1BLP-IN1BLN) 11 = Single-ended (IN1BLP)
R786 (0312h) DMIC1L Control	5:0	IN1L_DMIC_DLY [5:0]	00h	Input Path 1 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R788 (0314h) IN1R Control	15	IN1R_HPF	0	Input Path 1 (Right) HPF Enable 0 = Disabled 1 = Enabled
	7:1	IN1R_PGA_VOL [6:0]	40h	Input Path 1 (Right) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R789 (0315h) ADC Digital Volume 1R	14:13	IN1R_SRC [1:0]	00	Input Path 1 (Right) Source 00 = Differential (IN1ARP - IN1ARN) 01 = Single-ended (IN1ARP) 10 = Differential (IN1BRP-IN1BRN) 11 = Single-ended (IN1BRP)
R790 (0316h) DMIC1R Control	5:0	IN1R_DMIC_DLY [5:0]	00h	Input Path 1 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)
R792 (0318h) IN2L Control	15	IN2_HPF	0	Input Path 2 HPF Enable 0 = Disabled 1 = Enabled
	14:13	IN2_OSR [1:0]	01	Input Path 2 DMIC Oversample Rate When analogue input is selected (IN1_MODE=0), this bit controls the performance mode 00 = Low Power mode 01 = High Performance mode 1X = Reserved When digital microphone input is selected (IN2_MODE=1), this field controls the sample rate as below: 00 = 1.536MHz 01 = 3.072MHz 10 = Reserved 11 = 768kHz When IN2_OSR=11, the Input Path sample rate (for all input paths) must be in the range 8kHz to 16kHz.
	12:11	IN2_DMIC_SUP [1:0]	00	Input Path 2 DMIC Reference Select (Sets the DMICDAT2 and DMICCLK2 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	10	IN2_MODE	0	Input Path 2 Mode 0 = Analogue input 1 = Digital input

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:1	IN2_PGA_VOL [6:0]	40h	Input Path 2 PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R793 (0319h) ADC Digital Volume 2L	14:13	IN2_SRC [1:0]	00	Input Path 2 Source 00 = Differential (IN2AP - IN2AN) 01 = Single-ended (IN2AP) 10 = Differential (IN2BP-IN2BN) 11 = Single-ended (IN2BP)
R794 (031Ah) DMIC2L Control	5:0	IN2_DMIC_DLY [5:0]	00h	Input Path 2 Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN2_OSR.)

Table 3 Input Signal Path Configuration

INPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the input signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each input signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the IN_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the IN_VD_RAMP register. Note that the IN_VI_RAMP and IN_VD_RAMP registers should not be changed while a volume ramp is in progress.

The IN_VU bits control the loading of the input signal path digital volume and mute controls. When IN_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the input signal paths are updated when a 1 is written to IN_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the IN1/IN2 digital input paths is not equal to the 0dBFS level of the WM8998 digital core. The maximum digital input signal level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a -6dBFS input signal corresponds to a 0dBFS input to the WM8998 digital core functions.

The digital volume control register fields are described in Table 4 and Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R777 (0309h) Input Volume Ramp	6:4	IN_VD_RAMP [2:0]	010	Input Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	IN_VI_RAMP [2:0]	010	Input Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R785 (0311h) ADC Digital Volume 1L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1L_MUTE	1	Input Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN1L_VOL [7:0]	80h	Input Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R789 (0315h) ADC Digital Volume 1R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1R_MUTE	1	Input Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN1R_VOL [7:0]	80h	Input Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R793 (0319h) ADC Digital Volume 2L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN2_MUTE	1	Input Path 2 Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN2_VOL [7:0]	80h	Input Path 2 Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)

Table 4 Input Signal Path Digital Volume Control

Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
00.	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 5 Input Signal Path Digital Volume Range

DIGITAL MICROPHONE INTERFACE PULL-DOWN

The WM8998 provides integrated pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices.

Each of the pull-down resistors can be configured independently using the register bits described in Table 6. Note that, if the DMICDAT1 or DMICDAT2 digital microphone input paths are disabled, then the pull-down will be disabled on the respective pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3106 (0C22h) Misc Pad Ctrl 3	1	DMICDAT2_PD	0	DMICDAT2 Pull-Down Control 0 = Disabled 1 = Enabled
	0	DMICDAT1_PD	0	DMICDAT1 Pull-Down Control 0 = Disabled 1 = Enabled

Table 6 Digital Microphone Interface Pull-Down Control

DIGITAL CORE

The WM8998 digital core provides extensive mixing and processing capabilities for multiple signal paths. The configuration is highly flexible, and virtually every conceivable input/output connection can be supported between the available processing blocks.

The digital core provides parametric equalisation (EQ) functions, dynamic range control (DRC), and low-pass / high-pass filters (LHPF).

The WM8998 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between input (ADC) paths, output (DAC) paths, Digital Audio Interfaces (AIF1, AIF2 and AIF3) and SLIMbus paths operating at different sample rates and/or referenced to asynchronous clock domains.

The digital core incorporates a S/PDIF transmitter, which can provide a stereo S/PDIF output on a GPIO pin. Standard S/PDIF sample rates of 32kHz up to 192kHz can be supported.

The WM8998 incorporates two 1kHz tone generators which can be used for ‘beep’ functions through any of the audio signal paths.

A haptic signal generator is provided, for use with external haptic devices (eg. mechanical vibration actuators). Two Pulse Width Modulation (PWM) signal generators are also provided; the PWM waveforms can be modulated by an audio source within the digital core, and can be output on a GPIO pin.

An overview of the digital core processing and mixing functions is provided in Figure 19. An overview of the external digital interface paths is provided in Figure 20.

The control registers associated with the digital core signal paths are shown in Figure 21 through to Figure 36. The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

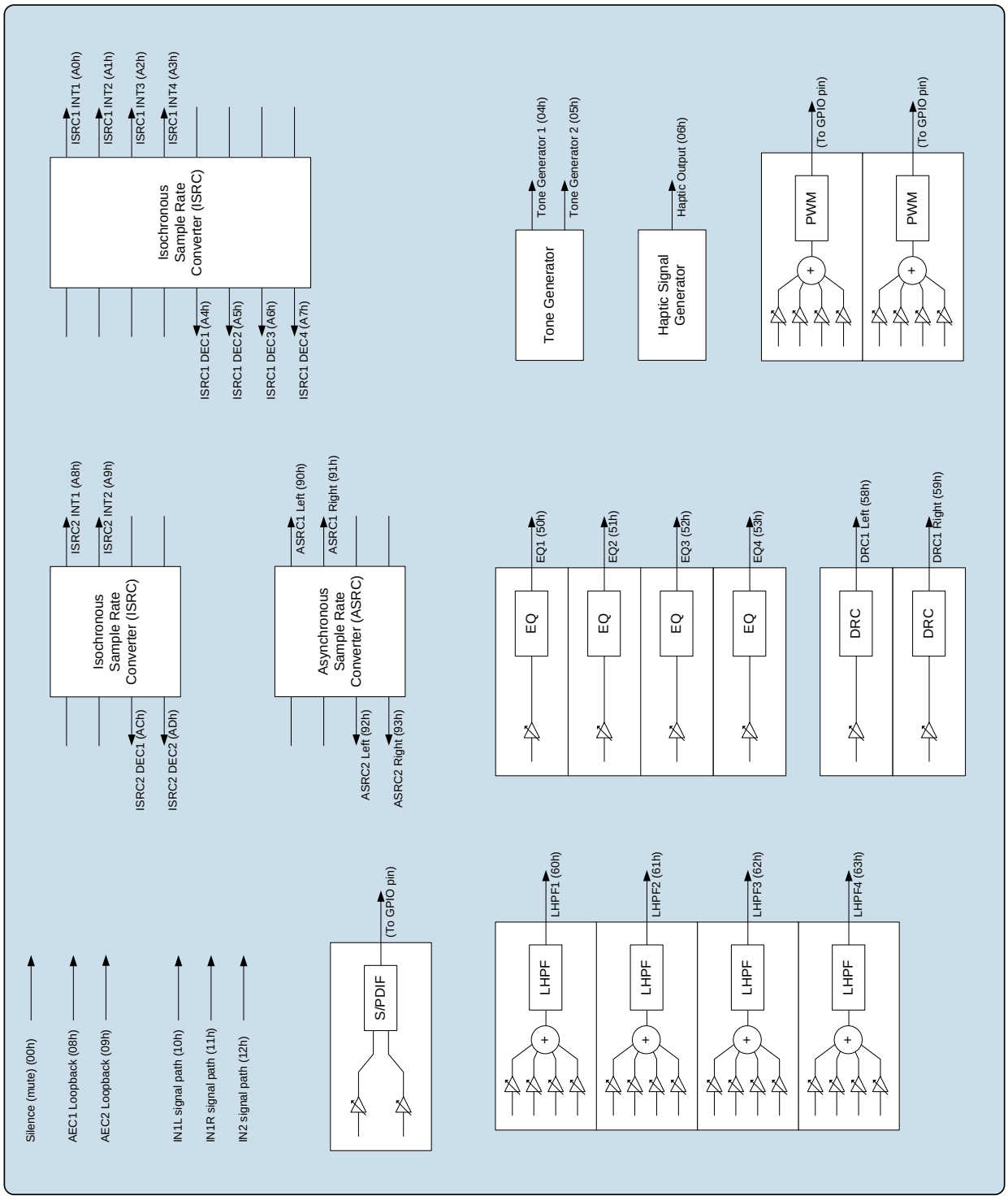


Figure 19 Digital Core - Internal Signal Processing

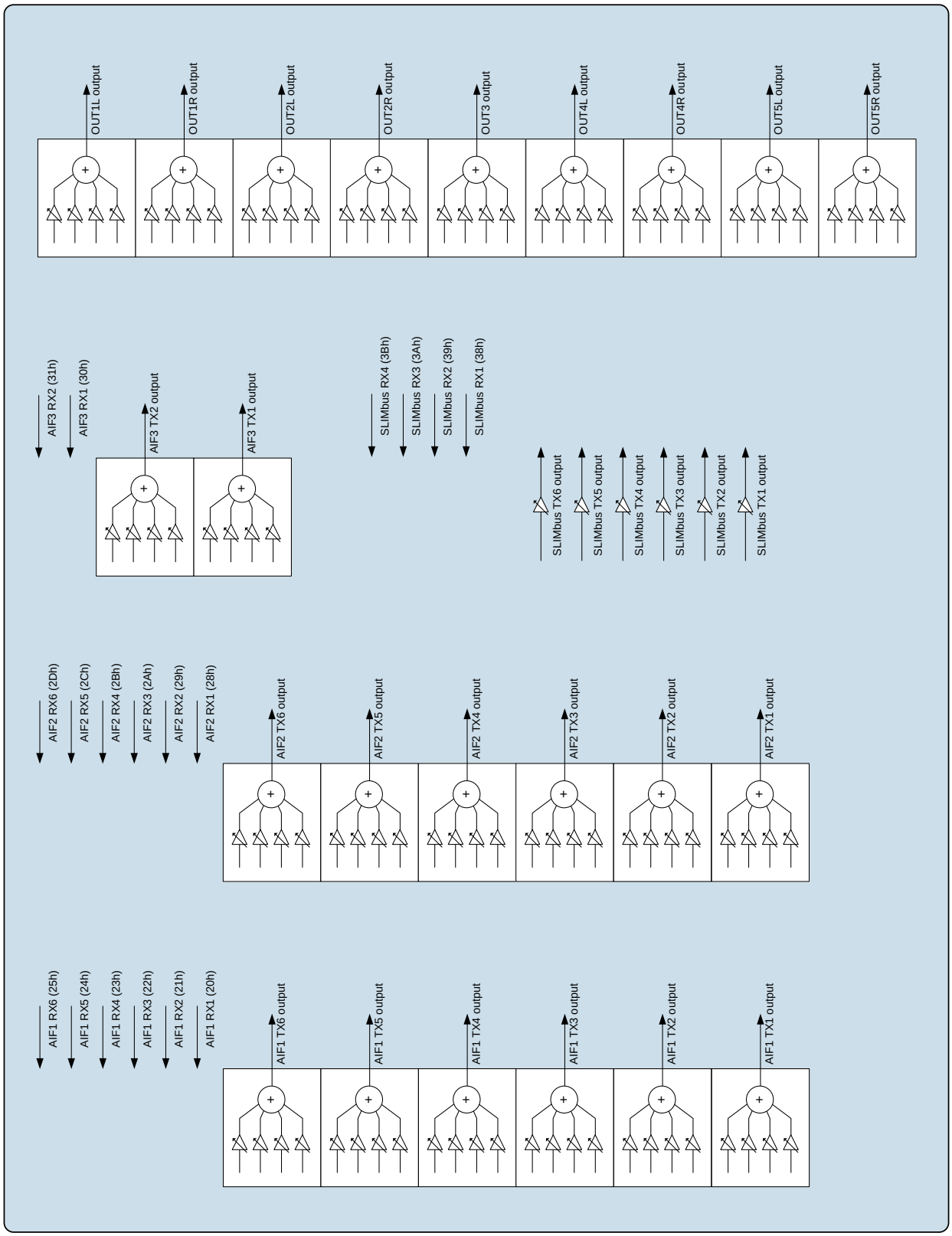


Figure 20 Digital Core - External Digital Interfaces

DIGITAL CORE MIXERS

The WM8998 provides an extensive digital mixing capability. The digital core signal processing blocks and audio interface paths are illustrated in Figure 19 and Figure 20.

A 4-input digital mixer is associated with many of these functions, as illustrated. The digital mixer circuit is identical in each instance, providing up to 4 selectable input sources, with independent volume control on each input.

The control registers associated with the digital core signal paths are shown in Figure 21 through to Figure 36. The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920).

Further description of the associated control registers is provided below. Generic register definitions are provided in Table 7.

The digital mixer input sources are selected using the associated *_SRC*n* registers; the volume control is implemented via the associated *_VOL*n* registers.

The ASRC, ISRC, SLIMbus, EQ and DRC functions support selectable input sources, but do not incorporate any digital mixing. The respective input source (*_SRC*n*) registers are identical to those of the digital mixers.

The *_SRC*n* registers select the input source(s) for the respective mixer or signal processing block. Note that the selected input source(s) must be configured for the same sample rate as the block(s) to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

A status bit associated with each of the configurable input sources provides readback for the respective signal path. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

The generic register definition for the digital mixers is provided in Table 7.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1600 (0640h) to R2920 (0B68h)	15	*_STSn Valid for every digital core function input (digital mixers, SLIMbus TX, ASRC, ISRC, SLIMbus, EQ and DRC inputs).	0	[Digital Core function] input *n* status 0 = Disabled 1 = Enabled
	7:1	*_VOLn Valid for every digital mixer, SLIMbus TX, EQ and DRC input.	40h	[Digital Core mixer] input *n* volume -32dB to +16dB in 1dB steps 00h to 20h = -32dB 21h = -31dB 22h = -30dB ... (1dB steps) 40h = 0dB ... (1dB steps) 50h = +16dB 51h to 7Fh = +16dB
	8:0	*_SRCn Valid for every digital core function input (digital mixers, SLIMbus TX, ASRC, ISRC, EQ	00h	[Digital Core function] input *n* source select 00h = Silence (mute) 04h = Tone generator 1 05h = Tone generator 2 06h = Haptic generator 08h = AEC1 loopback 09h = AEC2 loopback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		and DRC inputs).		10h = IN1L signal path 11h = IN1R signal path 12h = IN2 signal path 20h = AIF1 RX1 21h = AIF1 RX2 22h = AIF1 RX3 23h = AIF1 RX4 24h = AIF1 RX5 25h = AIF1 RX6 28h = AIF2 RX1 29h = AIF2 RX2 2Ah = AIF2 RX3 2Bh = AIF2 RX4 2Ch = AIF2 RX5 2Dh = AIF2 RX6 30h = AIF3 RX1 31h = AIF3 RX2 38h = SLIMbus RX1 39h = SLIMbus RX2 3Ah = SLIMbus RX3 3Bh = SLIMbus RX4 50h = EQ1 51h = EQ2 52h = EQ3 53h = EQ4 58h = DRC1 Left 59h = DRC1 Right 60h = LHPF1 61h = LHPF2 62h = LHPF3 63h = LHPF4 90h = ASRC1 Left 91h = ASRC1 Right 92h = ASRC2 Left 93h = ASRC2 Right A0h = ISRC1 INT1 A1h = ISRC1 INT2 A2h = ISRC1 INT3 A3h = ISRC1 INT4 A4h = ISRC1 DEC1 A5h = ISRC1 DEC2 A6h = ISRC1 DEC3 A7h = ISRC1 DEC4 A8h = ISRC2 INT1 A9h = ISRC2 INT2 ACh = ISRC2 DEC1 ADh = ISRC2 DEC2

Table 7 Digital Core Mixer Control Registers

DIGITAL CORE INPUTS

The digital core comprises multiple input paths as illustrated in Figure 21. Any of these inputs may be selected as a source to the digital mixers or signal processing functions within the WM8998 digital core.

Note that the outputs from other blocks within the Digital Core may also be selected as input to the digital mixers or signal processing functions within the WM8998 digital core. Those input sources, which are not shown in Figure 21, are described separately in other sections of the "Digital Core" description.

The bracketed numbers in Figure 21, eg. "(10h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the input signal paths is configured using the applicable IN_RATE, AIFn_RATE or SLIMRXn_RATE register - see Table 19. Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

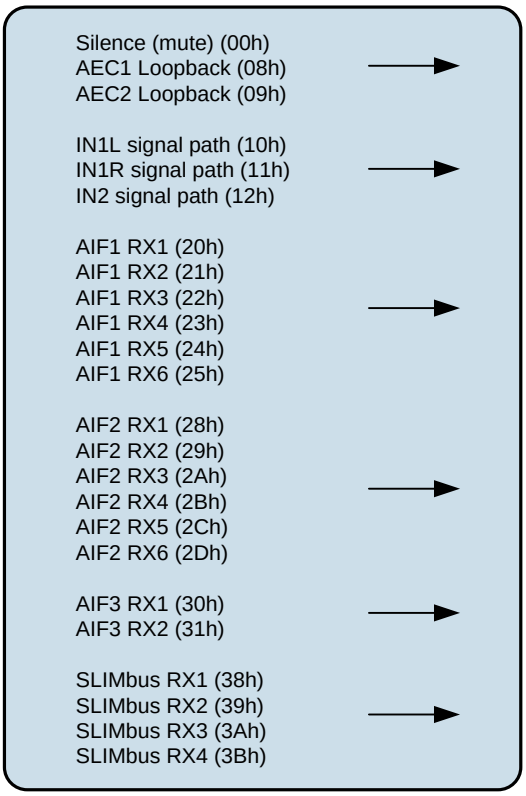


Figure 21 Digital Core Inputs

DIGITAL CORE OUTPUTS

The digital core comprises multiple output paths. The output paths associated with AIF1, AIF2 and AIF3 are illustrated in Figure 22. The output paths associated with OUT1, OUT2, OUT3, OUT4 and OUT5 are illustrated in Figure 23. The output paths associated with the SLIMbus interface are illustrated in Figure 24.

A 4-input mixer is associated with each of the AIFn or OUTn signal paths. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Note that there are no mixers associated with the SLIMbus output paths.

The AIF1, AIF2 and AIF3 output mixer control registers (see Figure 22) are located at register addresses R1792 (700h) through to R1935 (78Fh). The OUT1, OUT2, OUT3, OUT4 and OUT5 output mixer control registers (see Figure 23) are located at addresses R1664 (680h) through to R1743 (06CFh). The SLIMbus output control registers (see Figure 24) are located at addresses R1984 (7C0h) through to R2025 (7E9h).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective signal paths. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The sample rate for the output signal paths is configured using the applicable OUT_RATE, AIFn_RATE or SLIMTXn_RATE register - see Table 19. Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output mixer paths. If an attempt is made to enable an output mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

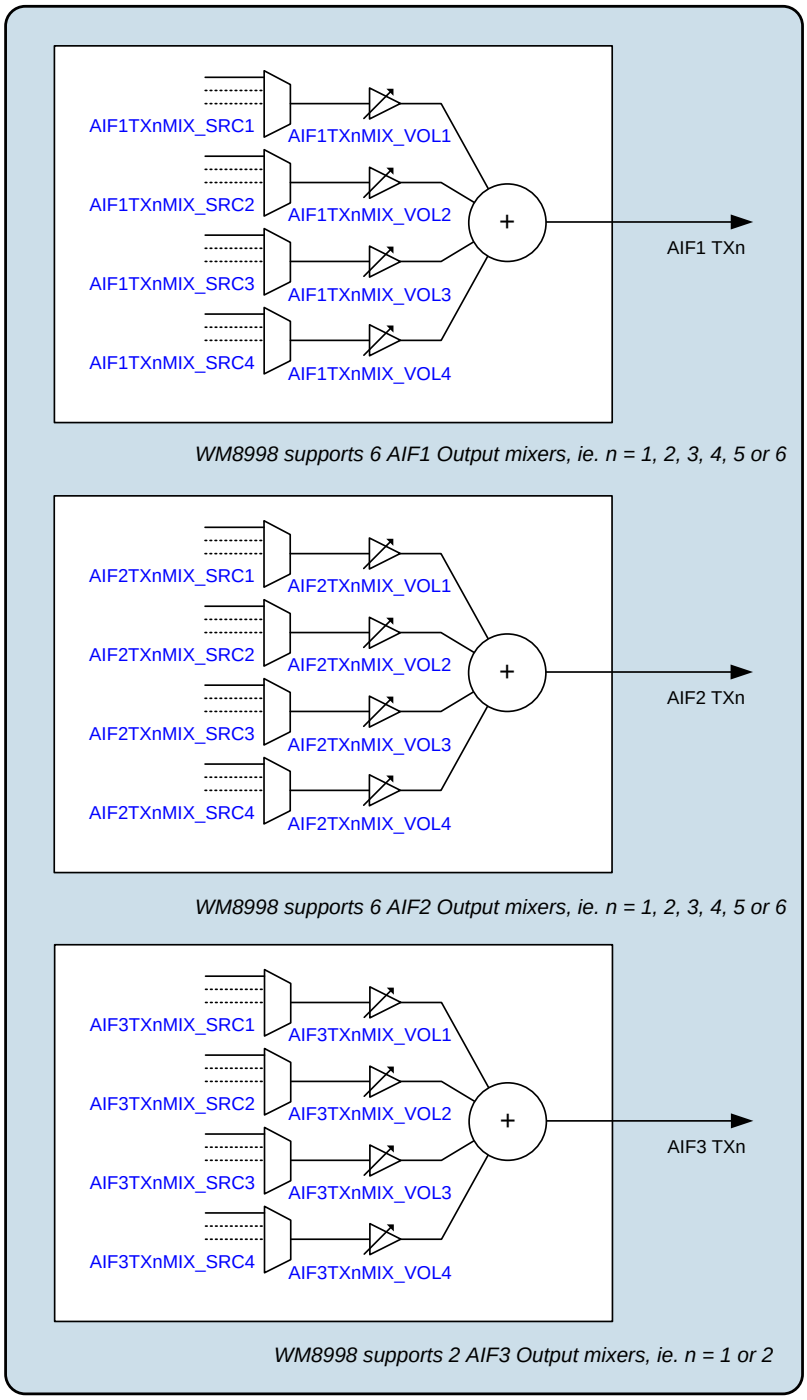


Figure 22 Digital Core AIF Outputs

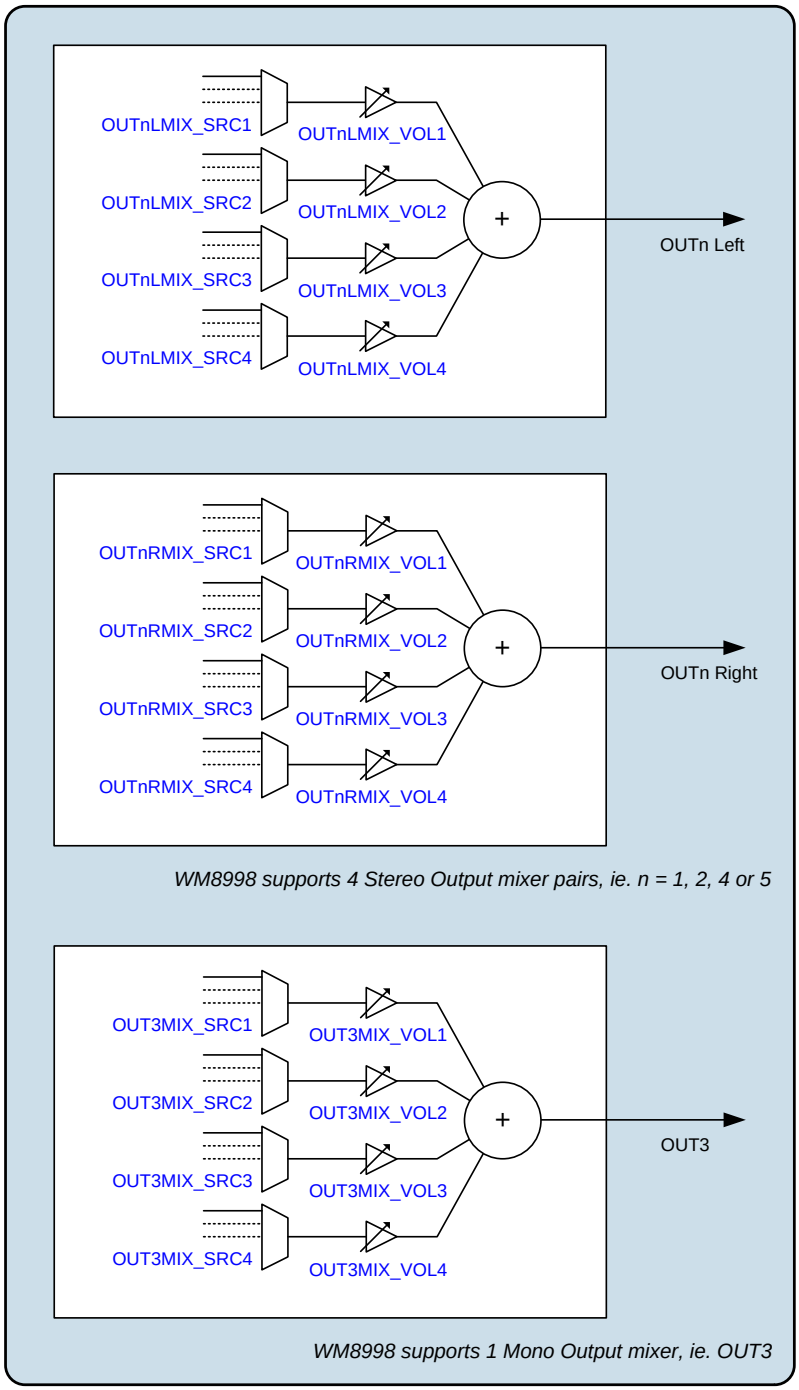


Figure 23 Digital Core OUTn Outputs

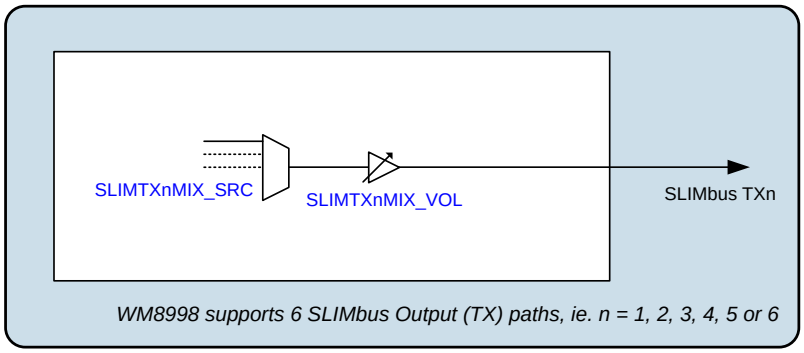


Figure 24 Digital Core SLIMbus Outputs

5-BAND PARAMETRIC EQUALISER (EQ)

The digital core provides four EQ processing blocks as illustrated in Figure 25. The input source for each EQ is selectable, and a digital volume control is provided for each path. Each EQ block supports 1 input and 1 output.

The EQ provides selective control of 5 frequency bands as described below.

The low frequency band (Band 1) filter can be configured either as a peak filter or a shelving filter. When configured as a shelving filter, is provides adjustable gain below the Band 1 cut-off frequency. As a peak filter, it provides adjustable gain within a defined frequency band that is centred on the Band 1 frequency.

The mid frequency bands (Band 2, Band 3, Band 4) filters are peak filters, which provide adjustable gain around the respective centre frequency.

The high frequency band (Band 5) filter is a shelving filter, which provides adjustable gain above the Band 5 cut-off frequency.

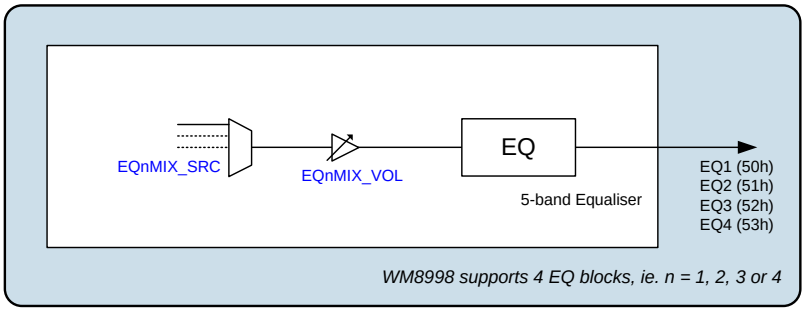


Figure 25 Digital Core EQ Blocks

The EQ1, EQ2, EQ3 and EQ4 input control registers (see Figure 25) are located at register addresses R2176 (880h) through to R2201 (899h).

The full list of digital mixer control registers is provided in the "Register Map" section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source for the respective EQ processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the EQ to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 25, eg. "(50h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the EQ function is configured using the FX_RATE register - see Table 19. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the EQ signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The control registers associated with the EQ functions are described in Table 9.

The cut-off or centre frequencies for the 5-band EQ are set using the coefficients held in the registers identified in Table 8. These coefficients are derived using tools provided in Cirrus's WISCE™ evaluation board control software; please contact your local Cirrus representative for more details.

EQ	REGISTER ADDRESSES
EQ1	R3602 (0E10h) to R3620 (0E24h)
EQ2	R3624 (0E28h) to R3642 (0E3Ah)
EQ3	R3646 (0E3Eh) to R3664 (0E53h)
EQ4	R3668 (0E54h) to R3686 (0E66h)

Table 8 EQ Coefficient Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	000h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = Reserved [6] = Reserved [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3600 (0E10h) EQ1_1	15:11	EQ1_B1_GAIN [4:0]	01100	EQ1 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ1_B2_GAIN [4:0]	01100	EQ1 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ1_B3_GAIN [4:0]	01100	EQ1 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	EQ1_ENA	0	EQ1 Enable 0 = Disabled 1 = Enabled
R3601 (0E11h) EQ1_2	15:11	EQ1_B4_GAIN [4:0]	01100	EQ1 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ1_B5_GAIN [4:0]	01100	EQ1 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ1_B1_MODE	0	EQ1 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3602 (0E12h) to R3620 (E24h)	15:0	EQ1_B1_* EQ1_B2_* EQ1_B3_* EQ1_B4_* EQ1_B5_*		EQ1 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.
R3622 (0E26h) EQ2_1	15:11	EQ2_B1_GAIN [4:0]	01100	EQ2 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ2_B2_GAIN [4:0]	01100	EQ2 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ2_B3_GAIN [4:0]	01100	EQ2 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ2_ENA	0	EQ2 Enable 0 = Disabled 1 = Enabled
R3623 (0E27h) EQ2_2	15:11	EQ2_B4_GAIN [4:0]	01100	EQ2 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ2_B5_GAIN [4:0]	01100	EQ2 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ2_B1_MODE	0	EQ2 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3624 (0E28h) to R3642 (E3Ah)	15:0	EQ2_B1_* EQ2_B2_* EQ2_B3_* EQ2_B4_* EQ2_B5_*		EQ2 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.
R3644 (0E3Ch) EQ3_1	15:11	EQ3_B1_GAIN [4:0]	01100	EQ3 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ3_B2_GAIN [4:0]	01100	EQ3 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ3_B3_GAIN [4:0]	01100	EQ3 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ3_ENA	0	EQ3 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3645 (0E3Dh) EQ3_2	15:11	EQ3_B4_GAIN [4:0]	01100	EQ3 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ3_B5_GAIN [4:0]	01100	EQ3 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ3_B1_MODE	0	EQ3 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3646 (0E3Eh) to R3664 (E50h)	15:0	EQ3_B1_* EQ3_B2_* EQ3_B3_* EQ3_B4_* EQ3_B5_*		EQ3 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.
R3666 (0E52h) EQ4_1	15:11	EQ4_B1_GAIN [4:0]	01100	EQ4 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ4_B2_GAIN [4:0]	01100	EQ4 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ4_B3_GAIN [4:0]	01100	EQ4 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ4_ENA	0	EQ4 Enable 0 = Disabled 1 = Enabled
R3667 (0E53h) EQ4_2	15:11	EQ4_B4_GAIN [4:0]	01100	EQ4 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ4_B5_GAIN [4:0]	01100	EQ4 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ4_B1_MODE	0	EQ4 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3668 (0E54h) to R3686 (E66h)	15:0	EQ4_B1_* EQ4_B2_* EQ4_B3_* EQ4_B4_* EQ4_B5_*		EQ4 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.

Table 9 EQ Enable and Gain Control

EQ GAIN SETTING	GAIN (dB)
00000	-12
00001	-11
00010	-10
00011	-9
00100	-8
00101	-7
00110	-6
00111	-5
01000	-4
01001	-3
01010	-2
01011	-1
01100	0
01101	+1
01110	+2
01111	+3
10000	+4
10001	+5
10010	+6
10011	+7
10100	+8
10101	+9
10110	+10
10111	+11
11000	+12
11001 to 11111	Reserved

Table 10 EQ Gain Control Range

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded EQ and digital mixing functions. If an attempt is made to enable an EQ signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

DYNAMIC RANGE CONTROL (DRC)

The digital core provides a stereo Dynamic Range Control (DRC) processing block as illustrated in Figure 26. The input sources to the DRC are selectable for each channel (ie. Left and Right), and independent volume control is provided for each path.

The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system, or to restrict the dynamic range of an output signal path.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates ‘anti-clip’ and ‘quick release’ features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

A Signal Detect function is provided within the DRC; this can be used to detect the presence of an audio signal, and used to trigger other events. The Signal Detect function can be used as an Interrupt event, or as a GPIO output, or used to trigger the Control Write Sequencer.

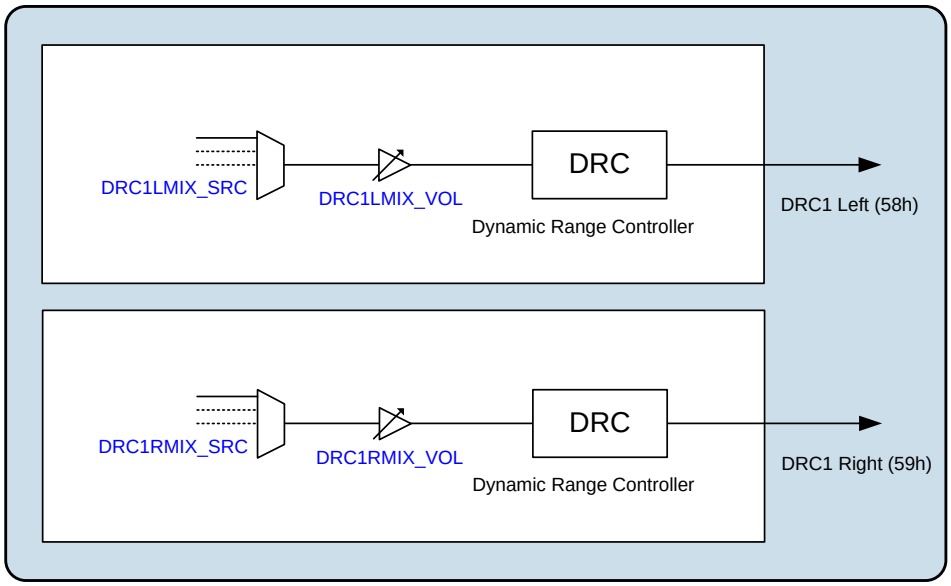


Figure 26 Dynamic Range Control (DRC) Block

The DRC1 input control registers (see Figure 26) are located at register addresses R2240 (8C0h) through to R2249 (08C9h).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source for the respective DRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the DRC to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The bracketed numbers in Figure 26, eg. “(58h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the DRC function is configured using the FX_RATE register - see Table 19. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the DRC signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The DRC functions are enabled using the control registers described in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3712 (0E80h) DRC1 ctrl1	1	DRC1L_ENA	0	DRC1 (Left) Enable 0 = Disabled 1 = Enabled
	0	DRC1R_ENA	0	DRC1 (Right) Enable 0 = Disabled 1 = Enabled

Table 11 DRC Enable

DRC Compression / Expansion / Limiting

The DRC supports two different compression regions, separated by a “Knee” at a specific input amplitude. In the region above the knee, the compression slope DRC1_HI_COMP applies; in the region below the knee, the compression slope DRC1_LO_COMP applies.

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope DRC1_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 27). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the DRC1_LO_COMP and DRC1_NG_EXP regions.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 27.

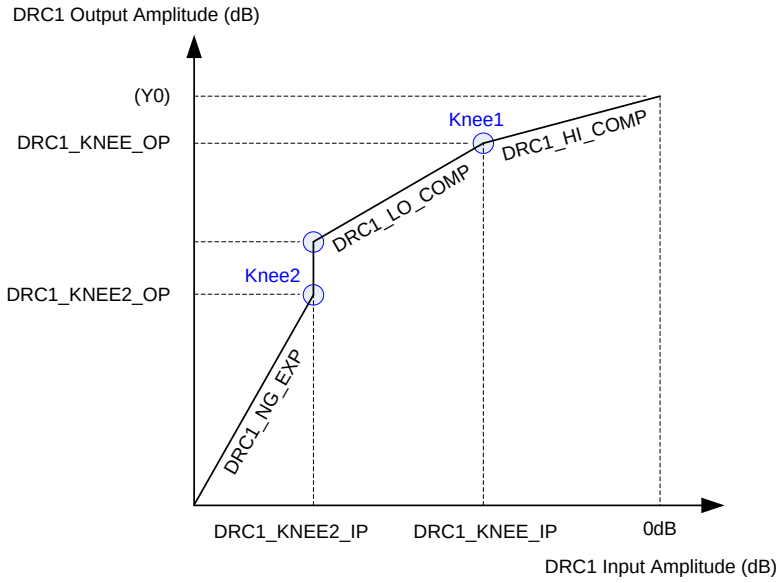


Figure 27 DRC Response Characteristic

The slope of the DRC response is determined by register fields DRC1_HI_COMP and DRC1_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the DRC1_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (ie. a change in input amplitude produces a larger change in output amplitude).

When the DRC1_KNEE2_OP knee is enabled (“Knee2” in Figure 27), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 12.

REF	PARAMETER	DESCRIPTION
1	DRC1_KNEE_IP	Input level at Knee1 (dB)
2	DRC1_KNEE_OP	Output level at Knee2 (dB)
3	DRC1_HI_COMP	Compression ratio above Knee1
4	DRC1_LO_COMP	Compression ratio below Knee1
5	DRC1_KNEE2_IP	Input level at Knee2 (dB)
6	DRC1_NG_EXP	Expansion ratio below Knee2
7	DRC1_KNEE2_OP	Output level at Knee2 (dB)

Table 12 DRC Response Parameters

The noise gate is enabled when the DRC1_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the DRC1_LO_COMP slope applies to all input signal levels below Knee1.

The DRC1_KNEE2_OP knee is enabled when the DRC1_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the DRC1_LO_COMP region.

The "Knee1" point in Figure 27 is determined by register fields DRC1_KNEE_IP and DRC1_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

Y0 = DRC1_KNEE_OP - (DRC1_KNEE_IP x DRC1_HI_COMP)

Gain Limits

The minimum and maximum gain applied by the DRC is set by register fields DRC1_MINGAIN, DRC1_MAXGAIN and DRC1_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 27. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by DRC1_MINGAIN. The mimimum gain in the Noise Gate region is set by DRC1_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DRC1_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

Dynamic Characteristics

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The DRC1_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The DRC1_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 13. Note that the register defaults are suitable for general purpose microphone use.

Anti-Clip Control

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRC1_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

Quick Release Control

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constant of DRC1_DCY.

The Quick-Release feature is enabled by setting the DRC1_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the

level set by DRC1_QR_THR, then the normal decay rate (DRC1_DCY) is ignored and a faster decay rate (DRC1_QR_DCY) is used instead.

Signal Activity Detect

The DRC incorporates a configurable signal detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an ADC or digital mic channel, or can be used to detect an audio signal received over the digital audio interface.

The DRC Signal Detect function is enabled by setting DRC1_SIG_DET register bit. (Note that DRC1 must also be enabled.) The detection threshold is either a Peak level (Crest Factor) or an RMS level, depending on the DRC1_SIG_DET_MODE register bit. When Peak level is selected, the threshold is determined by DRC1_SIG_DET_PK, which defines the applicable Crest Factor (Peak to RMS ratio) threshold. If RMS level is selected, then the threshold is set using DRC1_SIG_DET_RMS.

The DRC Signal Detect function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The DRC Signal Detect signal can be output directly on a GPIO pin as an external indication of the Signal Detection. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The Control Write Sequencer can be triggered by the DRC Signal Detect function. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit. See “Control Write Sequencer” for further details.

GPIO Outputs from DRC

The Dynamic Range Control (DRC) circuit provides a number of status outputs, which can be output directly on a GPIO pin as an external indication of the DRC Status. See “General Purpose Input / Output” to configure a GPIO pin for these functions.

Each of the DRC status outputs is described below.

The DRC Signal Detect flag indicates that a signal is present on the respective signal path. The threshold level for signal detection is configurable using the register fields are described in Table 13.

The DRC Anti-Clip flag indicates that the DRC Anti-Clip function has been triggered. In this event, the DRC gain is decreasing in response to a rising signal level. The flag is asserted until the DRC gain stablises.

The DRC Decay flag indicates that the DRC gain is increasing in response to a low level signal input. The flag is asserted until the DRC gain stabilises.

The DRC Noise Gate flag indicates that the DRC Noise Gate function has been triggered, indicating that an idle condition has been detected in the signal path.

The DRC Quick Release flag indicates that the DRC Quick Release function has been triggered. In this event, the DRC gain is increasing rapidly following detection of a short transient peak. The flag is asserted until the DRC gain stabilises.

DRC Register Controls

The DRC control registers are described in Table 13.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	000h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = Reserved [6] = Reserved [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3712 (0E80h) DRC1 ctrl1	15:11	DRC1_SIG_DET_RMS [4:0]	00h	DRC1 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DRC1_SIG_DET_MODE=1. 00h = -30dB 01h = -31.5dB …. (1.5dB steps) 1Eh = -75dB 1Fh = -76.5dB
	10:9	DRC1_SIG_DET_PK [1:0]	00	DRC1 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DRC1_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	8	DRC1_NG_ENA	0	DRC1 Noise Gate Enable 0 = Disabled 1 = Enabled
	7	DRC1_SIG_DET_MODE	0	DRC1 Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DRC1_SIG_DET	0	DRC1 Signal Detect Enable 0 = Disabled 1 = Enabled
	5	DRC1_KNEE2_OP_ENA	0	DRC1 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DRC1_QR	1	DRC1 Quick-release Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	DRC1_ANTICLIP	1	DRC1 Anti-clip Enable 0 = Disabled 1 = Enabled
	2	DRC1_WSEQ_SIG_DET_ENA	0	DRC1 Signal Detect Write Sequencer Select 0 = Disabled 1 = Enabled
R3713 (0E81h) DRC1 ctrl2	12:9	DRC1_ATK [3:0]	0100	DRC1 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100 to 1111 = Reserved
	8:5	DRC1_DCY [3:0]	1001	DRC1 Gain decay rate (seconds/6dB) 0000 = 1.45ms 0001 = 2.9ms 0010 = 5.8ms 0011 = 11.6ms 0100 = 23.25ms 0101 = 46.5ms 0110 = 93ms 0111 = 186ms 1000 = 372ms 1001 = 743ms 1010 = 1.49s 1011 = 2.97s 1100 to1111 = Reserved
	4:2	DRC1_MINGAIN [2:0]	100	DRC1 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved
	1:0	DRC1_MAXGAIN [1:0]	11	DRC1 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3714 (0E82h) DRC1 ctrl3	15:12	DRC1_NG_MIN GAIN [3:0]	0000	DRC1 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DRC1_NG_EXP [1:0]	00	DRC1 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DRC1_QR_THR [1:0]	00	DRC1 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	DRC1_QR_DCY [1:0]	00	DRC1 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DRC1_HI_COM P [2:0]	011	DRC1 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	DRC1_LO_COM P [2:0]	000	DRC1 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3715 (0E83h) DRC1 ctrl4	10:5	DRC1_KNEE_IP [5:0]	000000	DRC1 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DRC1_KNEE_OP [4:0]	00000	DRC1 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R3716 (0E84h) DRC1 ctrl5	9:5	DRC1_KNEE2_IP [4:0]	00000	DRC1 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC1_NG_ENA = 1.
	4:0	DRC1_KNEE2_OP [4:0]	00000	DRC1 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC1_KNEE2_OP_ENA = 1.

Table 13 DRC1 Control Registers

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DRC and digital mixing functions. If an attempt is made to enable a DRC signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

LOW PASS / HIGH PASS DIGITAL FILTER (LHPF)

The digital core provides four Low Pass Filter (LPF) / High Pass Filter (HPF) processing blocks as illustrated in Figure 28. A 4-input mixer is associated with each filter. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Each Low/High Pass Filter (LHPF) block supports 1 output.

The Low Pass Filter / High Pass Filter can be used to remove unwanted out-of-band noise from a signal path. Each filter can be configured either as a Low Pass filter or High Pass filter.

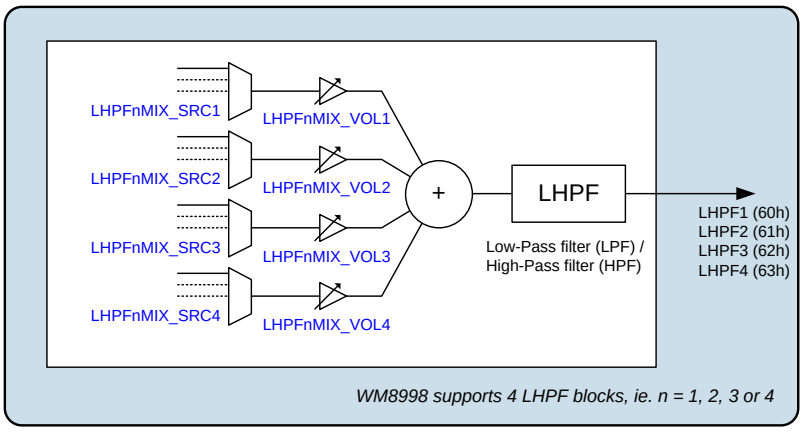


Figure 28 Digital Core LPF/HPF Blocks

The LHPF1, LHPF2, LHPF3 and LHPF4 mixer control registers (see Figure 28) are located at register addresses R2304 (900h) through to R2335 (91Fh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective LHPF processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the LHPF to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The bracketed numbers in Figure 28, eg. “(60h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the LHPF function is configured using the FX_RATE register - see Table 19. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the LHPF signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The control registers associated with the LHPF functions are described in Table 14.

The cut-off frequencies for the LHPF blocks are set using the coefficients held in registers R3777, R3781, R3785 and R3789 for LHPF1, LHPF2, LHPF3 and LHPF4 respectively. These coefficients are derived using tools provided in Cirrus’s WISCE™ evaluation board control software; please contact your local Cirrus representative for more details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	000h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = Reserved [6] = Reserved [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3776 (0EC0h) HPLPF1_1	1	LHPF1_MODE	0	Low/High Pass Filter 1 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF1_ENA	0	Low/High Pass Filter 1 Enable 0 = Disabled 1 = Enabled
R3777 (0EC1h) HPLPF1_2	15:0	LHPF1_COEFF [15:0]	0000h	Low/High Pass Filter 1 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3780 (0EC4h) HPLPF2_1	1	LHPF2_MODE	0	Low/High Pass Filter 2 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF2_ENA	0	Low/High Pass Filter 2 Enable 0 = Disabled 1 = Enabled
R3781 (0EC5h) HPLPF2_2	15:0	LHPF2_COEFF [15:0]	0000h	Low/High Pass Filter 2 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3784 (0EC8h) HPLPF3_1	1	LHPF3_MODE	0	Low/High Pass Filter 3 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF3_ENA	0	Low/High Pass Filter 3 Enable 0 = Disabled 1 = Enabled
R3785 (0EC9h) HPLPF3_2	15:0	LHPF3_COEFF [15:0]	0000h	Low/High Pass Filter 3 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3788 (0ECCh) HPLPF4_1	1	LHPF4_MODE	0	Low/High Pass Filter 4 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF4_ENA	0	Low/High Pass Filter 4 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3789 (0ECDh) HPLPF4_2	15:0	LHPF4_COEFF [15:0]	0000h	Low/High Pass Filter 4 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.

Table 14 Low Pass Filter / High Pass Filter Control

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded LHPF and digital mixing functions. If an attempt is made to enable an LHPF signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

SPDIF OUTPUT GENERATOR

The WM8998 incorporates an IEC-60958-3 compatible S/PDIF output generator, as illustrated in Figure 29; this provides a stereo S/PDIF output on a GPIO pin. The S/PDIF transmitter allows full control over the S/PDIF validity bits and channel status information.

The input sources to the S/PDIF transmitter are selectable for each channel, and independent volume control is provided for each path. The *TX1 and *TX2 registers control channels 'A' and 'B' (respectively) of the S/PDIF output.

The S/PDIF signal can be output directly on a GPIO pin. See "General Purpose Input / Output" to configure a GPIO pin for this function.

Note that the S/PDIF signal cannot be selected as input to the digital mixers or signal processing functions within the WM8998 digital core.

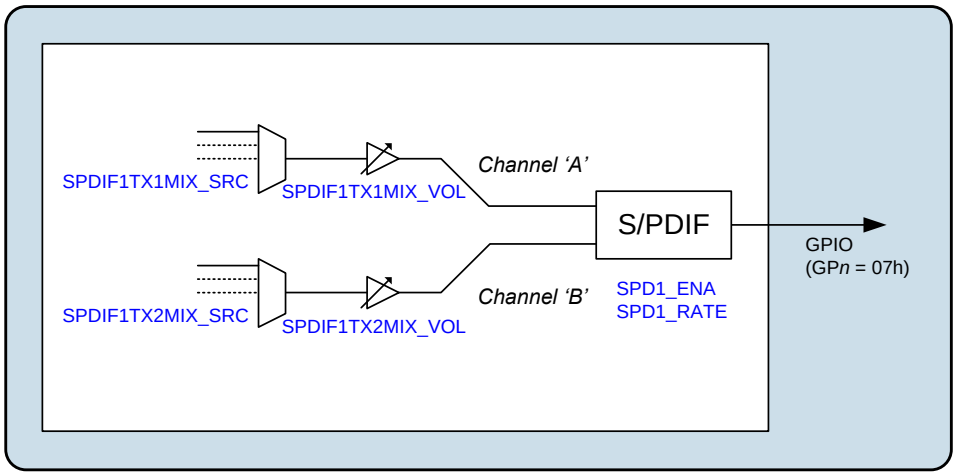


Figure 29 Digital Core S/PDIF Output Generator

The S/PDIF input control registers (see Figure 29) are located at register addresses R2048 (800h) through to R2057 (809h).

The full list of digital mixer control registers is provided in the "Register Map" section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the two S/PDIF channels. Note that the selected input source(s) must be synchronised to the SYSCLK clocking domain, and configured for the same sample rate as the S/PDIF generator. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The sample rate of the S/PDIF generator is configured using the SPD1_RATE register - see Table 19. The S/PDIF transmitter supports sample rates in the range 32kHz up to 192kHz. Note that sample rate conversion is required when linking the S/PDIF generator to any signal chain that is asynchronous and/or configured for a different sample rate.

The S/PDIF generator is enabled using the SPD1_ENA register bit, as described in Table 15.

The S/PDIF output contains audio data derived from the selected sources. Audio samples up to 24-bit width can be accommodated. The Validity bits and the Channel Status bits in the S/PDIF data are configured using the corresponding fields in registers R1474 (5C2h) to R1477 (5C5h).

Refer to S/PDIF specification (IEC 60958-3) for full details of the S/PDIF protocol and configuration parameters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1474 (05C2h) SPD1 TX Control	13	SPD1_VAL2	0	S/PDIF validity (Subframe B)
	12	SPD1_VAL1	0	S/PDIF validity (Subframe A)
	0	SPD1_ENA	0	S/PDIF Generator Enable 0 = Disabled 1 = Enabled
R1475 (05C3h) SPD1 TX Channel Status 1	15:8	SPD1_CATCODE [7:0]	00h	S/PDIF Category code
	7:6	SPD1_CHSTMODE [1:0]	00	S/PDIF Channel Status mode
	5:3	SPD1_PREEMPH [2:0]	000	S/PDIF De-emphasis mode
	2	SPD1_NOCOPY	0	S/PDIF Copyright status
	1	SPD1_NOAUDIO	0	S/PDIF Audio / Non-audio indication
	0	SPD1_PRO	0	S/PDIF Consumer / Professional Mode
R1476 (05C4h) SPD1 TX Channel Status 2	15:12	SPD1_FREQ [3:0]	0000	S/PDIF Indicated sample frequency
	11:8	SPD1_CHNUM2 [3:0]	1011	S/PDIF Channel number (Subframe B)
	7:4	SPD1_CHNUM1 [3:0]	0000	S/PDIF Channel number (Subframe A)
	3:0	SPD1_SRCNUM [3:0]	0001	S/PDIF Source number
R1477 (05C5h) SPD1 TX Channel Status 3	11:8	SPD1_ORGSAMP [3:0]	0000	S/PDIF Original sample frequency
	7:5	SPD1_TXWL [2:0]	000	S/PDIF Audio sample word length
	4	SPD1_MAXWL	0	S/PDIF Maximum audio sample word length
	3:2	SPD1_SC31_30 [1:0]	00	S/PDIF Channel Status [31:30]
	1:0	SPD1_CLKACU [1:0]	00	Transmitted clock accuracy

Table 15 S/PDIF Output Generator Control

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable the SPDIF generator, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Overclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

TONE GENERATOR

The WM8998 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

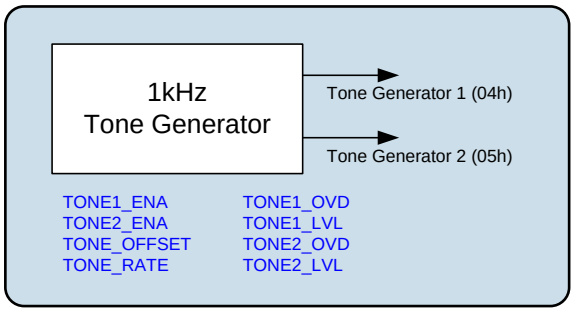


Figure 30 Digital Core Tone Generator

The tone generators can be selected as input to any of the digital mixers or signal processing functions within the WM8998 digital core. The bracketed numbers in Figure 30, eg. "(04h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the tone generators is configured using the TONE_RATE register - see Table 19. Note that sample rate conversion is required when routing the tone generator output(s) to any signal chain that is asynchronous and/or configured for a different sample rate.

The tone generators are enabled using the TONE1_ENA and TONE2_ENA register bits as described in Table 16. The phase relationship is configured using TONE_OFFSET.

The tone generators can also provide a configurable DC signal level, for use as a test signal. The DC output is selected using the TONEn_OVD register bits, and the DC signal amplitude is configured using the TONEn_LVL registers, as described in Table 16.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone Generator 1	9:8	TONE_OFFSET [1:0]	00	Tone Generator Phase Offset Sets the phase of Tone Generator 2 relative to Tone Generator 1 00 = 0 degrees (in phase) 01 = 90 degrees ahead 10 = 180 degrees ahead 11 = 270 degrees ahead
	5	TONE2_OVD	0	Tone Generator 2 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE2_LVL[23:0]
	4	TONE1_OVD	0	Tone Generator 1 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE1_LVL[23:0]
	1	TONE2_ENA	0	Tone Generator 2 Enable 0 = Disabled 1 = Enabled
	0	TONE1_ENA	0	Tone Generator 1 Enable 0 = Disabled 1 = Enabled
R33 (0021h) Tone Generator 2	15:0	TONE1_LVL [23:8]	1000h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R34 (0022h) Tone Generator 3	7:0	TONE1_LVL [7:0]	00h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R35 (0023h) Tone Generator 4	15:0	TONE2_LVL [23:8]	1000h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R36 (0024h) Tone Generator 5	7:0	TONE2_LVL [7:0]	00h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).

Table 16 Tone Generator Control

HAPTIC SIGNAL GENERATOR

The WM8998 incorporates a signal generator for use with haptic devices (eg. mechanical vibration actuators). The haptic signal generator is compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices.

The haptic signal generator is highly configurable, and includes the capability to execute a programmable event profile comprising three distinct operating phases.

The resonant frequency of the haptic signal output (for LRA devices) is selectable, providing support for many different actuator components.

The haptic signal generator is a digital signal generator which is incorporated within the digital core of the WM8998. The haptic signal may be routed, via one of the digital core output mixers, to a Class D speaker output for connection to the external haptic device, as illustrated in Figure 31. (Note that the digital PDM output paths may also be used for haptic signal output.)

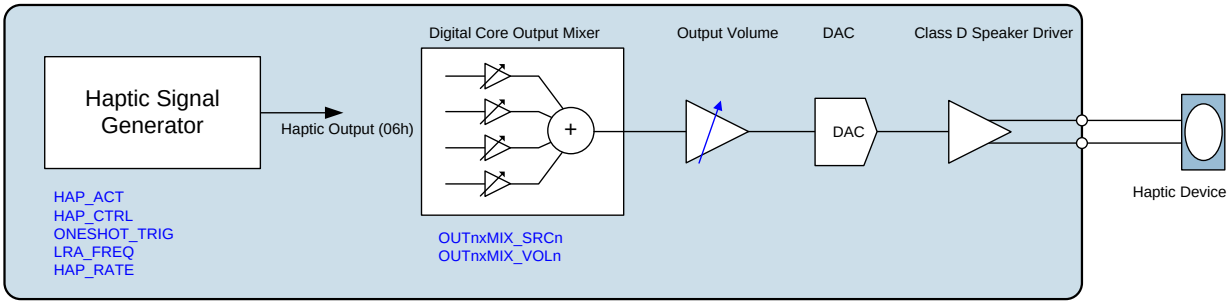


Figure 31 Digital Core Haptic Signal Generator

The bracketed number (06h) in Figure 31 indicates the corresponding *_SRC*n* register setting for selection of the haptic signal generator as an input to another digital core function.

The haptic signal generator is selected as input to one of the digital core output mixers by setting the *_SRC*n* register of the applicable output mixer to (06h).

The sample rate for the haptic signal generator is configured using the HAP_RATE register - see Table 19. Note that sample rate conversion is required when routing the haptic signal generator output to any signal chain that is asynchronous and/or configured for a different sample rate.

The haptic signal generator is configured for an ERM or LRA actuator using the HAP_ACT register bit. The required resonant frequency is configured using the LRA_FREQ field. (Note that the resonant frequency is only applicable to LRA actuators.)

The signal generator can be enabled in Continuous mode or configured for One-Shot mode using the HAP_CTRL register, as described in Table 17. In One-Shot mode, the output is triggered by writing to the ONESHOT_TRIG bit.

In One-Shot mode, the signal generator profile comprises the distinct phases (1, 2, 3). The duration and intensity of each output phase is programmable.

In Continuous mode, the signal intensity is controlled using the PHASE2_INTENSITY field only.

In the case of an ERM actuator (HAP_ACT = 0), the haptic output is a DC signal level, which may be positive or negative, as selected by the *_INTENSITY registers.

For an LRA actuator (HAP_ACT = 1), the haptic output is an AC signal; selecting a negative signal level corresponds to a 180 degree phase inversion. In some applications, phase inversion may be desirable during the final phase, to halt the physical motion of the haptic device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R144 (0090h) Haptics Control 1	4	ONESHOT_TRIG	0	Haptic One-Shot Trigger Writing '1' starts the one-shot profile (ie. Phase 1, Phase 2, Phase 3)
	3:2	HAP_CTRL [1:0]	00	Haptic Signal Generator Control 00 = Disabled 01 = Continuous 10 = One-Shot 11 = Reserved
	1	HAP_ACT	0	Haptic Actuator Select 0 = Eccentric Rotating Mass (ERM) 1 = Linear Resonant Actuator (LRA)
R145 (0091h) Haptics Control 2	14:0	LRA_FREQ [14:0]	7FFFh	Haptic Resonant Frequency Selects the haptic signal frequency (LRA actuator only, HAP_ACT = 1) Haptic Frequency (Hz) = System Clock / (2 x (LRA_FREQ+1)) where System Clock = 6.144MHz or 5.6448MHz, derived by division from SYSCLK or ASYNCCLK. If HAP_RATE<1000, then SYSCLK is the clock source, and the applicable System Clock frequency is determined by SYSCLK. If HAP_RATE>=1000, then ASYNCCLK is the clock source, and the applicable System Clock frequency is determined by ASYNCCLK. Valid for Haptic Frequency in the range 100Hz to 250Hz For 6.144MHz System Clock: 77FFh = 100Hz 4491h = 175Hz 2FFFh = 250Hz For 5.6448MHz System Clock: 6E3Fh = 100Hz 3EFFh = 175Hz 2C18h = 250Hz
R146 (0092h) Haptics phase 1 intensity	7:0	PHASE1_INTENSITY [7:0]	00h	Haptic Output Level (Phase 1) Selects the signal intensity of Phase 1 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R147 (0093h) Haptics Control phase 1 duration	8:0	PHASE1_DURATION [8:0]	000h	Haptic Output Duration (Phase 1) Selects the duration of Phase 1 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R148 (0094h) Haptics phase 2 intensity	7:0	PHASE2_INTENSITY [7:0]	00h	Haptic Output Level (Phase 2) Selects the signal intensity in Continuous mode or Phase 2 of one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R149 (0095h) Haptics phase 2 duration	10:0	PHASE2_DURATION [10:0]	000h	Haptic Output Duration (Phase 2) Selects the duration of Phase 2 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 7FFh = 1279.375ms
R150 (0096h) Haptics phase 3 intensity	7:0	PHASE3_INTENSITY [7:0]	00h	Haptic Output Level (Phase 3) Selects the signal intensity of Phase 3 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R151 (0097h) Haptics phase 3 duration	8:0	PHASE3_DURATION [8:0]	000h	Haptic Output Duration (Phase 3) Selects the duration of Phase 3 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R152 (0098h) Haptics Status	0	ONESHOT_STS	0	Haptic One-Shot status 0 = One-Shot event not in progress 1 = One-Shot event in progress

Table 17 Haptic Signal Generator Control

PWM GENERATOR

The WM8998 incorporates two Pulse Width Modulation (PWM) signal generators as illustrated in Figure 32. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

A 4-input mixer is associated with each PWM generator. The 4 input sources are selectable in each case, and independent volume control is provided for each path.

The PWM signal generators can be output directly on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

Note that the PWM output should always be disabled whenever the system clock, SYSCLK, is disabled. Failure to do this may result in a persistent logic ‘1’ DC output from the PWM generator. See “Clocking and Sample Rates” for details of system clocking and the associated control requirements.

Note that the PWM signal generators cannot be selected as input to the digital mixers or signal processing functions within the WM8998 digital core.

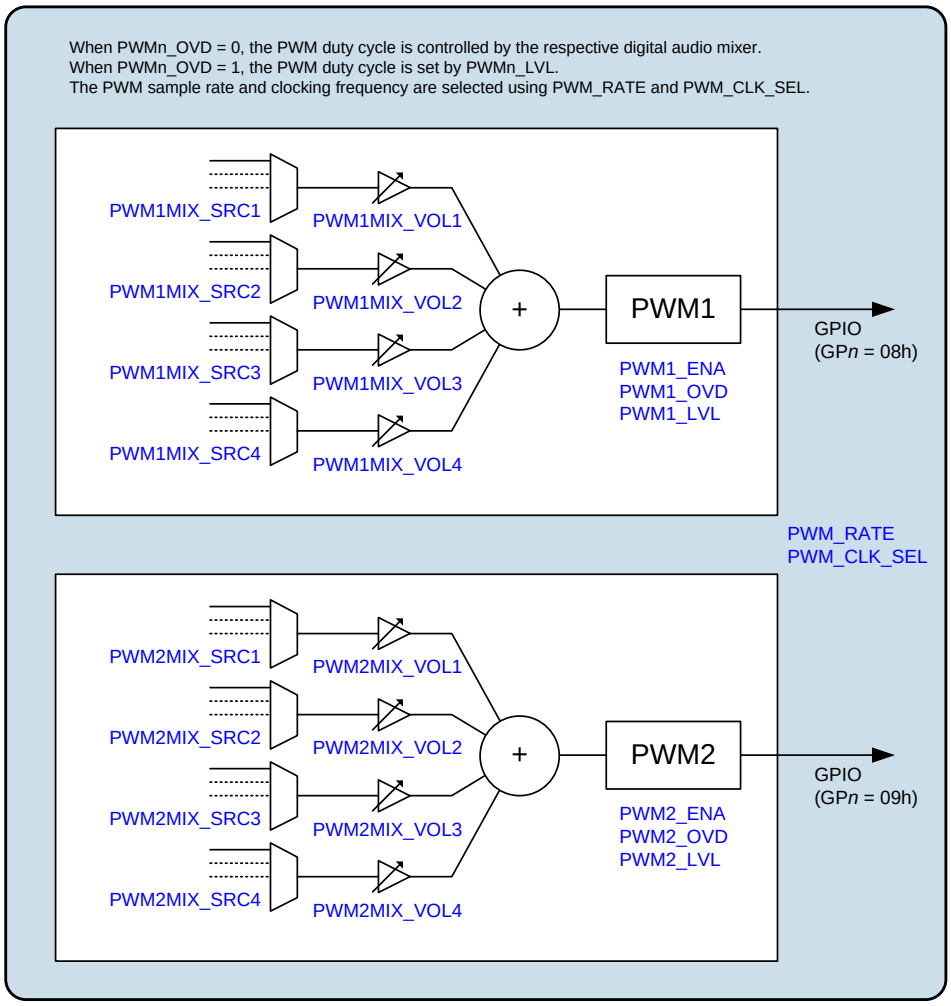


Figure 32 Digital Core Pulse Width Modulation (PWM) Generator

The PWM1 and PWM2 mixer control registers (see Figure 32) are located at register addresses R1600 (640h) through to R1615 (64Fh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective mixers. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see

"Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The PWM sample rate (cycle time) is configured using the PWM_RATE register - see Table 19. Note that sample rate conversion is required when linking the PWM generators to any signal chain that is asynchronous and/or configured for a different sample rate.

The PWM generators are enabled using PWM1_ENA and PWM2_ENA respectively, as described in Table 18.

Under default conditions (PWM*n*_OVD = 0), the duty cycle of the PWM generators is controlled by an audio signal path; a 4-input mixer is associated with each PWM generator, as illustrated in Figure 32.

When the PWM*n*_OVD bit is set, the duty cycle of the respective PWM generator is set to a fixed ratio; in this case, the duty cycle ratio is configurable using the PWM*n*_LVL registers.

The PWM generator clock frequency is selected using PWM_CLK_SEL. For best performance, this register should be set to the highest available setting. Note that the PWM generator clock must not be set to a higher frequency than SYSCLK (if PWM_RATE<1000) or ASYNCCLK (if PWM_RATE≥1000).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) PWM Drive 1	10:8	PWM_CLK_SEL [2:0]	000	PWM Clock Select 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only. PWM_CLK_SEL controls the resolution of the PWM generator; higher settings correspond to higher resolution. The PWM Clock must be less than or equal to SYSCLK (if PWM_RATE<1000) or less than or equal to ASYNCCLK (if PWM_RATE>=1000).
	5	PWM2_OVD	0	PWM2 Generator Override 0 = Disabled (PWM duty cycle is controlled by audio source) 1 = Enabled (PWM duty cycle is controlled by PWM2_LVL).
	4	PWM1_OVD	0	PWM1 Generator Override 0 = Disabled (PWM1 duty cycle is controlled by audio source) 1 = Enabled (PWM1 duty cycle is controlled by PWM1_LVL).
	1	PWM2_ENA	0	PWM2 Generator Enable 0 = Disabled 1 = Enabled
	0	PWM1_ENA	0	PWM1 Generator Enable 0 = Disabled 1 = Enabled
R49 (0031h) PWM Drive 2	9:0	PWM1_LVL [9:0]	100h	PWM1 Override Level Sets the PWM1 duty cycle when PWM1_OVD=1. Coded as 2's complement. 000h = 50% duty cycle 200h = 0% duty cycle
R50 (0032h) PWM Drive 3	9:0	PWM2_LVL [9:0]	100h	PWM2 Override Level Sets the PWM2 duty cycle when PWM2_OVD=1. Coded as 2's complement. 000h = 50% duty cycle 200h = 0% duty cycle

Table 18 Pulse Width Modulation (PWM) Generator Control

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable a PWM signal mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

SAMPLE RATE CONTROL

The WM8998 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between interfaces operating at different sample rates and/or referenced to asynchronous clock domains.

Two independent clock domains are supported, referenced to SYSCLK and ASYNCCLK respectively, as described in "Clocking and Sample Rates". Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

Up to five different sample rates may be in use at any time on the WM8998. Three of these sample rates must be synchronised to SYSCLK; the remaining two, where required, must be synchronised to ASYNCCLK.

Sample rate conversion is required when routing any audio path between digital functions that are asynchronous and/or configured for different sample rates.

The Asynchronous Sample Rate Converter (ASRC) provides two signal paths between the SYSCLK and ASYNCCLK domains. The ASRC is described later, and is illustrated in Figure 35.

There are two Isochronous Sample Rate Converters (ISRCs). These provide signal paths between different sample rates on the SYSCLK domain, or between sample rates on the ASYNCCLK domain. ISRC1 supports up to 4 signal paths; ISRC2 supports up to 2 signal paths. The ISRCs are described later, and are illustrated in Figure 36.

The sample rate of different blocks within the WM8998 digital core are controlled as illustrated in Figure 33 and Figure 34 - the *_RATE registers select the applicable sample rate for each respective group of digital functions.

The *_RATE registers should not be changed if any of the *_SRC*n* registers associated with the respective functions is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to the *_RATE registers. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated *_RATE registers. See Table 19 for further details.

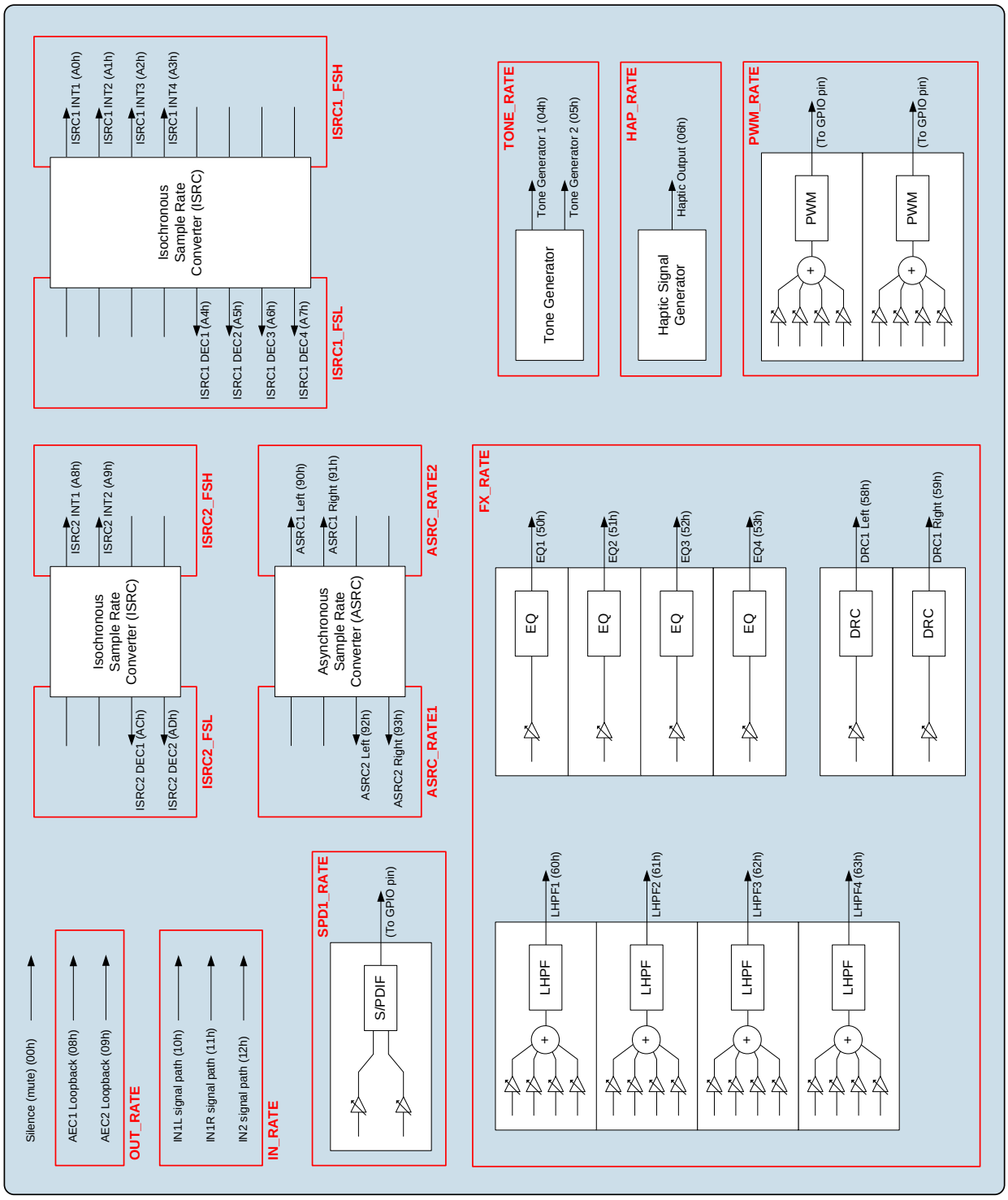


Figure 33 Digital Core Sample Rate Control (Internal Signal Processing)

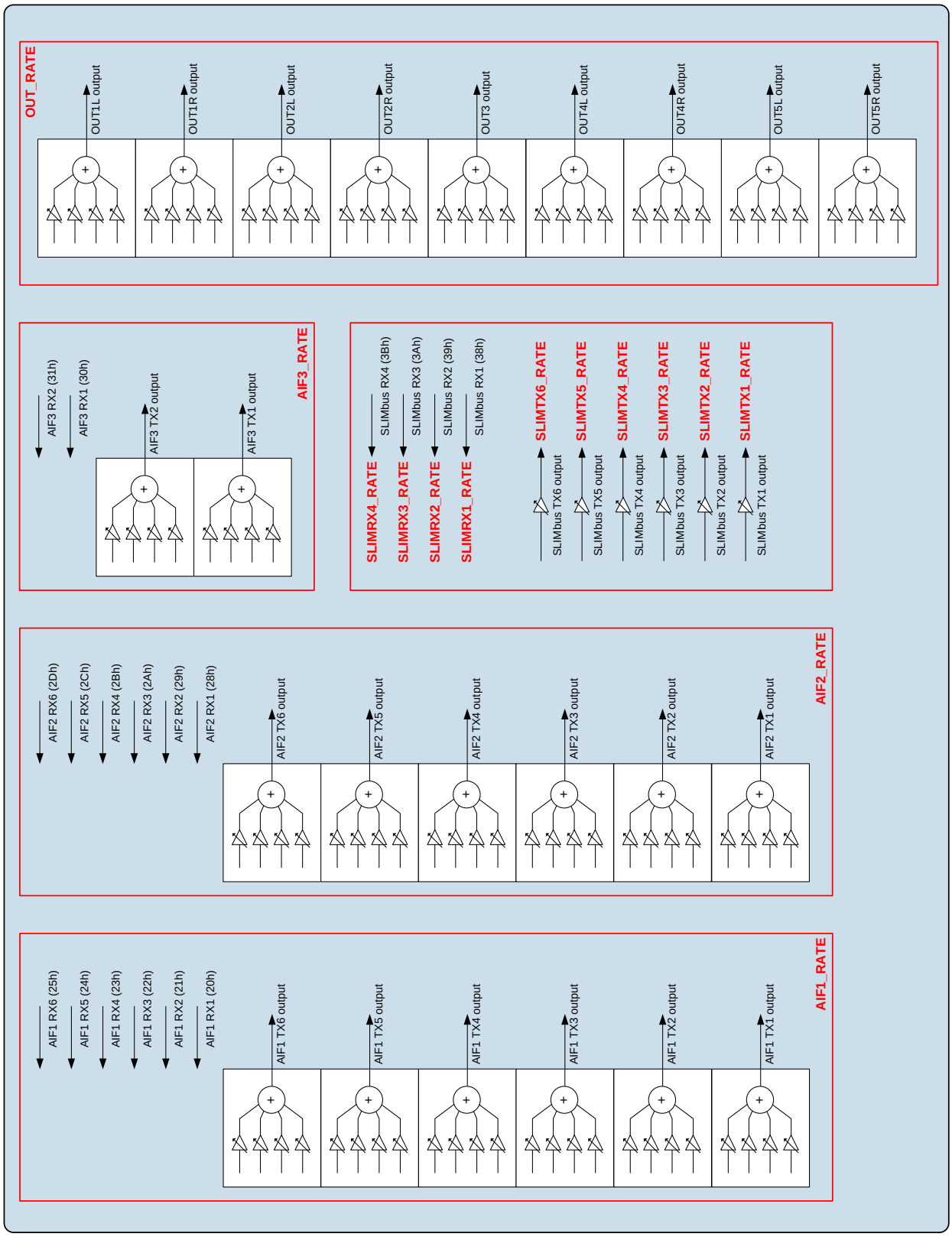


Figure 34 Digital Core Sample Rate Control (External Digital Interfaces)

The input signal paths may be selected as input to the digital mixers or signal processing functions. The sample rate for the input signal paths is configured using the IN_RATE register.

The output signal paths are derived from the respective output mixers. The sample rate for the output signal paths is configured using the OUT_RATE register. The sample rate of the AEC Loopback path is also set by the OUT_RATE register.

The AIFn RX inputs may be selected as input to the digital mixers or signal processing functions. The AIFn TX outputs are derived from the respective output mixers. The sample rates for digital audio interfaces (AIF1, AIF2 and AIF3) are configured using the AIF1_RATE, AIF2_RATE and AIF3_RATE registers respectively.

The SLIMbus interface supports up to 4 input channels and 6 output channels. The sample rate of each channel can be configured independently, using the SLIMTXn_RATE and SLIMRXn_RATE registers.

Note that the SLIMbus interface provides simultaneous support for SYSCLK-referenced and ASYNCCLK-referenced sample rates on different channels. For example, 48kHz and 44.1kHz SLIMbus audio paths can be simultaneously supported.

The EQ, LHPF and DRC functions can be enabled in any signal path within the digital core. The sample rate for these functions is configured using the FX_RATE register. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate.

The S/PDIF transmitter can be enabled on a GPIO pin. Stereo inputs to this function can be configured from any of the digital core inputs, mixers, or signal processing functions. The sample rate of the S/PDIF transmitter is configured using the SPD1_RATE register.

The tone generators can be selected as input to any of the digital mixers or signal processing functions. The associated sample rate is configured using the TONE_RATE register.

The haptic signal generator can be used to control an external vibe actuator, which can be driven directly by the Class D speaker output. The sample rate for the haptic signal generator is configured using the HAP_RATE register.

The PWM signal generators can be modulated by an audio source, derived from the associated signal mixers. The sample rate (cycle time) for the PWM signal generators is configured using the PWM_RATE register.

The sample rate control registers are described in Table 19. Refer to the register descriptions for details of the valid selections in each case. Note that the input (ADC) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain; different sample rates may be selected concurrently, but both these rates must be synchronised to SYSCLK.

The control registers associated with the ASRC and ISRCs are described in Table 20 and Table 21 respectively within the following sections.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone Generator 1	14:11	TONE_RATE [3:0]	0000	Tone Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R48 (0030h) PWM Drive 1	14:11	PWM_RATE [3:0]	0000	PWM Frequency (sample rate) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All PWM*n*MIX_SRC*m* registers should be set to 00h before changing PWM_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R144 0090h) Haptics Control 1	14:11	HAP_RATE [3:0]	0000	Haptic Signal Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R776 (0308h) Input Rate	14:11	IN_RATE [3:0]	0000	Input Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1032 (0408h) Output Rate 1	14:11	OUT_RATE [3:0]	0000	Output Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All OUT*n*xMIX_SRC*m* registers should be set to 00h before changing OUT_RATE.
R1283 (0503h) AIF1 Rate Ctrl	14:11	AIF1_RATE [3:0]	0000	AIF1 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF1TXMIX_SRC*n* registers should be set to 00h before changing AIF1_RATE.
R1347 (0543h) AIF2 Rate Ctrl	14:11	AIF2_RATE [3:0]	0000	AIF2 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF2TXMIX_SRC*n* registers should be set to 00h before changing AIF2_RATE.
R1411 (0583h) AIF3 Rate Ctrl	14:11	AIF3_RATE [3:0]	0000	AIF3 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF3TXMIX_SRC*n* registers should be set to 00h before changing AIF3_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1474 (05C2h) SPD1 TX Control	7:4	SPD1_RATE [3:0]	0000	S/PDIF Transmitter Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 32kHz to 192kHz. The SPDIF1TX1_SRC and SPDIF1TX2_SRC registers should be set to 00h before changing SPD1_RATE.
R1509 (05E5h) SLIMbus Rates 1	14:11	SLIMRX2_RATE [3:0]	0000	SLIMbus RX Channel 2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX1_RATE [3:0]	0000	SLIMbus RX Channel 1 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1510 (05E6h) SLIMbus Rates 2	14:11	SLIMRX4_RATE [3:0]	0000	SLIMbus RX Channel 4 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX3_RATE [3:0]	0000	SLIMbus RX Channel 3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1513 (05E9h) SLIMbus Rates 5	14:11	SLIMTX2_RATE [3:0]	0000	SLIMbus TX Channel 2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX2MIX_SRC*n* registers should be set to 00h before changing SLIMTX2_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:3	SLIMTX1_RATE [3:0]	0000	SLIMbus TX Channel 1 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX1MIX_SRC*n* registers should be set to 00h before changing SLIMTX1_RATE.
R1514 (05EAh) SLIMbus Rates 6	14:11	SLIMTX4_RATE [3:0]	0000	SLIMbus TX Channel 4 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX4MIX_SRC*n* registers should be set to 00h before changing SLIMTX4_RATE.
	6:3	SLIMTX3_RATE [3:0]	0000	SLIMbus TX Channel 3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX3MIX_SRC*n* registers should be set to 00h before changing SLIMTX3_RATE.
R1515 (05EBh) SLIMbus Rates 7	14:11	SLIMTX6_RATE [3:0]	0000	SLIMbus TX Channel 6 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX6MIX_SRC*n* registers should be set to 00h before changing SLIMTX6_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:3	SLIMTX5_RATE [3:0]	0000	SLIMbus TX Channel 5 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX5MIX_SRC*n* registers should be set to 00h before changing SLIMTX5_RATE.
R3584 (0E00h) FX_Ctrl	14:11	FX_RATE [3:0]	0000	FX Sample Rate (EQ, LHPF, DRC) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All EQ*n*MIX_SRC*m*, DRC1*x*MIX_SRC*m*, and LHPF*n*MIX_SRC*m* registers should be set to 00h before changing FX_RATE.

Table 19 Digital Core Sample Rate Control

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC)

The WM8998 supports multiple signal paths through the digital core. Two independent clock domains are supported, referenced to SYSCLK and ASYNCCLK respectively, as described in “Clocking and Sample Rates”. Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

The Asynchronous Sample Rate Converter (ASRC) provides two stereo signal paths between the SYSCLK and ASYNCCLK domains, as illustrated in Figure 35.

The sample rate on the SYSCLK domain is selected using the ASRC_RATE1 register - the rate can be set equal to SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

The sample rate on the ASYNCCLK domain is selected using the ASRC_RATE2 register - the rate can be set equal to ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

The ASRC_RATE1 and ASRC_RATE2 registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ASRC_RATE1 or ASRC_RATE2. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated ASRC_RATE1 or ASRC_RATE2 registers. See Table 20 for further details.

The ASRC supports sample rates 11.025kHz, 12kHz, 22.05kHz, 24kHz, 44.1kHz and 48kHz only. The applicable SAMPLE_RATE_n and ASYNC_SAMPLE_RATE_n registers must each select one of these valid sample rates.

The ASRC1 Left and ASRC1 Right paths convert from the SYSCLK domain to the ASYNCCLK domain. These paths are enabled using the ASRC1L_ENA and ASRC1R_ENA register bits respectively.

The ASRC2 Left and ASRC2 Right paths convert from the ASYNCCLK domain to the SYSCLK domain. These paths are enabled using the ASRC2L_ENA and ASRC2R_ENA register bits respectively.

Synchronisation (lock) between different clock domains is not instantaneous when the clocking or sample rate configurations are updated. The lock status of each ASRC path is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The ASRC Lock status of each ASRC path can be output directly on a GPIO pin as an external indication of ASRC Lock. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The WM8998 performs automatic checks to confirm that the SYSCLK or ASYNCCLK frequency is high enough to support the commanded ASRC and digital mixing functions. If an attempt is made to enable an ASRC signal path, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Register R3809 indicate the status of each of the ASRC signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which ASRC signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Asynchronous Sample Rate Converter (ASRC) signal paths and control registers are illustrated in Figure 35.

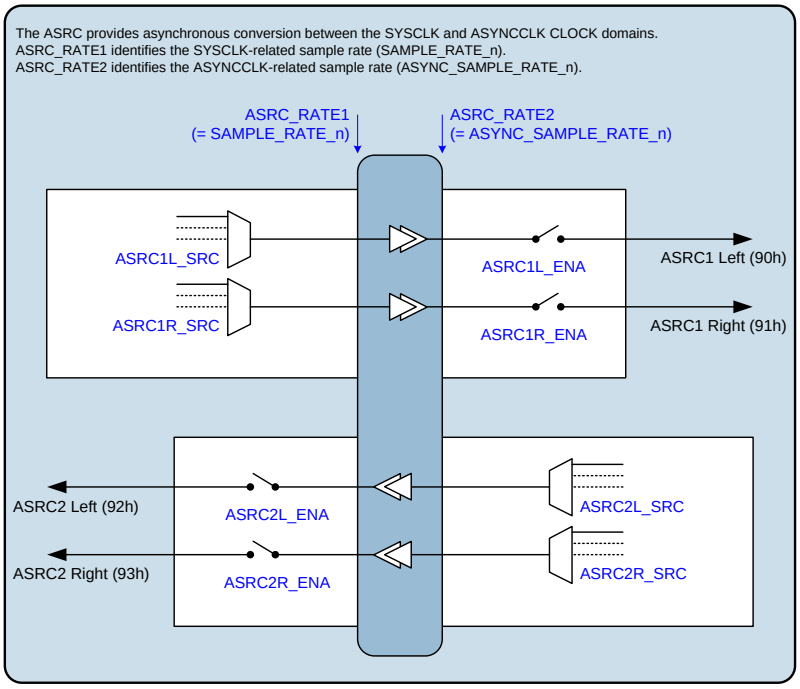


Figure 35 Asynchronous Sample Rate Converters (ASRCs)

The ASRC1 and ASRC2 input control registers (see Figure 35) are located at register addresses R2688 (A80h) through to R2712 (A98h).

The full list of digital mixer control registers is provided in the "Register Map" section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective ASRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ASRC to which they are connected.

The bracketed numbers in Figure 35, eg. "(90h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The register bits associated with the ASRCs are described in Table 20.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3808 (0EE0h) ASRC_ENABLE	3	ASRC2L_ENA	0	ASRC2 Left Enable (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2R_ENA	0	ASRC2 Right Enable (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC1L_ENA	0	ASRC1 Left Enable (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	ASRC1R_ENA	0	ASRC1 Right Enable (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
R3809 (0EE1h) ASRC_STATUS	3	ASRC2L_ENA_STS	0	ASRC2 Left Enable Status (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2R_ENA_STS	0	ASRC2 Right Enable Status (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC1L_ENA_STS	0	ASRC1 Left Enable Status (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC1R_ENA_STS	0	ASRC1 Right Enable Status (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
R3810 (0EE2h) ASRC_RATE1	14:11	ASRC_RATE1 [3:0]	0000	ASRC Sample Rate select for SYSCLK domain 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid for 11.025kHz, 12kHz, 22.05kHz, 24kHz, 44.1kHz and 48kHz only. The ASRC_IN1L_SRC and ASRC_IN1R_SRC registers should be set to 00h before ASRC_RATE1.
R3811 (0EE3h) ASRC_RATE2	14:11	ASRC_RATE2 [3:0]	1000	ASRC Sample Rate select for ASYNCCLK domain 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid for 11.025kHz, 12kHz, 22.05kHz, 24kHz, 44.1kHz and 48kHz only. The ASRC_IN2L_SRC and ASRC_IN2R_SRC registers should be set to 00h before ASRC_RATE2.

Table 20 Digital Core ASRC Control

ISOCHRONOUS SAMPLE RATE CONVERTER (ISRC)

The WM8998 supports multiple signal paths through the digital core. The Isochronous Sample Rate Converters (ISRCs) provide sample rate conversion between synchronised sample rates on the SYSCLK clock domain, or between synchronised sample rates on the ASYNCCLK clock domain.

There are two Isochronous Sample Rate Converters (ISRCs). ISRC1 provides four signal paths between two different sample rates; ISRC2 provides two signal paths between two different sample rates, as illustrated in Figure 36.

The sample rates associated with each ISRC can be set independently. Note that the two sample rates associated with any single ISRC must both be referenced to the same clock domain (SYSCLK or ASYNCCLK).

When an ISRC is used on the SYSCLK domain, then the associated sample rates may be selected from SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

When an ISRC is used on the ASYNCCLK domain, then the associated sample rates are ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

Each ISRC supports sample rates in the range 8kHz to 192kHz. The higher of the sample rates associated with each ISRC must be an integer multiple of the lower sample rate; integer ratios in the range 1 to 6 are supported on ISRC1; integer ratios in the range 1 to 24 are supported on ISRC2.

Each ISRC converts between a sample rate selected by ISRC*n*_FSL and a sample rate selected by ISRC*n*_FSH, (where ‘*n*’ identifies the applicable ISRC 1 or 2). Note that, in each case, the higher of the two sample rates must be selected by ISRCn_FSH.

The ISRC*n*_FSL and ISRC*n*_FSH registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ISRC*n*_FSL or ISRC*n*_FSH. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated ISRC*n*_FSL or ISRC*n*_FSH registers. See Table 21 for further details.

The ISRC*n* ‘interpolation’ paths (increasing sample rate) are enabled using the ISRC*n*_INT*m*_ENA register bits, (where ‘*m*’ identifies the applicable channel).

The ISRC*n* ‘decimation’ paths (decreasing sample rate) are enabled using the ISRC*n*_DEC*m*_ENA register bits.

A notch filter is provided in each of the ISRC paths; these are enabled using the ISRC*n*_NOTCH_ENA bits. The filter is configured automatically according to the applicable sample rate(s). It is recommended to enable the filter for typical applications. Disabling the filter will provide maximum ‘pass’ bandwidth, at the expense of degraded stopband attenuation.

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded ISRC and digital mixing functions. If an attempt is made to enable an ISRC signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R2920 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Isochronous Sample Rate Converter (ISRC) signal paths and control registers are illustrated in Figure 36.

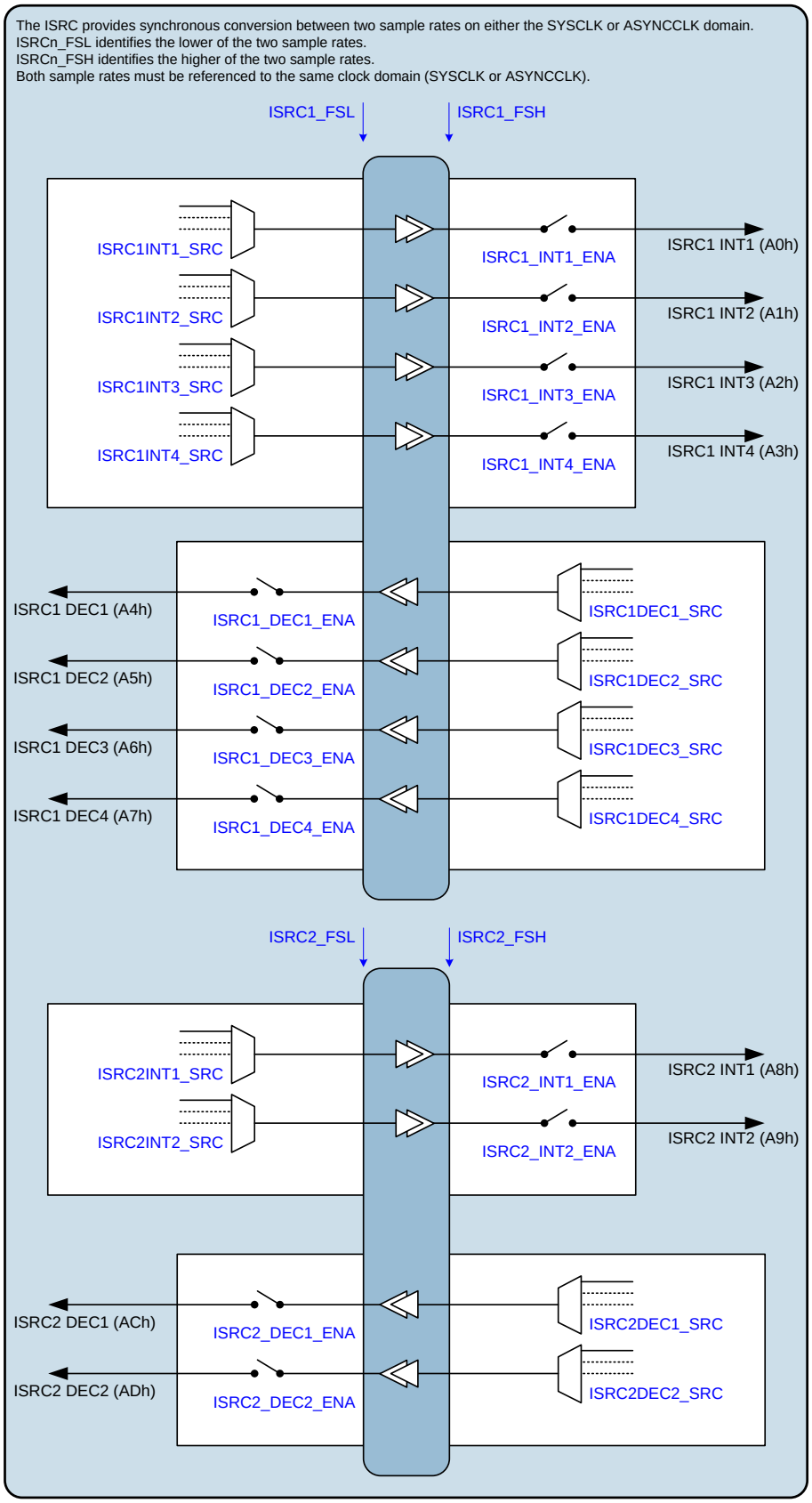


Figure 36 Isochronous Sample Rate Converters (ISRCs)

The ISRC input control registers (see Figure 36) are located at register addresses R2816 (B00h) through to R2920 (0B68h).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R2920). Generic register definitions are provided in Table 7.

The *_SRC registers select the input source(s) for the respective ISRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ISRC to which they are connected.

The bracketed numbers in Figure 36, eg. “(A4h)” indicate the corresponding *_SRC register setting for selection of that signal as an input to another digital core function.

The register bits associated with the ISRCs are described in Table 21.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3824 (0EF0h) ISRC 1 CTRL 1	14:11	ISRC1_FSH [3:0]	0000	ISRC1 High Sample Rate (Sets the higher of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_DEC*n*_SRC registers should be set to 00h before changing ISRC1_FSH.
R3825 (0EF1h) ISRC 1 CTRL 2	14:11	ISRC1_FSL [3:0]	0000	ISRC1 Low Sample Rate (Sets the lower of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_INT*n*_SRC registers should be set to 00h before changing ISRC1_FSL.
R3826 (0EF2h) ISRC 1 CTRL 3	15	ISRC1_INT1_ENA	0	ISRC1 INT1 Enable (Interpolation Channel 1 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC1_INT2_ENA	0	ISRC1 INT2 Enable (Interpolation Channel 2 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	13	ISRC1_INT3_ENA	0	ISRC1 INT3 Enable (Interpolation Channel 3 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC1_INT4_ENA	0	ISRC1 INT4 Enable (Interpolation Channel 4 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC1_DEC1_ENA	0	ISRC1 DEC1 Enable (Decimation Channel 1 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC1_DEC2_ENA	0	ISRC1 DEC2 Enable (Decimation Channel 2 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC1_DEC3_ENA	0	ISRC1 DEC3 Enable (Decimation Channel 3 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC1_DEC4_ENA	0	ISRC1 DEC4 Enable (Decimation Channel 4 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	0	ISRC1_NOTCH_ENA	0	ISRC1 Notch Filter Enable 0 = Disabled 1 = Enabled It is recommended to enable the notch filter for typical applications.
R3827 (0EF3h) ISRC 2 CTRL 1	14:11	ISRC2_FSH [3:0]	0000	ISRC2 High Sample Rate (Sets the higher of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_DEC*n*_SRC registers should be set to 00h before changing ISRC2_FSH.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3828 (0EF4h) ISRC 2 CTRL 2	14:11	ISRC2_FSL [3:0]	0000	ISRC2 Low Sample Rate (Sets the lower of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_INT*n*_SRC registers should be set to 00h before changing ISRC2_FSL.
R3829 (0EF5h) ISRC 2 CTRL 3	15	ISRC2_INT1_ENA	0	ISRC2 INT1 Enable (Interpolation Channel 1 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC2_INT2_ENA	0	ISRC2 INT2 Enable (Interpolation Channel 2 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC2_DEC1_ENA	0	ISRC2 DEC1 Enable (Decimation Channel 1 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC2_DEC2_ENA	0	ISRC2 DEC2 Enable (Decimation Channel 2 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	0	ISRC2_NOTCH_ENA	0	ISRC2 Notch Filter Enable 0 = Disabled 1 = Enabled It is recommended to enable the notch filter for typical applications.

Table 21 Digital Core ISRC Control

DIGITAL AUDIO INTERFACE

The WM8998 provides three audio interfaces, AIF1, AFI2 and AIF3. Each of these is independently configurable on the respective transmit (TX) and receive (RX) paths. AIF1 and AIF2 support up to 6 channels of input and output signal paths each; AIF3 supports up to 2 channels of input and output signal paths.

The data source(s) for the audio interface transmit (TX) paths can be selected from any of the WM8998 input signal paths, or from the digital core processing functions. The audio interface receive (RX) paths can be selected as inputs to any of the digital core processing functions or digital core outputs. See “Digital Core” for details of the digital core routing options.

The digital audio interfaces provide flexible connectivity for multiple processors and other audio devices. Typical connections include Applications Processor, Baseband Processor and Wireless Transceiver. Note that the SLIMbus interface also provides digital audio input/output paths, providing options for additional interfaces. A typical configuration is illustrated in Figure 37.

The audio interfaces AIF1, AIF2 and AIF3 are referenced to DBVDD1, DBVDD2 and DBVDD3 respectively, allowing the WM8998 to connect between application sub-systems on different voltage domains.

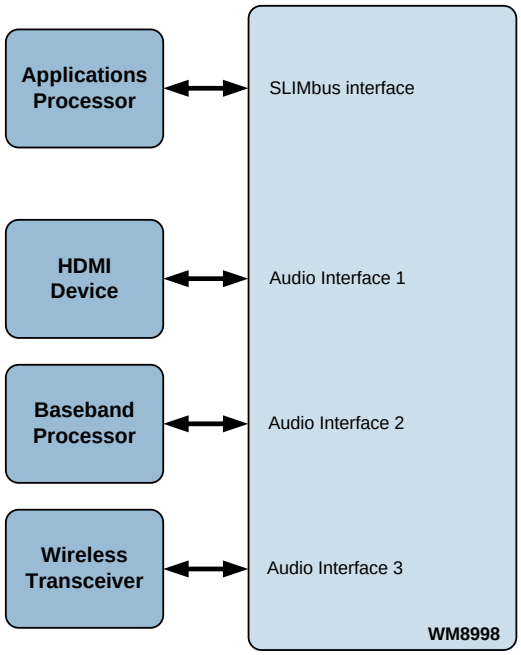


Figure 37 Typical AIF Connections

In the general case, the digital audio interface uses four pins:

- TXDAT: Data output
- RXDAT: Data input
- BCLK: Bit clock, for synchronisation
- LRCLK: Left/Right data alignment clock

In master interface mode, the clock signals BCLK and LRCLK are outputs from the WM8998. In slave mode, these signals are inputs, as illustrated below.

Four different audio data formats are supported by the digital audio interface:

- DSP mode A
- DSP mode B
- I2S
- Left Justified

The Left Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8998). These modes cannot be supported in Slave mode.

All four of these modes are MSB first. Data words are encoded in 2's complement format. Each of the audio interface modes is described in the following sections. Refer to the "Signal Timing Requirements" section for timing information.

Two variants of DSP mode are supported - 'Mode A' and 'Mode B'. Mono PCM operation can be supported using the DSP modes.

MASTER AND SLAVE MODE OPERATION

The WM8998 digital audio interfaces can operate as a master or slave as shown in Figure 38 and Figure 39. The associated control bits are described in "Digital Audio Interface Control".

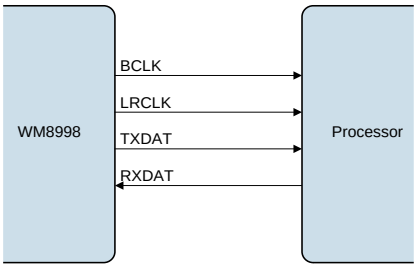


Figure 38 Master Mode

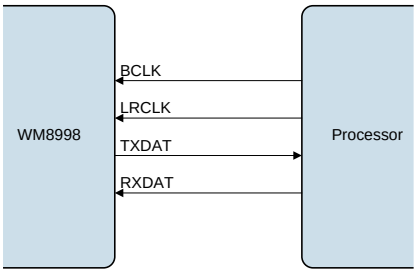


Figure 39 Slave Mode

AUDIO DATA FORMATS

The WM8998 digital audio interfaces can be configured to operate in I^2S, Left-Justified, DSP-A or DSP-B interface modes. Note that Left-Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8998).

The digital audio interfaces also provide flexibility to support multiple 'slots' of audio data within each LRCLK frame. This flexibility allows multiple audio channels to be supported within a single LRCLK frame.

The data formats described in this section are generic descriptions, assuming only one stereo pair of audio samples per LRCLK frame. In these cases, the AIF is configured to transmit (or receive) in the first available position in each frame (ie. the Slot 0 position).

The options for multi-channel operation are described in the following section ("AIF Timeslot Configuration").

The audio data modes supported by the WM8998 are described below. Note that the polarity of the BCLK and LRCLK signals can be inverted if required; the following descriptions all assume the default, non-inverted polarity of these signals.

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In master mode, the LRCLK output will resemble the frame pulse shown in Figure 40 and Figure 41. In slave mode, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

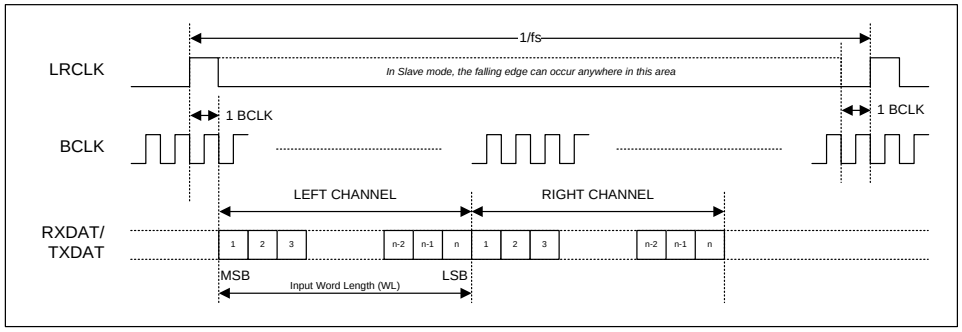


Figure 40 DSP Mode A Data Format

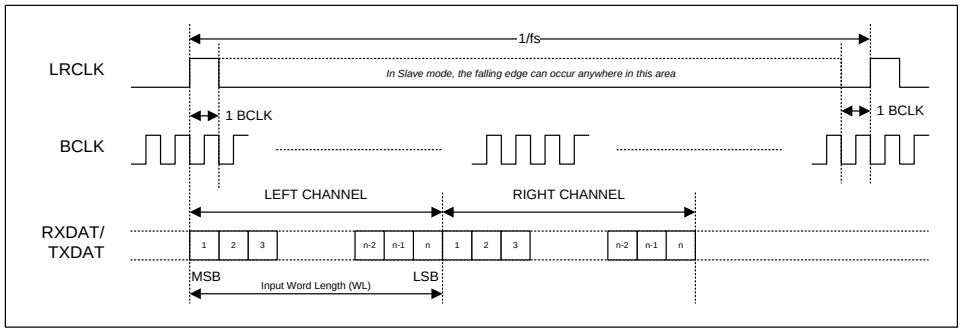


Figure 41 DSP Mode B Data Format

PCM operation is supported in DSP interface mode. WM8998 data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the WM8998 will be treated as Left Channel data. This data may be routed to the Left/Right playback paths using the control fields described in the “Digital Core” section.

In I²S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

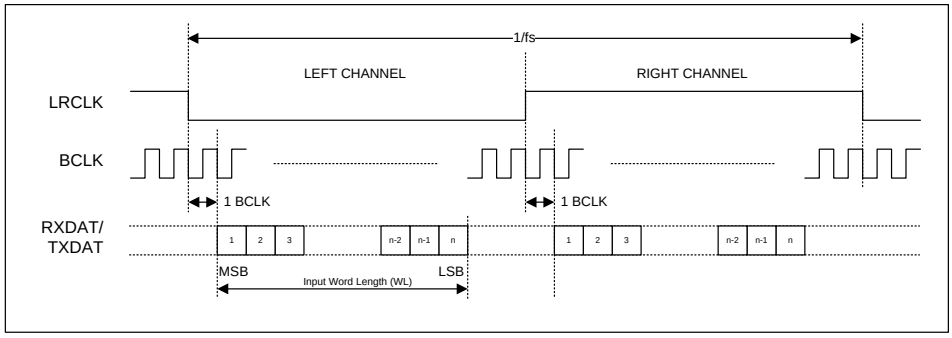


Figure 42 I2S Data Format (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

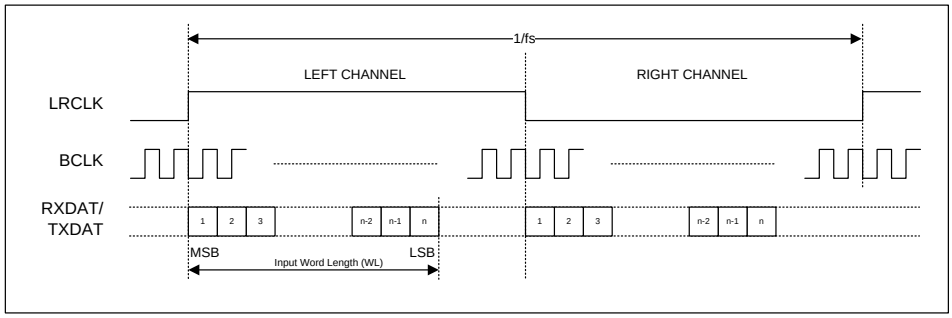


Figure 43 Left Justified Data Format (assuming n-bit word length)

AIF TIMESLOT CONFIGURATION

Digital audio interfaces AIF1 and AIF2 supports multi-channel operation; up to 6 input (RX) channels and 6 output (TX) channels can be supported simultaneously. A high degree of flexibility is provided to define the position of the audio samples within each LRCLK frame; the audio channel samples may be arranged in any order within the frame.

AIF3 also provides flexible configuration options, but supports only 1 stereo input and 1 stereo output pair.

Note that, on each interface, all input and output channels must operate at the same sample rate (fs).

Each of the audio channels can be enabled or disabled independently on the transmit (TX) and receive (RX) signal paths. For each enabled channel, the audio samples are assigned to one timeslot within the LRCLK frame.

In DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

The timeslots are assigned independently for the transmit (TX) and receive (RX) signal paths. There is no requirement to assign every available timeslot to an audio sample; some slots may be unused, if desired. Care is required, however, to ensure that no timeslot is allocated to more than one audio channel.

The number of BCLK cycles within a slot is configurable; this is the Slot Length. The number of valid data bits within a slot is also configurable; this is the Word Length. The number of BCLK cycles per LRCLK frame must be configured; it must be ensured that there are enough BCLK cycles within each LRCLK frame to transmit or receive all of the enabled audio channels.

Examples of the AIF Timeslot Configurations are illustrated in Figure 44 to Figure 47. One example is shown for each of the four possible data formats.

Figure 44 shows an example of DSP Mode A format. Four enabled audio channels are shown, allocated to timeslots 0 through to 3.

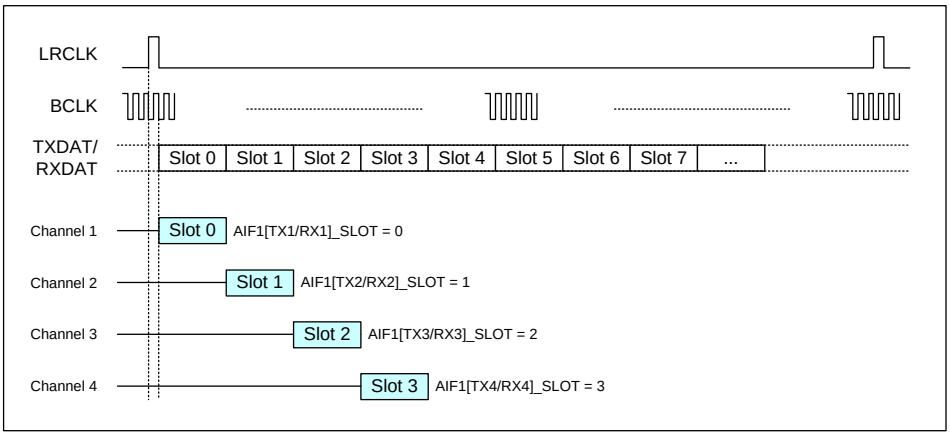


Figure 44 DSP Mode A Example

Figure 45 shows an example of DSP Mode B format. Six enabled audio channels are shown, with timeslots 4 and 5 unused.

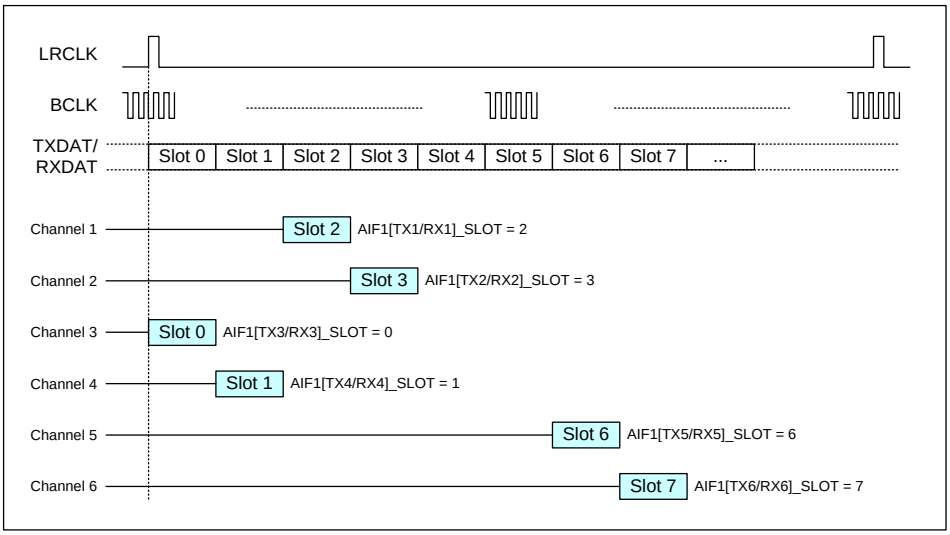


Figure 45 DSP Mode B Example

Figure 46 shows an example of I2S format. Four enabled channels are shown, allocated to timeslots 0 through to 3.

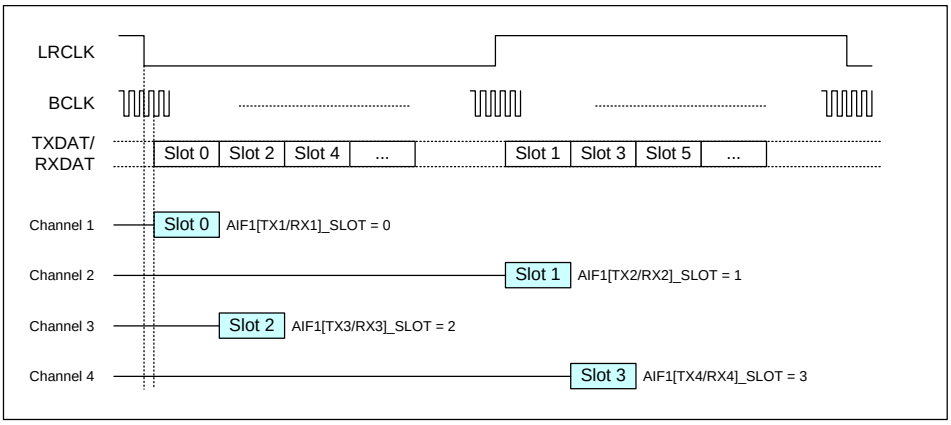


Figure 46 I2S Example

Figure 47 shows an example of Left Justified format. Six enabled channels are shown.

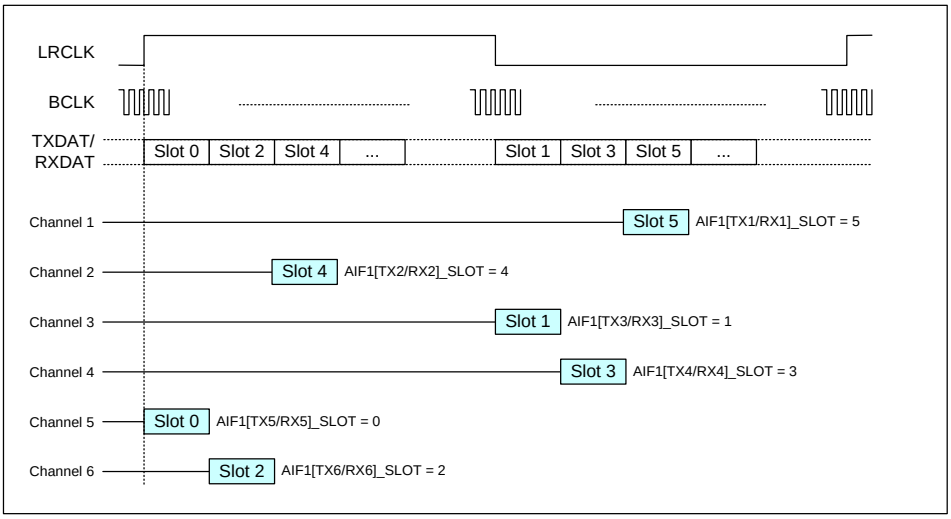


Figure 47 Left Justifed Example

TDM OPERATION BETWEEN THREE OR MORE DEVICES

The AIF operation described above illustrates how multiple audio channels can be interleaved on a single TXDAT or RXDAT pin. The interface uses Time Division Multiplexing (TDM) to allocate time periods to each of the audio channels in turn.

This form of TDM is implemented between two devices, using the electrical connections illustrated in Figure 38 or Figure 39.

It is also possible to implement TDM between three or more devices. This allows one CODEC to receive audio data from two other devices simultaneously on a single audio interface, as illustrated in Figure 48, Figure 49 and Figure 50.

The WM8998 provides full support for TDM operation. The TXDAT pin can be tri-stated when not transmitting data, in order to allow other devices to transmit on the same wire. The behaviour of the TXDAT pin is configurable, to allow maximum flexibility to interface with other devices in this way.

Typical configurations of TDM operation between three devices are illustrated in Figure 48, Figure 49 and Figure 50.

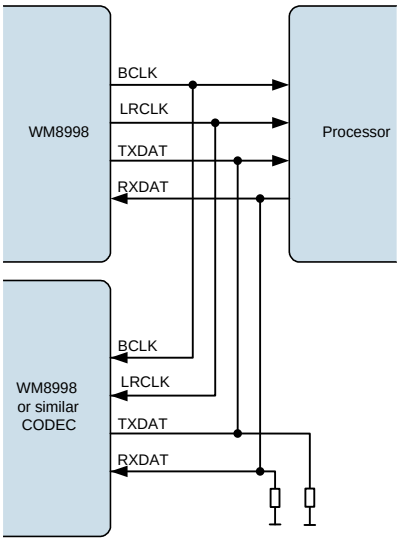


Figure 48 TDM with WM8998 as Master

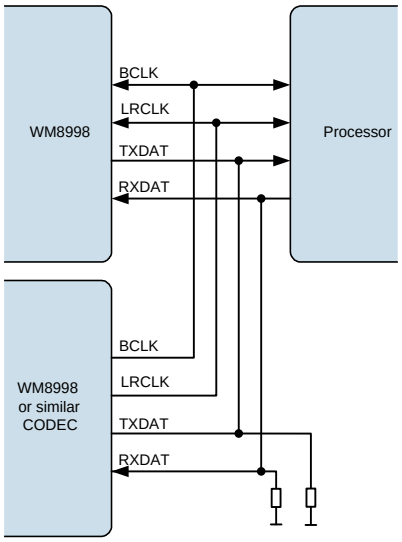


Figure 49 TDM with Other CODEC as Master

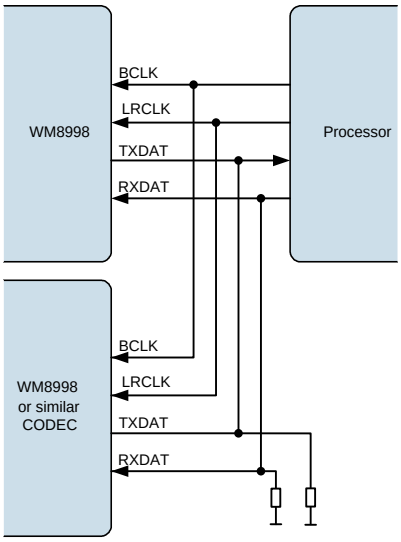


Figure 50 TDM with Processor as Master

Note:

The WM8998 is a 24-bit device. If the user operates the WM8998 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the RXDAT line and the TXDAT line in TDM mode.

DIGITAL AUDIO INTERFACE CONTROL

This section describes the configuration of the WM8998 digital audio interface paths.

AIF1 and AIF2 support up to 6 input signal paths and up to 6 output signal paths each. AIF3 supports up to 2 input and output signal paths. The digital audio interfaces AIF1, AIF2 and AIF3 can be configured as Master or Slave interfaces; mixed master/slave configurations are also possible.

Each input and output signal path can be independently enabled or disabled. The AIF output (TX) and AIF input (RX) paths use shared BCLK and LRCLK control signals.

The digital audio interface supports flexible data formats, selectable word-length, configurable timeslot allocations and TDM tri-state control.

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that any 'on-the-fly' re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

AIF SAMPLE RATE CONTROL

The AIF RX inputs may be selected as input to the digital mixers or signal processing functions within the WM8998 digital core. The AIF TX outputs are derived from the respective output mixers.

The sample rate for each digital audio interface AIFn is configured using the respective AIFn_RATE register - see Table 19 within the "Digital Core" section.

Note that sample rate conversion is required when routing the AIF paths to any signal chain that is asynchronous and/or configured for a different sample rate.

AIF MASTER / SLAVE CONTROL

The digital audio interfaces can operate in Master or Slave modes and also in mixed master/slave configurations. In Master mode, the BCLK and LRCLK signals are generated by the WM8998 when any of the respective digital audio interface channels is enabled. In Slave mode, these outputs are disabled by default to allow another device to drive these pins.

Master mode is selected on the AIFnBCLK pin using the AIFn_BCLK_MSTR register bit. In Master mode, the AIFnBCLK signal is generated by the WM8998 when one or more AIFn channels is enabled.

When the AIFn_BCLK_FRC bit is set in BCLK master mode, the AIFnBCLK signal is output at all times, including when none of the AIFn channels is enabled.

The AIFnBCLK signal can be inverted in Master or Slave modes using the AIFn_BCLK_INV register.

Master mode is selected on the AIFnLRCLK pin using the AIFn_LRCLK_MSTR register bit. In Master mode, the AIFnLRCLK signal is generated by the WM8998 when one or more AIFn channels is enabled.

When the AIFn_LRCLK_FRC bit is set in LRCLK master mode, the AIFnLRCLK signal is output at all times, including when none of the AIFn channels is enabled. Note that AIFnLRCLK is derived from AIFnBCLK, and an internal or external AIFnBCLK signal must be present to generate AIFnLRCLK.

The AIFnLRCLK signal can be inverted in Master or Slave modes using the AIFn_LRCLK_INV register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1 BCLK Ctrl	7	AIF1_BCLK_INV	0	AIF1 Audio Interface BCLK Invert 0 = AIF1BCLK not inverted 1 = AIF1BCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	6	AIF1_BCLK_FRC	0	AIF1 Audio Interface BCLK Output Control 0 = Normal 1 = AIF1BCLK always enabled in Master mode
	5	AIF1_BCLK_MSTR	0	AIF1 Audio Interface BCLK Master Select 0 = AIF1BCLK Slave mode 1 = AIF1BCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1282 (0502h) AIF1 Rx Pin Ctrl	2	AIF1_LRCLK_INV	0	AIF1 Audio Interface LRCLK Invert 0 = AIF1LRCLK not inverted 1 = AIF1LRCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	1	AIF1_LRCLK_FRC	0	AIF1 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF1LRCLK always enabled in Master mode
	0	AIF1_LRCLK_MSTR	0	AIF1 Audio Interface LRCLK Master Select 0 = AIF1LRCLK Slave mode 1 = AIF1LRCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.

Table 22 AIF1 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2 BCLK Ctrl	7	AIF2_BCLK_INV	0	AIF2 Audio Interface BCLK Invert 0 = AIF2BCLK not inverted 1 = AIF2BCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	6	AIF2_BCLK_FRC	0	AIF2 Audio Interface BCLK Output Control 0 = Normal 1 = AIF2BCLK always enabled in Master mode
	5	AIF2_BCLK_MSTR	0	AIF2 Audio Interface BCLK Master Select 0 = AIF2BCLK Slave mode 1 = AIF2BCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1346 (0542h) AIF2 Px Pin Ctrl	2	AIF2_LRCLK_INV	0	AIF2 Audio Interface LRCLK Invert 0 = AIF2LRCLK not inverted 1 = AIF2LRCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	1	AIF2_LRCLK_FRC	0	AIF2 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF2LRCLK always enabled in Master mode
	0	AIF2_LRCLK_MSTR	0	AIF2 Audio Interface LRCLK Master Select 0 = AIF2LRCLK Slave mode 1 = AIF2LRCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.

Table 23 AIF2 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3 BCLK Ctrl	7	AIF3_BCLK_INV	0	AIF3 Audio Interface BCLK Invert 0 = AIF3BCLK not inverted 1 = AIF3BCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	6	AIF3_BCLK_FRC	0	AIF3 Audio Interface BCLK Output Control 0 = Normal 1 = AIF3BCLK always enabled in Master mode
	5	AIF3_BCLK_MSTR	0	AIF3 Audio Interface BCLK Master Select 0 = AIF3BCLK Slave mode 1 = AIF3BCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1410 (0582h) AIF3 Rx Pin Ctrl	2	AIF3_LRCLK_INV	0	AIF3 Audio Interface LRCLK Invert 0 = AIF3LRCLK not inverted 1 = AIF3LRCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	1	AIF3_LRCLK_FRC	0	AIF3 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF3LRCLK always enabled in Master mode
	0	AIF3_LRCLK_MSTR	0	AIF3 Audio Interface LRCLK Master Select 0 = AIF3LRCLK Slave mode 1 = AIF3LRCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.

Table 24 AIF3 Master / Slave Control

AIF SIGNAL PATH ENABLE

The AIF1 and AIF2 interfaces support up to 6 input (RX) channels and up to 6 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 25.

The AIF3 interface supports up to 2 input (RX) channels and up to 2 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 26 and Table 27.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks.

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that this 'on-the-fly' re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

The WM8998 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable an AIF signal path, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error conditions can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1305 (0519h) AIF1 Tx Enables	5	AIF1TX6_ENA	0	AIF1 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1TX5_ENA	0	AIF1 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF1TX4_ENA	0	AIF1 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1TX3_ENA	0	AIF1 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1TX2_ENA	0	AIF1 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1TX1_ENA	0	AIF1 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1306 (051Ah) AIF1 Rx Enables	5	AIF1RX6_ENA	0	AIF1 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1RX5_ENA	0	AIF1 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	AIF1RX4_ENA	0	AIF1 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1RX3_ENA	0	AIF1 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1RX2_ENA	0	AIF1 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1RX1_ENA	0	AIF1 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 25 AIF1 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1369 (0559h) AIF2 TX Enables	5	AIF2TX6_ENA	0	AIF2 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2TX5_ENA	0	AIF2 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2TX4_ENA	0	AIF2 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF2TX3_ENA	0	AIF2 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF2TX2_ENA	0	AIF2 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2TX1_ENA	0	AIF2 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1370 (055Ah) AIF2 RX Enables	5	AIF2RX6_ENA	0	AIF2 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2RX5_ENA	0	AIF2 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2RX4_ENA	0	AIF2 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	AIF2RX3_ENA	0	AIF2 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF2RX2_ENA	0	AIF2 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2RX1_ENA	0	AIF2 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 26 AIF2 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1433 (0599h) AIF3 TX Enables	1	AIF3TX2_ENA	0	AIF3 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF3TX1_ENA	0	AIF3 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1434 (059Ah) AIF3 RX Enables	1	AIF3RX2_ENA	0	AIF3 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF3RX1_ENA	0	AIF3 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 27 AIF3 Signal Path Enable

AIF BCLK AND LRCLK CONTROL

The AIFnBCLK frequency is selected by the AIFn_BCLK_FREQ register. For each value of this register, the actual frequency depends upon whether AIFn is configured for a 48kHz-related sample rate or a 44.1kHz-related sample rate, as described below.

If AIFn_RATE<1000 (see Table 19), then AIFn is referenced to the SYSCLK clocking domain and the applicable frequency depends upon the SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3 registers.

If AIFn_RATE≥1000, then AIFn is referenced to the ASYNCCLK clocking domain and the applicable frequency depends upon the ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2 registers.

The selected AIFnBCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. See “Clocking and Sample Rates” for details of SYSCLK and ASYNCCLK domains, and the associated control registers.

The AIFnLRCLK frequency is controlled relative to AIFnBCLK by the AIFn_BCPF divider.

Note that the BCLK rate must be configured in Master or Slave modes, using the AIFn_BCLK_FREQ registers. The LRCLK rate(s) only require to be configured in Master mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1 BCLK Ctrl	4:0	AIF1_BCLK_FREQ [4:0]	01100	AIF1BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF1_RATE<1000, then AIF1 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF1_RATE>=1000, then AIF1 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF1BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1286 (0506h) AIF1 Tx BCLK Rate	12:0	AIF1_BCPF [12:0]	0040h	AIF1LRCLK Rate This register selects the number of BCLK cycles per AIF1LRCLK frame. AIF1LRCLK clock = AIF1BCLK / AIF1_BCPF Integer (LSB = 1), Valid from 8..8191

Table 28 AIF1 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2 BCLK Ctrl	4:0	AIF2_BCLK_FREQ [4:0]	01100	AIF2BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF2_RATE<1000, then AIF2 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF2_RATE>=1000, then AIF2 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF2BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1350 (0546h) AIF2 Rx BCLK Rate	12:0	AIF2_BCPF [12:0]	0040h	AIF2LRCLK Rate This register selects the number of BCLK cycles per AIF2LRCLK frame. AIF2LRCLK clock = AIF2BCLK / AIF2_BCPF Integer (LSB = 1), Valid from 8..8191

Table 29 AIF2 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3 BCLK Ctrl	4:0	AIF3_BCLK_FREQ [4:0]	01100	AIF3BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF3_RATE<1000, then AIF3 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF3_RATE>=1000, then AIF3 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF3BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1414 (0586h) AIF3 Rx BCLK Rate	12:0	AIF3_BCPF [12:0]	0040h	AIF3LRCLK Rate This register selects the number of BCLK cycles per AIF3LRCLK frame. AIF3LRCLK clock = AIF3BCLK / AIF3_BCPF Integer (LSB = 1), Valid from 8..8191

Table 30 AIF3 BCLK and LRCLK Control

AIF DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, word lengths and slot configurations for AIF1, AIF2 and AIF3 are described in Table 31, Table 32 and Table 33 respectively.

Note that Left-Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8998).

The AIFn Slot Length is the number of BCLK cycles in one timeslot within the overall LRCLK frame. The Word Length is the number of valid data bits within each timeslot. (If the word length is less than the slot length, then there will be unused BCLK cycles at the end of each timeslot.) The AIFn word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF input (RX) and AIF output (TX) channel, the position of the audio data sample within the LRCLK frame is configurable. The _SLOT registers define the timeslot position of the audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The timeslots are numbered as illustrated in Figure 44 through to Figure 47.

Note that, in DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1284 (0504h) AIF1 Format	2:0	AIF1_FMT [2:0]	000	AIF1 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1287 (0507h) AIF1 Frame Ctrl 1	13:8	AIF1TX_WL [5:0]	18h	AIF1 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1TX_SLOT_LEN [7:0]	18h	AIF1 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1288 (0508h) AIF1 Frame Ctrl 2	13:8	AIF1RX_WL [5:0]	18h	AIF1 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1RX_SLOT_LEN [7:0]	18h	AIF1 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1289 (0509h) to R1296 (0510h)	5:0	AIF1TX1_SLOT [5:0]	0h	AIF1 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1TX2_SLOT [5:0]	1h	
	5:0	AIF1TX3_SLOT [5:0]	2h	
	5:0	AIF1TX4_SLOT [5:0]	3h	
	5:0	AIF1TX5_SLOT [5:0]	4h	
	5:0	AIF1TX6_SLOT [5:0]	5h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1297 (0511h) to R1304 (0518h)	5:0	AIF1RX1_SLOT [5:0]	0h	AIF1 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1RX2_SLOT [5:0]	1h	
	5:0	AIF1RX3_SLOT [5:0]	2h	
	5:0	AIF1RX4_SLOT [5:0]	3h	
	5:0	AIF1RX5_SLOT [5:0]	4h	
	5:0	AIF1RX6_SLOT [5:0]	5h	

Table 31 AIF1 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1348 (0544h) AIF2 Format	2:0	AIF2_FMT [2:0]	000	AIF2 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1351 (0547h) AIF2 Frame Ctrl 1	13:8	AIF2TX_WL [5:0]	18h	AIF2 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2TX_SLOT_LEN [7:0]	18h	AIF2 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1352 (0548h) AIF2 Frame Ctrl 2	13:8	AIF2RX_WL [5:0]	18h	AIF2 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2RX_SLOT_LEN [7:0]	18h	AIF2 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1353 (0549h) to R1358 (054Eh)	5:0	AIF2TX1_SLOT [5:0]	0h	AIF2 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2TX2_SLOT [5:0]	1h	
	5:0	AIF2TX3_SLOT [5:0]	2h	
	5:0	AIF2TX4_SLOT [5:0]	3h	
	5:0	AIF2TX5_SLOT [5:0]	4h	
	5:0	AIF2TX6_SLOT [5:0]	5h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1361 (0551h) to R1366 (0556h)	5:0	AIF2RX1_SLOT [5:0]	0h	AIF2 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2RX2_SLOT [5:0]	1h	
	5:0	AIF2RX3_SLOT [5:0]	2h	
	5:0	AIF2RX4_SLOT [5:0]	3h	
	5:0	AIF2RX5_SLOT [5:0]	4h	
	5:0	AIF2RX6_SLOT [5:0]	5h	

Table 32 AIF2 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1412 (0584h) AIF3 Format	2:0	AIF3_FMT [2:0]	000	AIF3 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1415 (0587h) AIF3 Frame Ctrl 1	13:8	AIF3TX_WL [5:0]	18h	AIF3 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF3TX_SLOT_LEN [7:0]	18h	AIF3 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1416 (0588h) AIF3 Frame Ctrl 2	13:8	AIF3RX_WL [5:0]	18h	AIF3 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF3RX_SLOT_LEN [7:0]	18h	AIF3 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1417 (0589h) AIF3 Frame Ctrl 3	5:0	AIF3TX1_SLOT [5:0]	0h	AIF3 TX Channel 1 Slot position Defines the TX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1418 (058Ah) AIF3 Frame Ctrl 4	5:0	AIF3TX2_SLOT [5:0]	1h	AIF3 TX Channel 2 Slot position Defines the TX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63
R1425 (0591h) AIF3 Frame Ctrl 11	5:0	AIF3RX1_SLOT [5:0]	0h	AIF3 RX Channel 1 Slot position Defines the RX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1426 (0592h) AIF3 Frame Ctrl 12	5:0	AIF3RX2_SLOT [5:0]	1h	AIF3 RX Channel 2 Slot position Defines the RX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63

Table 33 AIF3 Digital Audio Data Control

AIF TDM AND TRI-STATE CONTROL

The AIFn output pins are tri-stated when the AIFn_TRI register is set.

Under default conditions, the AIFnTXDAT output is held at logic 0 when the WM8998 is not transmitting data (ie. during timeslots that are not enabled for output by the WM8998). When the AIFnTX_DAT_TRI register is set, the WM8998 tri-states the respective AIFnTXDAT pin when not transmitting data, allowing other devices to drive the AIFnTXDAT connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1281 (0501h) AIF1 Tx Pin Ctrl	5	AIF1TX_DAT_TRI	0	AIF1TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1283 (0503h) AIF1 Rate Ctrl	6	AIF1_TRI	0	AIF1 Audio Interface Tri-State Control 0 = Normal 1 = AIF1 Outputs are tri-stated

Table 34 AIF1 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1345 (0541h) AIF2 Tx Pin Ctrl	5	AIF2TX_DAT_TRI	0	AIF2TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1347 (0543h) AIF2 Rate Ctrl	6	AIF2_TRI	0	AIF2 Audio Interface Tri-State Control 0 = Normal 1 = AIF2 Outputs are tri-stated

Table 35 AIF2 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1409 (0581h) AIF3 Tx Pin Ctrl	5	AIF3TX_DAT_TRI	0	AIF3TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1411 (0583h) AIF3 Rate Ctrl	6	AIF3_TRI	0	AIF3 Audio Interface Tri-State Control 0 = Normal 1 = AIF3 Outputs are tri-stated

Table 36 AIF3 TDM and Tri-State Control

AIF DIGITAL PULL-UP AND PULL-DOWN

The WM8998 provides integrated pull-up and pull-down resistors on each of the AIFnLRCLK, AIFnBCLK and AIFnRXDAT pins. This provides a flexible capability for interfacing with other devices.

Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 37, Table 38 and Table 39. When the pull-up and pull-down resistors are both enabled, the WM8998 provides a 'bus keeper' function on the respective pin. The bus keeper function holds the logic level unchanged whenever the pin is undriven (eg. if the signal is tri-stated).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3107 (0C23h) Misc Pad Ctrl 4	5	AIF1LRCLK_PU	0	AIF1LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1LRCLK_PD and AIF1LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1LRCLK pin.
	4	AIF1LRCLK_PD	0	AIF1LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1LRCLK_PD and AIF1LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1LRCLK pin.
	3	AIF1BCLK_PU	0	AIF1BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1BCLK_PD and AIF1BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1BCLK pin.
	2	AIF1BCLK_PD	0	AIF1BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1BCLK_PD and AIF1BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1BCLK pin.
	1	AIF1RXDAT_PU	0	AIF1RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1RXDAT_PD and AIF1RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1RXDAT pin.
	0	AIF1RXDAT_PD	0	AIF1RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1RXDAT_PD and AIF1RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1RXDAT pin.

Table 37 AIF1 Digital Pull-Up and Pull-Down Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3108 (0C24h) Misc Pad Ctrl 5	5	AIF2LRCLK_PU	0	AIF2LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2LRCLK_PD and AIF2LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2LRCLK pin.
	4	AIF2LRCLK_PD	0	AIF2LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2LRCLK_PD and AIF2LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2LRCLK pin.
	3	AIF2BCLK_PU	0	AIF2BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2BCLK_PD and AIF2BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2BCLK pin.
	2	AIF2BCLK_PD	0	AIF2BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2BCLK_PD and AIF2BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2BCLK pin.
	1	AIF2RXDAT_PU	0	AIF2RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2RXDAT_PD and AIF2RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2RXDAT pin.
	0	AIF2RXDAT_PD	0	AIF2RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2RXDAT_PD and AIF2RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2RXDAT pin.

Table 38 AIF2 Digital Pull-Up and Pull-Down Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3109 (0C25h) Misc Pad Ctrl 6	5	AIF3LRCLK_PU	0	AIF3LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3LRCLK_PD and AIF3LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3LRCLK pin.
	4	AIF3LRCLK_PD	0	AIF3LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3LRCLK_PD and AIF3LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3LRCLK pin.
	3	AIF3BCLK_PU	0	AIF3BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3BCLK_PD and AIF3BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3BCLK pin.
	2	AIF3BCLK_PD	0	AIF3BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3BCLK_PD and AIF3BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3BCLK pin.
	1	AIF3RXDAT_PU	0	AIF3RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3RXDAT_PD and AIF3RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3RXDAT pin.
	0	AIF3RXDAT_PD	0	AIF3RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3RXDAT_PD and AIF3RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3RXDAT pin.

Table 39 AIF3 Digital Pull-Up and Pull-Down Control

SLIMBUS INTERFACE

The SLIMbus protocol is highly configurable and adaptable, supporting multiple audio signal paths, and mixed sample rates simultaneously. It also supports control messaging and associated communications between devices.

SLIMBUS DEVICES

The SLIMbus components comprise different device classes (Manager, Framer, Interface, Generic). Each component on the bus has an Interface Device, which provides bus management services for the respective component. One or more components on the bus will provide Manager and Framer Device functions; the Manager has the capabilities to administer the bus, whilst the Framer is responsible for driving the CLK line and for driving the DATA required to establish the Frame Structure on the bus. Note that only one Manager and one Framer Device will be active at any time. The Framer function can be transferred between Devices when required. Generic Devices provide the basic SLIMbus functionality for the associated Port(s), and for the Transport Protocol by which audio signal paths are established on the bus.

SLIMBUS FRAME STRUCTURE

The SLIMbus bit stream is formatted within a defined structure of Cells, Slots, Subframes, Frames, and Superframes:

- A single data bit is known as a Cell
- 4 Cells make a Slot
- 192 Slots make a Frame
- 8 Frames make a Superframe

The bit stream structure is configurable to some extent, but the Superframe definition always comprises 1536 slots. The transmitted/received bit rate is not fixed; it can be configured according to system requirements, and can be changed dynamically without interruption to active audio paths.

The SLIMbus CLK frequency (also the bus bit rate) is defined by a *Root Frequency (RF)* and a *Clock Gear (CG)*. In the top Clock Gear (Gear 10), the CLK frequency is equal to the Root Frequency. Each reduction in the Clock Gear halves the CLK frequency, and doubles the duration of the Superframe.

The SLIMbus bandwidth will typically comprise Control space (for bus messages, synchronisation etc.) and Data space (for audio paths). The precise allocation is configurable, and can be entirely Control space, if required.

The Subframe definition comprises the number of Slots per Subframe (6, 8, 24 or 32 Slots), and the number of these Slots (per Subframe) allocated as Control space. The applicable combination of Subframe length and Control space width are defined by the *Subframe Mode (SM)* parameter.

The SLIMbus Frame always comprises 192 Slots, regardless of the Subframe definition. A number of Slots are allocated to Control space, as noted above; the remaining Slots are allocated to Data space. Some of the Control space is required for Framing Information and for the Guide Channel (described below); the remainder of the Control space are allocated to the Message Channel.

CONTROL SPACE

Framing Information is provided in Slots 0 and 96 of every Frame. Slot 0 contains a 4-bit synchronisation code; Slot 96 contains the 32-bit Framing Information, transmitted 4 bits at a time over the 8 Frames that make up the SLIMbus Superframe. The Clock Gear, Root Frequency, Subframe configuration, along with some other parameters, are encoded within the Framing Information.

The Guide Channel occupies two Slots within Frame 0. This provides the necessary information for a SLIMbus component to acquire and verify the frame synchronisation. The Guide Channel occupies the first two Control space Slots within the first Frame of the bit stream, excluding the Framing Information Slots. Note that the exact Slot allocation will depend upon the applicable Subframe mode.

The Message Channel is allocated all of the Control space not used by the Framing Information or the Guide Channel. The Message Channel enables SLIMbus devices to communicate with each other, using a priority-based mechanism defined in the MIPI specification.

Messages may be broadcast to all devices on the bus, or can be addressed to specific devices using their allocated *Logical Address (LA)* or *Enumeration Address (EA)*. Note that, device-specific messages are directed to a particular device (ie. Manager, Framer, Interface or Generic) within a component on the bus.

DATA SPACE

The Data space can be organised into a maximum of 256 Data Channels. Each Channel, identified by a unique *Channel Number (CN)*, is a stream of one or more contiguous Slots, organised in a consistent data structure that repeats at a fixed interval.

A Data Channel is defined by its *Segment Length (SL)* (number of contiguous Slots allocated), Segment Interval (spacing between the first Slots of successive Segments), and Segment Offset (the Slot Number of the first allocated Slot within the Superframe). The Segment Interval and Segment Offset are collectively defined by a *Segment Distribution (SD)*, by which the SLIMbus Manager may configure (or re-configure) any Data Channel.

Each Segment may comprise TAG, AUX and DATA portions. Any of these portions may be 0-length; the exact composition depends on the *Transport Protocol (TP)* for the associated Channel (see below). The DATA portion must be wide enough to accommodate one full word of the Data Channel contents (data words cannot be spread across multiple segments).

The Segment Interval for each Data Channel represents the minimum spacing between consecutive data samples for that Channel. (Note - the minimum spacing applies if every allocated segment is populated with new data; in many cases, additional bandwidth is allocated, as described below, and not every allocated segment is used.)

The Segment Interval gives rise to Segment Windows for each Data Channel, aligned to the start of every Superframe. The Segment Window boundaries define the times within which each new data sample must be buffered, ready for transmission - adherence to these fixed boundaries allows Slot allocations to be moved within a Segment Window, without altering the signal latency. The Segment Interval may be either shorter or longer than the Frame length, but there is always an integer number of Segment Windows per Superframe.

The *Transport Protocol (TP)* defines the flow control or handshaking method used by the Ports associated with a Data Channel. The applicable flow control mode(s) depend on the relationship between the audio sample rate (flow rate) and the SLIMbus CLK frequency. If the two rates are synchronised and integer-related, then no flow control is needed; in other cases, the flow may be regulated by the use of a 'Presence' bit. The Presence bit can either be set by the source Device ('pushed' protocol), or by the sink Device ('pulled' protocol).

The Data Channel structure is defined in terms of the *Transport Protocol (TP)*, *Segment Distribution (SD)*, and the *Segment Length (SL)* parameters. Each of these is described above.

The Data Channel content definition includes a *Presence Rate (PR)* parameter (describing the nominal sample rate for the audio channel) and a *Frequency Locked (FL)* bit (identifying whether the data source is synchronised to the SLIMbus CLK). The *Data Length (DL)* parameter defines the size of each data sample (number of Slots). The *Auxiliary Bits Format (AF)* and *Data Type (DT)* parameters provide support for non-PCM encoded data channels; the *Channel Link (CL)* parameter is an indicator that channel CN is related to the previous channel, CN-1.

For a given Root Frequency and Clock Gear, the *Segment Length (SL)* and *Segment Distribution (SD)* parameters define the amount of SLIMbus bandwidth that is allocated to a given Data Channel. The minimum bandwidth requirements of a Data Channel are represented by the *Presence Rate (PR)* and *Data Length (DL)* parameters. The allocated SLIMbus bandwidth must be equal to or greater than the bandwidth of the data to be transferred.

The Segment Interval defines the repetition rate of the SLIMbus Slots allocated to consecutive data samples for a given Data Channel. The *Presence Rate (PR)* is the nominal sample rate of the audio path. The Segment Rate (determined by the Segment Interval value) must be equal to or greater than the Presence Rate for a given data channel. The following constraints must be observed, when configuring a SLIMbus channel:

- If Pushed or Pulled Transport Protocol is selected, the Segment Rate must be greater than the Presence Rate, to ensure that samples are not dropped as a result of clock drift.
- If Isochronous Transport Protocol is selected, the Segment Rate must be equal to the

Presence Rate. Isochronous Transport Protocol should only be selected if the data source is frequency-locked to the SLIMbus CLK (ie. the data source is synchronised to the SLIMbus Framer device).

SLIMBUS CONTROL SEQUENCES

This section describes the messages and general protocol associated with most aspects of the SLIMbus system.

Note that the SLIMbus specification permits some flexibility in Core Message support for different components. See “SLIMbus Interface Control” for details of which message(s) are supported on each of the SLIMbus devices that are present on the WM8998.

DEVICE MANAGEMENT & CONFIGURATION

This section describes the SLIMbus messages associated with configuring all devices on the SLIMbus interface.

When the SLIMbus interface starts up, it is required that one (and only one) of the components provides the Manager and Framer Device functions. Other devices can request connection to the bus after they have gained synchronisation.

The **REPORT_PRESENT (DC, DCV)** message may be issued by devices attempting to connect to the bus. The payload of this message contains the *Device Class (DC)* and *Device Class Version (DCV)* parameters, describing the type of device that is attempting to connect. This message may be issued autonomously by the connecting device, or else in response to a **REQUEST_SELF_ANNOUNCEMENT** message from the Manager Device.

After positively acknowledging the REPORT_PRESENT message, the Manager Device will then issue the **ASSIGN_LOGICAL_ADDRESS (LA)** message to allow the other device to connect to the bus. The payload of this message contains the *Logical Address (LA)* parameter only; this is the unique address by which the connected device will send and receive SLIMbus messages. The device is then said to be ‘enumerated’.

Once a device has been successfully connected to the bus, the Logical Address (LA) parameter can be changed at any time using the **CHANGE_LOGICAL_ADDRESS (LA)** message.

The **RESET_DEVICE** message commands an individual SLIMbus device to perform its reset procedure. As part of the reset, all associated ports will be reset, and any associated Data Channels will be cancelled. Note that, if the RESET_DEVICE command is issued to an Interface Device, it will cause a Component Reset (ie. all Devices within the associated component are reset). Under a Component Reset, every associated Device will release its Logical Address, and the Component will become disconnected from the bus.

INFORMATION MANAGEMENT

A memory map of Information Elements is defined for each Device. This is arranged in 3 x 1kByte blocks, comprising Core Information elements, Device Class-specific Information elements, and User Information elements respectively, as described in the MIPI specification. Note that the contents of the User Information portion for each WM8998 SLIMbus Device are reserved.

Read/Write access is implemented using the messages described below. Specific elements within the Information Map are identified using the *Element Code (EC)* parameter. In the case of Read access, a unique *Transaction ID (TID)* is assigned to each message relating to a particular read/write request.

The **REQUEST_INFORMATION (TID, EC)** message is used to instruct a device to respond with the indicated information. The payload of this message contains the *Transaction ID (TID)* and the *Element Code (EC)*.

The **REQUEST_CLEAR_INFORMATION (TID, EC, CM)** message is used to instruct a device to respond with the indicated information, and also to clear all, or parts, of the same information slice. The payload of this message contains the *Transaction ID (TID), Element Code (EC)*, and *Clear Mask (CM)*. The Clear Mask field is used to select which element(s) are to be cleared as part of the instruction.

The **REPLY_INFORMATION (TID, IS)** message is used to provide readback of a requested parameter. The payload of this message contains the *Transaction ID (TID)* and the *Information Slice (IS)*. The Information Slice byte(s) contain the value of the requested parameter.

The **CLEAR_INFORMATION (EC, CM)** message is used to clear all, or parts, of the indicated information slice. The payload of this message contains the *Element Code (EC)* and *Clear Mask (CM)*. The Clear Mask field is used to select which element(s) are to be cleared as part of the instruction.

The **REPORT_INFORMATION (EC, IS)** message is used to inform other devices about a change in a specified element in the Information Map. The payload of this message contains the *Element Code (EC)* and the *Information Slice (IS)*. The Information Slice byte(s) contain the new value of the applicable parameter.

VALUE MANAGEMENT (INCLUDING REGISTER ACCESS)

A memory map of Value Elements is defined for each Device. This is arranged in 3 x 1kByte blocks, comprising Core Value elements, Device Class-specific Value elements, and User Value elements respectively, as described in the MIPI specification. These elements are typically parameters used to configure Device behaviour.

The User Value elements of the Interface Device are used on WM8998 to support Read/Write access to the Register Map. Details of how to access specific registers are described in the "SLIMbus Interface Control" section.

Note that, with the exception of the User Value elements of the Interface Device, the contents of the User Value portion for each WM8998 SLIMbus Device are reserved.

Read/Write access is implemented using the messages described below. Specific elements within the Value Map are identified using the *Element Code (EC)* parameter. In the case of Read access, a unique *Transaction ID (TID)* is assigned to each message relating to a particular read/write request.

The **REQUEST_VALUE (TID, EC)** message is used to instruct a device to respond with the indicated information. The payload of this message contains the *Transaction ID (TID)* and the *Element Code (EC)*.

The **REPLY_VALUE (TID, VS)** message is used to provide readback of a requested parameter. The payload of this message contains the *Transaction ID (TID)* and the *Value Slice (VS)*. The Value Slice byte(s) contain the value of the requested parameter.

The **CHANGE_VALUE (EC, VU)** message is used to write data to a specified element in the Value Map. The payload of this message contains the *Element Code (EC)* and the *Value Update (VU)*. The Value Update byte(s) contain the new value of the applicable parameter.

FRAME & CLOCKING MANAGEMENT

This section describes the SLIMbus messages associated with changing the Frame or Clocking configuration. One or more configuration messages may be issued as part of a Reconfiguration Sequence; all of the updated parameters become active at once, when the Reconfiguration boundary is reached.

The **BEGIN_RECONFIGURATION** message is issued to define a Reconfiguration Boundary point: subsequent NEXT_* messages will become active at the first valid Superframe boundary following receipt of the **RECONFIGURE_NOW** message. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.) Both of these messages have no payload content.

The **NEXT_ACTIVE_FRAMER (LAIF, NCo, NCi)** message is used to select a new device as the active Framer. The payload of this message includes the *Logical Address, Incoming Framer (LAIF)*. Two other fields (NCo, NCi) define the number of clock cycles for which the CLK line shall be inactive during the handover.

The **NEXT_SUBFRAME_MODE (SM)** and **NEXT_CLOCK_GEAR (CG)** messages are used to re-configure the SLIMbus clocking or framing definition. The payload of each is the respective *Subframe Mode (SM) or Clock Gear (CG)* respectively.

The **NEXT_PAUSE_CLOCK (RT)** message instructs the active Framer to pause the bus. The payload of the message contains the Restart Time (RT), which indicates whether the interruption is to be of a specified time and/or phase duration.

The **NEXT_RESET_BUS** message instructs all components on the bus to be reset. In this case, all Devices on the bus are reset and are disconnected from the bus. Subsequent re-connection to the bus follows the same process as when the bus is first initialised.

The **NEXT_SHUTDOWN_BUS** message instructs all devices that the bus is to be shut down.

DATA CHANNEL CONFIGURATION

This section describes the procedure for configuring a SLIMbus Data Channel. Note that the Manager Device is responsible for allocating the available bandwidth as required for each Data Channel.

The **CONNECT_SOURCE (PN, CN)** and **CONNECT_SINK (PN, CN)** messages are issued to the respective devices, defining the Port(s) between which a Data Channel is to be established. Note that multiple destinations (sinks) can be configured for a channel, if required. The payload of each message contains the *Port Number (PN)* and the *Channel Number (CN)* parameters.

The **BEGIN_RECONFIGURATION** message is issued to define a Reconfiguration Boundary point: subsequent NEXT_* messages will become active at the first valid Superframe boundary following receipt of the **RECONFIGURE_NOW** message. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.)

The **NEXT_DEFINE_CHANNEL (CN, TP, SD, SL)** message informs the associated devices of the structure of the Data Channel. The payload of this message contains the *Channel Number (CN)*, *Transport Protocol (TP)*, *Segment Distribution (SD)*, and the *Segment Length (SL)* parameters for the Data Channel.

The **NEXT_DEFINE_CONTENT (CN, FL, PR, AF, DT, CL, DL)**, or **CHANGE_CONTENT (CN, FL, PR, AF, DT, CL, DL)** message provides more detailed information about the Data Channel contents. The payload of this message contains the *Channel Number (CN)*, *Frequency Locked (FL)*, *Presence Rate (PR)*, *Auxiliary Bits Format (AF)*, *Data Type (DT)*, *Channel Link (CL)*, and *Data Length (DL)* parameters.

The **NEXT_ACTIVATE_CHANNEL (CN)** message instructs the channel to be activated at the next Reconfiguration boundary. The payload of this message contains the *Channel Number (CN)* only.

The **RECONFIGURE_NOW** message completes the Reconfiguration sequence, causing all of the 'NEXT_' messages since the BEGIN_RECONFIGURATION to become active at the next valid Superframe boundary. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.)

Active channels can be reconfigured using the **CHANGE_CONTENT**, **NEXT_DEFINE_CONTENT**, or **NEXT_DEFINE_CHANNEL** messages. Note that these changes can be effected without interrupting the data channel; the **NEXT_DEFINE_CHANNEL**, for example, may be used to change a Segment Distribution, in order to reallocate the SLIMbus bandwidth.

An active channel can be paused using the **NEXT_DEACTIVATE_CHANNEL** message, and re-instated using the **NEXT_ACTIVATE_CHANNEL** message.

Data channels can be disconnected using the **DISCONNECT_PORT** or **NEXT_REMOVE_CHANNEL** messages. These messages provide equivalent functionality, but use different parameters (PN or CN respectively) to identify the affected signal path.

SLIMBUS INTERFACE CONTROL

The WM8998 features a MIPI-compliant SLIMbus interface, providing 4 channels of audio input and 6 channels of audio output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the WM8998 control registers.

The SLIMbus interface on WM8998 comprises a Generic Device and an Interface Device. A maximum of 10 Ports can be configured, providing up to 4 input (RX) channels and up to 6 output (TX) channels.

The audio paths associated with the SLIMbus interface are described in the “Digital Core” section.

The SLIMbus interface supports read/write access to the WM8998 control registers, as described later in this section.

The SLIMbus clocking rate and channel allocations are controlled by the Manager Device. The Message Channel and Data Channel bandwidth may be dynamically adjusted according to the application requirements. Note that the Manager Device functions are not implemented on the WM8998, and these bandwidth allocation requirements are outside the scope of this datasheet.

SLIMBUS DEVICE PARAMETERS

The SLIMbus interface on the WM8998 comprises two Devices. The Enumeration Address of each Device within the SLIMbus interface is derived from the parameters noted in Table 40.

DESCRIPTION	MANUFACTURER ID	PRODUCT CODE	DEVICE ID	INSTANCE VALUE	ENUMERATION ADDRESS
Generic	0x012F	0x6349	0x00	0x00	012F_6349_0000
Interface	0x012F	0x6349	0x7F	0x00	012F_6349_7F00

Table 40 SLIMbus Device Parameters

SLIMBUS MESSAGE SUPPORT

The SLIMbus interface on the WM8998 supports bus messages as noted in Table 41.

Additional notes regarding SLIMbus message support are noted below, and also in Table 42.

MESSAGE CODE MC[6:0]	DESCRIPTION	GENERIC	INTERFACE
Device Management Messages			
0x01	REPORT_PRESENT (DC, DCV)	S	S
0x02	ASSIGN_LOGICAL_ADDRESS (LA)	D	D
0x04	RESET_DEVICE ()	D	D
0x08	CHANGE_LOGICAL_ADDRESS (LA)	D	D
0x09	CHANGE_ARBITRATION_PRIORITY (AP)		
0x0C	REQUEST_SELF_ANNOUNCEMENT ()	D	D
0x0F	REPORT_ABSENT ()		
Data Channel Management Messages			
0x10	CONNECT_SOURCE (PN, CN)	D	
0x11	CONNECT_SINK (PN, CN)	D	
0x14	DISCONNECT_PORT (PN)	D	
0x18	CHANGE_CONTENT (CN, FL, PR, AF, DT, CL, DL)	D	
Information Management Messages			
0x20	REQUEST_INFORMATION (TID, EC)	D	D
0x21	REQUEST_CLEAR_INFORMATION (TID, EC, CM)	D	D
0x24	REPLY_INFORMATION (TID, IS)	S	S
0x28	CLEAR_INFORMATION (EC, CM)	D	D
0x29	REPORT_INFORMATION (EC, IS)		S
Reconfiguration Messages			
0x40	BEGIN_RECONFIGURATION ()	D	D
0x44	NEXT_ACTIVE_FRAMER (LAIF, NCo, NCi)		
0x45	NEXT_SUBFRAME_MODE (SM)		D
0x46	NEXT_CLOCK_GEAR (CG)		
0x47	NEXT_ROOT_FREQUENCY (RF)		
0x4A	NEXT_PAUSE_CLOCK (RT)		
0x4B	NEXT_RESET_BUS ()		
0x4C	NEXT_SHUTDOWN_BUS ()		
0x50	NEXT_DEFINE_CHANNEL (CN, TP, SD, SL)	D	
0x51	NEXT_DEFINE_CONTENT (CN, FL, PR, AF, DT, CL, DL)	D	
0x54	NEXT_ACTIVATE_CHANNEL (CN)	D	
0x55	NEXT_DEACTIVATE_CHANNEL (CN)	D	
0x58	NEXT_REMOVE_CHANNEL (CN)	D	
0x5F	RECONFIGURE_NOW ()	D	D
Value Management Messages			
0x60	REQUEST_VALUE (TID, EC)		D
0x61	REQUEST_CHANGE_VALUE (TID, EC, VU)		
0x64	REPLY_VALUE (TID, VS)		S
0x68	CHANGE_VALUE (EC, VU)		D

Table 41 SLIMbus Message Support

S = supported as a Source Device only. D = supported as a Destination Device only.

The WM8998 SLIMbus component must be reset prior to scheduling a Hardware Reset or Power-On Reset. This can be achieved using the RESET_DEVICE message (issued to the WM8998 Interface Device), or else using the NEXT_RESET_BUS message.

PARAMETER CODE	DESCRIPTION	COMMENTS
AF	Auxiliary Bits Format	
CG	Clock Gear	
CL	Channel Link	
CM	Clear Mask	WM8998 does not fully support this function. The CM bytes of the REQUEST_CLEAR_INFORMATION or CLEAR_INFORMATION messages must not be sent to WM8998 Devices. When either of these messages is received, all bits within the specified Information Slice will be cleared.
CN	Channel Number	
DC	Device Class	
DCV	Device Class Variation	
DL	Data Length	
DT	Data Type	WM8998 supports the following DT codes: 0h - Not indicated 1h - LPCM audio Note that 2's complement PCM can be supported with DT=0h.
EC	Element Code	
FL	Frequency Locked	
IS	Information Slice	
LA	Logical Address	
LAIF	Logical Address, Incoming Framer	
NCi	Number of Incoming Framer Clock Cycles	
NCo	Number of Outgoing Framer Clock Cycles	
PN	Port Number	Note that the Port Numbers of the WM8998 SLIMbus paths are register-configurable, as described in Table 43.
PR	Presence Rate	Note that the Presence Rate must be the same as the Sample Rate selected for the associated WM8998 SLIMbus path.
RF	Root Frequency	
RT	Restart Time	WM8998 supports the following RT codes: 0h -Fast Recovery 2h - Unspecified Delay When either of these values is specified, the WM8998 will resume toggling the CLK line within four cycles of the CLK line frequency.
SD	Segment Distribution	Note that any data channels that are assigned the same SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n value must also be assigned the same Segment Interval.
SL	Segment Length	
SM	Subframe Mode	
TID	Transaction ID	
TP	Transport Protocol	WM8998 supports the following TP codes for TX channels: 0h - Isochronous Protocol 1h - Pushed Protocol WM8998 supports the following TP codes for RX channels: 0h - Isochronous Protocol 2h - Pulled Protocol
VS	Value Slice	
VU	Value Update	

Table 42 SLIMbus Parameter Support

SLIMBUS PORT NUMBER CONTROL

The WM8998 SLIMbus interface supports up to 4 input (RX) channels and up to 6 output (TX) channels. The SLIMbus port numbers for these audio channels are configurable using the registers described in Table 43.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1490 (05D2h) SLIMbus RX Ports0	13:8	SLIMRX2_PORT _ADDR [5:0]	1	SLIMbus RX Channel n Port number Valid from 0..63
	5:0	SLIMRX1_PORT _ADDR [5:0]	0	
R1491 (05D3h) SLIMbus RX Ports1	13:8	SLIMRX4_PORT _ADDR [5:0]	3	
	5:0	SLIMRX3_PORT _ADDR [5:0]	2	
R1494 (05D6h) SLIMbus TX Ports0	13:8	SLIMTX2_PORT _ADDR [5:0]	9	SLIMbus TX Channel n Port number Valid from 0..63
	5:0	SLIMTX1_PORT _ADDR [5:0]	8	
R1495 (05D7h) SLIMbus TX Ports1	13:8	SLIMTX4_PORT _ADDR [5:0]	11	
	5:0	SLIMTX3_PORT _ADDR [5:0]	10	
R1496 (05D8) SLIMbus TX Ports2	13:8	SLIMTX6_PORT _ADDR [5:0]	13	
	5:0	SLIMTX5_PORT _ADDR [5:0]	12	

Table 43 SLIMbus Port Numbers

SLIMBUS SAMPLE RATE CONTROL

The SLIMbus RX inputs may be selected as input to the digital mixers or signal processing functions within the WM8998 digital core. The SLIMbus TX outputs are derived from the respective output mixers.

The sample rate for each SLIMbus channel is configured using the SLIMRXn_RATE and SLIMTXn_RATE registers - see Table 19 within the “Digital Core” section.

Note that the SLIMbus interface provides simultaneous support for SYSCLK-referenced and ASYNCCLK-referenced sample rates on different channels. For example, 48kHz and 44.1kHz SLIMbus audio paths can be simultaneously supported.

Sample rate conversion is required when routing the SLIMbus paths to any signal chain that is asynchronous and/or configured for a different sample rate.

SLIMBUS SIGNAL PATH ENABLE

The SLIMbus interface supports up to 4 input (RX) channels and up to 6 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 44.

Note that the SLIMbus audio channels can only be supported when the corresponding ports have been enabled by the Manager Device (ie. in addition to setting the respective enable bits). The status bits in Registers R1527 and R1528 indicate the status of each of the SLIMbus ports.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1525 (05F5h) SLIMbus RX Channel Enable	3	SLIMRX4_ENA	0	SLIMbus RX Channel n Enable 0 = Disabled 1 = Enabled
	2	SLIMRX3_ENA	0	
	1	SLIMRX2_ENA	0	
	0	SLIMRX1_ENA	0	
R1526 (05F6h) SLIMbus TX Channel Enable	5	SLIMTX6_ENA	0	SLIMbus TX Channel n Enable 0 = Disabled 1 = Enabled
	4	SLIMTX5_ENA	0	
	3	SLIMTX4_ENA	0	
	2	SLIMTX3_ENA	0	
	1	SLIMTX2_ENA	0	
	0	SLIMTX1_ENA	0	
R1527 (05F7h) SLIMbus RX Port Status	3	SLIMRX4_PORT_STS	0	SLIMbus RX Channel n Port Status (Read only) 0 = Disabled 1 = Configured and active
	2	SLIMRX3_PORT_STS	0	
	1	SLIMRX2_PORT_STS	0	
	0	SLIMRX1_PORT_STS	0	
R1528 (05F8h) SLIMbus TX Port Status	5	SLIMTX6_PORT_STS	0	SLIMbus TX Channel n Port Status (Read only) 0 = Disabled 1 = Configured and active
	4	SLIMTX5_PORT_STS	0	
	3	SLIMTX4_PORT_STS	0	
	2	SLIMTX3_PORT_STS	0	
	1	SLIMTX2_PORT_STS	0	
	0	SLIMTX1_PORT_STS	0	

Table 44 SLIMbus Signal Path Enable

SLIMBUS CONTROL REGISTER ACCESS

Control register access is supported via the SLIMbus interface. Full read/write access to all registers is possible, via the "User Value Elements" portion of the Value Map.

Register Write operations are implemented using the "CHANGE_VALUE" message. A maximum of two messages may be required, depending on circumstances: the first "CHANGE_VALUE" message selects the register page (bits [23:8] of the Control Register address); the second message contains the data and bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous Read or Write operation.

The associated parameters are described in Table 45 and Table 46, for the generic case of writing the value 0xVVVV to control register address 0xYYYYZZ.

Write Message 1 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	'SS' is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	'LL' is the 8-bit Logical Address of the message destination (ie. the WM8998 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0x800	Identifies the User Value element for selecting the Control Register page address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xYYYY	'YYYY' is bits [23:8] of the applicable Control Register address.

Table 45 Register Write Message (1)

Write Message 2 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	'SS' is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	'LL' is the 8-bit Logical Address of the message destination (ie. the WM8998 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0xUUU	Specifies the Value Map address, calculated as 0xA00 + (2 x 0xZZ), where 'ZZ' is bits [7:0] of the applicable Control Register address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xVVVV	'VVVV' is the 16-bit data to be written.

Table 46 Register Write Message (2)

Note that the first message may be omitted if its contents are unchanged from the previous CHANGE_VALUE message sent to the WM8998.

Register Read operations are implemented using the “CHANGE_VALUE” and “REQUEST_VALUE” messages. A maximum of two messages may be required, depending on circumstances: the “CHANGE_VALUE” message selects the register page (bits [23:8] of the Control Register address); the “REQUEST_VALUE” message contains bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous Read or Write operation.

The associated parameters are described in Table 47 and Table 48, for the generic case of reading the contents of control register address 0xYYYYZZ.

Read Message 1 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	‘SS’ is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	‘LL’ is the 8-bit Logical Address of the message destination (ie. the WM8998 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0x800	Identifies the User Value element for selecting the Control Register page address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xYYYY	‘YYYY’ is bits [23:8] of the applicable Control Register address.

Table 47 Register Read Message (1)

Read Message 2 – REQUEST_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	‘SS’ is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	‘LL’ is the 8-bit Logical Address of the message destination (ie. the WM8998 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0xUUU	Specifies the Value Map address, calculated as 0xA00 + (2 x 0xZZ), where ‘ZZ’ is bits [7:0] of the applicable Control Register address.
Slice Size	0b001	Selects 2-byte slice size
Transaction ID	0xTTTT	‘TTTT’ is the 16-bit Transaction ID for the message. The value is assigned by the SLIMbus Manager Device.

Table 48 Register Read Message (2)

Note that the first message may be omitted if its contents are unchanged from the previous CHANGE_VALUE message sent to the WM8998.

The WM8998 will respond to the Register Read commands in accordance with the normal SLIMbus protocols.

Note that the WM8998 assumes that sufficient Control Space Slots are available in which to provide its response before the next REQUEST_VALUE message is received. The WM8998 response is made using a REPLY_VALUE message; the SLIMbus Manager should wait until the REPLY_VALUE message has been received before sending the next REQUEST_VALUE message. If additional REQUEST_VALUE message(s) are received before the WM8998 response has been made, then the earlier REQUEST_VALUE message(s) will be ignored (ie. only the last REQUEST_VALUE message will be serviced)

SLIMBUS CLOCKING CONTROL

The clock frequency of the SLIMbus interface is not fixed, and may be set according to the application requirements. The clock frequency can be reconfigured dynamically as required.

The WM8998 SLIMbus interface does not include a Framer Device. Accordingly, the SLIMCLK pin is always an input pin on the WM8998.

The supported Root Frequencies are as defined in the MIPI Alliance specification for SLIMbus.

Under normal operating conditions, the SLIMbus interface operates with a fixed Root Frequency (RF); dynamic updates to the bus rate are applied using a selectable Clock Gear (CG) function. The Root Frequency and the Clock Gear setting are controlled by the Manager Device; these parameters are transmitted in every SLIMbus superframe to all devices on the bus.

In Gear 10 (the highest Clock Gear setting), the SLIMCLK input frequency is equal to the Root Frequency. In lower gears, the SLIMCLK frequency is reduced by increasing powers of 2.

The Clock Gear definition is shown in Table 49. Note that 24.576MHz Root Frequency is an example only; other frequencies are also supported.

CLOCK GEAR	DESCRIPTION	SLIMCLK FREQUENCY (assuming 24.576MHz Root Frequency)
10	Divide by 1	24.576MHz
9	Divide by 2	12.288MHz
8	Divide by 4	6.144MHz
7	Divide by 8	3.072MHz
6	Divide by 16	1.536MHz
5	Divide by 32	768kHz
4	Divide by 64	384kHz
3	Divide by 128	192kHz
2	Divide by 256	96kHz
1	Divide by 512	48kHz

Table 49 SLIMbus Clock Gear Selection

The SLIMCLK input can be used to provide a reference source for the Frequency Locked Loops (FLLs). The frequency of this reference is controlled using the SLIMCLK_REF_GEAR register, as described in Table 50.

The SLIMbus clock reference is generated using an adaptive divider on the SLIMCLK input. The divider automatically adapts to the SLIMbus Clock Gear (CG), giving a constant reference frequency for the FLL input.

Note that, if the Clock Gear (CG) on the bus is lower than the SLIMCLK_REF_GEAR, then the selected reference frequency cannot be supported, and the SLIMbus clock reference is disabled.

The SLIMbus clock reference is selected as input to the FLLs using the FLLn_REFCLK_SRC registers. See “Clocking and Sample Rates” for details of system clocking and the FLLs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1507 (05E3h) SLIMbus Framer Ref Gear	3:0	SLIMCLK_REF_ GEAR [3:0]	4h	SLIMbus Clock Reference control. Sets the SLIMbus reference clock relative to the SLIMbus Root Frequency (RF). 0h = Clock stopped 1h = Gear 1 (RF / 512) 2h = Gear 2 (RF / 256) 3h = Gear 3 (RF / 128) 4h = Gear 4 (RF / 64) 5h = Gear 5 (RF / 32) 6h = Gear 6 (RF / 16) 7h = Gear 7 (RF / 8) 8h = Gear 8 (RF / 4) 9h = Gear 9 (RF / 2) Ah = Gear 10 (RF) All other codes are Reserved

Table 50 SLIMbus Clock Reference Control

OUTPUT SIGNAL PATH

The WM8998 provides four stereo and one mono analogue output signal paths. These outputs comprise a ground-referenced headphone driver, ground-referenced line output driver, differential earpiece driver, differential speaker drivers and a digital output interface suitable for external speaker drivers. The output signal paths are summarised in Table 51.

SIGNAL PATH	DESCRIPTIONS	OUTPUT PINS
OUT1L, OUT1R	Ground-referenced headphone output	HPOUTL, HPOUTR
OUT2L, OUT2R	Ground-referenced line output	LINEOUTL, LINEOUTR
OUT3	Differential (BTL) earpiece output	EPOUTP, EPOUTN
OUT4L, OUT4R	Differential speaker output	SPKOUTLN, SPKOUTLP, SPKOUTRP, SPKOUTRN
OUT5L, OUT5R	Digital speaker (PDM) output	SPKDAT, SPKCLK

Table 51 Output Signal Path Summary

The analogue output paths incorporate high performance 24-bit sigma-delta DACs.

Under default conditions, the headphone and line drivers each provide a stereo, single-ended output. A mono mode is also available on these outputs, providing a differential (BTL) configuration. The ground-referenced headphone and line output paths incorporate a common mode feedback path for rejection of system-related noise. These outputs support direct connection to external loads, with no requirement for AC coupling capacitors.

The earpiece path provides a differential (BTL) output, suitable for a typical earpiece load. The differential configuration offers built-in common mode noise rejection.

The speaker output paths are configured to drive a stereo pair of differential (BTL) outputs. The Class D design offers high efficiency at large signal levels. With a suitable choice of external speaker, the Class D output can drive loudspeakers directly, without any additional filter components.

The digital output path provides a stereo Pulse Density Modulation (PDM) output interface, for connection to external audio devices.

Digital volume control is available on all outputs (analogue and digital), with programmable ramp control for smooth, glitch-free operation. Any two of the output signal paths may be selected as input to the Acoustic Echo Cancellation (AEC) loopback paths.

The WM8998 output signal paths are illustrated in Figure 51.

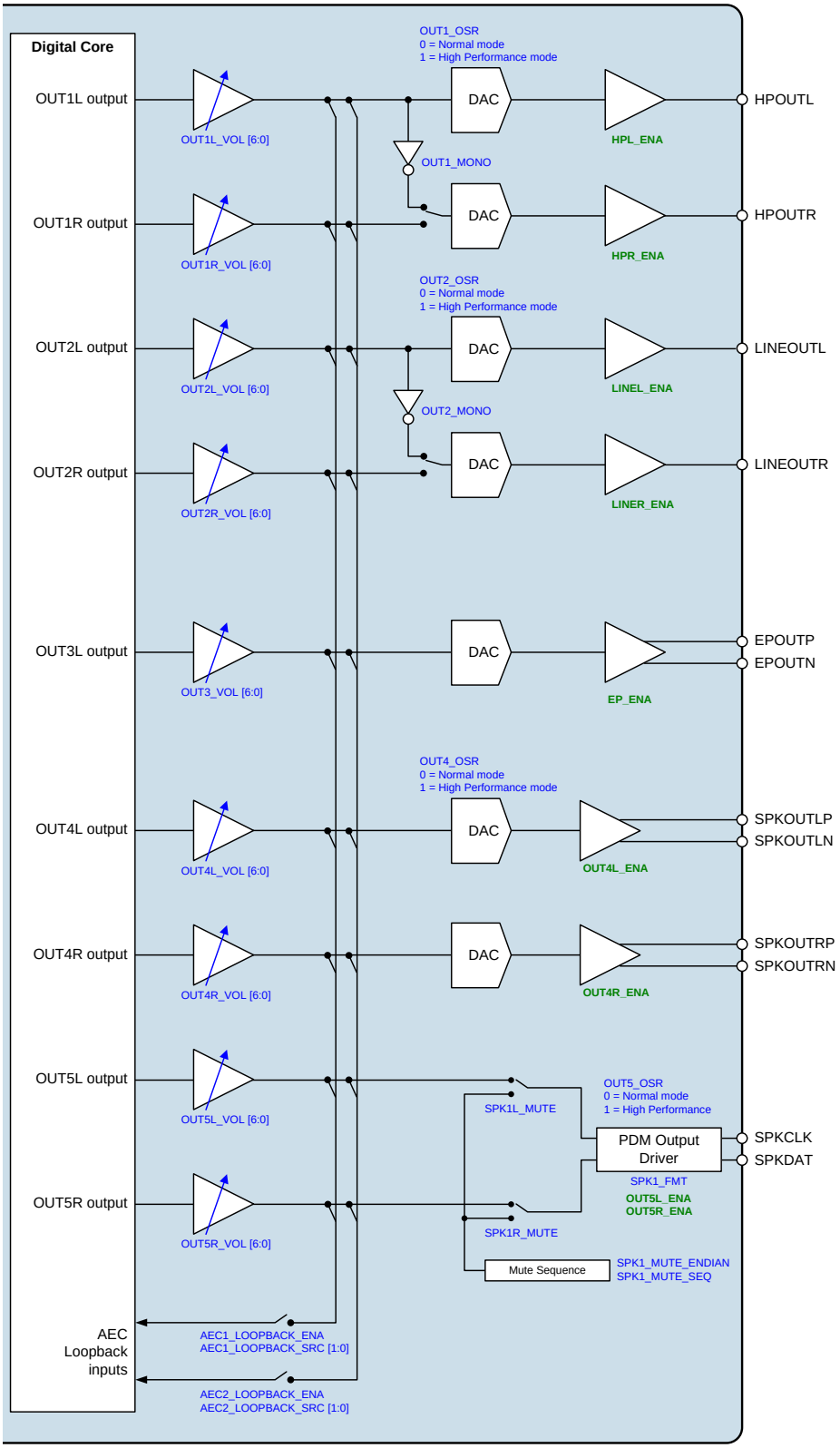


Figure 51 Output Signal Paths

OUTPUT SIGNAL PATH ENABLE

The output signal paths are enabled using the register bits described in Table 52. The respective bit(s) must be enabled for analogue or digital output on the respective output path(s).

The output signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The output signal path mute functions are controlled using the register bits described in Table 57.

The supply rails for outputs (OUT1, OUT2 and OUT3) are generated using an integrated dual-mode Charge Pump, CP1. The Charge Pump is enabled automatically by the WM8998 when required by the output drivers. See the "Charge Pumps, Regulators and Voltage Reference" section for further details.

Note that, to support HPOUT single-ended loads less than 15Ω, or HPOUT/EPOUT differential (BTL) loads less than 30Ω, the Charge Pump (CP1) must be configured for low impedance operation, as described in Table 53.

The WM8998 schedules a pop-suppressed control sequence to enable or disable the OUT1, OUT2, OUT3 and OUT4 signal paths. This is automatically managed in response to setting the respective HPx_ENA, LINEx_ENA, EP_ENA, or SPKOUTx_ENA register bits. See "Control Write Sequencer" for further details.

The output signal path enable/disable control sequences are inputs to the Interrupt circuit, and can be used to trigger an Interrupt event when a sequence completes. See "Interrupts" for further details.

The output signal path enable/disable control sequences can also generate a GPIO output, providing an external indication of the sequence status. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks.

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output signal paths and associated DACs. If an attempt is made to enable an output signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The status bits in Register R1025 and R1030 indicate the status of each of the output signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1024 (0400h) Output Enables 1	9	OUT5L_ENA	0	Output Path 5 (Left) Enable 0 = Disabled 1 = Enabled
	8	OUT5R_ENA	0	Output Path 5 (Right) Enable 0 = Disabled 1 = Enabled
	7	SPKOUTL_ENA	0	Output Path 4 (Left) Enable 0 = Disabled 1 = Enabled
	6	SPKOUTR_ENA	0	Output Path 4 (Right) Enable 0 = Disabled 1 = Enabled
	5	EP_ENA	0	Output Path 3 Enable 0 = Disabled 1 = Enabled
	3	LINEL_ENA	0	Output Path 2 (Left) Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	LINER_ENA	0	Output Path 2 (Right) Enable 0 = Disabled 1 = Enabled
	1	HPL_ENA	0	Output Path 1 (Left) Enable 0 = Disabled 1 = Enabled
	0	HPR_ENA	0	Output Path 1 (Right) Enable 0 = Disabled 1 = Enabled
R1025 (0401h) Output Status 1	9	OUT5L_ENA_STS	0	Output Path 5 (Left) Enable Status 0 = Disabled 1 = Enabled
	8	OUT5R_ENA_STS	0	Output Path 5 (Right) Enable Status 0 = Disabled 1 = Enabled
	7	OUT4L_ENA_STS	0	Output Path 4 (Left) Enable Status 0 = Disabled 1 = Enabled
	6	OUT4R_ENA_STS	0	Output Path 4 (Right) Enable Status 0 = Disabled 1 = Enabled
R1030 (0406h) Raw Output Status 1	5	OUT3_ENA_STS	0	Output Path 3 Enable Status 0 = Disabled 1 = Enabled
	3	OUT2L_ENA_STS	0	Output Path 2 (Left) Enable Status 0 = Disabled 1 = Enabled
	2	OUT2R_ENA_STS	0	Output Path 2 (Right) Enable Status 0 = Disabled 1 = Enabled
	1	OUT1L_ENA_STS	0	Output Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	OUT1R_ENA_STS	0	Output Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 52 Output Signal Path Enable

Note that, to support HPOUT single-ended loads less than 15Ω, or HPOUT/EPOUT differential (BTL) loads less than 30Ω, the Charge Pump (CP1) must be configured for low impedance operation, as described in Table 53.

Note that the low impedance mode, when required, should be configured before enabling any of the OUT1, OUT2 or OUT3 signal paths.

LOW IMPEDANCE MODE CONFIGURATION	
1	Write 0x0C01 to Register R1132 (0x046C)
2	Write 0x0C01 to Register R1134 (0x046E)
3	Write 0x0C01 to Register R1136 (0x0470)

Table 53 Charge Pump (CP1) Configuration for Low Impedance operation

For optimal power consumption, it is recommended to use the default Charge Pump (CP1) configuration whenever possible (ie. excluding the conditions described above). The default Charge Pump operation can be configured using the control sequence described in Table 54.

Note that the following control sequence is only required if Low Impedance operation has previously been selected. The OUT1, OUT2 and OUT3 signal paths should all be disabled when changing the Charge Pump configuration.

NORMAL MODE CONFIGURATION	
1	Write 0x0801 to Register R1132 (0x046C)
2	Write 0x0801 to Register R1134 (0x046E)
3	Write 0x0801 to Register R1136 (0x0470)

Table 54 Charge Pump (CP1) Configuration for Normal operation

OUTPUT SIGNAL PATH SAMPLE RATE CONTROL

The output signal paths are derived from the respective output mixers within the WM8998 digital core. The sample rate for the output signal paths is configured using the OUT_RATE register - see Table 19 within the “Digital Core” section.

Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

OUTPUT SIGNAL PATH CONTROL

A high performance mode can be selected on the output signal paths by setting the OUT*n*_OSR bit for the respective paths. When the OUT*n*_OSR bit is set, the audio performance is improved, but power consumption is also increased. It is recommended to always select the high performance setting (OUTn_OSR = 1) for Output Path 1 and Output Path 2.

The SPKCLK frequency of the PDM output path (OUT5) is controlled by the OUT5_OSR register, as described in Table 55. When the OUT5_OSR bit is set, the audio performance is improved, but power consumption is also increased.

Note that the SPKCLK frequencies noted in Table 55 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the SPKCLK frequencies will be scaled accordingly.

CONDITION	SPKCLK FREQUENCY
OUT5_OSR = 0	3.072MHz
OUT5_OSR = 1	6.144MHz

Table 55 SPKCLK Frequency

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) Output Path Config 1L	13	OUT1_OSR	0	Output Path 1 Oversample Rate 0 = Normal mode 1 = High Performance mode
R1048 (0418h) Output Path Config 2L	13	OUT2_OSR	0	Output Path 2 Oversample Rate 0 = Normal mode 1 = High Performance mode
R1064 (0428h) Output Path Config 4L	13	OUT4_OSR	0	Output Path 4 Oversample Rate 0 = Normal mode 1 = High Performance mode
R1072 (0430h) Output Path Config 5L	13	OUT5_OSR	0	Output Path 5 Oversample Rate 0 = Normal mode 1 = High Performance mode

Table 56 Output Signal Path Control

OUTPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the output signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each output signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the OUT_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the OUT_VD_RAMP register. Note that the OUT_VI_RAMP and OUT_VD_RAMP registers should not be changed while a volume ramp is in progress.

The OUT_VU bits control the loading of the output signal path digital volume and mute controls. When OUT_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the output signal paths are updated when a 1 is written to OUT_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

For correct gain ramp behaviour, the OUT_VU bits should not be written during the 0.28ms after any of the output path enable bits (see Table 52) have been asserted. It is recommended that the output path mute bit be set when the respective output driver is enabled; the signal path can then be un-muted after the 0.28ms has elapsed.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the OUT5 digital output path is not equal to the 0dBFS level of the WM8998 digital core. The maximum digital output level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a 0dBFS output from the digital core corresponds to a -6dBFS level in the PDM output.

The digital volume control register fields are described in Table 57 and Table 58.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1033 (0409h) Output Volume Ramp	6:4	OUT_VD_RAMP [2:0]	010	Output Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	OUT_VI_RAMP [2:0]	010	Output Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R1041 (0411h) DAC Digital Volume 1L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1L_MUTE	1	Output Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT1L_VOL [7:0]	80h	Output Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1045 (0415h) DAC Digital Volume 1R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1R_MUTE	1	Output Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT1R_VOL [7:0]	80h	Output Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1049 (0419h) DAC Digital Volume 2L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT2L_MUTE	1	Output Path 2 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT2L_VOL [7:0]	80h	Output Path 2 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1053 (041Dh) DAC Digital Volume 2R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT2R_MUTE	1	Output Path 2 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT2R_VOL [7:0]	80h	Output Path 2 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1057 (0421h) DAC Digital Volume 3L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT3_MUTE	1	Output Path 3 Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT3_VOL [7:0]	80h	Output Path 3 Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1065 (0429h) DAC Digital Volume 4L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT4L_MUTE	1	Output Path 4 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT4L_VOL [7:0]	80h	Output Path 4 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1069 (042Dh) DAC Digital Volume 4R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT4R_MUTE	1	Output Path 4 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT4R_VOL [7:0]	80h	Output Path 4 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1073 (0431h) DAC Digital Volume 5L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT5L_MUTE	1	Output Path 5 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT5L_VOL [7:0]	80h	Output Path 5 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)
R1077 (0435h) DAC Digital Volume 5R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT5R_MUTE	1	Output Path 5 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT5R_VOL [7:0]	80h	Output Path 5 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 58 for volume range)

Table 57 Output Signal Path Digital Volume Control

Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
3Fh	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 58 Output Signal Path Digital Volume Range

OUTPUT SIGNAL PATH NOISE GATE CONTROL

The WM8998 provides a digital noise gate function for each of the output signal paths. The noise gate ensures best noise performance when the signal path is idle. When the noise gate is enabled, and the applicable signal level is below the noise gate threshold, then the noise gate is activated, causing the signal path to be muted.

The noise gate function is enabled using the NGATE_ENA register, as described in Table 59.

For each output path, the noise gate may be associated with one or more of the signal path threshold detection functions using the _NGATE_SRC register fields. When more than one signal threshold is selected, then the output path noise gate is only activated (ie. muted) when all of the respective signal thresholds are satisfied.

For example, if the OUT1L noise gate is associated with the OUT1L and OUT1R signal paths, then the OUT1L signal path will only be muted if both the OUT1L and OUT1R signal levels are below the respective thresholds.

The noise gate threshold (the signal level below which the noise gate is activated) is set using NGATE_THR. Note that, for each output path, the noise gate threshold represents the signal level at the respective output pin(s) - the threshold is therefore independent of the digital volume and PGA gain settings.

Note that, although there is only one noise gate threshold level (NGATE_THR), each of the output path noise gates may be activated independently, according to the respective signal content and the associated threshold configuration(s).

To prevent erroneous triggering, a time delay is applied before the gate is activated; the noise gate is only activated (ie. muted) when the output levels are below the applicable signal level threshold(s) for longer than the noise gate 'hold time'. The 'hold time' is set using the NGATE_HOLD register.

When the noise gate is activated, the WM8998 gradually attenuates the respective signal path at the rate set by the OUT_VD_RAMP register (see Table 57). When the noise gate is de-activated, the output volume increases at the rate set by the OUT_VI_RAMP register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1043 (0413h) Noise Gate Select 1L	11:0	OUT1L_NGATE_SRC [11:0]	001h	Output Signal Path Noise Gate Source Enables one of more signal paths as inputs to the respective noise gate. If more than one signal path is enabled as an input, the noise gate is only activated (ie. muted) when all of the respective signal thresholds are satisfied. [11] = Reserved [10] = Reserved [9] = OUT5R [8] = OUT5L [7] = OUT4R [6] = OUT4L [5] = Reserved [4] = OUT3 [3] = OUT2R [2] = OUT2L [1] = OUT1R [0] = OUT1L Each bit is coded as: 0 = Disabled 1 = Enabled
R1047 (0417h) Noise Gate Select 1R	11:0	OUT1R_NGATE_SRC [11:0]	002h	
R1051 (041Bh) Noise Gate Select 2L	11:0	OUT2L_NGATE_SRC [11:0]	004h	
R1055 (041Fh) Noise Gate Select 2R	11:0	OUT2R_NGATE_SRC [11:0]	008h	
R1059 (0423h) Noise Gate Select 3L	11:0	OUT3_NGATE_SRC [11:0]	010h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1067 (042Bh) Noise Gate Select 4L	11:0	OUT4L_NGATE_ SRC [11:0]	040h	
R1071 (042Fh) Noise Gate Select 4R	11:0	OUT4R_NGATE_ SRC [11:0]	080h	
R1075 (0433h) Noise Gate Select 5L	11:0	OUT5L_NGATE_ SRC [11:0]	040h	
R1079 (0437h) Noise Gate Select 5R	11:0	OUT5R_NGATE_ SRC [11:0]	080h	
R1112 (0458h) Noise Gate Control	5:4	NGATE_HOLD [1:0]	00	Output Signal Path Noise Gate Hold Time (delay before noise gate is activated) 00 = 30ms 01 = 120ms 10 = 250ms 11 = 500ms
	3:1	NGATE_THR [2:0]	000	Output Signal Path Noise Gate Threshold 000 = -60dB 001 = -66dB 010 = -72dB 011 = -78dB 100 = -84dB 101 = -90dB 110 = -96dB 111 = -102dB
	0	NGATE_ENA	1	Output Signal Path Noise Gate Enable 0 = Disabled 1 = Enabled

Table 59 Output Signal Path Noise Gate Control

OUTPUT SIGNAL PATH AEC LOOPBACK

The WM8998 incorporates two loopback signal paths, which are ideally suited as a reference for Acoustic Echo Cancellation (AEC) processing. Any two of the output signal paths may be selected as the AEC loopback sources.

Note that the WM8998 cannot provide an integrated AEC capability, but the AEC loopback feature enables convenient hook-up to an external device for implementing the required signal processing algorithms.

The AEC Loopback sources are connected after the respective digital volume controls, as illustrated in Figure 51.

The AEC Loopback signals can be selected as input to any of the digital mixers within the WM8998 digital core. The sample rate for the AEC Loopback paths is configured using the OUT_RATE register - see Table 19 within the “Digital Core” section.

The AEC loopback function is enabled using the AEC*n*_LOOPBACK_ENA register bits, (where ‘n’ identifies the applicable path, AEC1 or AEC2). The source signals for the Transmit Path AEC function are selected using the AEC*n*_LOOPBACK_SRC bits.

The WM8998 performs automatic checks to confirm that the SYSCLK frequency is high enough to

support the AEC Loopback function. If an attempt is made to enable this function, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The AEC*n*_ENA_STS register bits indicate the status of the AEC Loopback functions. If an Underclocked Error condition occurs, then these bits can provide indication of whether the AEC Loopback function has been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1104 (0450h) DAC AEC Control 1	5:2	AEC1_LOOPBACK_SRC [3:0]	0000	Input source for Tx AEC1 function 0000 = OUT1L 0001 = OUT1R 0010 = OUT2L 0011 = OUT2R 0100 = OUT3 0110 = OUT4L 0111 = OUT4R 1000 = OUT5L 1001 = OUT5R All other codes are Reserved
	1	AEC1_ENA_STS	0	Transmit (Tx) Path AEC1 Control Status 0 = Disabled 1 = Enabled
	0	AEC1_LOOPBACK_ENA	0	Transmit (Tx) Path AEC1 Control 0 = Disabled 1 = Enabled
R1105 (0451h) DAC AEC Control 2	5:2	AEC2_LOOPBACK_SRC [3:0]	0000	Input source for Tx AEC2 function 0000 = OUT1L 0001 = OUT1R 0010 = OUT2L 0011 = OUT2R 0100 = OUT3 0110 = OUT4L 0111 = OUT4R 1000 = OUT5L 1001 = OUT5R All other codes are Reserved
	1	AEC2_ENA_STS	0	Transmit (Tx) Path AEC2 Control Status 0 = Disabled 1 = Enabled
	0	AEC2_LOOPBACK_ENA	0	Transmit (Tx) Path AEC2 Control 0 = Disabled 1 = Enabled

Table 60 Output Signal Path AEC Loopback Control

HEADPHONE/LINE/EARPIECE OUTPUTS AND MONO MODE

The headphone and line drivers can provide a mono differential (BTL) output; this is selected using the OUTn_MONO register bits. When the OUTn_MONO bit is set, then the respective Right channel output is an inverted copy of the Left channel output signal; this creates a differential output between the respective OUTnL and OUTnR pins.

In mono configuration, the effective gain of the signal path is increased by 6dB.

The mono (BTL) signal paths are illustrated in Figure 51.

The OUT1L and OUT1R output signal paths are associated with the analogue outputs HPOUTL and HPOUTR respectively.

The OUT2L and OUT2R output signal paths are associated with the analogue outputs LINEOUTL and LINEOUTR respectively.

The OUT3 output signal path is associated with the analogue outputs EPOUTP and EPOUTN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) Output Path Config 1L	12	OUT1_MONO	0	Output Path 1 Mono Mode (Configures HPOUTL and HPOUTR as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.
R1048 (0418h) Output Path Config 2L	12	OUT2_MONO	0	Output Path 2 Mono Mode (Configures LINEOUTL and LINEOUTR as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.

Table 61 Headphone Driver Mono Mode Control

The headphone and line driver outputs HPOUTL, HPOUTR, LINEOUTL and LINEOUTR are suitable for direct connection to external loads. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors.

The headphone and line outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pins must be connected to ground for normal operation of the respective outputs.

Note that the feedback pins should be connected to GND close to the respective headphone/line jack, as illustrated in Figure 52. In mono (differential) mode, the feedback pin(s) should be connected to the ground plane that is physically closest to the earpiece output PCB tracks.

The ground feedback path for HPOUTL and HPOUTR is provided via the HPOUTFB1 or HPOUTFB2 pins; the applicable connection must be selected using the ACCDET_SRC register, as described in Table 62.

The ground feedback path for LINEOUTL and LINEOUTR is provided via the LINEOUTFB pin. No register configuration is required for the LINEOUTFB connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R659 (0293h) Accessory Detect Mode 1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUTFB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUTFB2

Table 62 Headphone Output (HPOUT) Ground Feedback Control

The earpiece driver outputs EPOUTP and EPOUTN are suitable for direct connection to an earpiece. The output configuration is differential (BTL), driving both ends of the external load directly - note that there is no associated ground connection.

The headphone, line, and earpiece connections are illustrated in Figure 52.

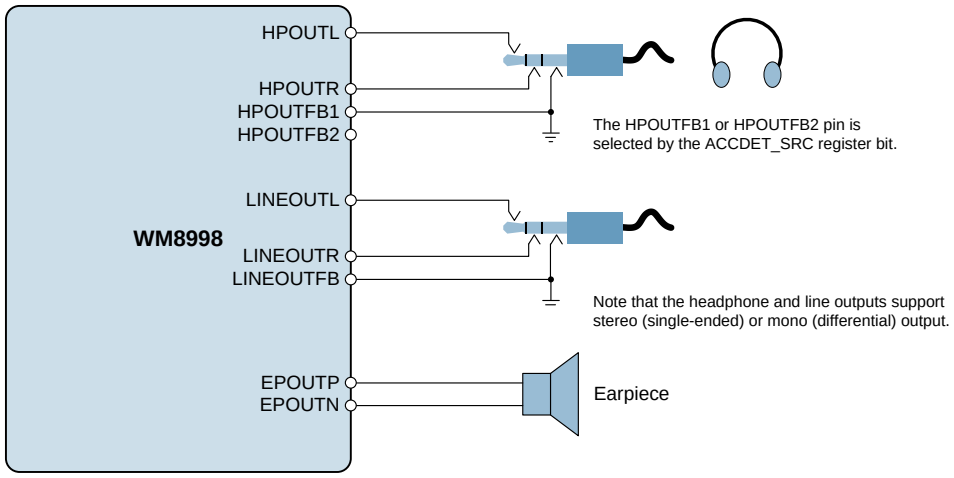


Figure 52 Headphone, Line, and Earpiece Connection

SPEAKER OUTPUTS (ANALOGUE)

The speaker driver outputs SPKOUTLP, SPKOUTLN, SPKOUTLP and SPKOUTLN provide two differential (BTL) outputs suitable for direct connection to external loudspeakers. The integrated Class D speaker driver provides high efficiency at large signal levels.

The speaker driver signal paths incorporate a boost function which shifts the signal levels between the AVDD and SPKVDD voltage domains. The boost is pre-configured (+12dB) for the recommended AVDD and SPKVDD operating voltages (see “Recommended Operating Conditions”).

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be connected directly to a lithium battery. Note that SPKVDDL powers the Left Speaker driver, and SPKVDDR powers the Right Speaker driver; it is assumed that SPKVDDL = SPKVDDR = SPKVDD.

Note that SYSCLK must be present and enabled when using the Class D speaker output; see “Clocking and Sample Rates” for details of SYSCLK and the associated register control fields.

The OUT4L and OUT4R output signal paths are associated with the analogue outputs SPKOUTLP, SPKOUTLN, SPKOUTLP and SPKOUTLN.

The Class D speaker output is a pulse width modulated signal, and requires external filtering in order to recreate the audio signal. With a suitable choice of external speakers, the speakers themselves can provide the necessary filtering. See “Applications Information” for further information on Class D speaker connections.

The external speaker connection is illustrated in Figure 53, assuming suitable speakers are chosen to provide the PWM filtering.

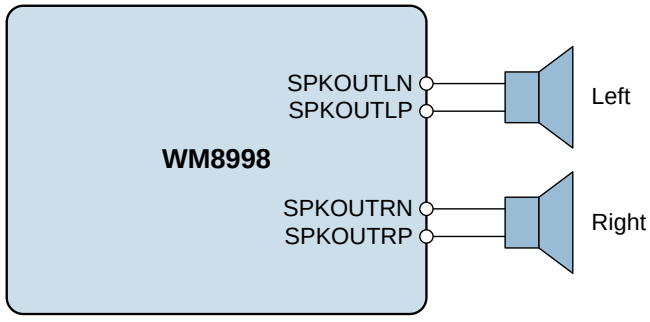


Figure 53 Speaker Connection

SPEAKER OUTPUTS (DIGITAL)

The WM8998 supports a two-channel Pulse Density Modulation (PDM) digital speaker interface; the PDM outputs are associated with the OUT5L and OUT5R output signal paths.

The PDM digital speaker interface is illustrated in Figure 54.

The OUT5L and OUT5R output signal paths are interleaved on the SPKDAT output pin, and clocked using SPKCLK.

Note that the PDM interface supports two different operating modes; these are selected using the SPK1_FMT register bit. See “Signal Timing Requirements” for detailed timing information in both modes.

When SPK1_FMT = 0 (Mode A), then the Left PDM channel is valid at the rising edge of SPKCLK; the Right PDM channel is valid at the falling edge of SPKCLK.

When SPK1_FMT = 1 (Mode B), then the Left PDM channel is valid during the low phase of SPKCLK; the Right PDM channel is valid during the high phase of SPKCLK.

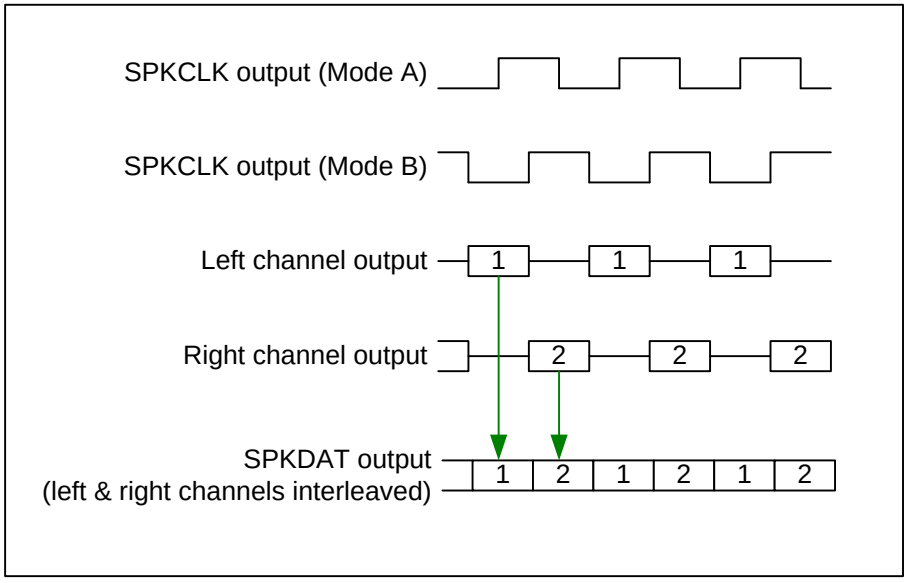


Figure 54 Digital Speaker (PDM) Interface Timing

Clocking for the PDM interface is derived from SYSCLK. Note that the SYSCLK_ENA register must also be set. See “Clocking and Sample Rates” for further details of the system clocks and control registers.

When the OUT5L or OUT5R output signal path is enabled, the PDM interface clock signal is output on the SPKCLK pin.

The output signal paths support normal and high performance operating modes, as described in the “Output Signal Path” section. The SPKCLK frequency is set according to the operating mode of the OUT5 output signal path, as described in Table 63.

Note that the SPKCLK frequencies noted in Table 63 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the SPKCLK frequency will be scaled accordingly.

OUT5_OSR	DESCRIPTION	SPKCLK FREQUENCY
0	Normal mode	3.072MHz
1	High Performance mode	6.144MHz

Table 63 SPKCLK Frequency

The PDM output channels can be independently muted. When muted, the default output on each channel is a DSD-compliant silent stream (0110_1001b). The mute output code can be programmed

to other values if required, using the SPK1_MUTE_SEQ register field. The mute output code can be transmitted MSB-first or LSB-first; this is selectable using the SPK1_MUTE_ENDIAN register.

Note that the PDM Mute function is not a soft-mute; the audio output is interrupted immediately when the PDM mute is asserted. It is recommended to use the Output Signal Path mute function before applying the PDM mute. See Table 57 for details of the OUT5L_MUTE and OUT5R_MUTE registers.

The PDM output interface registers are described in Table 64.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1168 (0490h) PDM SPK1 CTRL 1	13	SPK1R_MUTE	0	PDM Speaker Output 1 (Right) Mute 0 = Audio output (OUT5R) 1 = Mute Sequence output
	12	SPK1L_MUTE	0	PDM Speaker Output 1 (Left) Mute 0 = Audio output (OUT5L) 1 = Mute Sequence output
	8	SPK1_MUTE_ENDIAN	0	PDM Speaker Output 1 Mute Sequence Control 0 = Mute sequence is LSB first 1 = Mute sequence output is MSB first
	7:0	SPK1_MUTE_SEQ [7:0]	69h	PDM Speaker Output 1 Mute Sequence Defines the 8-bit code that is output on SPKDAT (left) or SPKDAT (right) when muted.
R1169 (0491h) PDM SPK1 CTRL 2	0	SPK1_FMT	0	PDM Speaker Output 1 timing format 0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK) 1 = Mode B (PDM data is valid during the high/low phase of SPKCLK)

Table 64 Digital Speaker (PDM) Output Control

The digital speaker (PDM) outputs SPKDAT and SPKCLK are intended for direct connection to a compatible external speaker driver. A typical configuration is illustrated in Figure 55.

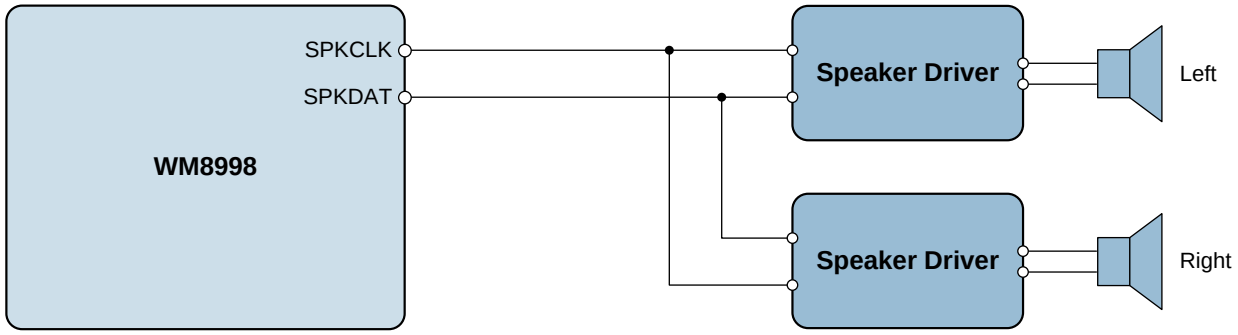


Figure 55 Digital Speaker (PDM) Connection

EXTERNAL ACCESSORY DETECTION

The WM8998 provides external accessory detection functions which can sense the presence and impedance of external components. This can be used to detect the insertion or removal of an external headphone or headset, and to provide an indication of key/button push events.

Jack insertion is detected using the JACKDET pin, which must be connected to a switch contact within the jack socket. An Interrupt event is generated whenever a jack insertion or jack removal event is detected. The jack detect function can also be used to trigger a Wake-Up transition (ie. exit from Sleep mode) and/or to trigger the Control Write Sequencer.

Suppression of pops and clicks caused by jack insertion or removal is provided using the MICDET clamp function. This function can also be used to trigger interrupt events, a Wake-Up transition (ie. exit from Sleep mode) and/or to trigger the Control Write Sequencer. The integrated General Purpose Switch can be synchronised with the MICDET clamp, to provide additional pop suppression capability.

Microphones, push-buttons and other accessories can be detected via the MICDET1 or MICDET2 pins. The presence of a microphone, and the status of a hookswitch can be detected. This feature can also be used to detect push-button operation.

Headphone impedance can be detected via the HPDETL and HPDETR pins; this can be used to set different gain levels or other configuration settings according to the type of load connected. For example, different settings may be applicable to Headphone or Line output loads.

The MICVDD power domain must be enabled when using the Microphone Detect function. (Note that MICVDD is not required for the Jack Detect or Headphone Detect functions.) The MICVDD power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See “Charge Pumps, Regulators and Voltage Reference” for details of these circuits.

The internal 32kHz clock must be present and enabled when using the jack insertion or accessory detection functions; see “Clocking and Sample Rates” for details of the internal 32kHz clock and associated register control fields.

JACK DETECT

The WM8998 provides support for jack insertion switch detection. The jack insertion status can be read using the relevant register status bit. A jack insertion or removal can also be used to trigger an interrupt (IRQ) event or to trigger the Control Write Sequencer.

When the WM8998 is in the low-power Sleep mode (see “Low Power Sleep Configuration”), the jack detect function can be used as a ‘wake-up’ input; a typical use case is where an application is idle in standby mode until a headphone or headset jack is inserted.

Jack insertion and removal is detected using the JACKDET pin. The recommended external connection circuit is illustrated in Figure 56.

The jack detect feature is enabled using JD1_ENA; the jack insertion status can be read using the JD1_STS register.

The JACKDET input de-bounce is selected using the JD1_DB register, as described in Table 65. Note that the de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required.

Note that the Jack Detect signal, JD1, can be used as an input to the MICDET Clamp function. This provides additional functionality relating to jack insertion or jack removal events.

An Interrupt Request (IRQ) event is generated whenever a jack insertion or jack removal is detected (see “Interrupts”). Separate ‘mask’ bits are provided to enable IRQ events on the rising and/or falling edge of the JD1 status.

The Control Write Sequencer can be triggered by a jack insertion or jack removal detection. This is enabled using register bits described in the “Low Power Sleep Configuration” section.

The control registers associated with the Jack Detect function are described in Table 65.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R723 (02D3h) Jack detect analogue	0	JD1_ENA	0	JACKDET enable 0 = Disabled 1 = Enabled
R3413 (0D55h) AOD IRQ Raw Status	0	JD1_STS	0	JACKDET input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET pin is pulled 'low' on Jack insertion.)
R3414 (0D56h) Jack detect debounce	0	JD1_DB	0	JACKDET input de-bounce 0 = Disabled 1 = Enabled

Table 65 Jack Detect Control

A recommended connection circuit, including headphone output and microphone connections, is shown in Figure 56. See "Applications Information" for details of recommended external components.

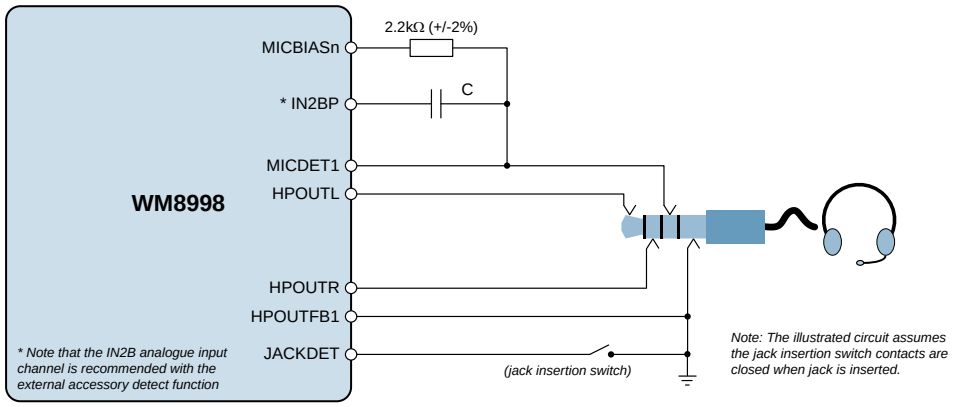


Figure 56 Jack Detect and External Accessory Connections

The internal comparator circuit used to detect the JACKDET status is illustrated in Figure 57.

The threshold voltages for the jack detect circuit are noted in the "Electrical Characteristics". Note that separate thresholds are defined for jack insertion and jack removal.

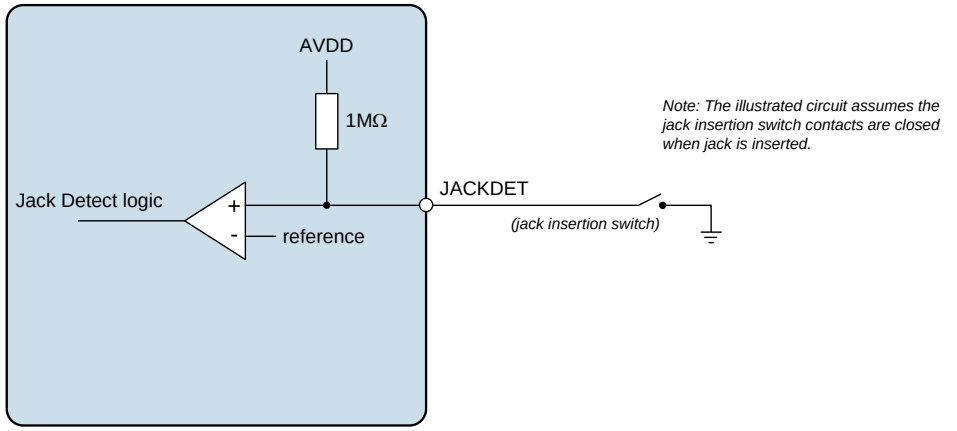


Figure 57 Jack Detect Comparator

JACK POP SUPPRESSION (MICDET CLAMP AND GP SWITCH)

Under typical configuration of a 3.5mm headphone/accessory jack connection, there is a risk of pops and clicks arising from jack insertion or removal. This can occur when the headphone load makes momentary contact with the MICBIAS output when the jack is not fully inserted, as illustrated in Figure 58.

The WM8998 provides a MICDET Clamp function to suppress pops and clicks caused by jack insertion or removal. The clamp is activated by a configurable logic function derived from external logic inputs. The clamp status can be read using the relevant register status bit. The clamp status can also be used to trigger an interrupt (IRQ) event or to trigger the Control Write Sequencer.

When the WM8998 is in the low-power Sleep mode, the MICDET Clamp function can be used as a 'wake-up' input; a typical use case is where an application is idle in standby mode until a headphone or headset jack is inserted. This feature is enabled using the control bits described in Table 73 within the "Low Power Sleep Configuration" section.

The MICDET Clamp function is controlled by a selectable logic condition, derived from the JD1 and/or GP5 signals. The function is enabled and configured using the MICD_CLAMP_MODE register.

The JD1 signal is derived from the Jack Detect function (see Table 65). The GP5 signal is derived from the GPIO5 input pin (see "General Purpose Input / Output").

When the MICDET Clamp is active, the MICDET1/HPOUTFB2 and HPOUTFB1/MICDET2 pins are short-circuited together. The grounding of the MICDET pin is achieved via the applicable HPOUTFB pin - it is assumed that the HPOUTFB connection is grounded externally, as shown in Figure 58.

The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET Clamp. The clamp status can be read using the MICD_CLAMP_STS register.

The MICDET Clamp de-bounce is selected using the MICD_CLAMP_DB register, as described in Table 66. Note that the de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required.

An Interrupt Request (IRQ) event is generated whenever the MICDET Clamp is asserted or de-asserted (see "Interrupts"). Separate 'mask' bits are provided to enable IRQ events on the rising and/or falling edge of the MICDET Clamp status.

The Control Write Sequencer can be triggered by the MICDET Clamp status. This is enabled using register bits described in the "Low Power Sleep Configuration" section.

The MICDET Clamp function is illustrated in Figure 58. Note that the jack plug is shown partially removed, with the MICDET1 pin in contact with the headphone load.

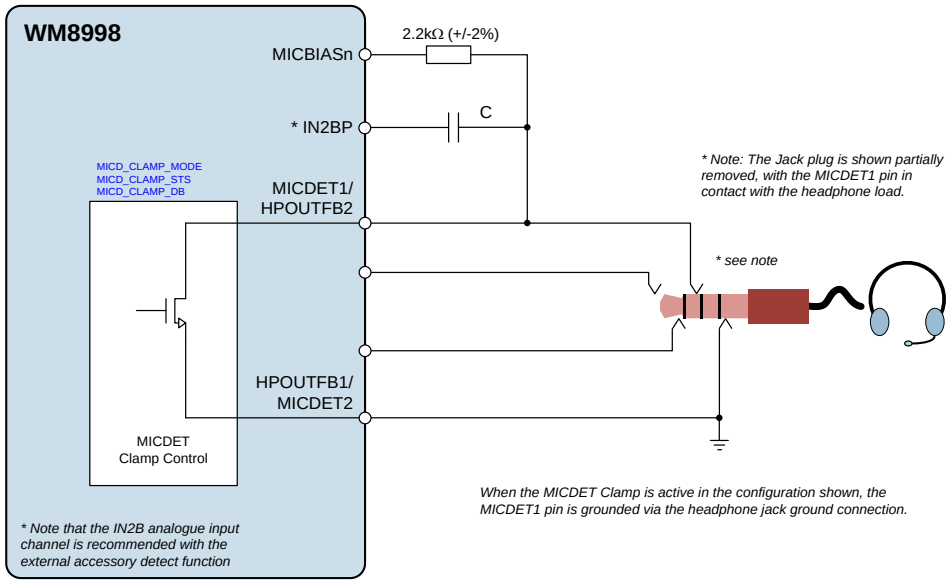


Figure 58 MICDET Clamp circuit

In applications where a large de-coupling capacitance is present on the MICBIAS output, the MICDET Clamp function alone may be unable to discharge the capacitor sufficiently to eliminate pops and clicks associated with jack insertion and removal. In this case, it may be desirable to use the General Purpose Switch within the WM8998 to provide isolation from the MICBIAS output; an example circuit is shown in Figure 59.

The General Purpose Switch is configured using SW1_MODE. This register allows the switch to be disabled, enabled, or synchronised to the MICDET Clamp status, as described in Table 66.

For jack pop suppression, it is recommended to set SW1_MODE=11. In this case, the switch contacts are open whenever the MICDET Clamp is active, and the switch contacts are closed whenever the MICDET Clamp is inactive.

Normal accessory functions are supported when the switch contacts (GPSWP and GPSWN) are closed, and the MICDET Clamp is inactive. Ground clamping of MICDET, and isolation of MICBIAS are achieved when the switch contacts are open, and the MICDET Clamp is active.

Note that the MICDET Clamp function must also be configured appropriately when using this method of pop suppression control.

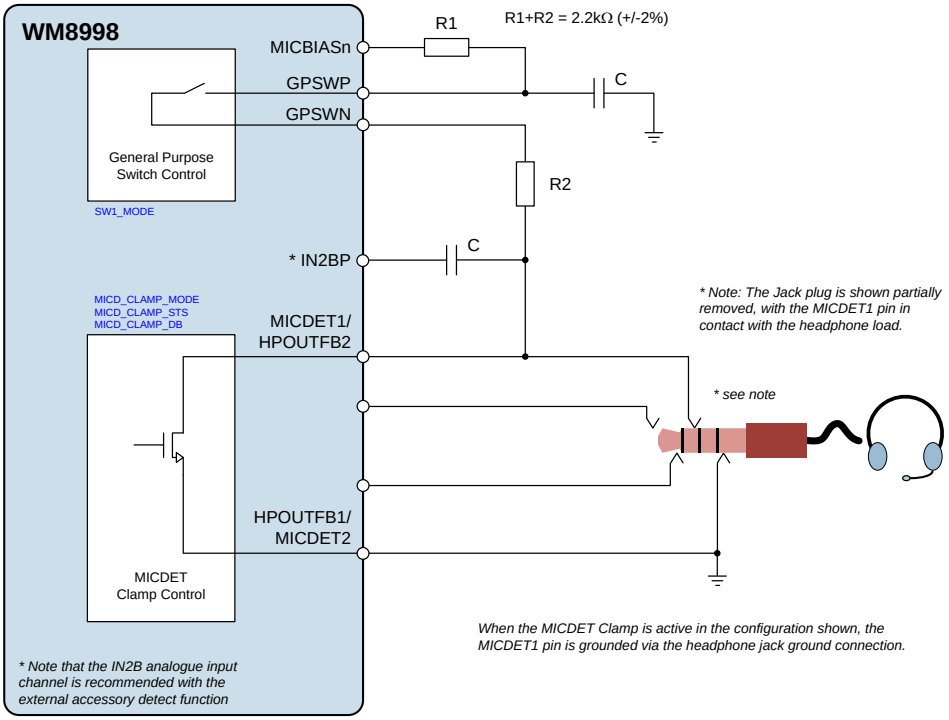


Figure 59 General Purpose Switch Circuit

The control registers associated with the MICDET Clamp and General Purpose Switch functions are described in Table 66.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R674 (02A2h) Micd Clamp control	3:0	MICD_CLAMP_MODE [3:0]	0000	MICDET Clamp Mode 0h = Disabled 1h = Active (MICDET1 and MICDET2 are shorted together) 2h = Reserved 3h = Reserved 4h = Active when JD1=0 5h = Active when JD1=1 6h = Active when GP5=0 7h = Active when GP5=1 8h = Active when JD1=0 or GP5=0 9h = Active when JD1=0 or GP5=1 Ah = Active when JD1=1 or GP5=0 Bh = Active when JD1=1 or GP5=1 Ch = Active when JD1=0 and GP5=0 Dh = Active when JD1=0 and GP5=1 Eh = Active when JD1=1 and GP5=0 Fh = Active when JD1=1 and GP5=1
R3096 (0C18h) GP Switch 1	1:0	SW1_MODE [1:0]	00	General Purpose Switch control 00 = Disabled (open) 01 = Enabled (closed) 10 = Enabled when MICDET Clamp is active 11 = Enabled when MICDET Clamp is not active
R3413 (0D55h) AOD IRQ Raw Status	3	MICD_CLAMP_STS	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active
R3414 (0D56h) Jack detect debounce	3	MICD_CLAMP_DB	0	MICDET Clamp de-bounce 0 = Disabled 1 = Enabled

Table 66 MICDET Clamp and General Purpose Switch Control

MICROPHONE DETECT

The WM8998 microphone detection circuit measures the impedance of an external load connected to one of the MICDET pins. This feature can be used to detect the presence of a microphone, and the status of the associated hookswitch. It can also be used to detect push-button status or the connection of other external accessories.

The microphone detection circuit measures the impedance connected to MICDET1 or MICDET2. In the discrete measurement mode (ACCDET_MODE=000), the function reports whether the measured impedance lies within one of 8 pre-defined levels. In the ADC measurement mode (ACCDET_MODE=111), a more specific result is provided in the form of a 7-bit ADC output.

The microphone detection circuit typically uses one of the MICBIAS outputs as a reference. The WM8998 will automatically enable the appropriate MICBIAS when required in order to perform the detection function; this allows the detection function to be supported in low-power standby operating conditions.

Note that the MICVDD power domain must be enabled when using the microphone detection function. This power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See “Charge Pumps, Regulators and Voltage Reference” for details of these circuits.

To select microphone detection on one of the MICDET pins, the ACCDET_MODE register must be set to 000 or 111 (depending on the desired measurement mode). The ACCDET_MODE register is defined in Table 67.

The WM8998 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET_MODE=000.

The microphone detection circuit can be enabled on the MICDET1 pin or the MICDET2 pin, selected by the ACCDET_SRC register.

The microphone detection circuit uses MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 as a reference. The applicable source is configured using the MICD_BIAS_SRC register.

When ACCDET_MODE is set to 000 or 111, then Microphone detection is enabled by setting MICD_ENA.

When microphone detection is enabled, the WM8998 performs a number of measurements in order to determine the MICDET impedance. The measurement process is repeated at a cyclic rate controlled by MICD_RATE. (The MICD_RATE register selects the delay between completion of one measurement and the start of the next.) When the microphone detection result has settled, the WM8998 indicates valid data by setting the MICD_VALID bit.

When the discrete measurement mode is selected (ACCDET_MODE=000), the measured impedance is only deemed valid after more than one successive measurement has produced the same result. The MICD_DBTIME register provides control of the de-bounce period; this can be either 2 measurements or 4 measurements.

When the microphone detection result has settled (ie. after the applicable de-bounce period), the WM8998 indicates valid data by setting the MICD_VALID bit. The measured impedance is indicated using the MICD_LVL and MICD_STS register bits, as described in Table 67.

The MICD_VALID bit, when set, remains asserted for as long as the microphone detection function is enabled (ie. while MICD_ENA = 1). If the detected impedance changes, then the MICD_LVL and MICD_STS fields will change, but the MICD_VALID bit will remain set, indicating valid data at all times.

The 8 pre-defined impedance levels (including the ‘no accessory detected’ level) allow detection of a typical microphone and up to 6 push-buttons. Each measurement level can be enabled or disabled independently; this provides flexibility according to the required thresholds, and offers a faster measurement time in some applications. The MICD_LVL_SEL register is described in detail later in this section.

Note that the impedance levels quoted in the MICD_LVL description assume that a microphone (475Ω to 30kΩ impedance) is also present on the MICDET pin. The limits quoted in the “Electrical Characteristics” refer to the combined effective impedance on the MICDET pin. Typical external components are described in the “Applications Information” section.

When the ADC measurement mode is selected (ACCDET_MODE=111), the detection function must be disabled before the measurement can be read. When the WM8998 indicates valid data (MICD_VALID=1), the detection must be disabled by setting MICD_ENA=0.

The ADC measurement mode generates two output results, contained within the MICDET_ADCVAL and MICDET_ADCVAL_DIFF registers. These registers contain the most recent measurement value (MICDET_ADCVAL) and the measurement difference value (MICDET_ADCVAL_DIFF). The difference value indicates the difference between the latest measurement and the previous measurement; this can be used to determine whether the measurement is stable and reliable.

Note that the MICDET_ADCVAL and MICDET_ADCVAL_DIFF registers do not follow a linear coding. The appropriate test condition for accepting the measurement value (or for re-scheduling the measurement) will vary depending on the application requirements, and depending on the expected impedance value.

The microphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event every time an accessory insertion, removal or impedance change is detected. See “Interrupts” for further details.

The microphone detection function can also generate a GPIO output, providing an external indication of the microphone detection. This GPIO output is pulsed every time an accessory insertion, removal or impedance change is detected. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The register fields associated with Microphone Detection (or other accessories) are described in

Table 67. The external circuit configuration is illustrated in Figure 60.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R659 (0293h) Accessory Detect Mode 1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUTFB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUTFB2
	2:0	ACCDET_MODE [2:0]	00	Accessory Detect Mode Select 000 = Microphone detect (MICDETn, discrete mode) 001 = Headphone detect (HPDETL) 010 = Headphone detect (HPDETR) 011 = Reserved 100 = Headphone detect (MICDETn) 101 = Reserved 110 = Reserved 111 = Microphone detect (MICDETn, ADC mode) Note that the MICDETn measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC register bit.
R675 (02A3h) Mic Detect 1	15:12	MICD_BIAS_STARTTIME [3:0]	0001	Mic Detect Bias Startup Delay (If MICBIAS is not enabled already, this field selects the delay time allowed for MICBIAS to startup prior to performing the MICDET function.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms
	11:8	MICD_RATE [3:0]	0001	Mic Detect Rate (Selects the delay between successive MICDET measurements.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:4	MICD_BIAS_SRC [1:0]	00	Accessory Detect (MICDET) reference select 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	1	MICD_DBTIME	1	Mic Detect De-bounce 0 = 2 measurements 1 = 4 measurements Only valid when ACCDET_MODE=000.
	0	MICD_ENA	0	Mic Detect Enable 0 = Disabled 1 = Enabled
R676 (02A4h) Mic Detect 2	7:0	MICD_LVL_SEL [7:0]	1001_1111	Mic Detect Level Select (enables Mic/Accessory Detection in specific impedance ranges) [7] = Enable >475 ohm detection [6] = Not used - must be set to 0 [5] = Not used - must be set to 0 [4] = Enable 375 ohm detection [3] = Enable 155 ohm detection [2] = Enable 73 ohm detection [1] = Enable 40 ohm detection [0] = Enable 18 ohm detection Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin. Only valid when ACCDET_MODE=000.
R677 (02A5h) Mic Detect 3	10:2	MICD_LVL [8:0]	0_0000_0000	Mic Detect Level (indicates the measured impedance) [8] = >475 ohm, <30k ohm [7] = Not used [6] = Not used [5] = 375 ohm [4] = 155 ohm [3] = 73 ohm [2] = 40 ohm [1] = 18 ohm [0] = <3 ohm Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin. Only valid when ACCDET_MODE=000.
	1	MICD_VALID	0	Mic Detect Data Valid 0 = Not Valid 1 = Valid
	0	MICD_STS	0	Mic Detect Status 0 = No Mic/Accessory present (impedance is >30k ohm) 1 = Mic/Accessory is present (impedance is <30k ohm) Only valid when ACCDET_MODE=000.
R683 02ABh Mic Detect 4	15:8	MICDET_ADCVAL_DIFF [7:0]	00h	Mic Detect ADC Level (Difference) Only valid when ACCDET_MODE=111.
	6:0	MICDET_ADCVAL [6:0]	00h	Mic Detect ADC Level Only valid when ACCDET_MODE=111.

Table 67 Microphone Detect Control

The external connections for the Microphone Detect circuit are illustrated in Figure 60. In typical applications, it can be used to detect a microphone or button press.

Note that, when using the Microphone Detect circuit, it is recommended to use one of the Right channel analogue microphone input paths, to ensure best immunity to electrical transients arising from the external accessory.

The voltage reference for the microphone detection is configured using the MICD_BIAS_SRC register, as described in Table 67. The microphone detection function will automatically enable the applicable reference when required for MICDET impedance measurement.

If the selected reference (MICBIAS1, MICBIAS2 or MICBIAS3) is not already enabled (ie. if MICB*n*_ENA = 0, where *n* is 1, 2 or 3 as appropriate), then the applicable MICBIAS source will be enabled for short periods of time only, every time the impedance measurement is scheduled. To allow time for the MICBIAS source to start-up, a time delay is applied before the measurement is performed; this is configured using the MICD_BIAS_STARTTIME register, as described in Table 67.

The MICD_BIAS_STARTTIME register should be set to 16ms or more if MICB*n*_RATE = 1 (pop-free start-up / shut-down). The MICD_BIAS_STARTTIME register should be set to 0.25ms or more if MICB*n*_RATE = 0 (fast start-up / shut-down).

If the selected reference is not enabled continuously (ie. if MICB*n*_ENA = 0), then the applicable MICBIAS discharge bit (MICB*n*_DISCH) should be set to 0.

The MICBIAS sources are configured using the registers described in the “Charge Pumps, Regulators and Voltage Reference” section.

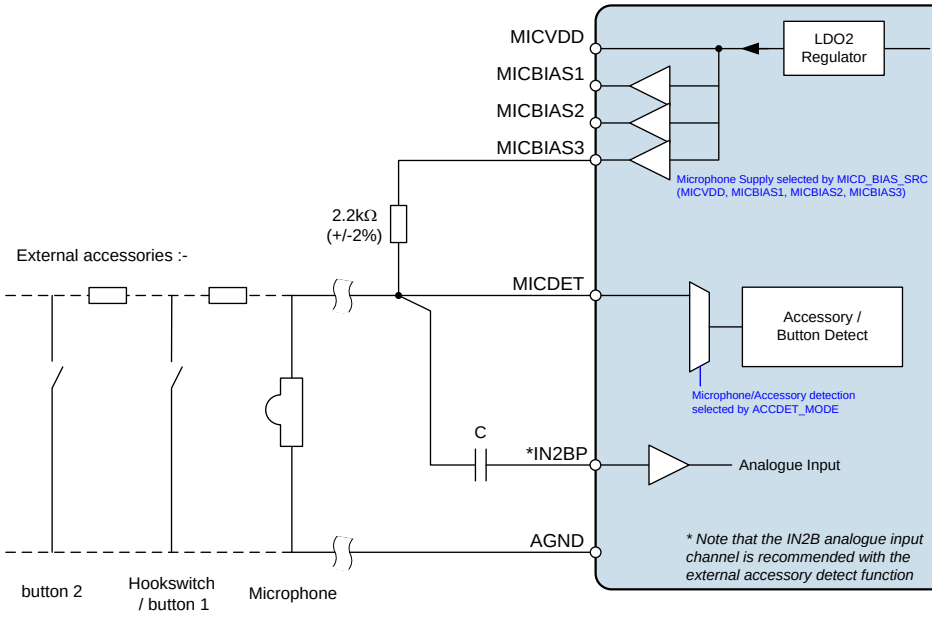


Figure 60 Microphone and Accessory Detect Interface

When the discrete measurement mode is selected (ACCDET_MODE=000), the MICD_LVL_SEL [7:0] register bits allow each of the impedance measurement levels to be enabled or disabled independently. This allows the function to be tailored to the particular application requirements.

If one or more bits within the MICD_LVL_SEL register is set to 0, then the corresponding impedance level will be disabled. Any measured impedance which lies in a disabled level will be reported as the next lowest, enabled level.

For example, the MICD_LVL_SEL [2] bit enables the detection of impedances around 73Ω. If MICD_LVL_SEL [2] = 0, then an external impedance of 73Ω will not be indicated as 73Ω but will be indicated as 40Ω; this would be reported in the MICD_LVL register as MICD_LVL [2] = 1.

With all measurement levels enabled, the WM8998 can detect the presence of a typical microphone and up to 6 push-buttons. The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required.

See “Applications Information” for typical recommended external components for microphone, video

or push-button accessory detection.

The accuracy of the microphone detect function is assured whenever the connected load is within the applicable limits specified in the “Electrical Characteristics”. It is required that a 2.2kΩ (2%) resistor must also be connected between MICDET and the selected MICBIAS reference; note that different resistor values will lead to inaccuracy in the impedance measurement.

Note that the connection of a microphone will change the measured impedance on the MICDET pin; see “Applications Information” for recommended components for typical applications.

The measurement time varies between 100µs and 500µs, depending on the impedance of the external load. A high impedance will be measured faster than a low impedance.

The timing of the microphone detect function is illustrated in Figure 61. Two different cases are shown, according to whether MICBIAS*n* is enabled periodically by the impedance measurement function (MICB*n*_ENA=0), or is enabled at all times (MICB*n*_ENA=1).

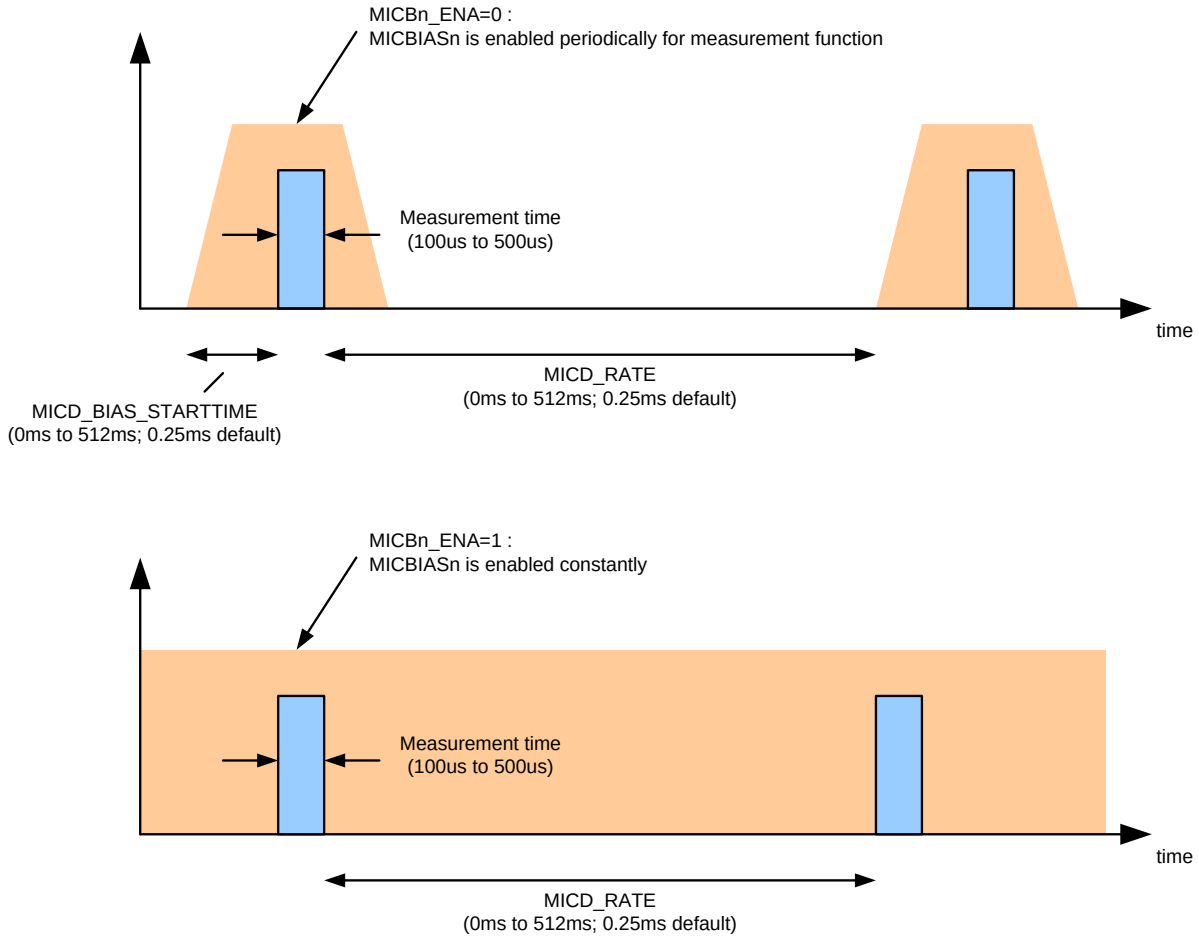


Figure 61 Microphone and Accessory Detect Timing

HEADPHONE DETECT

The WM8998 headphone detection circuit measures the impedance of an external headphone load. This feature can be used to set different gain levels or to apply other configuration settings according to the type of load connected. Separate monitor pins are provided for headphone detection on the left and right channels of HPOUT.

Headphone detection can be enabled on the HPDETL pin or the HPDETR pin. Under recommended configuration, these pins provide measurement of the HPOUTL and HPOUTR loads respectively.

The headphone detect function can also be enabled on the MICDET1 pin or the MICDET2 pin. Note that, in this configuration, any MICBIAS output that is connected to the selected MICDET pin must be disabled and floating (MICBn_ENA=0, MICBn_DISCH=0).

The applicable headphone detection pin is selected using the ACCDET_MODE register. When MICDETn is selected (ACCDET_MODE=100), the applicable MICDETn pin is determined by the ACCDET_SRC register, as described in Table 69.

The WM8998 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET_MODE=000.

The impedance measurement range is configured using the HP_IMPEDANCE_RANGE register. This register should be set in accordance with the expected load impedance.

Note that setting the HP_IMPEDANCE_RANGE register is not required for detection on the MICDETn pins (ACCDET_MODE=100). Note also that the impedance measurement range in this mode is different to the HPDETL and HPDETR measurement modes.

Headphone detection on the selected channel is commanded by writing a '1' to the HP_POLL register bit.

For correct operation, the respective output driver(s) must be disabled when headphone detection is commanded on HPOUTL or HPOUTR. The required register settings are shown in Table 68.

See Table 52 for details of the HPL_ENA and HPR_ENA register bits. The applicable headphone output(s) must not be enabled until after the headphone detection has completed.

DESCRIPTION	REQUIREMENT
HPOUTL Impedance measurement	HPL_ENA = 0
HPOUTR Impedance measurement	HPR_ENA = 0

Table 68 Output Configuration for Headphone Detect

When headphone detection is commanded, the WM8998 uses an adjustable current source to determine the connected impedance. A sweep of measurement currents is applied. The rate of this sweep can be adjusted using the HP_CLK_DIV register.

The timing of the current source ramp is also controlled by the HP_HOLDTIME register. It is recommended that the default setting (000b) be used for this parameter.

Completion of the headphone detection is indicated by the HP_DONE register bit. When this bit is set, the measured load impedance can be read from the HP_LVL register. Note that, after the HP_DONE bit has been asserted, it will remain asserted until a subsequent headphone detection measurement is commanded.

The headphone detection result (HP_LVL) is restricted to values that are close to the range defined by the HP_IMPEDANCE_RANGE register. If the HP_LVL register reports an impedance that is outside the selected range, then it is recommended to adjust the HP_IMPEDANCE_RANGE value and repeat the measurement. For minimum measurement time, the lowest impedance range (HP_IMPEDANCE_RANGE=00) should be selected in the first instance.

The headphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event on completion of the headphone detection - see "Interrupts".

The headphone detection function can also generate a GPIO output, providing an external indication of the headphone detection. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The register fields associated with Headphone Detection are described in Table 69. The external circuit configuration is illustrated in Figure 62.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R659 (0293h) Accessory Detect Mode 1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUTFB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUTFB2
	2:0	ACCDET_MODE [2:0]	00	Accessory Detect Mode Select 000 = Microphone detect (MICDETn, discrete mode) 001 = Headphone detect (HPDETL) 010 = Headphone detect (HPDETR) 011 = Reserved 100 = Headphone detect (MICDETn) 101 = Reserved 110 = Reserved 111 = Microphone detect (MICDETn, ADC mode) Note that the MICDETn measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC register bit.
R667 (029Bh) Headphone Detect 1	10:9	HP_IMPEDANCE _RANGE [1:0]	00	Headphone Detect Range 00 = 4 ohms to 30 ohms 01 = 8 ohms to 100 ohms 10 = 100 ohms to 1k ohms 11 = 1k ohms to 10k ohms Only valid when ACCDET_MODE=001 or ACCDET_MODE=010.
	7:5	HP_HOLDTIME [2:0]	000	Headphone Detect Hold Time (Selects the hold time between ramp up and ramp down of the headphone detect current source. The clock cycle rate is set by HP_CLK_DIV.) 000 = 1 clock cycle 001 = 4 clock cycles 010 = 16 clock cycles 011 = 64 clock cycles 100 = 256 clock cycles 101 = 512 clock cycles 110 = 768 clock cycles 111 =1024 clock cycles
	4:3	HP_CLK_DIV [1:0]	00	Headphone Detect Clock Rate (Selects the clocking rate of the headphone detect adjustable current source.) 00 = 32kHz 01 = 16kHz 10 = 8kHz 11 = 4kHz
	0	HP_POLL	0	Headphone Detect Enable Write 1 to start HP Detect function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R668 (029Ch) Headphone Detect 2	15	HP_DONE	0	Headphone Detect Status 0 = HP Detect not complete 1 = HP Detect done
	14:0	HP_LVL [14:0]	0000h	Headphone Detect Level LSB = 0.5ohm 8 = 4ohm or less 9 = 4.5 ohm 10 = 5 ohm 11 = 5.5 ohm …. 20,000 = 10k ohm or more When ACCDET_MODE=001 or 010, this field is valid from 4ohm to10k ohm. When ACCDET_MODE=100, this field is valid from 400ohm to 6k ohm. Note that, when ACCDET_MODE=001 or 010, the HP_LVL readback is only valid within the range selected by HP_IMPEDANCE_RANGE. If HP_LVL reports a value outside the selected range, then the range should be adjusted and the measurement repeated. A result of 0 ohms may be reported if the measurement is less than the minimum value for the selected range.

Table 69 Headphone Detect Control

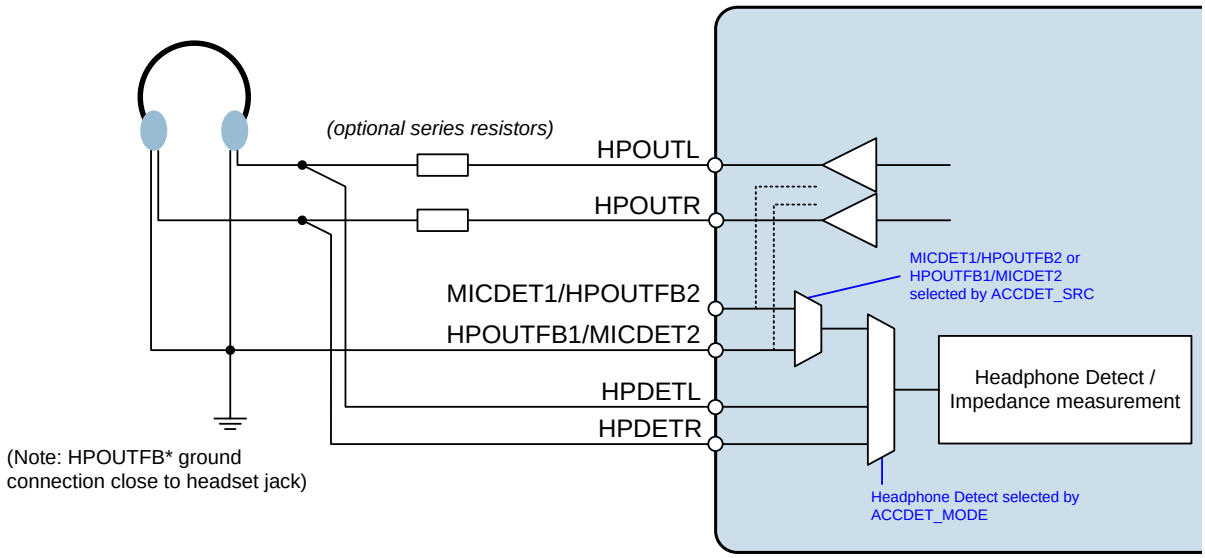


Figure 62 Headphone Detect Interface

The external connections for the Headphone Detect circuit are illustrated in Figure 62. Note that only the HPOUTL or HPOUTR headphone outputs should be connected to HPDETL or HPDETR pins - impedance measurement is not supported on LINEOUTL, LINEOUTR, EPOUTP or EPOUTN.

Note that, where external resistors are connected in series with the headphone load, as illustrated, it is recommended that the HPDET*x* connection is to the headphone side of the resistors. If the HPDET*x* connection is made to the WM8998 'end' of these resistors, this will lead to a corresponding offset in the measured impedance.

Note that the measurement accuracy of the headphone detect function may be up to +/-20%.

Under default conditions, the measurement time varies between 17ms and 244ms, depending on the impedance of the external load. A high impedance will be measured faster than a low impedance.

LOW POWER SLEEP CONFIGURATION

The WM8998 supports a low-power 'Sleep' mode, where most functions are disabled, and power consumption is minimised. A selectable 'Wake-Up' event can be configured to return the device to full operation and/or execute a specific response to the particular Wake-Up condition.

A Wake-Up event is triggered via hardware input pin(s); in typical applications, these inputs are associated with jack insert (via the JACKDET analogue input) or external push-button detection (via the GPIO5 digital input). A Wake-Up transition can also be triggered using the LDOENA pin to enable LDO1 (assuming that DCVDD is supplied by LDO1).

The WM8998 enters Sleep mode when LDO1 is disabled, causing the DCVDD supply to be removed. The AVDD, DBVDD1, and LDOVDD supplies must be present throughout the Sleep mode duration.

Note that it is assumed that DCVDD is supplied by LDO1; see the "Charge Pumps, Regulators and Voltage Reference" for specific control requirements where DCVDD is not powered from LDO1.

SLEEP MODE

The WM8998 enters Sleep mode when LDO1 is disabled, causing the DCVDD supply to be removed. (LDO1 can be controlled using the LDO1_ENA register bit, or using the LDOENA pin; both of these controls must be de-asserted to disable the LDO.) The AVDD, DBVDD1, and LDOVDD supplies must be present throughout the Sleep mode; under these conditions, and with LDO1 disabled, most of the Digital Core (and control registers) are held in reset.

Note that it is assumed that DCVDD is supplied by LDO1; see the "Charge Pumps, Regulators and Voltage Reference" for specific control requirements where DCVDD is not powered from LDO1.

The system clocks (SYSCLK, ASYNCCLK) are not required in Sleep mode, and the external clock inputs (MCLKn) may be stopped, except as described below.

If de-bounce is enabled on any of the configured Wake-Up signals (JACKDET or GPIO5), then the 32kHz clock must be active during Sleep mode (see "Clocking and Sample Rates"). The 32kHz clock must be derived from the MCLK2 pin in this case. The 32kHz clock must be configured using CLK_32K_ENA and CLK_32K_SRC before Sleep mode is entered.

The MCLK2 frequency limit in Sleep mode (see "Signal Timing Requirements") must be observed before entering Sleep mode, and maintained until after Wake-Up.

Selected functions and control registers are maintained via an 'Always-On' internal supply domain in Sleep mode. The 'Always-On' control registers are listed in Table 70. These registers are maintained (ie. not reset) in Sleep mode.

Note that the Control Interface is not supported in Sleep mode. Read/Write access to the 'Always-On' registers is not possible in Sleep mode.

REGISTER ADDRESS	LABEL	REFERENCE
40h	WKUP_MICD_CLAMP_FALL	See Table 73
	WKUP_MICD_CLAMP_RISE	
	WKUP_GP5_FALL	
	WKUP_GP5_RISE	
	WKUP_JD1_FALL	
	WKUP_JD1_RISE	
41h	WSEQ_ENA_MICD_CLAMP_FALL	See Table 74
	WSEQ_ENA_MICD_CLAMP_RISE	
	WSEQ_ENA_GP5_FALL	
	WSEQ_ENA_GP5_RISE	
	WSEQ_ENA_JD1_FALL	
	WSEQ_ENA_JD1_RISE	
66h	WSEQ_MICD_CLAMP_RISE_INDEX	See “Control Write Sequencer”
67h	WSEQ_MICD_CLAMP_FALL_INDEX	
68h	WSEQ_GP5_RISE_INDEX	
69h	WSEQ_GP5_FALL_INDEX	
6Ah	WSEQ_JD1_RISE_INDEX	
6Bh	WSEQ_JD1_FALL_INDEX	
100h	CLK_32K_ENA	See “Clocking and Sample Rates”
	CLK_32K_SRC	
210h	LDO1_VSEL	See “Charge Pumps, Regulators and Voltage Reference”
	LDO1_DISCH	
	LDO1_BYPASS	
	LDO1_ENA	
02A2h	MICD_CLAMP_MODE	See “External Accessory Detection”
02D3h	JD1_ENA	See “External Accessory Detection”
0C04h	GP5_DIR	See “General Purpose Input / Output”
	GP5_PU	
	GP5_PD	
	GP5_POL	
	GP5_OP_CFG	
	GP5_DB	
	GP5_LVL	
	GP5_FN	
0C0Fh	IRQ_POL	See “Interrupts”
	IRQ_OP_CFG	
0C10h	GP_DBTIME	See “General Purpose Input / Output”
0C18h	SW1_MODE	
0C20h	LDO1ENA_PD	See “Charge Pumps, Regulators and Voltage Reference”
	LDO1ENA_PU	
	MCLK2_PD	See “Clocking and Sample Rates”
	RESET_PU	See “Hardware Reset, Software Reset, Wake-Up, and Device ID”
	RESET_PD	
0D0Fh	IM_IRQ1	See “Interrupts”
0D1Fh	IM_IRQ2	
0D50h	MICD_CLAMP_FALL_TRIG_STS	See Table 72
	MICD_CLAMP_RISE_TRIG_STS	
	GP5_FALL_TRIG_STS	

REGISTER ADDRESS	LABEL	REFERENCE
	GP5_RISE_TRIG_STS	
	JD1_FALL_TRIG_STS	
	JD1_RISE_TRIG_STS	
0D51h	MICD_CLAMP_FALL_EINT1	See “Interrupts”
	MICD_CLAMP_RISE_EINT1	
	GP5_FALL_EINT1	
	GP5_RISE_EINT1	
	JD1_FALL_EINT1	
	JD1_RISE_EINT1	
0D52h	MICD_CLAMP_FALL_EINT2	See “Interrupts”
	MICD_CLAMP_RISE_EINT2	
	GP5_FALL_EINT2	
	GP5_RISE_EINT2	
	JD1_FALL_EINT2	
	JD1_RISE_EINT2	
0D53h	IM_MICD_CLAMP_FALL_EINT1	See “Interrupts”
	IM_MICD_CLAMP_RISE_EINT1	
	IM_GP5_FALL_EINT1	
	IM_GP5_RISE_EINT1	
	IM_JD1_FALL_EINT1	
	IM_JD1_RISE_EINT1	
0D54h	IM_MICD_CLAMP_FALL_EINT2	See “Interrupts”
	IM_MICD_CLAMP_RISE_EINT2	
	IM_GP5_FALL_EINT2	
	IM_GP5_RISE_EINT2	
	IM_JD1_FALL_EINT2	
	IM_JD1_RISE_EINT2	
0D56h	MICD_CLAMP_DB	See “External Accessory Detection”
	JD1_DB	
3000h to 31FFh	WSEQ_DATA_WIDTHn	See “Control Write Sequencer”
	WSEQ_ADDRn	
	WSEQ_DELAYn	
	WSEQ_DATA_STARTn	
	WSEQ_DATAn	

Table 70 Sleep Mode ‘Always-On’ Control Registers

The ‘Always-On’ digital input / output pins are listed in Table 71. All other digital input pins will have no effect in Sleep mode. The $\overline{\text{IRQ}}$ output is normally de-asserted in Sleep mode.

Note that, in Sleep mode, the $\overline{\text{IRQ}}$ output can only be asserted in response to the JD1 or GP5 control signals (these described in the following section). If the $\overline{\text{IRQ}}$ output is asserted in Sleep mode, it can only be de-asserted after a Wake-Up transition.

PIN NAME	DESCRIPTION	REFERENCE
LDOENA	Enable pin for LDO1	See “Charge Pumps, Regulators and Voltage Reference”
$\overline{\text{RESET}}$	Digital Reset input (active low)	See “Hardware Reset, Software Reset, Wake-Up, and Device ID”
MCLK2	Master clock 2	See “Clocking and Sample Rates”
GPIO5	General Purpose pin GPIO5	See “General Purpose Input / Output”
$\overline{\text{IRQ}}$	Interrupt Request (IRQ) output	See “Interrupts”

Table 71 Sleep Mode ‘Always-On’ Digital Input Pins

A Wake-Up transition is triggered using the JD1 or GP5 control signals (defined below).

It is assumed that DCVDD is supplied by LDO1. The AVDD, DBVDD1 and LDOVDD supplies must be present throughout the Sleep mode duration. See "Charge Pumps, Regulators and Voltage Reference" for specific control requirements where DCVDD is not powered from LDO1.

Note that a logic '1' applied to the LDOENA pin will also cause a Wake-Up transition. In this event, however, the configurable Wake-Up events (described below) are not applicable.

SLEEP CONTROL SIGNALS - JD1, GP5, MICDET CLAMP

The internal control signals JD1 and GP5 are provided to support the low-power Sleep mode. The MICDET Clamp status is controlled by a selectable logic function, derived from JD1 and/or GP5. A rising or falling edge of these signals can be used to trigger a Wake-Up transition (ie. exit from Sleep mode).

The JD1, GP5 and MICDET Clamp status signals can also be used to trigger the Control Write Sequencer and/or the Interrupt Controller.

Note that it is possible to enable more than one response from these control signals. For example, a particular edge transition could trigger a Wake-Up transition, and also a Control Write Sequence.

The JD1, GP5 and MICDET Clamp status signals are described in this section. The Wake-Up, Write Sequencer, and Interrupt actions are described in the sections that follow.

The JD1 signal is derived from the Jack Detect function (see "External Accessory Detection"). This input can be used to trigger Wake-Up or other actions in response to a jack insertion or jack removal detection.

When the JD1 signal is enabled, it indicates the status of the JACKDET input pin. See Table 65 for details of the associated control registers.

The GP5 signal is derived from the GPIO5 input pin (see "General Purpose Input / Output"). This input can be used to trigger Wake-Up or other actions in response to a logic level input detected on the GPIO5 pin.

When using the GP5 signal, the GPIO5 pin must be configured as a GPIO input (GP5_DIR=1, GP5_FN=01h). An internal pull-up or pull-down resistor may be enabled on the GPIO5 pin if required.

The GPIO pin control registers are defined in Table 75.

The MICDET Clamp status is controlled by the JD1 and/or GP5 signals (see "External Accessory Detection"). The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET Clamp. The clamp status can be used to trigger Wake-Up or other actions in response to a jack insertion or jack removal detection.

The MICDET Clamp function is configured using the MICD_CLAMP_MODE register, as described in Table 66.

Whenever a rising or falling edge is detected on JD1, GP5 or MICDET Clamp status, the WM8998 will assert the respective trigger status (_TRIG_STS) bit. The trigger status bits are latching fields and, once they are set, they are not reset until a '1' is written to the respective register bit(s).

The JD1, GP5 and MICDET Clamp trigger status bits are described in Table 72.

The trigger status bits can be used to control Wake-Up and Write Sequencer actions. The JD1, GP5 and MICDET Clamp signals are inputs to the Interrupt Controller. Each of these functions is described in the following sections.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3408 (0D50h) AOD wkup and trig	7	MICD_CLAMP_FALL_TRIG_STS	0	MICDET Clamp Trigger Status (Falling edge triggered) Note: Cleared when a '1' is written
	6	MICD_CLAMP_RISE_TRIG_STS	0	MICDET Clamp Trigger Status (Rising edge triggered) Note: Cleared when a '1' is written
	5	GP5_FALL_TRIG_STS	0	GP5 Trigger Status (Falling edge triggered) Note: Cleared when a '1' is written
	4	GP5_RISE_TRIG_STS	0	GP5 Trigger Status (Rising edge triggered) Note: Cleared when a '1' is written
	3	JD1_FALL_TRIG_STS	0	JD1 Trigger Status (Falling edge triggered) Note: Cleared when a '1' is written
	2	JD1_RISE_TRIG_STS	0	JD1 Trigger Status (Rising edge triggered) Note: Cleared when a '1' is written

Table 72 JD1, GP5 and MICDET Clamp Trigger Status Registers

Note that the de-bounce function on all inputs (including JD1, GP5 and MICDET Clamp status) use the 32kHz clock (see "Clocking and Sample Rates"). The 32kHz clock must be enabled whenever input de-bounce functions are required.

Note that the MCLK2 input pin is on the 'Always-On' domain, and is supported in Sleep mode. (MCLK1 input is not supported in Sleep mode.)

If input de-bounce is enabled in Sleep mode, the 32kHz clock must use MCLK2 (direct) input as its source (CLK_32K_SRC = 01).

WAKE-UP TRANSITION

A Wake-Up transition (exit from Sleep) can be associated with any of the JD1, GP5 or MICDET Clamp trigger status bits. This is selected using the register bits described in Table 73.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R64 (0040h) Wake Control	7	WKUP_MICD_CLAMP_FALL	0	MICDET Clamp (Falling) Wake-Up Select 0 = Disabled 1 = Enabled
	6	WKUP_MICD_CLAMP_RISE	0	MICDET Clamp (Rising) Wake-Up Select 0 = Disabled 1 = Enabled
	5	WKUP_GP5_FALL	0	GP5 (Falling) Wake-Up Select 0 = Disabled 1 = Enabled
	4	WKUP_GP5_RISE	0	GP5 (Rising) Wake-Up Select 0 = Disabled 1 = Enabled
	3	WKUP_JD1_FALL	0	JD1 (Falling) Wake-Up Select 0 = Disabled 1 = Enabled
	2	WKUP_JD1_RISE	0	JD1 (Rising) Wake-Up Select 0 = Disabled 1 = Enabled

Table 73 JD1, GP5 and MICDET Clamp Wake-Up Control Registers

When a valid 'Wake-Up' event is detected, the WM8998 will enable LDO1 (and DCVDD), and a user-configurable Boot Sequence is executed (see "Hardware Reset, Software Reset, Wake-Up, and Device ID").

Note that the trigger status (_TRIG_STS) bits are latching fields. Care is required when resetting these bits, to ensure the intended device behaviour - resetting the _TRIG_STS register(s) may cause LDO1 (and DCVDD) to be disabled.

For normal device operation following a 'Wake-Up' transition, the LDO1_ENA register must be set (or the LDOENA pin asserted) before the _TRIG_STS bit(s) are reset. (Note that further options are described in the next section.)

For recommended use of the Sleep / Wake-Up functions, it is assumed that DCVDD is powered from the output of LDO1 (see "Charge Pumps, Regulators and Voltage Reference").

If DCVDD is powered externally (not from LDO1), then the JD1, GP5 and MICDET Clamp inputs cannot trigger a Wake-Up transition directly; a Wake-Up transition will only occur by re-application of DCVDD. In this configuration, the JD1, GP5 or MICDET Clamp inputs can provide a signal to the host processor, via the $\overline{IRQ}$ output; if a Wake-Up transition is required, this can be implemented by the host processor controlling the DCVDD supply.

If DCVDD is powered externally, then the WKUP_* control bits described in Table 73 must be held at 0 at all times.

WRITE SEQUENCE CONTROL

A Control Write Sequence can be associated with any of the JD1, GP5 or MICDET Clamp trigger status bits. This is selected using the register bits described in Table 74.

Note that the JD1, GP5 and MICDET Clamp trigger status bits can be used to trigger the Control Write Sequencer at any time. This feature may be used during normal operation, or immediately following a Wake-Up transition.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (0041h) Sequence Control	7	WSEQ_ENA_MICD_CLAMP_FALL	0	MICDET Clamp (Falling) Write Sequencer Select 0 = Disabled 1 = Enabled
	6	WSEQ_ENA_MICD_CLAMP_RISE	0	MICDET Clamp (Rising) Write Sequencer Select 0 = Disabled 1 = Enabled
	5	WSEQ_ENA_GP5_FALL	0	GP5 (Falling) Write Sequencer Select 0 = Disabled 1 = Enabled
	4	WSEQ_ENA_GP5_RISE	0	GP5 (Rising) Write Sequencer Select 0 = Disabled 1 = Enabled
	3	WSEQ_ENA_JD1_FALL	0	JD1 (Falling) Write Sequencer Select 0 = Disabled 1 = Enabled
	2	WSEQ_ENA_JD1_RISE	0	JD1 (Rising) Write Sequencer Select 0 = Disabled 1 = Enabled

Table 74 JD1, GP5 and MICDET Clamp Write Sequencer Control Registers

When a valid 'Write Sequencer' control event is detected, the respective control sequence will be scheduled. See "Control Write Sequencer" for further details.

Note that the trigger status (_TRIG_STS) bits are latching fields. Care is required when resetting these bits, to ensure the intended device behaviour - resetting the _TRIG_STS register(s) may cause LDO1 (and DCVDD) to be disabled.

A valid clock (SYSCLK) must be enabled whenever a Control Write Sequence is scheduled.

If the JD1, GP5 or MICDET Clamp trigger status bits are associated with the Control Write Sequencer (using the register bits in Table 74) and also configured as Wake-Up events (using the register bits in Table 73), then the Boot Sequence must be programmed to configure and enable SYSCLK. (Note that the default SYSCLK frequency must be used in this case.)

The Boot Sequence (see "Hardware Reset, Software Reset, Wake-Up, and Device ID") is scheduled as part of the Wake-Up transition, and provides the capability to configure SYSCLK (and other register settings) prior to the Control Write Sequencer being triggered.

Note that, if the Control Write Sequencer is triggered during normal operation, then SYSCLK will typically be already available, and no additional requirements will apply.

To return to Sleep mode following a Wake-Up / Write Sequence, the last step of the control sequence must be to write '1' to the applicable trigger status bit(s). The _TRIG_STS bit(s) will be reset, LDO1 will be disabled, and the WM8998 will be in Sleep mode. (The LDO1_ENA bit must be set to 0, and the LDOENA pin must not be asserted.)

To remain 'On' at the end of a Wake-up / Write Sequence, the control sequence must write '1' to the LDO1_ENA bit before resetting the trigger status bit(s). Alternatively, the host processor should assert the LDOENA pin before resetting the trigger status bit(s).

When the Control Write Sequencer is triggered during normal operation, it can be programmed to select the Sleep mode by writing '0' to the LDO1_ENA bit. (The LDOENA pin must not be asserted.)

See "Charge Pumps, Regulators and Voltage Reference" for details of the LDO1_ENA control bit.

INTERRUPT CONTROL

An Interrupt Request (IRQ) event can be associated with the JD1, GP5 or MICDET Clamp signals. Separate 'mask' bits are provided to enable IRQ events on the rising and/or falling edges of each signal.

See "Interrupts" for further details.

GENERAL PURPOSE INPUT / OUTPUT

The WM8998 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The GPIO input functions can be used to generate an Interrupt (IRQ) event. The GPIO and Interrupt circuits support the following functions:

- Logic input / Button detect (GPIO input)
- Logic '1' and logic '0' output (GPIO output)
- Interrupt (IRQ) status output
- Clock output
- Frequency Locked Loop (FLL) status output
- Frequency Locked Loop (FLL) Clock output
- IEC-60958-3 compatible S/PDIF output
- Pulse Width Modulation (PWM) Signal output
- Headphone Detection status output
- Microphone / Accessory Detection status output
- Output Signal Path Enable/Disable status output
- Boot Sequence status output
- Asynchronous Sample Rate Converter (ASRC) Lock status and Configuration Error output
- Isochronous Sample Rate Converter (ISRC) Configuration Error output
- Over-Temperature, Short Circuit Protection, and Speaker Shutdown status output
- Dynamic Range Control (DRC) status output
- Control Write Sequencer status output
- Control Interface Error status output
- Clocking Error status output

Note that the GPIO pins are referenced to different power domains (DBVDD1, DBVDD2 or DBVDD3), as noted in the "Pin Description" section.

In addition to the functions described in this section, the GPIO5 pin can be configured as an input to the Control Write Sequencer (see "Control Write Sequencer"). See also Table 74 for details of the associated register control fields.

The GPIO5 pin is one of the 'Always On' digital input / output pins and can be used as a 'Wake-Up' input in the low-power 'Sleep' mode. The GPIO5 pin can also be used as an input to the MICDET Clamp function, supporting additional functionality relating to jack insertion or jack removal events See "Low Power Sleep Configuration" for further details.

The WM8998 also incorporates a General Purpose Switch feature, which can be used as a controllable analogue switch; details of this are provided at the end of this "General Purpose Input / Output" section.

GPIO CONTROL

For each GPIO, the selected function is determined by the GP*n*_FN field, where n identifies the GPIO pin (1, 2, 3, 4 or 5). The pin direction, set by GP*n*_DIR, must be set according to function selected by GP*n*_FN.

When a pin is configured as a GPIO input (GP*n*_DIR = 1, GP*n*_FN = 01h), the logic level at the pin can be read from the respective GP*n*_LVL bit. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective GP*n*_DB bit. The de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required. The de-bounce time is configurable using the GP_DBTIME register. See “Clocking and Sample Rates” for further details of the WM8998 clocking configuration.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

Integrated pull-up and pull-down resistors are provided on each of the GPIO pins; these can be configured independently using the GP*n*_PU and GP*n*_PD fields. Note that, if GP*n*_PU and GP*n*_PD are both set for any GPIO pin, then the pull-up and pull-down will be disabled.

When a pin is configured as a GPIO output (GP*n*_DIR = 0, GP*n*_FN = 01h), its level can be set to logic 0 or logic 1 using the GP*n*_LVL field. Note that the GP*n*_LVL registers are ‘write only’ when the respective GPIO pin is configured as an output.

When a pin is configured as an output (GP*n*_DIR = 0), the polarity can be inverted using the GP*n*_POL bit. When GP*n*_POL = 1, then the selected output function is inverted. In the case of Logic Level output (GP*n*_FN = 01h), the external output will be the opposite logic level to GP*n*_LVL when GP*n*_POL = 1.

A GPIO output can be either CMOS driven or Open Drain. This is selected on each pin using the respective GP*n*_OP_CFG bit.

The register fields that control the GPIO pins are described in Table 75.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3072 (0C00h) GPIO1 CTRL to R3076 (0C04h) GPIO5 CTRL	15	GPn_DIR	1	GPIOn Pin Direction 0 = Output 1 = Input
	14	GPn_PU	0	GPIOn Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GPn_PD	1	GPIOn Pull-Down Enable 0 = Disabled 1 = Enabled
	11	GPn_LVL	0	GPIOn level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GPn_POL is set, the register is the opposite logic level to the external pin. Note that the GP*n*_LVL register is 'write only' when GP*n*_DIR=0.
	10	GPn_POL	0	GPIOn Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	GPn_OP_CFG	0	GPIOn Output Configuration 0 = CMOS 1 = Open Drain
	8	GPn_DB	1	GPIOn Input De-bounce 0 = Disabled 1 = Enabled
	6:0	GPn_FN [6:0]	01h	GPIOn Pin Function (see Table 76 or Table 77 for details)
R3088 (0C10h) GPIO Debounce Config	15:12	GP_DBTIME [3:0]	0001	GPIO Input de-bounce time 0h = 100us 1h = 1.5ms 2h = 3ms 3h = 6ms 4h = 12ms 5h = 24ms 6h = 48ms 7h = 96ms 8h = 192ms 9h = 384ms Ah = 768ms Bh to Fh = Reserved
Note: *n* is a number (1, 2, 3, 4 or 5) that identifies the individual GPIO.				

Table 75 GPIO Control

GPIO FUNCTION SELECT

The available GPIO functions for GPIO pins 1, 2, 3 and 4 are described in Table 76. A subset of these functions is available for GPIO5, as described in Table 77.

The function of each GPIO is set using the GP*n*_FN register, where n identifies the GPIO pin (1, 2, 3, 4 or 5). Note that the respective GP*n*_DIR must also be set according to whether the function is an input or output.

GPn_FN	DESCRIPTION	COMMENTS
00h		No function
01h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input.
02h	IRQ1 Output	Interrupt (IRQ1) output 0 = IRQ1 not asserted 1 = IRQ1 asserted
03h	IRQ2 Output	Interrupt (IRQ2) output 0 = IRQ2 not asserted 1 = IRQ2 asserted
04h	OPCLK Clock Output	Configurable clock output derived from SYSCLK
05h	FLL1 Clock	Clock output from FLL1
06h	FLL2 Clock	Clock output from FLL2
07h	S/PDIF Output	IEC-60958-3 compatible S/PDIF output
08h	PWM1 Output	Configurable Pulse Width Modulation output PWM1
09h	PWM2 Output	Configurable Pulse Width Modulation output PWM2
0Ah	SYSCLK Underclocked Error	Indicates that an unsupported clocking configuration has been attempted 0 = Normal 1 = SYSCLK underclocking error
0Bh	ASYNCCLK Underclocked Error	Indicates that an unsupported clocking configuration has been attempted 0 = Normal 1 = ASYNCCLK underclocking error
0Ch	FLL1 Lock	Indicates FLL1 Lock status 0 = Not locked 1 = Locked
0Dh	FLL2 Lock	Indicates FLL2 Lock status 0 = Not locked 1 = Locked
0Fh	FLL1 Clock OK	Indicates FLL1 Clock OK status 0 = FLL1 Clock output is not active 1 = FLL1 Clock output is active
10h	FLL2 Clock OK	Indicates FLL2 Clock OK status 0 = FLL2 Clock output is not active 1 = FLL2 Clock output is active
12h	Headphone detect	Indicates Headphone Detection status 0 = Headphone Detect not complete 1 = Headphone Detect complete
13h	Microphone detect	Microphone Detect (MICDET accessory) IRQ output A single 31µs pulse is output whenever an accessory insertion, removal or impedance change is detected.
15h	Write Sequencer status	Indicates Write Sequencer status A short pulse is output when the Write Sequencer has completed all scheduled sequences.

GPn_FN	DESCRIPTION	COMMENTS
16h	Control Interface Address Error	Indicates Control Interface Address error 0 = Normal 1 = Control Interface Address error
1Ah	ASRC1 Lock	Indicates ASRC1 Lock status 0 = Not locked 1 = Locked
1Bh	ASRC2 Lock	Indicates ASRC2 Lock status 0 = Not locked 1 = Locked
1Ch	ASRC Configuration Error	Indicates ASRC configuration error 0 = ASRC configuration OK 1 = ASRC configuration error
1Dh	DRC1 Signal Detect	Indicates DRC1 Signal Detect status 0 = Signal threshold not exceeded 1 = Signal threshold exceeded
1Eh	DRC1 Anti-Clip Active	Indicates DRC1 Anti-Clip status 0 = Anti-Clip is not active 1 = Anti-Clip is active
1Fh	DRC1 Decay Active	Indicates DRC1 Decay status 0 = Decay is not active 1 = Decay is active
20h	DRC1 Noise Gate Active	Indicates DRC1 Noise Gate status 0 = Noise Gate is not active 1 = Noise Gate is active
21h	DRC1 Quick Release Active	Indicates DRC1 Quick Release status 0 = Quick Release is not active 1 = Quick Release is active
27h	Mixer Dropped Sample Error	Indicates a dropped sample in the digital core mixers 0 = Normal 1 = Mixer dropped sample error
2Bh	Speaker Overheat Shutdown	Indicates Shutdown Temperature status 0 = Temperature is below shutdown level 1 = Temperature is above shutdown level
2Ch	Speaker Overheat Warning	Indicates Warning Temperature status 0 = Temperature is below warning level 1 = Temperature is above warning level
2Dh	Underclocked Error	Indicates insufficient SYSCLK or ASYNCCLK cycles for one or more of the selected signal paths or signal processing functions. Increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported. 0 = Normal 1 = Underclocked error
2Eh	Overclocked Error	Indicates that an unsupported device configuration has been attempted, as the clocking requirements of the requested configuration exceed the device limits. 0 = Normal 1 = Overclocked error
2Fh	HPL Enable Status	HPOUTL Enable Status A short pulse is output when the HPOUTL Enable control sequence has completed.
30h	HPR Enable Status	HPOUTR Enable Status A short pulse is output when the HPOUTR Enable control sequence has completed.
31h	LINEL Enable Status	LINEOUTL Enable Status A short pulse is output when the LINEOUTL Enable control sequence has completed.

GPn_FN	DESCRIPTION	COMMENTS
32h	LINER Enable Status	LINEOUTR Enable Status A short pulse is output when the LINEOUTR Enable control sequence has completed.
33h	EP Enable Status	EPOUT Enable Status A short s pulse is output when the EPOUT Enable control sequence has completed.
34h	HPL Disable Status	HPOUTL Disable Status A short pulse is output when the HPOUTL Disable control sequence has completed.
35h	HPR Disable Status	HPOUTR Disable Status A short pulse is output when the HPOUTR Disable control sequence has completed.
36h	LINEL Disable Status	LINEOUTL Disable Status A short pulse is output when the LINEOUTL Disable control sequence has completed.
37h	LINER Disable Status	LINEOUTR Disable Status A short pulse is output when the LINEOUTR Disable control sequence has completed.
38h	EP Disable Status	EPOUT Disable Status A short pulse is output when the EPOUT Disable control sequence has completed.
3Dh	OPCLK Async Clock Output	Configurable clock output derived from ASYNCCLK
44h	Boot Done	Boot Status A short pulse is output when the Boot Sequence has completed.
45h	SPKL Enable Status	SPKOUTL Enable Status A short pulse is output when the SPKOUTL Enable control sequence has completed.
46h	SPKR Enable Status	SPKOUTR Enable Status A short pulse is output when the SPKOUTR Enable control sequence has completed.
47h	SPKL Disable Status	SPKOUTL Disable Status A short pulse is output when the SPKOUTL Disable control sequence has completed.
48h	SPKR Disable Status	SPKOUTR Disable Status A short pulse is output when the SPKOUTR Disable control sequence has completed.
4Bh	SYSCLK_ENA Status	SYSCLK_ENA Status 0 = SYSCLK_ENA is enabled 1 = SYSCLK_ENA is disabled
4Ch	ASYNC_CLK_ENA Status	ASYNC_CLK_ENA Status 0 = ASYNC_CLK_ENA is enabled 1 = ASYNC_CLK_ENA is disabled
4Dh	ISRC1 Configuration Error	Indicates ISRC1 configuration error 0 = ISRC configuration OK 1 = ISRC configuration error
4Eh	ISRC2 Configuration Error	Indicates ISRC2 configuration error 0 = ISRC configuration OK 1 = ISRC configuration error
5Fh	SPKOUTL Short Circuit Status	SPKOUTL Short Circuit status 0 = Normal 1 = Short Circuit detected
60h	SPKOUTR Short Circuit Status	SPKOUTR Short Circuit status 0 = Normal 1 = Short Circuit detected
61h	Speaker Shutdown Status	Speaker Shutdown Status 0 = Normal

GPn_FN	DESCRIPTION	COMMENTS
		1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)

Table 76 GPIO Function Select (GPIO1, GPIO2, GPIO3, GPIO4)

GPn_FN	DESCRIPTION	COMMENTS
00h		No function
01h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input.
02h	IRQ1 Output	Interrupt (IRQ1) output 0 = IRQ1 not asserted 1 = IRQ1 asserted
03h	IRQ2 Output	Interrupt (IRQ2) output 0 = IRQ2 not asserted 1 = IRQ2 asserted
04h	OPCLK Clock Output	Configurable clock output derived from SYSCLK
05h	FLL1 Clock	Clock output from FLL1
06h	FLL2 Clock	Clock output from FLL2
08h	PWM1 Output	Configurable Pulse Width Modulation output PWM1
09h	PWM2 Output	Configurable Pulse Width Modulation output PWM2
3Dh	OPCLK Async Clock Output	Configurable clock output derived from ASYNCCLK

Table 77 GPIO Function Select (GPIO5)

BUTTON DETECT (GPIO INPUT)

GP*n*_FN = 01h.

Button detect functionality can be selected on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The same functionality can be used to support a Jack Detect input function.

It is recommended to enable the GPIO input de-bounce feature when using GPIOs as button input or Jack Detect input.

The GP*n*_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable de-bounce controls. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

The de-bounced GPIO signals are also inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bits are latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

LOGIC ‘1’ AND LOGIC ‘0’ OUTPUT (GPIO OUTPUT)

GP*n*_FN = 01h.

The WM8998 can be programmed to drive a logic high or logic low level on a GPIO pin by selecting the “GPIO Output” function as described in “GPIO Control”.

The output logic level is selected using the respective GP*n*_LVL bit. Note that the GP*n*_LVL registers are ‘write only’ when the respective GPIO pin is configured as an output.

The polarity of the GPIO output can be inverted using the GP*n*_POL registers. If GP*n*_POL=1, then the external output will be the opposite logic level to GP*n*_LVL.

INTERRUPT (IRQ) STATUS OUTPUT

GP*n*_FN = 02h, 03h.

The WM8998 has an Interrupt Controller which can be used to indicate when any selected Interrupt events occur. An interrupt can be generated by any of the events described throughout the GPIO function definition above. Individual interrupts may be masked in order to configure the Interrupt as required. See “Interrupts” for further details.

The Interrupt Controller supports two separate Interrupt Request (IRQ) outputs. The IRQ1 or IRQ2 status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that the IRQ1 status is output on the $\overline{\text{IRQ}}$ pin at all times.

OPCLK AND OPCLK_ASYNC CLOCK OUTPUT

GP*n*_FN = 04h, 3Dh.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. The OPCLK frequency is controlled by OPCLK_DIV and OPCLK_SEL. The OPCLK output is enabled using the OPCLK_ENA register, as described in Table 78.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. The OPCLK_ASYNC frequency is controlled by OPCLK_ASYNC_DIV and OPCLK_ASYNC_SEL. The OPCLK_ASYNC output is enabled using the OPCLK_ASYNC_ENA register

It is recommended to disable the clock output (OPCLK_ENA=0 or OPCLK_ASYNC_ENA=0) before making any change to the respective OPCLK_DIV, OPCLK_SEL, OPCLK_ASYNC_DIV or OPCLK_ASYNC_SEL registers.

The OPCLK or OPCLK_ASYNC Clock outputs can be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that the OPCLK source frequency cannot be higher than the SYSCLK frequency. The OPCLK_ASYNC source frequency cannot be higher than the ASYNCCLK frequency. The maximum output frequency supported for GPIO output is noted in the “Electrical Characteristics”.

See “Clocking and Sample Rates” for more details of the system clocks (SYSCLK and ASYNCCLK).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R329 (0149h) Output system clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (ie. SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.
R330 (014Ah) Output async clock	15	OPCLK_ASYNC_ ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_ASYNC_ DIV [4:0]	00h	OPCLK_ASYNC Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_ASYNC_ SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (ie. ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.

Table 78 OPCLK and OPCLK_ASYNC Control

FREQUENCY LOCKED LOOP (FLL) STATUS OUTPUT

GP*n*_FN = 0Ch, 0Dh, 0Fh, 10h.

The WM8998 supports FLL status flags, which may be used to control other events. See "Clocking and Sample Rates" for more details of the FLL.

The 'FLL Clock OK' signals indicate that the respective FLL has started up and is providing an output clock. The 'FLL Lock' signals indicate whether FLL Lock has been achieved.

The FLL Clock OK and FLL Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

The FLL Clock OK and FLL Lock signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising and falling edges of these signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

FREQUENCY LOCKED LOOP (FLL) CLOCK OUTPUT

GP*n*_FN = 05h, 06h.

Clock outputs derived from the FLLs may be output on a GPIO pin. The GPIO output from each FLLn (where 'n' is 1 or 2) is controlled by the respective FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers, as described in Table 79.

It is recommended to disable the clock output (FLLn_GPCLK_ENA=0) before making any change to the respective FLLn_GPCLK_DIV register.

Note that the FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers affect the GPIO outputs only; they do not affect the FLL frequency. The maximum output frequency supported for GPIO output is noted in the "Electrical Characteristics".

The Frequency Locked Loop (FLL) Clock outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

See "Clocking and Sample Rates" for more details of the WM8998 system clocking and for details of how to configure the FLLs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R394 (018Ah) FLL1 GPIO Clock	7:1	FLL1_GPCLK_DIV [6:0]	02h	FLL1 GPIO Clock Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL1_GPCLK_DIV)
	0	FLL1_GPCLK_ENA	0	FLL1 GPIO Clock Enable 0 = Disabled 1 = Enabled
R426 (01AAh) FLL2 GPIO Clock	7:1	FLL2_GPCLK_DIV [6:0]	02h	FLL2 GPIO Clock Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL2_GPCLK_DIV)
	0	FLL2_GPCLK_ENA	0	FLL2 GPIO Clock Enable 0 = Disabled 1 = Enabled

Table 79 FLL Clock Output Control

SPDIF AUDIO OUTPUT

GP*n*_FN = 07h.

The WM8998 incorporates an IEC-60958-3 compatible S/PDIF transmitter, which can be selected as a GPIO output. The S/PDIF transmitter supports stereo audio channels, and allows full control over the S/PDIF validity bits and channel status information.

The S/PDIF signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Digital Core” for details of how to configure the S/PDIF output generator.

PULSE WIDTH MODULATION (PWM) SIGNAL OUTPUT

GP*n*_FN = 08h, 09h.

The WM8998 incorporates two Pulse Width Modulation (PWM) signal generators which can be enabled as GPIO outputs. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

The Pulse Width Modulation (PWM) outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Digital Core” for details of how to configure the PWM signal generators.

Note that the PWM output should always be disabled (PWMn_ENA=0, as described in Table 18) whenever the system clock, SYSCLK, is disabled. Failure to do this may result in a persistent logic ‘1’ DC output from the PWM generator. See “Clocking and Sample Rates” for details of system clocking and the associated control requirements.

HEADPHONE DETECTION STATUS OUTPUT

GP*n*_FN = 12h.

The WM8998 provides a headphone detection circuit on the HPDETL and HPDETR pins to measure the impedance of an external load connected to the headphone outputs. See “External Accessory Detection” for further details.

A logic signal from the headphone detection circuit may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set low when a Headphone Detect measurement is triggered, and is set high when the Headphone Detect function has completed. A rising edge indicates completion of a Headphone Detect measurement.

The headphone detection circuit is also an input to the Interrupt control circuit. An interrupt event is triggered whenever a headphone detection measurement has completed. Note that the HPDET_EINT flag is also asserted when the headphone detection is initiated. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

MICROPHONE / ACCESSORY DETECTION STATUS OUTPUT

GP*n*_FN = 13h.

The WM8998 provides an impedance measurement circuit on the MICDETn pins to detect the connection of a microphone or other external accessory. See “External Accessory Detection” for further details.

A logic signal from the microphone detect circuit may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a pulse duration of 31µs whenever an accessory insertion, removal or impedance change is detected.

The microphone detection circuit is also an input to the Interrupt control circuit. An interrupt event is triggered whenever an accessory insertion, removal or impedance change is detected. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

OUTPUT SIGNAL PATH ENABLE/DISABLE STATUS OUTPUT

GP*n*_FN = 2Fh, 30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h, 38h, 45h, 46h, 47h, 48h.

Whenever the OUT1, OUT2, OUT3 or OUT4 signal path is enabled or disabled, a pop-suppression control sequence is triggered. Status outputs indicating the progress of these sequences are provided. See "Output Signal Path" for details of the Output Enable functions.

A logic signal from the Output Signal Path control functions may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control". This logic signal is set high for a short pulse duration (approx. 100ns) whenever the respective Enable/Disable control sequence has completed. The Output Signal Path control sequence status outputs are described in Table 80.

The Output Signal Path control sequences also provide inputs to the Interrupt control circuit. An interrupt event is triggered on completion of the respective control sequence. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

GPN_FN	DESCRIPTION	COMMENTS
2Fh	HPOUTL Enable Status	A short pulse is output when the respective Enable/Disable control sequence has completed.
30h	HPOUTR Enable Status	
31h	LINEOUTL Enable Status	
32h	LINEOUR Enable Status	
33h	EPOUT Enable Status	
34h	HPOUTL Disable Status	
35h	HPOUTR Disable Status	
36h	LINEOUTL Disable Status	
37h	LINEOUR Disable Status	
38h	EPOUT Disable Status	
45h	SPKOUTL Enable Status	
46h	SPKOUTR Enable Status	
47h	SPKOUTL Disable Status	
48h	SPKOUTR Disable Status	

Table 80 Output Signal Path Enable/Disable Status Indications

BOOT DONE STATUS OUTPUT

GP*n*_FN = 44h.

The WM8998 executes a user-configurable Boot Sequence following Power-On Reset (POR), Hardware Reset, Software Reset or Wake-Up (from Sleep mode). Control register writes should not be attempted while the Boot Sequence is running.

For details of the Boot Sequence, see "Control Write Sequencer".

The BOOT_DONE_STS register bit (see Table 115) indicates the status of the Boot Sequence. (When BOOT_DONE_STS=1, then the Boot Sequence is complete.)

A logic signal from the Boot Sequence function may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control". This logic signal is set high for a short pulse duration (approx. 100ns) when the Boot Sequence has completed. To output this signal, the Boot Sequence must be programmed to configure a GPIO pin for this function. Note that, under default register conditions, completion of the Boot Sequence is indicated via the Interrupt circuit.

The BOOT_DONE_STS signal is also an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of this signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC) LOCK STATUS OUTPUT

GP*n*_FN = 1Ah, 1Bh.

The WM8998 maintains a flag indicating the lock status of the Asynchronous Sample Rate Converters (ASRCs), which may be used to control other events if required. See “Digital Core” for more details of the ASRCs.

The ASRC Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ASRC Lock signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the ASRC Lock signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC) CONFIGURATION ERROR STATUS OUTPUT

GPn_FN = 1Ch.

The WM8998 performs automatic checks to confirm that the ASRCs are configured with valid settings. Invalid settings include conditions where one of the associated sample rates is higher than 48kHz. If an invalid ASRC configuration is detected, this can be indicated using the GPIO and/or Interrupt functions.

The ASRC Configuration Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ASRC Configuration Error signal is an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the ASRC Configuration Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

ISOCHRONOUS SAMPLE RATE CONVERTER (ISRC) CONFIGURATION ERROR STATUS OUTPUT

GPn_FN = 4Dh, 4Eh.

The WM8998 performs automatic checks to confirm that the ISRCs are configured with valid settings. Invalid settings include conditions where an invalid combination of sample rates is configured. If an invalid ISRC configuration is detected, this can be indicated using the GPIO and/or Interrupt functions.

The ISRC Configuration Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ISRC Configuration Error signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the ISRC Configuration Error signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

OVER-TEMPERATURE, SHORT CIRCUIT PROTECTION, AND SPEAKER SHUTDOWN STATUS OUTPUT

GP*n*_FN = 2Bh, 2Ch, 5Fh, 60h, 61h.

The WM8998 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. A GPIO pin can be used to indicate either an Overheat Warning Temperature event or an Overheat Shutdown Temperature event.

The WM8998 provides short circuit protection on the Class D speaker output paths.

The status of each of the short circuit detection circuits may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

If the Overheat Shutdown Temperature is exceeded, or if a short circuit is detected on the Class D speaker outputs, then the Class D speaker outputs will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, the Speaker Shutdown signal will be asserted. The speaker driver shutdown status can also be output directly on a GPIO pin.

The Overtemperature, Short Circuit protection, and Speaker Shutdown status flags are inputs to the Interrupt control circuit. An interrupt event may be triggered on the applicable edges of these signals. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

DYNAMIC RANGE CONTROL (DRC) STATUS OUTPUT

GP*n*_FN = 1Dh, 1Eh, 1Fh, 20h, 21h.

The Dynamic Range Control (DRC) circuits provide status outputs, which may be used to control other events if required.

The DRC status flags may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The DRC status outputs are described in Table 81.

See “Digital Core” for more details of the DRC.

GPN_FN	DESCRIPTION	COMMENTS
1Dh	DRC1 Signal Detect	Indicates a signal is present on the respective DRC path. The threshold level is configurable (see Table 13).
1Eh	DRC1 Anti-Clip Active	Indicates the DRC anti-clip function has been triggered; the DRC gain is decreasing in response to a rising signal level.
1Fh	DRC1 Decay Active	Indicates that the DRC gain is increasing in response to a low-level signal input.
20h	DRC1 Noise Gate Active	Indicates that the DRC noise gate has been triggered; an idle signal condition has been detected.
21h	DRC1 Quick Release Active	Indicates that the DRC quick-release function has been triggered; the DRC gain is increasing rapidly following detection of a short transient peak.

Table 81 Dynamic Range Control (DRC) Status Indications

CONTROL WRITE SEQUENCER STATUS OUTPUT

GP*n*_FN = 15h.

The WM8998 Control Write Sequencer (WSEQ) can be used to execute a sequence of register write operations in response to a simple trigger event. See “Control Write Sequencer” for details of the Control Write Sequencer.

The WSEQ_BUSY register bit (see Table 109) indicates the status of the Control Write Sequencer. When WSEQ_BUSY=1, this indicates that one or more Write Sequence operations are in progress or are queued for sequential execution.

A logic signal from the Write Sequencer function may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a short pulse duration (approx. 100ns) whenever the Write Sequencer has completed all scheduled sequences, and there are no more pending operations.

The Write Sequencer status is an input to the Interrupt control circuit. An interrupt event is triggered on completion of a Control Sequence. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

CONTROL INTERFACE ERROR STATUS OUTPUT

GP*n*_FN = 16h.

The WM8998 is controlled by writing to registers through a 2-wire (I2C) serial control interface, as described in the “Control Interface” section. The SLIMbus interface also supports read/write access to the control registers, as described in the “SLIMbus Interface Control” section.

The WM8998 performs automatic checks to confirm if a register access is successful. Register access will be unsuccessful if an invalid register address is selected. If an invalid or unsuccessful register operation is attempted, this can be indicated using the GPIO and/or Interrupt functions.

The Control Interface Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The Control Interface Error signal is an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the Control Interface Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

SYSTEM CLOCKS ENABLE STATUS OUTPUT

GP*n*_FN = 4Bh, 4Ch.

The WM8998 requires a system clock (SYSCLK) for its internal functions and to support the input/output signal paths. The WM8998 can support two independent clock domains, with selected functions referenced to the ASYNCCLK clock domain. See “Clocking and Sample Rates” for details of these clocks.

The SYSCLK_ENA and ASYNC_CLK_ENA registers (see Table 90) control the SYSCLK and ASYNCCLK signals respectively. When ‘0’ is written to these registers, the host processor must wait until the WM8998 has shut down the associated functions before issuing any other register write commands.

The SYSCLK Enable and ASYNCCLK Enable status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The SYSCLK Enable and ASYNCCLK Enable signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered when the respective clock functions have been shut down. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

CLOCKING ERROR STATUS OUTPUT

GP*n*_FN = 0Ah, 0Bh, 27h, 2Dh, 2Eh.

The WM8998 performs automatic checks to confirm that the system clocks are correctly configured according to the commanded functionality. An invalid configuration is one where there are insufficient clock cycles to support the digital processing required by the commanded signal paths.

An Underclocked Error condition is where there are insufficient clock cycles for the requested functionality, and increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported.

An Overclocked Error condition is where the requested functionality cannot be supported, as the clocking requirements of the requested configuration exceed the device limits.

The system clocks (SYSCLK and, where applicable, ASYNCCLK) must be enabled before any signal path is enabled. If an attempt is made to enable a signal path, and there are insufficient clock cycles to support that path, then the attempt will be unsuccessful. Note that any signal paths that are already active will not be affected under these circumstances.

The Clocking Error signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The Clocking Error conditions are described in Table 82.

The Clocking Error signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising and falling edges of the Clocking Error signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

GPN_FN	DESCRIPTION	COMMENTS
0Ah	SYSCLK Underclocked	Indicates insufficient SYSCLK cycles for the commanded functionality.
0Bh	ASYNCCLK Underclocked	Indicates insufficient ASYNCCLK cycles for the commanded functionality.
27h	Mixer Dropped Sample Error	Indicates a dropped sample in the digital core mixer function.
2Dh	Underclocked Error	Indicates insufficient SYSCLK or ASYNCCLK cycles for one or more of the selected signal paths or signal processing functions. Increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported. Status bits associated with specific sub-systems provide further de-bug capability. The INnx_ENA_STS bits in register R769 indicate the status of each of the input (analogue or digital microphone) signal paths. The OUTnx_ENA_STS bits in registers R1025 and R1030 indicate the status of each of the output (Headphone, Earpiece, Speaker or PDM) signal paths. The ASRCnx_ENA_STS bits in register R3809 indicate the status of each of the ASRC signal paths. The FX_STS field in register R3585 indicates the status of each of the Effects (EQ, DRC or LHPF) signal paths. The *MIX_STSn fields in registers R1600 to R3000 indicate the status of each of the Digital Core mixer signal paths. The ISRCn and AIFn functions are also inputs to the Underclocked Error status indication, but there are no specific _STS register bits associated with these.
2Eh	Overclocked Error	Indicates that an unsupported device configuration has been attempted, as the clocking requirements of the requested configuration exceed the device limits.

Table 82 Clocking Error Status Indications

GENERAL PURPOSE SWITCH

The WM8998 provides a General Purpose Switch, which can be used as a controllable analogue switch for external functions. The switch is implemented between the GPSWP and GPSWN pins. Note that this feature is entirely independent to the GPIOn pins.

The General Purpose Switch is configured using SW1_MODE. This register allows the switch to be disabled, enabled, or synchronised to the MICDET Clamp status, as described in Table 83.

The switch is a bi-directional analogue switch, offering flexibility in the potential circuit applications. Refer to the “Absolute Maximum Ratings” and “Electrical Characteristics” for further details.

The switch can be used in conjunction with the MICDET Clamp function, in order suppress pops and clicks associated with jack insertion and removal. An example circuit is shown in Figure 59, within the “External Accessory Detection” section. Note that the MICDET Clamp function must also be configured appropriately when using this method of pop suppression control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3096 (0C18h) GP Switch 1	1:0	SW1_MODE [1:0]	00	General Purpose Switch control 00 = Disabled (open) 01 = Enabled (closed) 10 = Enabled when MICDET Clamp is active 11 = Enabled when MICDET Clamp is not active

Table 83 General Purpose Switch control

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the Jack Detect and GPIO input pins, headphone / accessory detection, FLL / ASRC Lock detection, and Clocking configuration error indications. (See Table 84, Table 85 and Table 86 for a full definition of the Interrupt Controller inputs.) Any combination of these inputs can be used to trigger an Interrupt Request (IRQ) event.

The Interrupt Controller supports two sets of interrupt registers. This allows two separate Interrupt Request (IRQ) outputs to be generated, and for each IRQ to report a different set of input or status conditions.

For each Interrupt Request (IRQ1 and IRQ2) output, there is an Interrupt register field associated with each of the interrupt inputs. These fields are asserted whenever a logic edge is detected on the respective input. Some inputs are triggered on rising edges only; some are triggered on both edges. Separate rising and falling interrupt registers are provided for the JD1 and GP5 signals. The Interrupt register fields for IRQ1 are described in Table 84. The Interrupt register fields for IRQ2 are described in Table 85. The Interrupt flags can be polled at any time, or else in response to the Interrupt Request (IRQ) output being signalled via the $\overline{\text{IRQ}}$ pin or a GPIO pin.

All of the Interrupts are edge-triggered, as noted above. Many of these are triggered on both the rising and falling edges and, therefore, the Interrupt registers cannot indicate which edge has been detected. The “Raw Status” fields described in Table 86 provide readback of the current value of the corresponding inputs to the Interrupt Controller. Note that the status of any GPIO inputs can be read using the GPn_LVL registers, as described in Table 75.

The UNDERCLOCKED_STS and OVERCLOCKED_STS registers represent the logical ‘OR’ of status flags from multiple sub-systems. The status bits in registers R3364 to R3366 (see Table 86) provide readback of these lower-level signals. See “Clocking and Sample Rates” for a description of the Underclocked and Overclocked Error conditions.

Individual mask bits can enable or disable different functions from the Interrupt controller. The mask bits are described in Table 84 (for IRQ1) and Table 85 (for IRQ2). Note that a masked interrupt input will not assert the corresponding interrupt register field, and will not cause the associated Interrupt Request (IRQ) output to be asserted.

The Interrupt Request (IRQ) outputs represent the logical ‘OR’ of the associated interrupt registers. (IRQ1 is derived from the _EINT1 registers; IRQ2 is derived from the _EINT2 registers). The Interrupt register fields are latching fields and, once they are set, they are not reset until a ‘1’ is written to the respective register bit(s). The Interrupt Request (IRQ) outputs are not reset until each of the associated interrupts has been reset.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin using the register bits described in Table 75. The GPIO de-bounce circuit uses the 32kHz clock, which must be enabled whenever the GPIO de-bounce function is required.

A de-bounce circuit is always enabled on the FLL status inputs; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL status inputs. Note that the “Raw Status” fields (described in Table 86), are valid without clocking, and can be used to provide FLL status readback when system clocks are not available.

The IRQ outputs can be globally masked using the IM_IRQ1 and IM_IRQ2 register bits. When not masked, the IRQ status can be read from IRQ1_STS and IRQ2_STS for the respective IRQ outputs.

The IRQ1 output is provided externally on the $\overline{\text{IRQ}}$ pin. Under default conditions, this output is ‘Active Low’. The polarity can be inverted using the IRQ_POL register. The $\overline{\text{IRQ}}$ output can be either CMOS driven or Open Drain; this is selected using the IRQ_OP_CFG register. Note that the $\overline{\text{IRQ}}$ output is referenced to the DBVDD1 power domain.

The IRQ1 and IRQ2 signals may be output on a GPIO pin - see “General Purpose Input / Output”.

The WM8998 Interrupt Controller circuit is illustrated in Figure 63. (Note that not all interrupt inputs are shown.) The associated control fields are described in Table 84, Table 85 and Table 86.

Note that, under default register conditions, the ‘Boot Done’ status is the only un-masked interrupt source; a falling edge on the $\overline{\text{IRQ}}$ pin will indicate completion of the Boot Sequence.

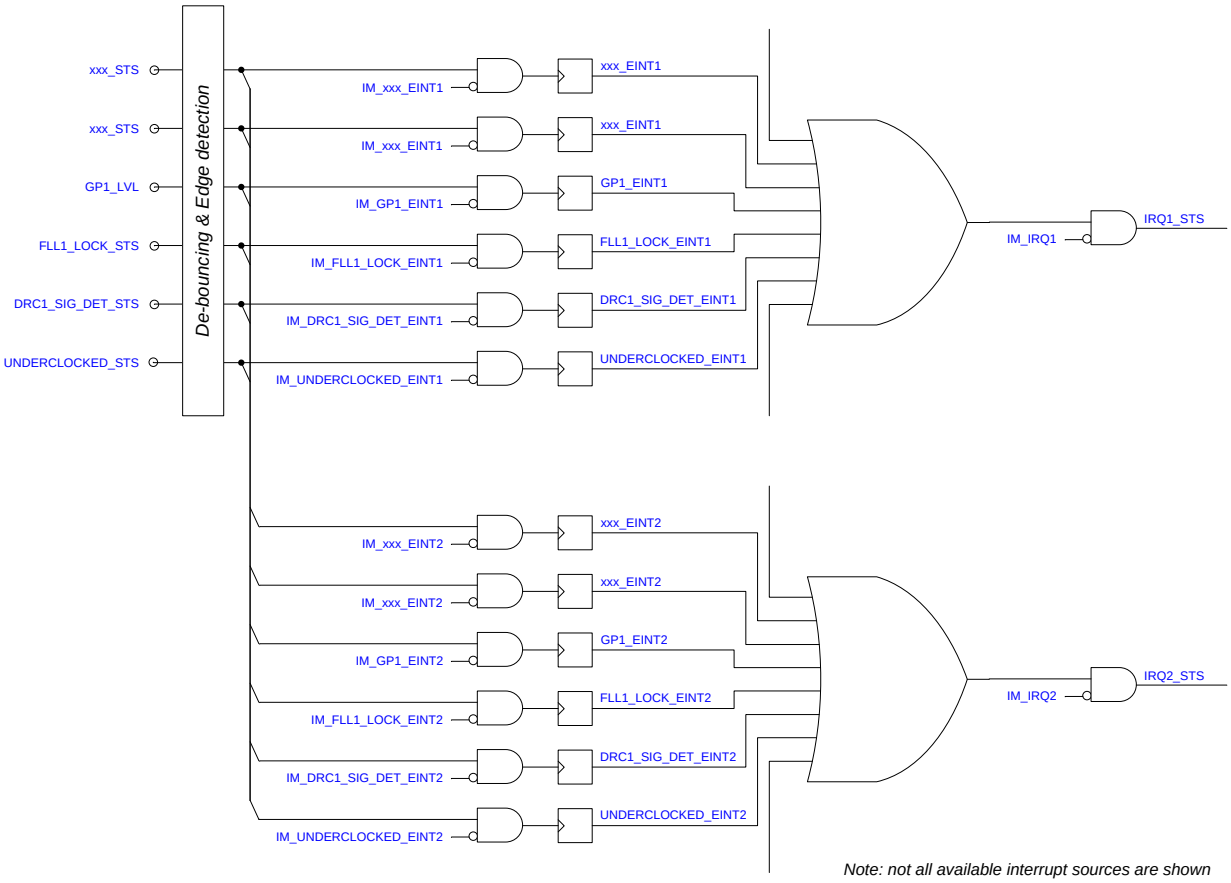


Figure 63 Interrupt Controller

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3087 (0C0Fh) IRQ CTRL 1	10	IRQ_POL	1	IRQ Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	IRQ_OP_CFG	0	IRQ Output Configuration 0 = CMOS 1 = Open Drain
R3328 (0D00h) Interrupt Status 1	3	GP4_EINT1	0	GPIO4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP3_EINT1	0	GPIO3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP2_EINT1	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT1	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3329 (0D01h) Interrupt	15	SPKR_DISABLE _DONE_EINT1	0	SPKOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Status 2	14	SPKL_DISABLE_DONE_EINT1	0	SPKOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	SPKR_ENABLE_DONE_EINT1	0	SPKOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	SPKL_ENABLE_DONE_EINT1	0	SPKOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3330 (0D02h) Interrupt Status 3	15	SPK_OVERHEAT_WARN_EINT1	0	Speaker Overheat Warning Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	SPK_OVERHEAT_EINT1	0	Speaker Overheat Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	13	HPDET_EINT1	0	Headphone Detect Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	MICDET_EINT1	0	Microphone / Accessory Detect Interrupt (Detection event triggered) Note: Cleared when a '1' is written.
	11	WSEQ_DONE_EINT1	0	Write Sequencer Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DRC1_SIG_DET_EINT1	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC2_LOCK_EINT1	0	ASRC2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	ASRC1_LOCK_EINT1	0	ASRC1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	UNDERCLOCKED_EINT1	0	Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	OVERCLOCKED_EINT1	0	Overclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	FLL2_LOCK_EINT1	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	FLL1_LOCK_EINT1	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	CLKGEN_ERR_EINT1	0	SYSCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	CLKGEN_ERR_ASYNC_EINT1	0	ASYNCCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3331 (0D03h) Interrupt	12	CTRLIF_ERR_EINT1	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Status 4	11	MIXER_DROPPED_SAMPLE_EINT1		Mixer Dropped Sample Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	ASYNC_CLK_ENA_LOW_EINT1	0	ASYNC_CLK_ENA Interrupt (Triggered on ASYNCCLK shut-down) Note: Cleared when a '1' is written.
	9	SYSCLK_ENA_LOW_EINT1	0	SYSCLK_ENA Interrupt (Triggered on SYSCLK shut-down) Note: Cleared when a '1' is written.
	8	ISRC1_CFG_ERR_EINT1	0	ISRC1 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	ISRC2_CFG_ERR_EINT1	0	ISRC2 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	LINER_ENABLE_DONE_EINT1	0	LINEOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	LINEL_ENABLE_DONE_EINT1	0	LINEOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HPR_ENABLE_DONE_EINT1	0	HPOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_ENABLE_DONE_EINT1	0	HPOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3332 (0D04h) Interrupt Status 5	14	EP_ENABLE_DONE_EINT1	0	EPOUT Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	EP_DISABLE_DONE_EINT1	0	EPOUT Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	LINER_DISABLE_DONE_EINT1	0	LINEOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	LINEL_DISABLE_DONE_EINT1	0	LINEOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	HPR_DISABLE_DONE_EINT1	0	HPOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	HPL_DISABLE_DONE_EINT1	0	HPOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	8	BOOT_DONE_EINT1	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	ASRC_CFG_ERR_EINT1	0	ASRC Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	FLL2_CLOCK_OK_EINT1	0	FLL2 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	FLL1_CLOCK_OK_EINT1	0	FLL1 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3333 (0D05h) Interrupt Status 6	14	SPK_SHUTDOWN_EINT1	0	Speaker Shutdown Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	SPKR_SHORT_EINT1	0	SPKOUTR Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	SPKL_SHORT_EINT1	0	SPKOUTL Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3336 (0D08h) to R3341 (0D0Dh)		IM_*	(see note)	For each *_EINT1 interrupt register in R3328 to R3333, a corresponding mask bit (IM_*) is provided in R3336 to R3341. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
		Note : The BOOT_DONE_EINT1 interrupt is '0' (un-masked) by default; all other interrupts are '1' (masked) by default.		
R3343 (0D0Fh) Interrupt Control	0	IM_IRQ1	0	IRQ1 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.
R3409 (0D51h) AOD IRQ1	7	MICD_CLAMP_FALL_EINT1	0	MICDET Clamp Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	6	MICD_CLAMP_RISE_EINT1	0	MICDET Clamp Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	GP5_FALL_EINT1	0	GP5 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	4	GP5_RISE_EINT1	0	GP5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	JD1_FALL_EINT1	0	JD1 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	2	JD1_RISE_EINT1	0	JD1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3411 (0D53h) AOD IRQ Mask IRQ1		IM_*	1	For each *_EINT1 interrupt register in R3409, a corresponding mask bit (IM_*) is provided in R3411. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt

Table 84 Interrupt 1 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3344 (0D10h) IRQ2 Status 1	3	GP4_EINT2	0	GPIO4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP3_EINT2	0	GPIO3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP2_EINT2	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT2	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3345 (0D11h) IRQ2 Status 2	15	SPKR_DISABLE_DONE_EINT2	0	SPKOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	14	SPKL_DISABLE_DONE_EINT2	0	SPKOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	SPKR_ENABLE_DONE_EINT2	0	SPKOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	SPKL_ENABLE_DONE_EINT2	0	SPKOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3346 (0D12h) IRQ2 Status 3	15	SPK_OVERHEAT_WARN_EINT2	0	Speaker Overheat Warning Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	SPK_OVERHEAT_EINT2	0	Speaker Overheat Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	13	HPDET_EINT2	0	Headphone Detect Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	MICDET_EINT2	0	Microphone / Accessory Detect Interrupt (Detection event triggered) Note: Cleared when a '1' is written.
	11	WSEQ_DONE_EINT2	0	Write Sequencer Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DRC1_SIG_DET_EINT2	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC2_LOCK_EINT2	0	ASRC2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	ASRC1_LOCK_EINT2	0	ASRC1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	UNDERCLOCKED_EINT2	0	Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	OVERCLOCKED_EINT2	0	Overclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	FLL2_LOCK_EINT2	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	FLL1_LOCK_EINT2	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	CLKGEN_ERR_EINT2	0	SYSCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	CLKGEN_ERR_ASYNC_EINT2	0	ASYNCCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3347 (0D13h) IRQ2 Status 4	12	CTRLIF_ERR_EINT2	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	MIXER_DROPPED_SAMPLE_EINT2		Mixer Dropped Sample Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	ASYNC_CLK_ENA_LOW_EINT2	0	ASYNC_CLK_ENA Interrupt (Triggered on ASYNCCLK shut-down) Note: Cleared when a '1' is written.
	9	SYSCLK_ENA_LOW_EINT2	0	SYSCLK_ENA Interrupt (Triggered on SYSCLK shut-down) Note: Cleared when a '1' is written.
	8	ISRC1_CFG_ERR_EINT2	0	ISRC1 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	ISRC2_CFG_ERR_EINT2	0	ISRC2 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	LINER_ENABLE_DONE_EINT2	0	LINEOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	LINEL_ENABLE_DONE_EINT2	0	LINEOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HPR_ENABLE_DONE_EINT2	0	HPOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_ENABLE_DONE_EINT2	0	HPOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3348 (0D14h) IRQ2 Status 5	14	EP_ENABLE_DONE_EINT2	0	EPOUT Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	EP_DISABLE_DONE_EINT2	0	EPOUT Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	LINER_DISABLE_DONE_EINT2	0	LINEOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	LINEL_DISABLE_DONE_EINT2	0	LINEOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	HPR_DISABLE_DONE_EINT2	0	HPOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	HPL_DISABLE_DONE_EINT2	0	HPOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	8	BOOT_DONE_EINT2	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	ASRC_CFG_ERR_EINT2	0	ASRC Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	FLL2_CLOCK_OK_EINT2	0	FLL2 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	FLL1_CLOCK_OK_EINT2	0	FLL1 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3349 (0D15h) IRQ2 Status 6	14	SPK_SHUTDOWN_EINT2	0	Speaker Shutdown Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	SPKR_SHORT_EINT2	0	SPKOUTR Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	SPKL_SHORT_EINT2	0	SPKOUTL Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3352 (0D18h) to R3357 (0D1Dh)		IM_*	(see note)	For each *_EINT2 interrupt register in R3344 to R3349, a corresponding mask bit (IM_*) is provided in R3352 to R3357. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
		Note : The BOOT_DONE_EINT2 interrupt is '0' (un-masked) by default; all other interrupts are '1' (masked) by default.		
R3359 (0D1Fh) IRQ2 Control	0	IM_IRQ2	0	IRQ2 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.
R3410 (0D52h) AOD IRQ2	7	MICD_CLAMP_FALL_EINT2	0	MICDET Clamp Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	6	MICD_CLAMP_RISE_EINT2	0	MICDET Clamp Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	GP5_FALL_EINT2	0	GP5 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	4	GP5_RISE_EINT2	0	GP5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	JD1_FALL_EINT2	0	JD1 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	JD1_RISE_EINT2	0	JD1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3412 (0D54h) AOD IRQ Mask IRQ2		IM_*	1	For each *_EINT2 interrupt register in R3410, a corresponding mask bit (IM_*) is provided in R3412. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt

Table 85 Interrupt 2 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3360 (0D20h) Interrupt Raw Status 1	15	SPKR_DISABLE_DONE_STS	0	SPKOUTR Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	14	SPKL_DISABLE_DONE_STS	0	SPKOUTL Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	13	SPKR_ENABLE_DONE_STS	0	SPKOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	12	SPKL_ENABLE_DONE_STS	0	SPKOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R3361 (0D21h) Interrupt Raw Status 2	15	SPK_OVERHEAT_WARN_STS	0	Speaker Overheat Warning Status 0 = Normal 1 = Warning temperature exceeded
	14	SPK_OVERHEAT_STS	0	Speaker Overheat Status 0 = Normal 1 = Shutdown temperature exceeded
	11	WSEQ_DONE_STS	0	Write Sequencer Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	9	DRC1_SIG_DET_STS	0	DRC1 Signal Detect Status 0 = Normal 1 = Signal detected
	8	ASRC2_LOCK_STS	0	ASRC2 Lock Status 0 = Not locked 1 = Locked
	7	ASRC1_LOCK_STS	0	ASRC1 Lock Status 0 = Not locked 1 = Locked
	6	UNDERCLOCKED_STS	0	Underclocked Error Status 0 = Normal 1 = Underclocked Error
	5	OVERCLOCKED_STS	0	Overclocked Error Status 0 = Normal 1 = Overclocked Error
	3	FLL2_LOCK_STS	0	FLL2 Lock Status 0 = Not locked 1 = Locked
	2	FLL1_LOCK_STS	0	FLL1 Lock Status 0 = Not locked 1 = Locked

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	CLKGEN_ERR_STS	0	SYSCLK Underclocked Error Status 0 = Normal 1 = Underclocked Error
	0	CLKGEN_ERR_ASYNC_STS	0	ASYNCCLK Underclocked Error Status 0 = Normal 1 = Underclocked Error
R3362 (0D22h) Interrupt Raw Status 3	12	CTRLIF_ERR_STS	0	Control Interface Error Status 0 = Normal 1 = Control Interface Error
	11	MIXER_DROPPED_SAMPLE_STS		Mixer Dropped Sample Status 0 = Normal 1 = Dropped Sample Error
	10	ASYNC_CLK_ENA_LOW_STS	0	ASYNC_CLK_ENA Status 0 = ASYNC_CLK_ENA is enabled 1 = ASYNC_CLK_ENA is disabled When a '0' is written to ASYNCCLK_ENA, then no other control register writes should be attempted until ASYNC_CLK_ENA_LOW_STS=1.
	9	SYSCLK_ENA_LOW_STS	0	SYSCLK_ENA Status 0 = SYSCLK_ENA is enabled 1 = SYSCLK_ENA is disabled When a '0' is written to SYSCLK_ENA, then no other control register writes should be attempted until SYSCLK_ENA_LOW_STS=1.
	8	ISRC1_CFG_ERR_STS	0	ISRC1 Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	7	ISRC2_CFG_ERR_STS	0	ISRC2 Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	3	LINER_ENABLE_DONE_STS	0	LINEOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	2	LINER_ENABLE_DONE_STS	0	LINEOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	1	HPR_ENABLE_DONE_STS	0	HPOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HPL_ENABLE_DONE_STS	0	HPOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R3363 (0D23h) Interrupt Raw Status 4	14	EP_ENABLE_DONE_STS	0	EPOUT Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	13	EP_DISABLE_DONE_STS	0	EPOUT Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	12	LINER_DISABLE_DONE_STS	0	LINEOUTR Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	11	LINER_DISABLE_DONE_STS	0	LINEOUTL Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	HPR_DISABLE_DONE_STS	0	HPOUTR Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	9	HPL_DISABLE_DONE_STS	0	HPOUTL Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	8	BOOT_DONE_STS	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
	3	ASRC_CFG_ERR_STS	0	ASRC Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	1	FLL2_CLOCK_OK_STS	0	FLL2 Clock OK Interrupt 0 = FLL2 Clock is not OK 1 = FLL2 Clock is OK
	0	FLL1_CLOCK_OK_STS	0	FLL1 Clock OK Interrupt 0 = FLL1 Clock is not OK 1 = FLL1 Clock is OK
R3364 (0D24h) Interrupt Raw Status 5	14	PWM_OVERCLOCKED_STS	0	Indicates an Overclocked Error condition for each respective sub-system. The bits are coded as: 0 = Normal 1 = Overclocked The OVERCLOCKED_STS bit will be asserted whenever any of these register bits is asserted.
	13	FX_CORE_OVERCLOCKED_STS	0	
	12	DAC_SYS_OVERCLOCKED_STS	0	
	11	DAC_WARP_OVERCLOCKED_STS	0	
	10	ADC_OVERCLOCKED_STS	0	
	9	MIXER_OVERCLOCKED_STS	0	
	7	AIF3_ASYNC_OVERCLOCKED_STS	0	
	6	AIF2_ASYNC_OVERCLOCKED_STS	0	
	5	AIF1_ASYNC_OVERCLOCKED_STS	0	
	3	AIF3_SYNC_OVERCLOCKED_STS	0	
	2	AIF2_SYNC_OVERCLOCKED_STS	0	
	1	AIF1_SYNC_OVERCLOCKED_STS	0	
	0	PAD_CTRL_OVERCLOCKED_STS	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3365 (0D25h) Interrupt Raw Status 6	15	SLIMBUS_SUBSYS_OVERCLOCKED_STS	0	Indicates an Overclocked Error condition for each respective sub-system. The bits are coded as: 0 = Normal 1 = Overclocked The OVERCLOCKED_STS bit will be asserted whenever any of these register bits is asserted.
	14	SLIMBUS_ASYNC_OVERCLOCKED_STS	0	
	13	SLIMBUS_SYNC_OVERCLOCKED_STS	0	
	12	ASRC_ASYNC_SYS_OVERCLOCKED_STS	0	
	11	ASRC_ASYNC_WARP_OVERCLOCKED_STS	0	
	10	ASRC_SYNC_SYS_OVERCLOCKED_STS	0	
	9	ASRC_SYNC_WARP_OVERCLOCKED_STS	0	
	1	ISRC2_OVERCLOCKED_STS	0	
	0	ISRC1_OVERCLOCKED_STS	0	
R3366 (0D26h) Interrupt Raw Status 7	15	SPDIF_SYNC_OVERCLOCKED_STS	0	Indicates an Underclocked or Overclocked Error condition for each respective sub-system. The bits are coded as: 0 = Normal 1 = Overclocked The UNDERCLOCKED_STS or OVERCLOCKED_STS bit (as applicable) will be asserted whenever any of these register bits is asserted.
	10	AIF3_UNDERCLOCKED_STS	0	
	9	AIF2_UNDERCLOCKED_STS	0	
	8	AIF1_UNDERCLOCKED_STS	0	
	6	ISRC2_UNDERCLOCKED_STS	0	
	5	ISRC1_UNDERCLOCKED_STS	0	
	4	FX_UNDERCLOCKED_STS	0	
	3	ASRC_UNDERCLOCKED_STS	0	
	2	DAC_UNDERCLOCKED_STS	0	
	1	ADC_UNDERCLOCKED_STS	0	
	0	MIXER_UNDERCLOCKED_STS	0	
R3368 (0D28h) Interrupt Raw Status 8	14	SPK_SHUTDOWN_STS	0	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)
	13	SPKOUTR_SHORT_STS	0	SPKOUTR Short Circuit Status 0 = Normal 1 = Short Circuit detected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12	SPKOUTL_SHORT_STS	0	SPKOUTL Short Circuit Status 0 = Normal 1 = Short Circuit detected
R3392 (0D40h) Interrupt Pin Status	1	IRQ2_STS	0	IRQ2 Status IRQ2_STS is the logical 'OR' of all unmasked _EINT2 interrupts. 0 = Not asserted 1 = Asserted
	0	IRQ1_STS	0	IRQ1 Status IRQ1_STS is the logical 'OR' of all unmasked _EINT1 interrupts. 0 = Not asserted 1 = Asserted
R3413 (0D55h) AOD IRQ Raw Status	3	MICD_CLAMP_STS	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active
	2	GP5_STS	0	GP5 Status 0 = Not asserted 1 = Asserted
	0	JD1_STS	0	JACKDET input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET pin is pulled 'low' on Jack insertion.)

Table 86 Interrupt Status

CLOCKING AND SAMPLE RATES

The WM8998 requires a clock reference for its internal functions and also for the input (ADC) paths, output (DAC) paths and digital audio interfaces. Under typical clocking configurations, all commonly-used audio sample rates can be derived directly from the external reference; for additional flexibility, the WM8998 incorporates two Frequency Locked Loop (FLL) circuits to perform frequency conversion and filtering.

External clock signals may be connected via MCLK1 and MCLK2. (These inputs are referenced to the DBVDD1 power domain.) In AIF Slave modes, the BCLK signals may be used as a reference for the system clocks. The SLIMbus interface can provide the clock reference, when used as the input to one of the FLLs. To avoid audible glitches, all clock configurations must be set up before enabling playback.

SYSTEM CLOCKING

The WM8998 supports two independent clock domains, referenced to the SYSCLK and ASYNCCLK system clocks respectively.

Up to five different sample rates may be independently selected for specific audio interfaces and other input/output signal paths. Each selected sample rate must be synchronised either to SYSCLK or to ASYNCCLK, as described later.

The two system clocks are independent (ie. not synchronised). Stereo full-duplex sample rate conversion is supported, allowing asynchronous audio data to be mixed and to be routed between independent interfaces. See “Digital Core” for further details.

Each subsystem within the WM8998 digital core is clocked at a dynamically-controlled rate, limited by the SYSCLK (or ASYNCCLK) frequency, as applicable. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK and ASYNCCLK frequencies are configured.

If the SUBSYS_MAX_FREQ bit is set to ‘0’, then the digital core clocking rate is restricted to a maximum of 24.576MHz (or 22.5792MHz), even if a higher system clock frequency is configured.

The maximum digital core clocking rates of 49.152MHz (or 45.1584MHz) are only supported when SUBSYS_MAX_FREQ is set to ‘1’, and the DCVDD voltage is 1.8V (nominal).

See “Recommended Operating Conditions” for details of the DCVDD operating conditions. Note that, if DCVDD is less than the minimum level for >24.576MHz clocking, then SUBSYS_MAX_FREQ must be set to ‘0’.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R353 (0161h) Dynamic Frequency Scaling 1	0	SUBSYS_MAX_FREQ	0	Digital Core Clocking Limit Sets the maximum digital core clocking rate. The higher rate should only be selected when the DCVDD voltage is 1.8V (nominal). 0 = 24.576MHz (22.5792MHz) 1 = 49.152MHz (45.1584MHz)

Table 87 System Clocking

SAMPLE RATE CONTROL

The WM8998 supports two independent clock domains, referenced to SYSCLK and ASYNCCLK respectively.

Different sample rates may be selected for each of the audio interfaces (AIF1, AIF2, AIF3, SLIMbus), and for the input (ADC) and output (DAC) paths. Each of these must be referenced either to SYSCLK or to ASYNCCLK. (Note that the SLIMbus interface supports multiple sample rates, selected independently for each input or output channel.)

The WM8998 can support a maximum of five different sample rates at any time. The supported sample rates range from 8kHz to 192kHz.

Up to three different sample rates can be selected using the SAMPLE_RATE_1, SAMPLE_RATE_2 and SAMPLE_RATE_3 registers. These must each be numerically related to each other and to the SYSCLK frequency (further details of these requirements are provided in Table 88 and the accompanying text).

The remaining two sample rates can be selected using the ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2 registers. These sample rates must be numerically related to each other and to the ASYNCCLK frequency (further details of these requirements are provided in Table 89 and the accompanying text).

Each of the audio interfaces, input paths and output paths is associated with one of the sample rates selected by the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers.

Note that if any two interfaces are operating at the same sample rate, but are not synchronised, then one of these must be referenced to the ASYNCCLK domain, and the other to the SYSCLK domain.

Note that, when any of the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers is written to, the activation of the new setting is automatically synchronised by the WM8998 to ensure continuity of all active signal paths. The SAMPLE_RATE_n_STS and ASYNC_SAMPLE_RATE_n_STS registers provide readback of the sample rate selections that have been implemented.

There are some restrictions to be observed regarding the sample rate control configuration, as noted below:

- The input (ADC / Digital Microphone) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain.
- All external clock references (MCLK input or Slave mode AIF input) must be within 1% of the applicable register setting(s).
- The S/PDIF sample rate is valid from 32kHz to 192kHz.
- The Asynchronous Sample Rate Converter (ASRC) supports sample rates 11.025kHz, 12kHz, 22.05kHz, 24kHz, 44.1kHz and 48kHz only. The SYSCLK and ASYNCCLK sample rates must each be set to one of these valid sample rates.
- The Isochronous Sample Rate Converters (ISRCs) support sample rates 8kHz to 192kHz. For each ISRC, the higher sample rate must be an integer multiple of the lower rate. Integer ratios in the range 1 to 6 are supported on ISRC1; integer ratios in the range 1 to 24 are supported on ISRC2.

AUTOMATIC SAMPLE RATE DETECTION

The WM8998 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2 and AIF3). Note that this is only possible when the respective interface is operating in Slave mode (ie. when LRCLK and BCLK are inputs to the WM8998).

Automatic sample rate detection is enabled using the RATE_EST_ENA register bit. The LRCLK input pin selected for sample rate detection is set using the LRCLK_SRC register.

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. Note that the function will only detect sample rates that match one of the SAMPLE_RATE_DETECT_n registers.

If one of the selected audio sample rates is detected on the selected LRCLK input, then a Control Write Sequence will be triggered. A unique sequence of actions may be programmed for each of the detected sample rates. Note that the applicable control sequences must be programmed by the user for each detection outcome. See “Control Write Sequencer” for further details.

The TRIG_ON_STARTUP register controls whether the sample rate detection circuit responds to the initial detection of the applicable interface (ie. when the AIFn interface starts up).

When TRIG_ON_STARTUP=0, then the detection circuit will only respond (ie. trigger the Control Write Sequencer) to a change in the detected sample rate - the initial sample rate detection will be ignored. (Note that the ‘initial sample rate detection’ is the first detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers.)

When TRIG_ON_STARTUP=1, then the detection circuit will trigger the Control Write Sequencer whenever a selected sample rate is detected, including when the AIF interface starts up, or when the

sample rate detection is first enabled.

As described above, setting TRIG_ON_STARTUP=0 is designed to inhibit any response to the initial detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers. Note that, if the LRCLK_SRC setting is changed, or if the detection function is disabled and re-enabled, then a subsequent detection of a matching sample rate may trigger the Control Write Sequencer, regardless of the TRIG_ON_STARTUP setting.

There are some restrictions to be observed regarding the automatic sample rate detection, as noted below:

- The same sample rate must not be selected on more than one of the SAMPLE_RATE_DETECT_n registers.
- Sample rates 192kHz and 176.4kHz must not be selected concurrently.
- Sample rates 96kHz and 88.2kHz must not be selected concurrently.

The control registers associated with the automatic sample rate detection function are described in Table 90.

SYSCLK AND ASYNCCLK CONTROL

The SYSCLK and ASYNCCLK clocks may be provided directly from external inputs (MCLK, or slave mode BCLK inputs). Alternatively, the SYSCLK and ASYNCCLK clocks can be derived using the integrated FLL(s), with MCLK, BCLK, LRCLK or SLIMCLK as a reference.

The required SYSCLK frequency is dependent on the SAMPLE_RATE_n registers. Table 88 illustrates the valid SYSCLK frequencies for every supported sample rate.

The SYSCLK_FREQ and SYSCLK_FRAC registers are used to identify the applicable SYSCLK frequency. It is recommended that the highest possible SYSCLK frequency is selected.

The chosen SYSCLK frequency must be valid for all of the SAMPLE_RATE_n registers. It follows that all of the SAMPLE_RATE_n registers must select numerically-related values, ie. all from the same cell as represented in Table 88.

Sample Rate	SAMPLE_RATE_n	SYSCLK Frequency	SYSCLK_FREQ	SYSCLK_FRAC
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, or 49.152MHz	000, 001, 010, or 011	0
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz, or 45.1584MHz	000, 001, 010, or 011	1
Note that each of the SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.				

Table 88 SYSCLK Frequency Selection

The required ASYNCCLK frequency is dependent on the ASYNC_SAMPLE_RATE_n registers. Table 89 illustrates the valid ASYNCCLK frequencies for every supported sample rate.

The ASYNC_CLK_FREQ register is used to identify the applicable ASYNCCLK frequency. It is recommended that the highest possible ASYNCCLK frequency is selected.

Note that, if all the sample rates in the system are synchronised to SYSCLK, then the ASYNCCLK may not be required at all. In this case, the ASYNCCLK should be disabled (see Table 90), and the associated register values are not important.

Sample Rate	ASYNC_SAMPLE_RATE_n	ASYNCCLK Frequency	ASYNC_CLK_FREQ
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, or 49.152MHz	000, 001, 010, or 011
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz or 45.1584MHz	000, 001, 010, or 011
Note that each of the ASYNC_SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.			

Table 89 ASYNCCLK Frequency Selection

The WM8998 supports automatic clocking configuration. The programmable dividers associated with the ADCs, DACs and all Digital Core functions are configured automatically, with values determined from the SYSCLK_FREQ, SAMPLE_RATE_n, ASYNC_CLK_FREQ and ASYNC_SAMPLE_RATE_n fields.

Note that the digital audio interface (AIF) clocking rates must be configured separately.

The sample rates of each AIF, the input (ADC) paths, output (DAC) paths and Digital Core functions are selected as described in the respective sections. Stereo full-duplex sample rate conversion is supported in multiple configurations to allow digital audio to be routed between interfaces and for asynchronous audio data to be mixed. See “Digital Core” for further details.

The SYSCLK_SRC register is used to select the SYSCLK source, as described in Table 90. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The SYSCLK_FREQ and SYSCLK_FRAC registers are set according to the frequency of the selected SYSCLK source.

The SYSCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the SYSCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK frequency is configured.

If the SUBSYS_MAX_FREQ bit is set to ‘0’, then the digital core clocking rate is restricted to a maximum of 24.576MHz (or 22.5792MHz), even if a higher SYSCLK frequency is configured. The SUBSYS_MAX_FREQ should only be set to ‘1’ when the applicable DCVDD condition is satisfied, as described in Table 87.

The SAMPLE_RATE_n registers are set according to the sample rate(s) that are required by one or more of the WM8998 audio interfaces. The WM8998 supports sample rates ranging from 8kHz to 192kHz.

The SYSCLK signal is enabled by the register bit SYSCLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting SYSCLK_ENA=1. This bit should be set to 0 when reconfiguring the clock sources (see below for additional requirements when setting SYSCLK_ENA=0).

When disabling SYSCLK, note that all of the input, output or digital core functions associated with the SYSCLK clock domain must be disabled before setting SYSCLK_ENA=0.

When '0' is written to SYSCLK_ENA, the host processor must wait until the WM8998 has shut down the associated functions before issuing any other register write commands. The SYSCLK Enable status can be polled via the SYSCLK_ENA_LOW_STS bit (see Table 86), or else monitored using the Interrupt or GPIO functions.

The SYSCLK Enable status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". The corresponding Interrupt event indicates that the WM8998 has shut down the SYSCLK functions and is ready to accept register write commands.

The SYSCLK Enable status can be output directly on a GPIO pin as an external indication of the SYSCLK status. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The required control sequence for disabling SYSCLK is summarised below:

- Disable all SYSCLK-associated functions (inputs, outputs, digital core)
- Set SYSCLK_ENA = 0
- Wait until SYSCLK_ENA_LOW = 1 (or wait for the corresponding IRQ/GPIO event)

The ASYNC_CLK_SRC register is used to select the ASYNCCLK source, as described in Table 90. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The ASYNC_CLK_FREQ register is set according to the frequency of the selected ASYNCCLK source.

The ASYNCCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the ASYNCCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible ASYNCCLK frequency is configured.

If the SUBSYS_MAX_FREQ bit is set to '0', then the digital core clocking rate is restricted to a maximum of 24.576MHz (or 22.5792MHz), even if a higher ASYNCCLK frequency is configured. The SUBSYS_MAX_FREQ should only be set to '1' when the applicable DCVDD condition is satisfied, as described in Table 87.

The ASYNC_SAMPLE_RATE_n registers are set according to the sample rate(s) of any audio interface that is not synchronised to the SYSCLK clock domain.

The ASYNCCLK signal is enabled by the register bit ASYNC_CLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting ASYNC_CLK_ENA=1. This bit should be set to 0 when reconfiguring the clock sources (see below for additional requirements when setting ASYNC_CLK_ENA=0).

When disabling ASYNCCLK, note that all of the input, output or digital core functions associated with the ASYNCCLK clock domain must be disabled before setting ASYNC_CLK_ENA=0.

When '0' is written to ASYNC_CLK_ENA, the host processor must wait until the WM8998 has shut down the associated functions before issuing any other register write commands. The ASYNCCLK Enable status can be polled via the ASYNC_CLK_ENA_LOW_STS bit (see Table 86), or else monitored using the Interrupt or GPIO functions.

The ASYNCCLK Enable status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". The corresponding Interrupt event indicates that the WM8998 has shut down the ASYNCCLK functions and is ready to accept register write commands.

The ASYNCCLK Enable status can be output directly on a GPIO pin as an external indication of the ASYNCCLK status. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The required control sequence for disabling ASYNCCLK is summarised below:

- Disable all ASYNCCLK-associated functions (inputs, outputs, digital core)
- Set ASYNCCLK_ENA = 0
- Wait until ASYNCCLK_ENA_LOW = 1 (or wait for the corresponding IRQ/GPIO event)

The SYSCLK (and ASYNCCLK, when applicable) clocks must be configured and enabled before any audio path is enabled.

The WM8998 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable a signal path or processing function, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

An Underclocked Error condition is where there are insufficient clock cycles for the requested functionality, and increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported.

An Overclocked Error condition is where the requested functionality cannot be supported, as the clocking requirements of the requested configuration exceed the device limits.

The SYSCLK Underclocked condition, ASYNCCLK Underclocked condition, and other Clocking Error conditions can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

MISCELLANEOUS CLOCK CONTROLS

The WM8998 requires a 32kHz clock for miscellaneous de-bounce functions. This can be generated automatically from SYSCLK, or may be input directly as MCLK1 or MCLK2. The 32kHz clock source is selected using the CLK_32K_SRC register. The 32kHz clock is enabled using the CLK_32K_ENA register.

The 32kHz clock can be maintained in Sleep mode, if required for de-bouncing any of the configured Wake-Up signals (eg. JACKDET or GPIO5). Note that the 32kHz clock must be derived from the MCLK2 pin in this case (CLK_32K_SRC=01). See “Low Power Sleep Configuration” for more details of the Sleep mode.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The WM8998 provides integrated pull-down resistors on the MCLK1 and MCLK2 pins. This provides a flexible capability for interfacing with other devices.

The clocking scheme for the WM8998 is illustrated in Figure 64.

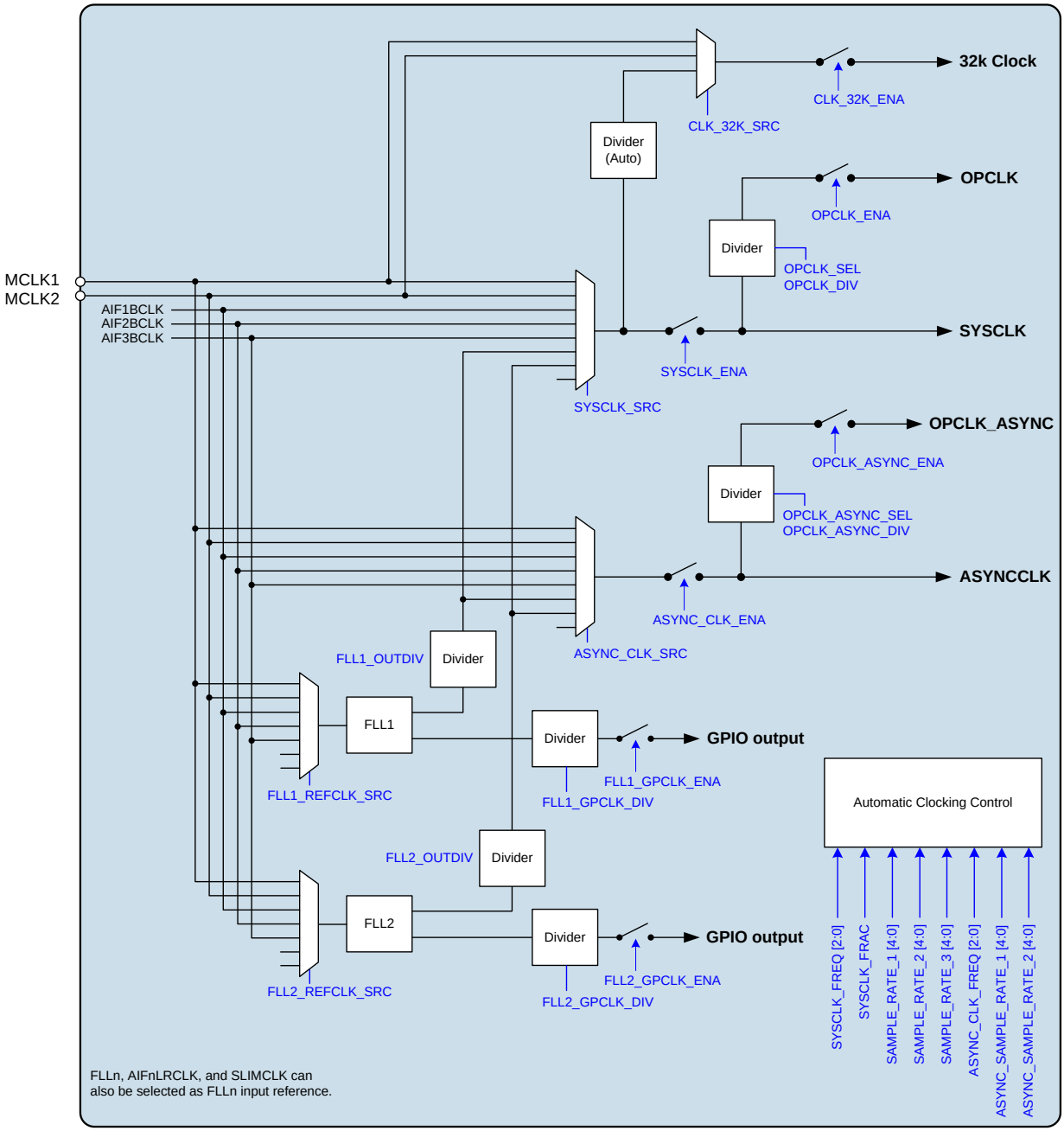


Figure 64 System Clocking

The WM8998 clocking control registers are described in Table 90.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R256 (0100h) Clock 32k 1	6	CLK_32K_ENA	0	32kHz Clock Enable 0 = Disabled 1 = Enabled
	1:0	CLK_32K_SRC [1:0]	10	32kHz Clock Source 00 = MCLK1 (direct) 01 = MCLK2 (direct) 10 = SYSCLK (automatically divided) 11 = Reserved
R257 (0101h) System Clock 1	15	SYSCLK_FRAC	0	SYSCLK Frequency 0 = SYSCLK is a multiple of 6.144MHz 1 = SYSCLK is a multiple of 5.6448MHz
	10:8	SYSCLK_FREQ [2:0]	011	SYSCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (ie. SAMPLE_RATE_n = 01XXX).
	6	SYSCLK_ENA	0	SYSCLK Control 0 = Disabled 1 = Enabled SYSCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.
	3:0	SYSCLK_SRC [3:0]	0100	SYSCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK All other codes are Reserved
R258 (0102h) Sample rate 1	4:0	SAMPLE_RATE_1 [4:0]	10001	Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R259 (0103h) Sample rate 2	4:0	SAMPLE_RATE_2 [4:0]	10001	Sample Rate 2 Select *Register coding is same as SAMPLE_RATE_1.*
R260 (0104h) Sample rate 3	4:0	SAMPLE_RATE_3 [4:0]	10001	Sample Rate 3 Select *Register coding is same as SAMPLE_RATE_1.*
R266 (010Ah) Sample rate 1 status	4:0	SAMPLE_RATE_1_STS [4:0]	00000	Sample Rate 1 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R267 (010Bh) Sample rate 2 status	4:0	SAMPLE_RATE_2_STS [4:0]	00000	Sample Rate 2 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R268 (010Ch) Sample rate 3 status	4:0	SAMPLE_RATE_3_STS [4:0]	00000	Sample Rate 3 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R274 (0112h) Async clock 1	10:8	ASYNC_CLK_FREQ [2:0]	011	ASYNCCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (ie. ASYNC_SAMPLE_RATE_n = 01XXX).
	6	ASYNC_CLK_ENA	0	ASYNCCLK Control 0 = Disabled 1 = Enabled ASYNCCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.
	3:0	ASYNC_CLK_SRC [3:0]	0101	ASYNCCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R275 (0113h) Async sample rate 1	4:0	ASYNC_SAMPLE_RATE_1 [4:0]	10001	ASYNC Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved
R276 (0114h) Async sample rate 2	4:0	ASYNC_SAMPLE_RATE_2 [4:0]	10001	ASYNC Sample Rate 2 Select *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R283 (011Bh) Async sample rate 1 status	4:0	ASYNC_SAMPLE_RATE_1_STS [4:0]	00000	ASYNC Sample Rate 1 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R284 (011Ch) Async sample rate 2 status	4:0	ASYNC_SAMPLE_RATE_2_STS [4:0]	00000	ASYNC Sample Rate 2 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R329 (0149h) Output system clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (ie. SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R330 (014Ah) Output async clock	15	OPCLK_ASYNC_ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_ASYNC_DIV [4:0]	00h	OPCLK_ASYNC Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_ASYNC_SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (ie. ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.
R338 (0152h) Rate Estimator 1	4	TRIG_ON_STARTUP	0	Automatic Sample Rate Detection Start-Up select 0 = Do not trigger Write Sequence on initial detection 1 = Always trigger the Write Sequencer on sample rate detection
	3:1	LRCLK_SRC [2:0]	000	Automatic Sample Rate Detection source 000 = AIF1LRCLK 010 = AIF2LRCLK 100 = AIF3LRCLK All other values are Reserved
	0	RATE_EST_ENA	0	Automatic Sample Rate Detection control 0 = Disabled 1 = Enabled
R339 (0153h) Rate Estimator 2	4:0	SAMPLE_RATE_DETECT_A [4:0]	00h	Automatic Detection Sample Rate A (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R340 (0154h) Rate Estimator 3	4:0	SAMPLE_RATE_DETECT_B [4:0]	00h	Automatic Detection Sample Rate B (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R341 (0155h) Rate Estimator 4	4:0	SAMPLE_RATE_DETECT_C [4:0]	00h	Automatic Detection Sample Rate C (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R342 (0156h) Rate Estimator 5	4:0	SAMPLE_RATE_DETECT_D [4:0]	00h	Automatic Detection Sample Rate D (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3104 (0C20h) Misc Pad Ctrl 1	13	MCLK2_PD	0	MCLK2 Pull-Down Control 0 = Disabled 1 = Enabled
R3105 (0C21h) Misc Pad Ctrl 2	12	MCLK1_PD	0	MCLK1 Pull-Down Control 0 = Disabled 1 = Enabled

Table 90 Clocking Control

In AIF Slave modes, it is important to ensure the applicable clock domain (SYSCLK or ASYNCCLK) is synchronised with the associated external LRCLK. This can be achieved by selecting an MCLK input that is derived from the same reference as the LRCLK, or can be achieved by selecting the external BCLK or LRCLK signal as a reference input to one of the FLLs, as a source for SYSCLK or ASYNCCLK.

If the AIF clock domain is not synchronised with the LRCLK, then clicks arising from dropped or repeated audio samples will occur, due to the inherent tolerances of multiple, asynchronous, system clocks. See “Applications Information” for further details on valid clocking configurations.

BCLK AND LRCLK CONTROL

The digital audio interfaces (AIF1, AIF2 and AIF3) use BCLK and LRCLK signals for synchronisation. In master mode, these are output signals, generated by the WM8998. In slave mode, these are input signals to the WM8998. It is also possible to support mixed master/slave operation.

The BCLK and LRCLK signals are controlled as illustrated in Figure 65. See the “Digital Audio Interface Control” section for further details of the relevant control registers.

Note that the BCLK and LRCLK signals are synchronised to SYSCLK or ASYNCCLK, depending upon the applicable clocking domain for the respective interface. See “Digital Core” for further details.

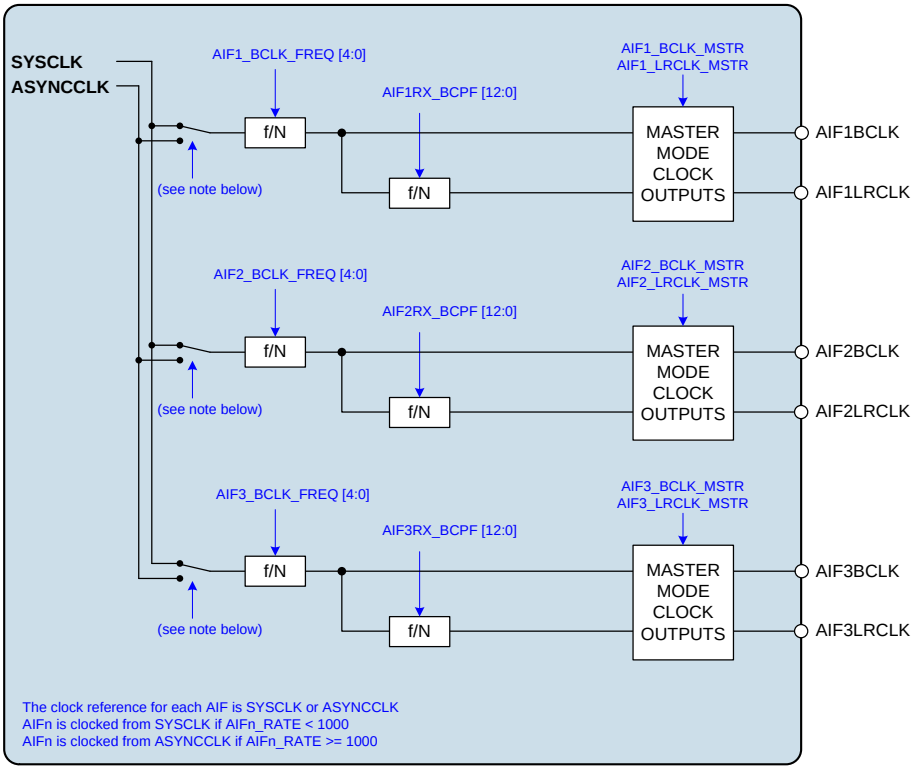


Figure 65 BCLK and LRCLK Control

CONTROL INTERFACE CLOCKING

Register map access is possible with or without a system clock. Clocking is provided from SYSCLK; the SYSCLK_SRC register selects the applicable SYSCLK source.

See “Control Interface” for further details of control register access.

FREQUENCY LOCKED LOOP (FLL)

Two integrated FLLs are provided to support the clocking requirements of the WM8998. These can be enabled and configured independently according to the available reference clocks and the application requirements. The reference clock may be a high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz).

The FLL is tolerant of jitter and may be used to generate a stable output clock from a less stable input reference. The FLL characteristics are summarised in “Electrical Characteristics”. Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Mode” section below. Configurable spread-spectrum modulation can be applied to the FLL outputs, to control EMI effects.

Each of the FLLs comprises two sub-systems - the ‘main’ loop and the ‘synchroniser’ loop; these can be used together to maintain best frequency accuracy and noise (jitter) performance across multiple use-cases. The two-loop design enables the FLL to synchronise effectively to an input clock that may be intermittent or noisy, whilst also achieving the performance benefits of a stable clock reference that may be asynchronous to the audio data.

The main loop takes a constant and stable clock reference as its input. For best performance, a high frequency (eg. 12.288MHz) reference is recommended. The main FLL loop will free-run without any clock reference if the input signal is removed; it can also be configured to initiate an output in the absence of any reference signal.

The synchroniser loop takes a separate clock reference as its input. The synchroniser input may be intermittent (eg. during voice calls only). The FLL uses the synchroniser input, when available, as the frequency reference. To achieve the designed performance advantage, the synchroniser input must be synchronous with the audio data.

Note that, if only a single clock input reference is used, this must be configured as the main FLL input reference. The synchroniser should be disabled in this case.

The synchroniser loop should only be used when the main loop clock reference is present. If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then the synchroniser should be disabled.

The FLL is enabled using the FLL*n*_ENA register bit (where *n* = 1 or 2 for the corresponding FLL). The FLL Synchroniser is enabled using the FLL*n*_SYNC_ENA register bit.

Note that the other FLL registers should be configured before enabling the FLL; the FLL*n*_ENA bit should be set as the final step of the FLL*n* enable sequence.

The FLL_SYNC_ENA bit should not be changed if FLL*n*_ENA = 1; the FLLn_ENA bit should be cleared before changing FLL*n*_SYNC_ENA.

The FLL supports configurable free-running operation, using the FLL*n*_FREERUN register bits described in the next section. Note that, once the FLL output has been established, the FLL will always free-run when the input reference clock is stopped, regardless of the FLL*n*_FREERUN bits.

To disable the FLL while the input reference clock has stopped, the respective FLL*n*_FREERUN bit must be set to ‘1’, before setting the FLL*n*_ENA bit to ‘0’.

When changing any of the FLL configuration fields, it is recommended that the digital circuit be disabled via FLL*n*_ENA and then re-enabled after the other register settings have been updated. If the FLL configuration is changed while the FLL is enabled, the respective FLL*n*_FREERUN bit should be set before updating any other FLL fields. A minimum delay of 32µs should be allowed between setting FLL*n*_FREERUN and writing to the required FLL register fields. The FLL*n*_FREERUN bit should remain set until after the FLL has been reconfigured.

Note that, if the FLL*n*_N or FLL*n*_THETA fields are changed while the FLL is enabled, the FLL*n*_CTRL_UPD bit must also be written, as described below. As a general rule, however, it is recommended to configure the FLL (and FLL Synchroniser, if applicable), before setting the

corresponding _ENA register bit(s).

The FLL configuration requirements are illustrated in Figure 66.

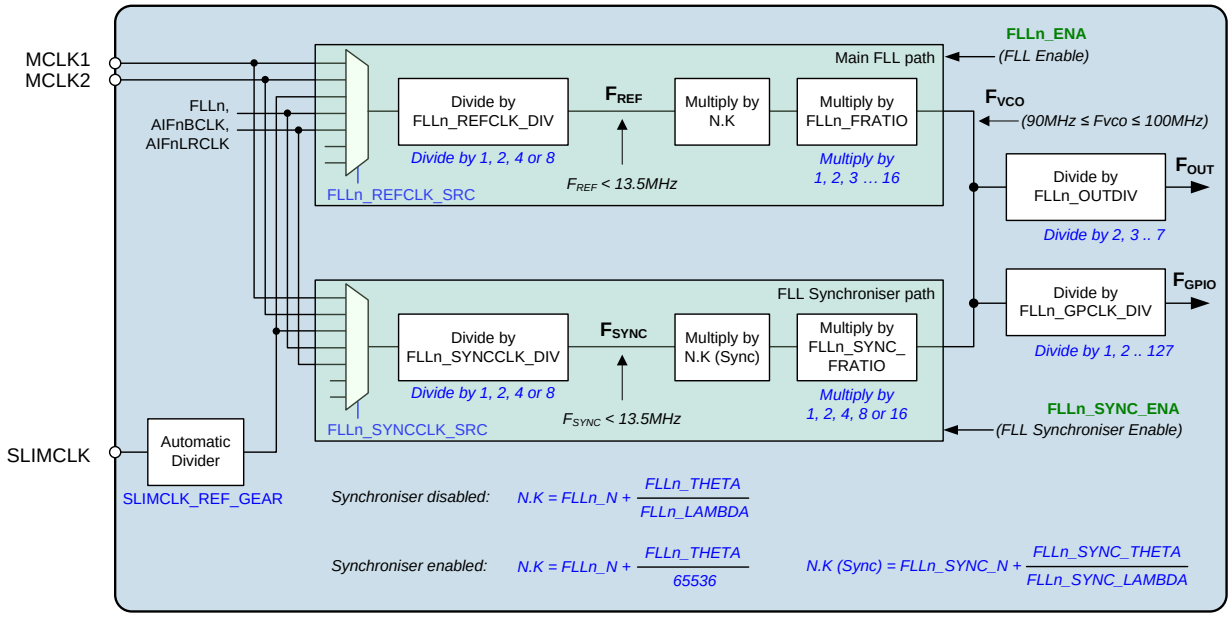


Figure 66 FLL Configuration

The procedure for configuring the FLL is described below. Note that the configuration of the main FLL path and the FLL Synchroniser path are very similar. One or both paths must be configured, depending on the application requirements:

- If a single clock input reference is used, then only the main FLL path should be used.
- If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then only the main FLL path should be used.
- If two clock input references are used, then the constant or low-noise clock is configured on the main FLL path, and the high-accuracy clock is configured on the FLL synchroniser path. Note that the synchroniser input must be synchronous with the audio data.

The following description is applicable to FLL1 and FLL2. The associated register control fields are described in Table 95 and Table 96 respectively.

The main input reference is selected using FLLn_REFCLK_SRC. The synchroniser input reference is selected using FLLn_SYNCCLK_SRC. The available options in each case comprise MCLK1, MCLK2, SLIMCLK, AIFnBCLK, AIFnLRCLK, or the output from another FLL.

The SLIMCLK reference is controlled by an adaptive divider on the external SLIMCLK input. The divider automatically adapts to the SLIMbus Clock Gear, to provide a constant reference frequency for the FLL. See “SLIMbus Interface Control” for details.

The FLL*n*_REFCLK_DIV field controls a programmable divider on the main input reference. The FLL*n*_SYNCCLK_DIV field controls a programmable divider on the synchroniser input reference. Each input can be divided by 1, 2, 4 or 8. These registers should be set to bring each reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected. (Note that additional guidelines also apply, as described below.)

The FLL output frequency, relative to the main input reference F_{REF}, is directly determined from FLL*n*_FRATIO, FLL*n*_OUTDIV and the real number represented by N.K.

The integer value, N, is held in the FLL*n*_N register field. The fractional portion, K, is determined by the FLL*n*_THETA and FLL*n*_LAMBDA fields.

The FLL output frequency is generated according to the following equation:

$F_{OUT} = (F_{VCO} / FLLn_OUTDIV)$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$F_{VCO} = (F_{REF} \times N.K \times FLLn_FRATIO)$

F_{REF} is the input frequency, as determined by FLL*n*_REFCLK_DIV.

F_{VCO} must be in the range 90MHz to 100MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie on or between the frequencies quoted above cannot be guaranteed across the full range of device operating conditions.

In order to follow the above requirements for F_{VCO}, the value of FLL*n*_OUTDIV should be selected according to the desired output F_{OUT}. The divider, FLL*n*_OUTDIV, must be set so that F_{VCO} is in the range 90MHz to 100MHz. The available divisions are integers from 2 to 7. Some typical settings of FLL*n*_OUTDIV are noted in Table 91.

OUTPUT FREQUENCY F_{OUT}	FLL*n*_OUTDIV
22.5 MHz to 26 MHz	100 (divide by 4)
45 MHz to 50 MHz	010 (divide by 2)

Table 91 Selection of FLL*n*_OUTDIV

The FLL*n*_FRATIO field selects the frequency division ratio of the FLL input. The FLL*n*_GAIN field is used to optimise the FLL, according to the input frequency. As a general guide, these fields should be selected as described in Table 92. (Note that additional guidelines also apply, as described below.)

REFERENCE FREQUENCY F_{REF}	FLL*n*_FRATIO	FLL*n*_GAIN
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)
128kHz - 256kHz	3h (divide by 4)	0h (1x gain)
64kHz - 128kHz	7h (divide by 8)	0h (1x gain)
Less than 64kHz	Fh (divide by 16)	0h (1x gain)

Table 92 Selection of FLL*n*_FRATIO and FLL*n*_GAIN

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$F_{VCO} = (F_{OUT} \times FLLn_OUTDIV)$

The value of N.K can then be determined as follows:

$N.K = F_{VCO} / (FLLn_FRATIO \times F_{REF})$

Note that, in the above equations:

FLL*n*_OUTDIV is the F_{OUT} clock ratio.

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable.

FLL*n*_FRATIO is the F_{VCO} clock ratio (1, 2, 3 … 16).

If the above equations produce an integer value for N.K, then the value of FLL*n*_FRATIO should be adjusted to a different, odd-number division (eg. divide by 3), and the value of N.K re-calculated. A non-integer value of N.K is recommended for best performance of the FLL. (If possible, the FLL*n*_FRATIO value should be decreased to the nearest alternative odd-number division. If a suitable lower value does not exist, FLL*n*_FRATIO should be increased to the nearest odd-number division instead.)

After the value of FLL*n*_FRATIO has been determined, the input frequency, F_{REF}, must be compared with the maximum frequency limit noted in Table 93. If the input frequency (after division by FLL*n*_REFCLK_DIV) is higher than the applicable limit, then the FLL*n*_REFCLK_DIV division ratio should be increased, and the value of N.K re-calculated. (Note that the same value of FLL*n*_FRATIO as already calculated should be used, when deriving the new value of N.K.)

FLL*n*_FRATIO	REFERENCE FREQUENCY F_{REF} - MAXIMUM VALUE
0h (divide by 1)	13.5 MHz
1h (divide by 2)	6.144 MHz
2h (divide by 3)	
3h (divide by 4)	3.072 MHz
4h (divide by 5)	
5h (divide by 6)	2.8224 MHz
6h (divide by 7)	
7h (divide by 8)	1.536 MHz
8h (divide by 9)	
9h (divide by 10)	
Ah (divide by 11)	
Bh (divide by 12)	
Ch (divide by 13)	
Dh (divide by 14)	
Eh (divide by 15)	
Fh (divide by 16)	768 kHz

Table 93 Maximum FLL input frequency (function of FLLn_FRATIO)

The value of N is held in the FLL*n*_N register field.

The value of K is determined by the FLL*n*_THETA and FLL*n*_LAMBDA fields, as described later.

The FLL*n*_N, FLL*n*_THETA and FLL*n*_LAMBDA fields are all coded as integers (LSB = 1).

If the FLL*n*_N or FLL*n*_THETA registers are updated while the FLL is enabled (FLL*n*_ENA=1), then the new values will only be effective when a '1' is written to the FLL*n*_CTRL_UPD bit. This makes it possible to update the two registers simultaneously, without disabling the FLL.

Note that, when the FLL is disabled (FLL*n*_ENA=0), then the FLL*n*_N and FLL*n*_THETA registers can be updated without writing to the FLL*n*_CTRL_UPD bit.

The values of FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described later.

A similar procedure applies for the deriviation of the FLL Synchroniser parameters - assuming that this function is used.

The FLL*n*_SYNC_FRATIO field selects the frequency division ratio of the FLL synchroniser input. The FLL*n*_GAIN and FLL*n*_SYNC_DFSAT fields are used to optimise the FLL, according to the input frequency. These fields should be set as described in Table 94.

Note that the FLL*n*_SYNC_FRATIO register coding is not the same as the FLL*n*_FRATIO register.

SYNCHRONISER FREQUENCY F_{SYNC}	FLL*n*_SYNC_FRATIO	FLLn_SYNC_GAIN	FLLn_SYNC_DFSAT
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)	0 (wide bandwidth)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)	0 (wide bandwidth)
128kHz - 256kHz	2h (divide by 4)	0h (1x gain)	0 (wide bandwidth)
64kHz - 128kHz	3h (divide by 8)	0h (1x gain)	1 (narrow bandwidth)
Less than 64kHz	4h (divide by 16)	0h (1x gain)	1 (narrow bandwidth)

Table 94 Selection of FLL*n*_SYNC_FRATIO, FLL*n*_SYNC_GAIN, FLL*n*_SYNC_DFSAT

The FLL operating frequency, F_{VCO}, is the same frequency calculated as described above.

The value of N.K (Sync) can then be determined as follows:

N.K (Sync) = F_{VCO} / (FLL*n*_SYNC_FRATIO x F_{SYNC})

Note that, in the above equations:

F_{SYNC} is the synchroniser input frequency, after division by FLL*n*_SYNCCLK_DIV, where applicable.

FLL*n*_SYNC_FRATIO is the F_{VCO} clock ratio (1, 2, 4, 8 or 16).

The value of N (Sync) is held in the FLL*n*_SYNC_N register field.

The value of K (Sync) is determined by the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields.

The FLL*n*_SYNC_N, FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields are all coded as integers (LSB = 1).

In Fractional Mode, with the synchroniser disabled (K > 0, and FLL*n*_SYNC_ENA = 0), the register fields FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described below.

The equivalent procedure is also used to derive the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA register values from the corresponding synchroniser parameters. (This is only required if the synchroniser is enabled.)

Calculate GCD(FLL) using the 'Greatest Common Denominator' function:

GCD(FLL) = GCD(FLL*n*_FRATIO x F_{REF}, F_{VCO})

where GCD(x, y) is the greatest common denominator of x and y

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable.

Next, calculate FLL*n*_THETA and FLL*n*_LAMBDA using the following equations:

FLL*n*_THETA = (F_{VCO} - (FLL_N x FLL*n*_FRATIO x F_{REF})) / GCD(FLL)

FLL*n*_LAMBDA = (FLL*n*_FRATIO x F_{REF}) / GCD(FLL)

Note that, in the operating conditions described above, the values of FLL*n*_THETA and FLL*n*_LAMBDA must be co-prime (ie. not divisible by any common integer). The calculation above ensures that the values will be co-prime. The value of K must be a fraction less than 1 (ie. FLL*n*_THETA must be less than FLL*n*_LAMBDA).

In Fractional Mode, with the synchroniser enabled (K > 0, and FLLn_SYNC_ENA = 1), the value of FLL*n*_THETA is calculated as described below. The value of FLLn_LAMBDA is ignored in this case.

FLLn_THETA = K x 65536

The FLL control registers are described in Table 95 and Table 96. Example settings for a variety of reference frequencies and output frequencies are shown in Table 99.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1 Control 1	0	FLL1_ENA	0	FLL1 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 enable sequence, ie. after the other FLL registers have been configured.
R370 (0172h) FLL1 Control 2	15	FLL1_CTRL_UPD	0	FLL1 Control Update Write '1' to apply the FLL1_N and FLL1_THETA register settings. (Only valid when FLL1_ENA=1)
	9:0	FLL1_N [9:0]	008h	FLL1 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.
R371 (0173h) FLL1 Control 3	15:0	FLL1_THETA [15:0]	0018h	FLL1 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.
R372 (0174h) FLL1 Control 4	15:0	FLL1_LAMBDA [15:0]	007Dh	FLL1 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1.
R373 (0175h) FLL1 Control 5	11:8	FLL1_FRATIO [3:0]	0h	FLL1 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
	3:1	FLL1_OUTDIV [2:0]	010	FLL1 F_{OUT} clock divider 000 = Reserved 001 = Reserved 010 = Divide by 2 011 = Divide by 3 100 = Divide by 4 101 = Divide by 5 110 = Divide by 6 111 = Divide by 7 (F_{OUT} = F_{VCO} / FLL1_OUTDIV)
R374 (0176h) FLL1 Control 6	7:6	FLL1_REFCLK_DIV [1:0]	00	FLL1 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL1_REFCLK_SRC	0000	FLL1 Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R377 (0179h) FLL1 Control 7	5:2	FLL1_GAIN [3:0]	0000	FLL1 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R385 (0181h) FLL1 Synchroniser 1	0	FLL1_SYNC_ENA	0	FLL1 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 synchroniser enable sequence, ie. after the other synchroniser registers have been configured.
R386 (0182h) FLL1 Synchroniser 2	9:0	FLL1_SYNC_N [9:0]	000h	FLL1 Integer multiply for F_{SYNC} (LSB = 1)
R387 (0183h) FLL1 Synchroniser 3	15:0	FLL1_SYNC_THETA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R388 (0184h) FLL1 Synchroniser 4	15:0	FLL1_SYNC_LAMBDA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R389 (0185h) FLL1 Synchroniser 5	10:8	FLL1_SYNC_FRATIO [2:0]	000	FLL1 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R390 (0186h) FLL1 Synchroniser 6	7:6	FLL1_SYNCCLK_DIV [1:0]	00	FLL1 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL1_SYNCCLK_SRC	0000	FLL1 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R391 (0187h) FLL1 Synchroniser 7	5:2	FLL1_SYNC_GAIN [3:0]	0000	FLL1 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
	0	FLL1_SYNC_DFSAT	1	FLL1 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 95 FLL1 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R401 (0191h) FLL2 Control 1	0	FLL2_ENA	0	FLL2 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 enable sequence, ie. after the other FLL registers have been configured.
R402 (0192h) FLL2 Control 2	15	FLL2_CTRL_UPD	0	FLL2 Control Update Write '1' to apply the FLL2_N and FLL2_THETA register settings. (Only valid when FLL2_ENA=1)
	9:0	FLL2_N [9:0]	008h	FLL2 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R403 (0193h) FLL2 Control 3	15:0	FLL2_THETA [15:0]	0018h	FLL2 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.
R404 (0194h) FLL2 Control 4	15:0	FLL2_LAMBDA [15:0]	007Dh	FLL2 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1.
R405 (0195h) FLL2 Control 5	11:8	FLL2_FRATIO [3:0]	0h	FLL2 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
	3:1	FLL2_OUTDIV [2:0]	010	FLL2 F_{OUT} clock divider 000 = Reserved 001 = Reserved 010 = Divide by 2 011 = Divide by 3 100 = Divide by 4 101 = Divide by 5 110 = Divide by 6 111 = Divide by 7 (F_{OUT} = F_{VCO} / FLL2_OUTDIV)
R406 (0196h) FLL2 Control 6	7:6	FLL2_REFCLK_ DIV [1:0]	00	FLL2 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL2_REFCLK_S RC	0000	FLL2 Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R409 (0199h) FLL2 Control 7	5:2	FLL2_GAIN [3:0]	0000	FLL2 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R417 (01A1h) FLL2 Synchroniser 1	0	FLL2_SYNC_ENA	0	FLL2 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 synchroniser enable sequence, ie. after the other synchroniser registers have been configured.
R418 (01A2h) FLL2 Synchroniser 2	9:0	FLL2_SYNC_N [9:0]	000h	FLL2 Integer multiply for F_{SYNC} (LSB = 1)
R419 (01A3h) FLL2 Synchroniser 3	15:0	FLL2_SYNC_THETA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R420 (01A4h) FLL2 Synchroniser 4	15:0	FLL2_SYNC_LAMBDA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R421 (01A5h) FLL2 Synchroniser 5	10:8	FLL2_SYNC_FRATIO [2:0]	000	FLL2 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16
R422 (01A6h) FLL2 Synchroniser 6	7:6	FLL2_SYNCCLK_DIV [1:0]	00	FLL2 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL2_SYNCCLK _SRC	0000	FLL2 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R423 (01A7h) FLL2 Synchroni ser 7	5:2	FLL2_SYNC_GAI N [3:0]	0000	FLL2 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
	0	FLL2_SYNC_DF SAT	1	FLL2 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 96 FLL2 Register Map

FREE-RUNNING FLL MODE

The FLL can generate a clock signal even when no external reference is available. This may be because the normal input reference has been interrupted, or may be during a standby or start-up period when no initial reference clock is available.

Free-running FLL mode is enabled using the FLLn_FREERUN register. (Note that FLLn_ENA must also be enabled in Free-running FLL mode.)

In Free-running FLL mode, the normal feedback mechanism of the FLL is halted, and the FLL oscillates independently of the external input reference(s).

If the FLL was previously operating normally, (with an input reference clock), then the FLL output frequency will remain unchanged when Free-running FLL mode is enabled. The FLL output will be independent of the input reference while operating in free-running mode with FLLn_FREERUN=1.

The main FLL loop will always continue to free-run if the input reference clock is stopped (regardless of the FLLn_FREERUN setting). If FLLn_FREERUN=0, the FLL will re-lock to the input reference whenever it is available.

In free-running mode, (with FLLn_FREERUN=1), the FLL integrator value (part of the feedback mechanism) can be commanded directly using the FLLn_FRC_INTEG_VAL register. The integrator value in this register is applied to the FLL when a ‘1’ is written to the FLLn_FRC_INTEG_UPD bit.

If the FLL is started up in free-running mode, (ie. it was not previously running), then the default value of FLLn_FRC_INTEG_VAL will be applied.

The FLL integrator value (part of the feedback mechanism) can be read from the FLLn_INTEG register; the value of this field may be stored for later use. Note that the readback value of the FLLn_INTEG register is only valid when FLLn_FREERUN=1, and the FLLn_INTEG_VALID bit is set.

The FLL integrator setting does not ensure a specific output frequency for the FLL across all devices and operating conditions; some level of variation will apply.

The free-running FLL clock may be selected as the SYSCLK source or ASYNCCLK source as shown Figure 64.

The control registers applicable to Free-running FLL mode are described in Table 97.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1 Control 1	1	FLL1_FREERUN	1	FLL1 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R375 (0177h) FLL1 Loop Filter Test 1	15	FLL1_FRC_INTEG_UPD	0	Write '1' to apply the FLL1_FRC_INTEG_VAL setting. (Only valid when FLL1_FREERUN=1)
	11:0	FLL1_FRC_INTEG_VAL [11:0]	181h	FLL1 Forced Integrator Value
R376 (0178h) FLL1 NCO Test 0	15	FLL1_INTEG_VALID	0	FLL1 Integrator Valid Indicates if the FLL1_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL1_INTEG [11:0]	000h	FLL1 Integrator Value (Read-only) Indicates the current FLL1 integrator setting. Only valid when FLL1_INTEG_VALID = 1.
R401 (0191h) FLL2 Control 1	1	FLL2_FREERUN	0	FLL2 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R407 (0197h) FLL2 Loop Filter Test 1	15	FLL2_FRC_INTEG_UPD	0	Write '1' to apply the FLL2_FRC_INTEG_VAL setting. (Only valid when FLL2_FREERUN=1)
	11:0	FLL2_FRC_INTEG_VAL [11:0]	000h	FLL2 Forced Integrator Value
R408 (0198h) FLL2 NCO Test 0	15	FLL2_INTEG_VALID	0	FLL2 Integrator Valid Indicates if the FLL2_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL2_INTEG [11:0]	000h	FLL2 Integrator Value (Read-only) Indicates the current FLL2 integrator setting. Only valid when FLL2_INTEG_VALID = 1.

Table 97 Free-Running FLL Mode Control

SPREAD SPECTRUM FLL CONTROL

The WM8998 can apply modulation to the FLL outputs, using spread spectrum techniques. This can be used to control the EMI characteristics of the circuits that are clocked via the FLLs.

Each of the FLLs can be individually configured for Triangle modulation, Zero Mean Frequency Modulation (ZMFM) or Dither. The amplitude and frequency parameters of the spread spectrum functions is also programmable, using the registers described in Table 98.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R393 (0189h) FLL1 Spread Spectrum	5:4	FLL1_SS_AMPL [1:0]	00	FLL1 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL1_SS_FREQ [1:0]	00	FLL1 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL1_SS_SEL [1:0]	00	FLL1 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither
R425 (01A9h) FLL2 Spread Spectrum	5:4	FLL2_SS_AMPL [1:0]	00	FLL2 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL2_SS_FREQ [1:0]	00	FLL2 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL2_SS_SEL [1:0]	00	FLL2 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither

Table 98 FLL Spread Spectrum Control

FLL INTERRUPTS AND GPIO OUTPUT

For each FLL, the WM8998 supports an 'FLL Clock OK' signal which, when asserted, indicates that the FLL has started up and is providing an output clock. Each FLL also supports an 'FLL Lock' signal which indicates whether FLL Lock has been achieved.

The FLL Clock OK status and FLL Lock status are inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". Note that these Interrupt signals are de-bounced, and require clocking to be present in order to assert the respective Interrupt; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL signals.

The FLL Clock OK and FLL Lock signals can be output directly on a GPIO pin as an external indication of the FLL status. See "General Purpose Input / Output" to configure a GPIO pin for these functions. (These GPIO outputs are not de-bounced, and do not require clocking to be present.)

Clock output signals derived from the FLL can be output on a GPIO pin. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The FLL clocking configuration is illustrated in Figure 66.

EXAMPLE FLL CALCULATION

The following example illustrates how to derive the FLL1 registers to generate 49.152 MHz output (F_{OUT}) from a 12.000 MHz reference clock (F_{REF}). Note that, for this calculation, it is assumed that the synchroniser is disabled.

- Set FLL1_REFCLK_DIV in order to generate F_{REF} <=13.5MHz:
  FLL1_REFCLK_DIV = 00 (divide by 1)
- Set FLL1_OUTDIV for the required output frequency as shown in Table 91:-
  F_{OUT} = 49.152 MHz, therefore FLL1_OUTDIV = 2h (divide by 2)
- Set FLL1_FRATIO for the given reference frequency as shown in Table 92:
  F_{REF} = 12MHz, therefore FLL1_FRATIO = 0h (divide by 1)
- Calculate F_{VCO} as given by $F_{VCO} = F_{OUT}$ x FLL1_OUTDIV:-
  F_{VCO} = 49.152 x 2 = 98.304MHz
- Calculate N.K as given by N.K = F_{VCO} / (FLL1_FRATIO x F_{REF}):
  N.K = 98.304 / (1 x 12) = 8.192
- Determine FLL1_N from the integer portion of N.K:-
  FLL1_N = 8 (008h)
- Determine GCD(FLL), as given by GCD(FLL) = GCD(FLL1_FRATIO x F_{REF}, F_{VCO}):
  GCD(FLL) = GCD(1 x 12000000, 98304000) = 96000
- Determine FLL1_THETA, as given by
  FLL1_THETA = (F_{VCO} - (FLL1_N x FLL1_FRATIO x F_{REF})) / GCD(FLL):
  FLL1_THETA = (98304000 - (8 x 1 x 12000000)) / 96000
  FLL1_THETA = 24 (0018h)
- Determine FLL_LAMBDA, as given by
  FLL1_LAMBDA = (FLL1_FRATIO x F_{REF}) / GCD(FLL):
  FLL1_LAMBDA = (1 x 12000000) / 96000
  FLL1_LAMBDA = 125 (007Dh)

EXAMPLE FLL SETTINGS

Table 99 provides example FLL settings for generating 49.152MHz SYSCLK from a variety of low and high frequency reference inputs. Note that, in these examples, it is assumed that the synchroniser is disabled.

FLL (Main Loop) Settings									
F_{SOURCE}	F_{OUT} (MHz)	F_{REF} Divider	N.K	FRATIO	F_{VCO} (MHz)	OUTDIV	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	49.152	1	204.8	15	98.304	2	0CCh	0004h	0005h
32.768 kHz	49.152	1	187.5	16	98.304	2	0BBh	0001h	0002h
48 kHz	49.152	1	136.5333	15	98.304	2	088h	0008h	000Fh
128 kHz	49.152	1	109.7143	7	98.304	2	06Dh	0005h	0007h
512 kHz	49.152	1	38.4	5	98.304	2	026h	0002h	0005h
1.536 MHz	49.152	1	21.3333	3	98.304	2	015h	0001h	0003h
3.072 MHz	49.152	1	10.6667	3	98.304	2	00Ah	0002h	0003h
11.2896 MHz	49.152	1	8.7075	1	98.304	2	008h	0068h	0093h
12.000 MHz	49.152	1	8.192	1	98.304	2	008h	0018h	007Dh
12.288 MHz	49.152	2	5.3333	3	98.304	2	005h	0001h	0003h
13.000 MHz	49.152	1	7.5618	1	98.304	2	007h	0391h	0659h
19.200 MHz	49.152	2	10.24	1	98.304	2	00Ah	0006h	0019h
24 MHz	49.152	2	8.192	1	98.304	2	008h	0018h	007Dh
26 MHz	49.152	2	7.5618	1	98.304	2	007h	0391h	0659h
27 MHz	49.152	2	7.2818	1	98.304	2	007h	013Dh	0465h

F_{OUT} = (F_{SOURCE} / F_{REF} Divider) * N.K * FRATIO / OUTDIV
The values of N and K are contained in the FLLn_N, FLLn_THETA and FLLn_LAMBDA registers as shown above.
See Table 95 and Table 96 for the coding of the FLLn_REFCLK_DIV, FLLn_FRATIO and FLLn_OUTDIV registers.

Table 99 Example FLL Settings – Synchroniser Disabled

Table 100 provides example FLL settings for generating 49.152MHz SYSCLK, with the synchroniser enabled. The main loop and the synchroniser loop must each be configured according to the respective input source.

FLL (Main Loop) Settings									
F_{SOURCE}	F_{OUT} (MHz)	F_{REF} Divider	N.K	FRATIO	F_{VCO} (MHz)	OUTDIV	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	49.152	1	204.8	15	98.304	2	0CCh	CCCCh	0000h
32.768 kHz	49.152	1	187.5	16	98.304	2	0BBh	8000h	0000h
48 kHz	49.152	1	136.5333	15	98.304	2	088h	8888h	0000h
128 kHz	49.152	1	109.7143	7	98.304	2	06Dh	B6DBh	0000h
512 kHz	49.152	1	38.4	5	98.304	2	026h	6666h	0000h
1.536 MHz	49.152	1	21.3333	3	98.304	2	015h	5555h	0000h
3.072 MHz	49.152	1	10.6667	3	98.304	2	00Ah	AAAAh	0000h
11.2896 MHz	49.152	1	8.7075	1	98.304	2	008h	B51Dh	0000h
12.000 MHz	49.152	1	8.192	1	98.304	2	008h	3126h	0000h
12.288 MHz	49.152	2	5.3333	3	98.304	2	005h	5555h	0000h
13.000 MHz	49.152	1	7.5618	1	98.304	2	007h	8FD5h	0000h
19.200 MHz	49.152	2	10.24	1	98.304	2	00Ah	3D70h	0000h
24 MHz	49.152	2	8.192	1	98.304	2	008h	3126h	0000h
26 MHz	49.152	2	7.5618	1	98.304	2	007h	8FD5h	0000h
27 MHz	49.152	2	7.2818	1	98.304	2	007h	4822h	0000h
FLL (Synchroniser Loop) Settings									
F_{SOURCE}	F_{OUT} (MHz)	F_{SYNC} Divider	N.K (SYNC)	FRATIO (SYNC)	F_{VCO} (MHz)	OUTDIV	FLLn_ SYNC_N	FLLn_ SYNC_ THETA	FLLn_ SYNC_ LAMBDA
32.000 kHz	49.152	1	192	16	98.304	2	0C0h	0000h	0000h
32.768 kHz	49.152	1	187.5	16	98.304	2	0BBh	0001h	0002h
48 kHz	49.152	1	128	16	98.304	2	080h	0000h	0000h
128 kHz	49.152	1	96	8	98.304	2	060h	0000h	0000h
512 kHz	49.152	1	96	2	98.304	2	060h	0000h	0000h
1.536 MHz	49.152	1	64	1	98.304	2	040h	0000h	0000h
3.072 MHz	49.152	1	32	1	98.304	2	020h	0000h	0000h
11.2896 MHz	49.152	1	8.7075	1	98.304	2	008h	0068h	0093h
12.000 MHz	49.152	1	8.192	1	98.304	2	008h	0018h	007Dh
12.288 MHz	49.152	1	8	1	98.304	2	008h	0000h	0000h
13.000 MHz	49.152	1	7.5618	1	98.304	2	007h	0391h	0659h
19.200 MHz	49.152	2	10.24	1	98.304	2	00Ah	0006h	0019h
24 MHz	49.152	2	8.192	1	98.304	2	008h	0018h	007Dh
26 MHz	49.152	2	7.5618	1	98.304	2	007h	0391h	0659h
27 MHz	49.152	2	7.2818	1	98.304	2	007h	013Dh	0465h

$F_{OUT} = (F_{SOURCE} / F_{REF}$ Divider) * 3 * N.K * FRATIO / OUTDIV

The values of N and K are contained in the FLLn_N, FLLn_THETA and FLLn_LAMBDA registers. See Table 95 and Table 96 for the coding of the FLL configuration registers. Note that the register coding of FLLn_FRATIO is different to FLLn_SYNC_FRATIO.

Table 100 Example FLL Settings – Synchroniser Enabled

CONTROL INTERFACE

The WM8998 is controlled by writing to its control registers. Readback is available for all registers. Note that the SLIMbus interface also supports read/write access to the WM8998 control registers - see “SLIMbus Interface Control”.

Note that the Control Interface function can be supported with or without system clocking. Where applicable, the register map access is synchronised with SYSCLK in order to ensure predictable operation of cross-domain functions. See “Clocking and Sample Rates” for further details of Control Interface clocking.

When SYSCLK is present and enabled, register access is possible on all of the Control Interfaces (including SLIMbus) simultaneously.

When SYSCLK is disabled, then register access will only be supported on whichever interface (I2C or SLIMbus) is the first to attempt any register access after SYSCLK has stopped. Full access via all interfaces will be restored when SYSCLK is enabled.

The WM8998 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset, Software Reset or Wake-Up (from Sleep mode). A further sequence of device initialisation writes must then be executed by the host application. Note that Control Register writes should not be attempted until the Boot Sequence has completed. The host system should ensure that the WM8998 is ready before attempting the initialisation sequence (or any other) Control Register writes. See “Power-On Reset (POR)” and “Hardware Reset, Software Reset, Wake-Up, and Device ID” for further details.

The WM8998 performs automatic checks to confirm that the control interface does not attempt a Read or Write operation to an invalid register address. The Control Interface Address Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The Control Interface is a 2-wire (I2C) interface, comprising the following pins:

- SDA - serial interface data input/output
- SCLK - serial interface clock input
- ADDR - logic level controlling the I2C device ID

The Control Interface configuration registers are described in Table 101.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Ctrl IF I2C1 CFG 1	1:0	I2C1_AUTO_INC [1:0]	01	I2C Address auto-increment select 00 = Disabled 01 = Increment by 1 on each access 10 = Increment by 2 on each access 11 = Increment by 3 on each access
R11 (0Bh) Ctrl IF I2C1 CFG 2	6:0	I2C1_DEV_ID [6:0]	1Ah	I2C Device ID (Read Only) Note that this 7-bit field identifies bits [7:1] of the I2C device ID. The read/write bit is appended to these 7 bits.
R3105 (0C21h) Misc Pad Ctrl 2	0	ADDR_PD	1	ADDR Pull-down enable 0 = Disabled 1 = Enabled

Table 101 Control Interface Configuration

The WM8998 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8998 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the address of each register in the WM8998).

The device ID is selectable using the ADDR pin, as described in Table 102. The LSB of the Device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

The ADDR logic level is referenced to the DBVDD1 power domain. An internal pull-down resistor is enabled by default on the ADDR pin; this can be configured using the ADDR_PD register bit described in Table 101.

ADDR	DEVICE ID
Logic 0	0011 010x = 34h (write) / 35h (read)
Logic 1	0011 011x = 36h (write) / 37h (read)

Table 102 Control Interface Device ID Selection

The WM8998 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device ID, and subsequent address/data byte(s) will follow. The WM8998 responds to the start condition and shifts in the next eight bits on SDA (8-bit device ID, including Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8998, then the WM8998 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is set incorrectly, the WM8998 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8998, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM8998 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM8998 supports the following read and write operations:

- Single write
- Single read
- Multiple write (with optional auto-increment)
- Multiple read (with optional auto-increment)

The sequence of signals associated with a single register write operation is illustrated in Figure 67.

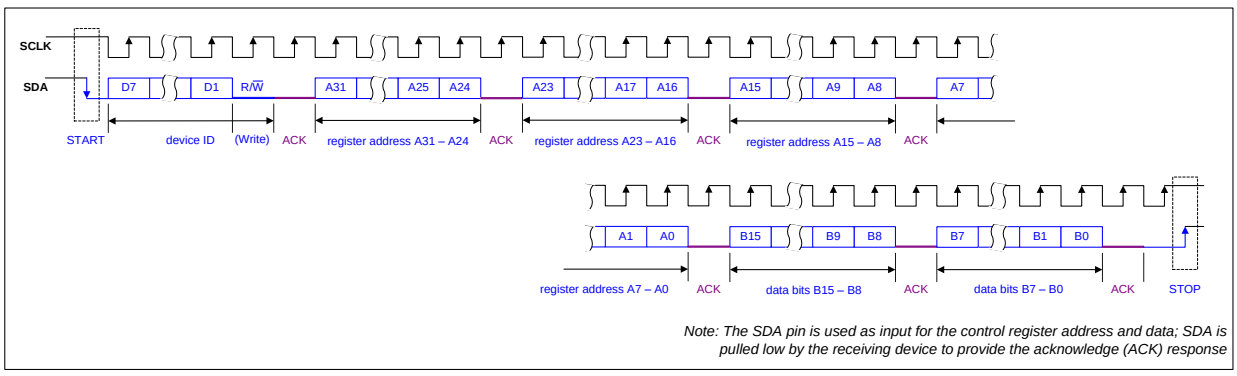


Figure 67 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 68.

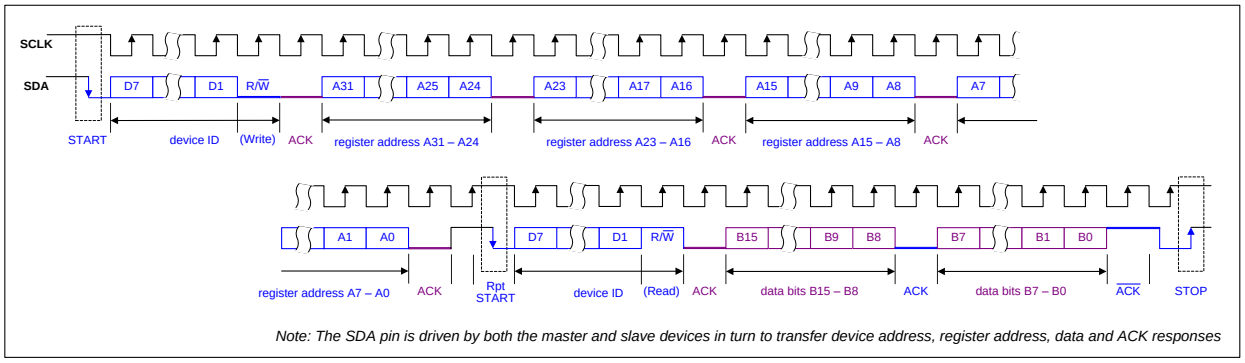


Figure 68 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 103.

Note that, for multiple write and multiple read operations, the auto-increment option may be enabled. The I2C multiple transfers illustrated below assume that "auto-increment by 1" is selected in each case. Auto-increment is enabled by default, as noted in Table 101.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
$\overline{A}$	Not Acknowledge (SDA High)	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8998	
[Grey field]	Data flow from WM8998 to bus master	

Table 103 Control Interface (I2C) Terminology

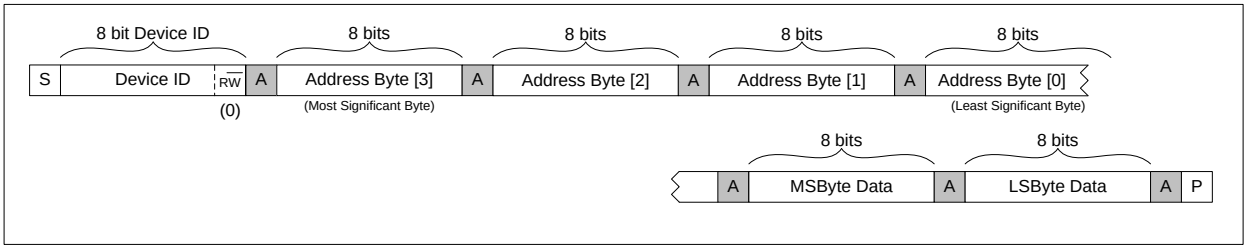


Figure 69 Single Register Write to Specified Address

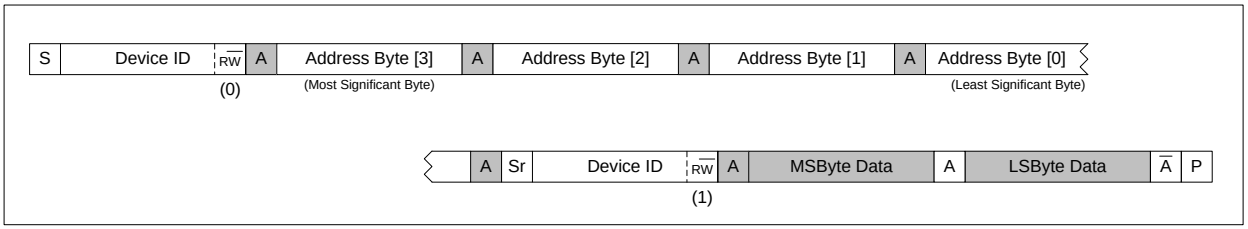


Figure 70 Single Register Read from Specified Address

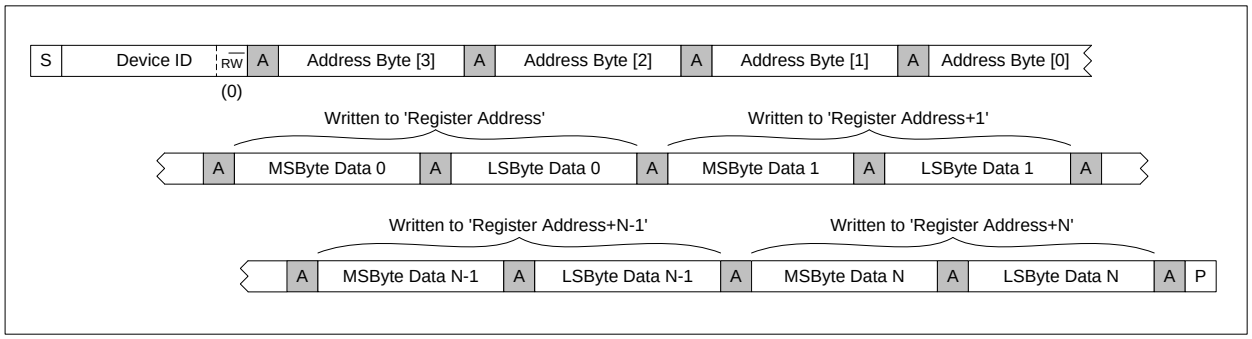


Figure 71 Multiple Register Write to Specified Address using Auto-increment

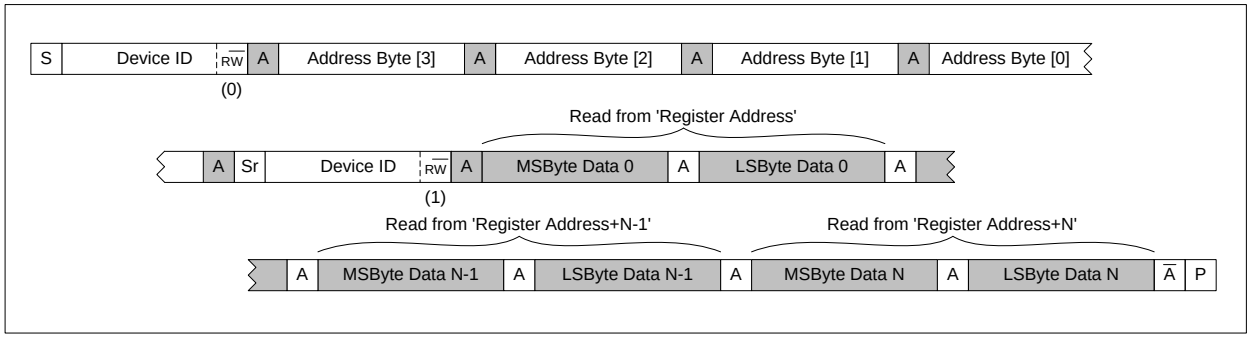


Figure 72 Multiple Register Read from Specified Address using Auto-increment

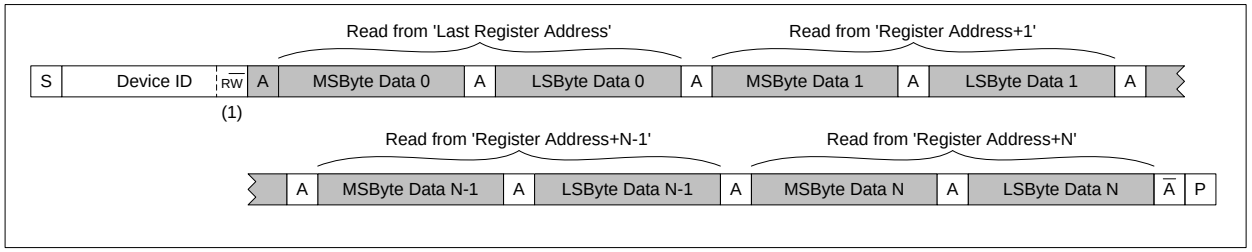


Figure 73 Multiple Register Read from Last Address using Auto-increment

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. The auto-increment function supports selectable address increments for each successive register access. This function is controlled using the I2C1_AUTO_INC register. Auto-increment (by 1) is enabled by default, as described in Table 101.

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the WM8998 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for pop-suppressed start-up and shut-down of each headphone/earpiece output driver are provided (these are scheduled automatically when the respective output paths are enabled or disabled). Other control sequences can be programmed, and may be associated with Jack Detect, MICDET Clamp, Wake-Up or Sample Rate Detection functions - these sequences are automatically scheduled whenever a corresponding event is detected.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The 'start index' of a control sequence within the sequencer's memory may be commanded directly by the host processor. In the case of an output path enable/disable event, or sequences associated with Jack Detect, Wake-Up or Sample Rate Detection, the applicable 'start index' is held in a user-programmed control register for each sequence.

The Control Write Sequencer may be triggered in a number of ways, as described above. Multiple sequences will be queued if necessary, and each is scheduled in turn. When all of the queued sequences have completed, the sequencer stops, and an Interrupt status flag is asserted.

A valid clock (SYSCLK) must be enabled whenever a Control Write Sequence is scheduled. See "Clocking and Sample Rates" for further details.

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 104.

The Write Sequencer is enabled using the WSEQ_ENA bit. The index location of the first command in the selected sequence is held in the WSEQ_START_INDEX register.

Writing a '1' to the WSEQ_START bit commands the sequencer to execute a control sequence, starting at the given index. Note that, if the sequencer is already running, then the WSEQ_START command will be queued, and will be executed later when the sequencer becomes available.

Note that the mechanism for queuing multiple sequence requests has some limitations, when using the WSEQ_START bit to trigger the write sequencer. If a sequence is initiated using the WSEQ_START bit, no other control sequences should be triggered until the sequence completes. The WSEQ_BUSY bit (described in Table 109) provides an indication of the sequencer status, and can be used to confirm that sequence has completed. Control sequences triggered by another other method are queued if necessary, and scheduled in turn.

The Write Sequencer can be interrupted by writing a '1' to the WSEQ_ABORT bit. Note that this command will only abort a sequence that is currently running; if other sequence commands are pending and not yet started, these sequences will not be aborted by writing to the WSEQ_ABORT bit.

The Write Sequencer stores up to 256 register write commands. These are defined in Registers R12288 (3000h) to R12799 (31FFh). Each of the 256 possible commands is defined in 2 control registers - see Table 110 for a description of these registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (0016h) Write Sequencer Ctrl 0	11	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence.
	10	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. At the end of the sequence, this bit will be reset by the Write Sequencer.
	9	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled Only applies to sequences triggered using the WSEQ_START bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:0	WSEQ_START_INDEX [8:0]	000h	Sequence Start Index This field contains the index location in the sequencer memory of the first command in the selected sequence. Only applies to sequences triggered using the WSEQ_START bit. Valid from 0 to 255 (0FFh).

Table 104 Write Sequencer Control - Initiating a Sequence

AUTOMATIC SAMPLE RATE DETECTION SEQUENCES

The WM8998 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2 and AIF3), when operating in AIF Slave mode. Automatic sample rate detection is enabled using the RATE_EST_ENA register bit (see Table 90).

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. If one of the selected audio sample rates is detected, then the Control Write Sequencer will be triggered. The applicable start index location within the sequencer memory is separately configurable for each detected sample rate.

The WSEQ_SAMPLE_RATE_DETECT_A_INDEX register defines the sequencer start index corresponding to the SAMPLE_RATE_DETECT_A sample rate. Equivalent start index values are defined for the other sample rates, as described in Table 105.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The automatic sample rate detection control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset, Software Reset and in Sleep mode.

See “Clocking and Sample Rates” for further details of the automatic sample rate detection function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R97 (0061h) Sample Rate Sequence Select 1	8:0	WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0]	1FFh	Sample Rate A Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate A detection. Valid from 0 to 255 (0FFh).
R98 (0062h) Sample Rate Sequence Select 2	8:0	WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0]	1FFh	Sample Rate B Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate B detection. Valid from 0 to 255 (0FFh).
R99 (0063h) Sample Rate Sequence Select 3	8:0	WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0]	1FFh	Sample Rate C Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate C detection. Valid from 0 to 255 (0FFh).
R100 (0064h) Sample Rate Sequence Select 4	8:0	WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0]	1FFh	Sample Rate D Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate D detection. Valid from 0 to 255 (0FFh).

Table 105 Write Sequencer Control - Automatic Sample Rate Detection

JACK DETECT, GPIO, MICDET CLAMP, AND WAKE-UP SEQUENCES

The WM8998 supports external accessory detection and GPIO functions. The JD1 signal (associated with external accessory detection) and the GP5 signal (associated with the GPIO5 pin) can be used to trigger the Control Write Sequencer.

The JD1 signal is configured using the register bits described in Table 65. The GP5 signal is derived from the GPIO5 pin, which is configured using the register bits described in Table 75.

The MICDET Clamp is controlled by the JD1 and/or GP5 signals, as described in Table 66. The MICDET Clamp status can also be used to trigger the Control Write Sequencer.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the JD1, GP5 or MICDET Clamp. This is configured using the register bits described in Table 74.

If one of the selected logic conditions is detected, the Control Write Sequencer will be triggered. The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The WSEQ_GP5_RISE_INDEX register defines the sequencer start index corresponding to a GP5 Rising Edge event. Equivalent start index values are defined for the other logic conditions, as described in Table 106.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The JD1, GP5 and MICDET Clamp control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset, Software Reset and in Sleep mode.

See “Low Power Sleep Configuration” for further details of the JD1, GP5 and MICDET Clamp status signals. See also “General Purpose Input / Output” for details of the GPIO5 pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R102 (0066h) Always On Triggers Sequence Select 1	8:0	WSEQ_MICD_CLAMP_RISE_INDEX [8:0]	1FFh	MICDET Clamp (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with MICDET Clamp (Rising) detection. Valid from 0 to 255 (0FFh).
R103 (0067h) Always On Triggers Sequence Select 2	8:0	WSEQ_MICD_CLAMP_FALL_INDEX [8:0]	1FFh	MICDET Clamp (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with MICDET Clamp (Falling) detection. Valid from 0 to 255 (0FFh).
R104 (0068h) Always On Triggers Sequence Select 3	8:0	WSEQ_GP5_RISE_INDEX [8:0]	1FFh	GP5 (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with GP5 (Rising) detection. Valid from 0 to 255 (0FFh).
R105 (0069h) Always On Triggers Sequence Select 4	8:0	WSEQ_GP5_FALL_INDEX [8:0]	1FFh	GP5 (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with GP5 (Falling) detection. Valid from 0 to 255 (0FFh).
R106 (006Ah) Always On Triggers Sequence Select 5	8:0	WSEQ_JD1_RISE_INDEX [8:0]	1FFh	JD1 (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with JD1 (Rising) detection. Valid from 0 to 255 (0FFh).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R107 (006Bh) Always On Triggers Sequence Select 6	8:0	WSEQ_JD1_FALL_INDEX [8:0]	1FFh	JD1 (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with JD1 (Falling) detection. Valid from 0 to 255 (0FFh).

Table 106 Write Sequencer Control - JD1, GP5 and MICDET Clamp

A valid clock (SYSCLK) must be enabled whenever a Control Write Sequence is scheduled.

If the JD1, GP5 or MICDET Clamp trigger status bits are associated with the Control Write Sequencer (using the register bits in Table 74) and also configured as Wake-Up events (using the register bits in Table 73), then the Boot Sequence must be programmed to configure and enable SYSCLK. (Note that the default SYSCLK frequency must be used in this case.)

The Boot Sequence (see below) is scheduled as part of the Wake-Up transition, and provides the capability to configure SYSCLK (and other register settings) prior to the Control Write Sequencer being triggered.

Note that, if the Control Write Sequencer is triggered during normal operation, then SYSCLK will typically be already available, and no additional requirements will apply.

DRC SIGNAL DETECT SEQUENCES

The Dynamic Range Control (DRC) function within the WM8998 Digital Core provides a configurable signal detect function. This allows the signal level at the DRC input to be monitored and used to trigger other events.

The DRC Signal Detect function is enabled and configured using the register fields described in Table 13.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the DRC1 Signal Detect output. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit.

When the DRC Signal Detect sequence is enabled, the Control Write Sequencer will be triggered whenever the DRC1 Signal Detect output transitions (high or low). The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The WSEQ_DRC1_SIG_DET_RISE_SEQ_INDEX register defines the sequencer start index corresponding to a DRC Signal Detect Rising Edge event, as described in Table 107. The WSEQ_DRC1_SIG_DET_FALL_SEQ_INDEX register defines the sequencer start index corresponding to a DRC Signal Detect Falling Edge event.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The DRC Signal Detect sequences cannot be independently enabled for rising and falling edges. Instead, a start index of 1FFh can be used to disable the sequence for either edge, if required.

The DRC Signal Detect control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset, Software Reset and in Sleep mode.

See “Digital Core” for further details of the Dynamic Range Control (DRC) function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R110 (006Eh) Trigger Sequence Select 32	8:0	WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0]	1FFh	DRC1 Signal Detect (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Rising) detection. Valid from 0 to 255 (0FFh).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R111 (006Fh) Trigger Sequence Select 33	8:0	WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0]	1FFh	DRC1 Signal Detect (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Falling) detection. Valid from 0 to 255 (0FFh).

Table 107 Write Sequencer Control - DRC Signal Detect

BOOT SEQUENCE

The WM8998 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset, Software Reset or Wake-Up (from Sleep mode).

See "Power-On Reset (POR)" and "Hardware Reset, Software Reset, Wake-Up, and Device ID" for further details.

The Boot Sequence configures the WM8998 with factory-set parameters. User-defined register operations may be added to the Boot Sequence if required (eg. to automatically enable SYSCLK as part of the Boot Sequence). Further details of the sequencer memory are provided later in this section. Note that all control sequences are maintained in the sequencer memory through Hardware Reset, Software Reset and in Sleep mode.

If the Boot Sequence is programmed to enable SYSCLK, note that the default SYSCLK frequency must be used. If a different SYSCLK frequency is required, this must be configured after the Boot Sequence has completed.

The start index location of the the Boot Sequence is 192 (0C0h).

The Boot Sequence can be commanded at any time by writing '1' to the WSEQ_BOOT_START bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write Sequencer Ctrl 2	1	WSEQ_BOOT_START	0	Writing a 1 to this bit starts the write sequencer at the index location configured for the Boot Sequence. The Boot Sequence start index is 192 (0C0h).

Table 108 Write Sequencer Control - Boot Sequence

SEQUENCER OUTPUTS AND READBACK

The status of the Write Sequencer can be read using the WSEQ_BUSY and WSEQ_CURRENT_INDEX registers, as described in Table 109.

When the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy.

The index address of the most recent Write Sequencer command can be read from the WSEQ_CURRENT_INDEX field. This can be used to provide a precise indication of the Write Sequencer progress.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (0017h) Write Sequencer Ctrl 1	9	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy
	8:0	WSEQ_CURRENT_INDEX [8:0] (read only)	000h	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.

Table 109 Write Sequencer Control - Status Readback

The Write Sequencer status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The Write Sequencer status can be output directly on a GPIO pin as an external indication of the Write Sequencer. See “General Purpose Input / Output” to configure a GPIO pin for this function.

PROGRAMMING A SEQUENCE

A Control Write Sequence comprises a series of write operations to data bits (or groups of bits) within the control register map. Each write operation is defined by a block of 2 registers, each containing 5 fields, as described below.

The block of 2 registers is replicated 256 times, defining each of the sequencer’s 256 possible index addresses. Many sequences can be stored in the sequencer memory at the same time, with each assigned a unique range of index addresses.

The WSEQ_DELAYn register is used to identify the ‘end of sequence’ position, as described below.

Note that, in the following descriptions, the term ‘*n*’ denotes the sequencer index address (valid from 0 to 255).

WSEQ_DATA_WIDTH*n* is a 3-bit field which identifies the width of the data block to be written. Note that the maximum value of this field selects a width of 8-bits; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Write Sequencer.

WSEQ_ADDR*n* is a 13-bit field containing the register address in which the data should be written.

WSEQ_DELAY*n* is a 4-bit field which controls the waiting time between the current step and the next step in the sequence (ie. the delay occurs after the write in which it was called). The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 3.3µs up to 1s per step. Setting this field to 0xF identifies the step as the last in the sequence.

If WSEQ_DELAYn = 0h or Fh, the step execution time is 3.3µs

For all other values, the step execution time is $61.44\mu s \times ((2^{WSEQ_DELAY}) - 1)$

WSEQ_DATA_START*n* is a 4-bit field which identifies the LSB position within the selected control register to which the data should be written. For example, setting WSEQ_DATA_START*n* = 0100 will select bit 4 as the LSB position of the data to be written.

WSEQ_DATA*n* is an 8-bit field which contains the data to be written to the selected control register. The WSEQ_DATA_WIDTH*n* field determines how many of these bits are written to the selected control register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH*n*) are ignored.

The register definitions for Step 0 are described in Table 110. The equivalent definitions also apply to Step 1 through to Step 255, in the subsequent register address locations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12288 (3000h) WSEQ Sequence 1	15:13	WSEQ_DATA_ WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	12:0	WSEQ_ADDR0 [12:0]	0000h	Control Register Address to be written to in this sequence step.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12289 (3001h) WSEQ Sequence 2	15:12	WSEQ_DELAY0 [3:0]	0000	Time delay after executing this step. 00h = 3.3us 01h to 0Eh = 61.44us x ((2^WSEQ_DELAY)-1) 0Fh = End of sequence marker
	11:8	WSEQ_DATA_START0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15
	7:0	WSEQ_DATA0 [7:0]	00h	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA*n* are ignored. It is recommended that unused bits be set to 0.

Table 110 Write Sequencer Control - Programming a Sequence

SEQUENCER MEMORY DEFINITION

The Write Sequencer memory defines up to 256 write operations; these are indexed as 0 to 255 in the sequencer memory map.

Following Power-On Reset (POR), the sequencer memory will contain the Boot Sequence, and the OUT1, OUT2, OUT3, OUT4 signal path enable/disable sequences. The remainder of the sequencer memory will be undefined on power-up. See the “Applications Information” section for a summary of the WM8998 memory reset conditions.

User-defined sequences can be programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset, Software Reset and in Sleep mode.

The default control sequences can be overwritten in the sequencer memory, if required. Note that the headphone and earpiece output path enable registers (HPx_ENA, LINEx_ENA, EP_ENA, SPKOUTx_ENA) will always trigger the Write Sequencer (at the pre-determined start index addresses).

Writing ‘1’ to the WSEQ_LOAD_MEM bit will clear the sequencer memory to the POR state.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write Sequencer Ctrl 2	0	WSEQ_LOAD_MEM	0	Writing a 1 to this bit resets the sequencer memory to the POR state.

Table 111 Write Sequencer Control - Load Memory Control

User-defined sequences must be assigned space within the Write Sequencer memory. The start index for the user-defined sequences is configured using the registers described in Table 105 and Table 106. The Boot Sequence has a fixed start address, as referenced in Table 108.

The sequencer memory is illustrated in Figure 74. The pre-programmed sequencer index locations are highlighted. User-defined sequences should be programmed in other areas of the sequencer memory.

Any user-defined additions to the Boot Sequence should be configured at index location 208 upwards. The final step of the Boot Sequence must be programmed with WSEQ_DELAYn = 0xF, identifying the end of the sequence. If there are no user-defined additions to the Boot Sequence, then the default values of sequencer index 208 should be left unchanged.

Other user-defined sequences can be configured at index locations 209 upwards (excluding any index locations that have been allocated to the Boot Sequence).

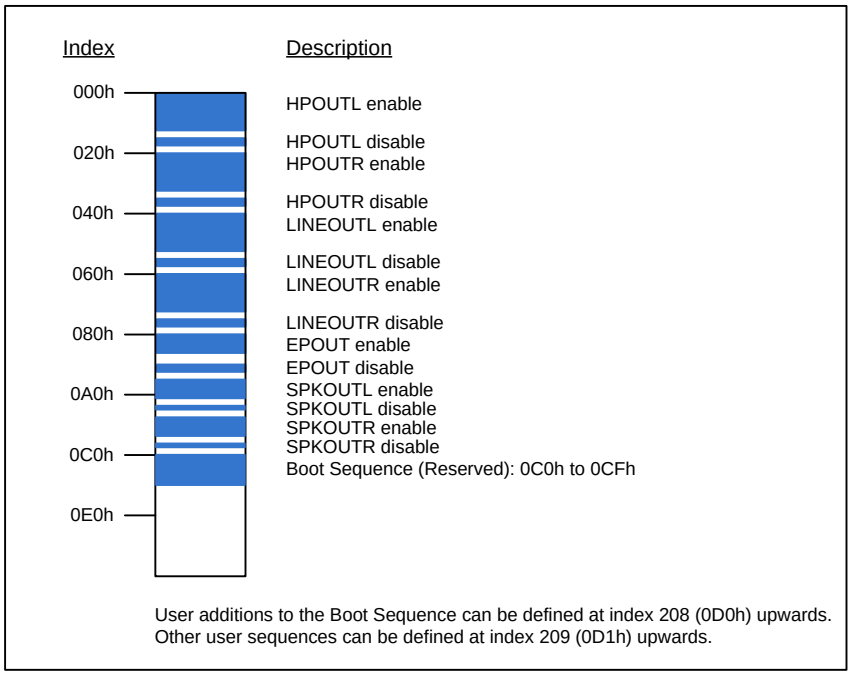


Figure 74 Write Sequencer Memory

Further details of the pre-programmed sequencer index locations are provided in Table 112.

SEQUENCE NAME	START INDEX	DEFAULT SEQUENCE INDEX RANGES
HPOUTL Enable	0 (000h)	0 to 19
HPOUTL Disable	24 (018h)	24 to 27
HPOUTR Enable	32 (020h)	32 to 51
HPOUTR Disable	56 (038h)	56 to 59
LINEOUTL Enable	64 (040h)	64 to 83
LINEOUTL Disable	88 (058h)	88 to 91
LINEOUTR Enable	96 (060h)	96 to 115
LINEOUTR Disable	120 (078h)	120 to 123
EPOUT Enable	128 (080h)	128 to 137
EPOUT Disable	144 (090h)	144 to 147
SPKOUTL Enable	152 (098h)	152 to 163
SPKOUTL Disable	164 (0A4h)	164 to 171
SPKOUTR Enable	172 (0ACh)	172 to 183
SPKOUTR Disable	184 (0B8h)	184 to 191
Boot Sequence	192 (0C0h)	192 to 207
Note: User additions to the Boot Sequence can be defined at index 208 upwards; Other user sequences can be defined at index 209 upwards.		

Table 112 Default Sequencer Memory Allocation

CHARGE PUMPS, REGULATORS AND VOLTAGE REFERENCE

The WM8998 incorporates two Charge Pump circuits and two LDO Regulator circuits to generate supply rails for internal functions and to support external microphone requirements. The WM8998 also provides three MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones or powering digital microphones.

Refer to the “Applications Information” section for recommended external components.

CHARGE PUMPS AND LDO2 REGULATOR

Charge Pump 1 (CP1) is used to generate the positive and negative supply rails for the analogue output drivers. CP1 is enabled automatically by the WM8998 when required by the output drivers.

Charge Pump 2 (CP2) powers LDO2, which provides the supply rail for analogue input circuits and for the MICBIAS generators. CP2 and LDO2 are enabled using the CP2_ENA register bit.

The 32kHz clock must be configured and enabled when using CP2. See “Clocking and Sample Rates” for details of the system clocks.

When CP2 and LDO2 are enabled, the MICVDD voltage can be selected using the LDO2_VSEL control field. Note that, when one or more of the MICBIAS generators is operating in normal (regulator) mode, then the MICVDD voltage must be at least 200mV greater than the highest selected MICBIASn output voltage(s).

When CP2 and LDO2 are enabled, an internal bypass path may be selected, connecting the MICVDD pin directly to the CPVDD supply. This path is controlled using the CP2_BYPASS register. Note that the bypass path is only supported when CP2 is enabled.

When CP2 is disabled, the CP2VOUT pin can be configured to be floating or to be actively discharged. This is selected using the CP2_DISCH register bit.

When LDO2 is disabled, the MICVDD pin can be configured to be floating or to be actively discharged. This is selected using the LDO2_DISCH register bit.

The MICVDD pin is connected to the output of LDO2. Note that the MICVDD does not support direct connection to an external supply; MICVDD is always powered internally to the WM8998.

The Charge Pumps and LDO2 Regulator circuits are illustrated in Figure 75. The associated register control bits are described in Table 113.

Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to the “Applications Information” section for recommended external components.

MICBIAS BIAS (MICBIAS) CONTROL

There are three MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones or powering digital microphones. Refer to the “Applications Information” section for recommended external components.

The MICBIAS generators are powered from MICVDD, which is generated by an internal Charge Pump and LDO, as illustrated in Figure 75.

The MICBIAS outputs can be independently enabled using the MICB*n*_ENA register bits (where *n* = 1, 2 or 3 for MICBIAS1, 2 or 3 respectively).

When a MICBIAS output is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using the MICB*n*_DISCH register bits.

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. The applicable mode is selected using the MICB*n*_BYPASS registers.

In Regulator mode, the output voltage is selected using the MICB*n*_LVL register bits. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered from the MICVDD pin, and use the internal bandgap circuit as a reference.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required, using the MICBn_EXT_CAP register bits. (This may be appropriate for a digital microphone supply.) It is

important that the external capacitance is compatible with the applicable MICBn_EXT_CAP setting. The compatible load conditions are detailed in the “Electrical Characteristics” section.

In Bypass mode, the output pin (MICBIAS1, MICBIAS2 or MICBIAS3) is connected directly to MICVDD. This enables a low power operating state. Note that the MICBn_EXT_CAP register settings are not applicable in Bypass mode; there are no restrictions on the external MICBIAS capacitance in Bypass mode.

The MICBIAS generators incorporate a pop-free control circuit to ensure smooth transitions when the MICBIAS outputs are enabled or disabled in Bypass mode; this feature is enabled using the MICB*n*_RATE registers.

The MICBIAS generators are illustrated in Figure 75. The MICBIAS control register bits are described in Table 113.

The maximum output current for each MICBIAS*n* pin is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode.

VOLTAGE REFERENCE CIRCUIT

The WM8998 incorporates a voltage reference circuit, powered by AVDD. This circuit ensures the accuracy of the LDO Regulator and MICBIAS voltage settings.

LDO1 REGULATOR AND DCVDD SUPPLY

The LDO1 voltage regulator is intended for generating the DCVDD domain, which powers the digital core functions on the WM8998. In this configuration, the LDO output (LDOVOUT) should be connected to the DCVDD pin. Note that the use of the LDO1 regulator to power external circuits cannot be supported by the WM8998.

LDO1 is powered by LDOVDD and can be controlled using hardware or software controls. Note that, depending on the application requirements, it may be necessary to use both the hardware and software enables for LDO1, as described below.

Under hardware control, LDO1 is enabled when a logic ‘1’ is applied to the LDOENA pin. The logic level is determined with respect to the DBVDD1 voltage domain. LDO1 is also enabled when the LDO1_ENA software control register is set to 1. Note that, to disable LDO1, the hardware and software controls must both be de-asserted.

When LDO1 is enabled, an internal bypass path may be selected, connecting the LDOVOUT pin directly to the LDOVDD supply. This path is controlled using the LDO1_BYPASS register. Note that the bypass path is only supported when LDO1 is enabled.

When LDO1 is disabled, the LDOVOUT pin can be configured to be floating or to be actively discharged. This is selected using the LDO1_DISCH register bit.

When LDO1 is enabled, the LDOVOUT voltage can be controlled using the LDO1_VSEL register. Setting LDO1_HI_PWR=1 will override the LDO1_VSEL register and select 1.8V LDO output voltage. Note that, under default conditions, LDO1_HI_PWR is set to ‘1’.

It is possible to supply DCVDD from an external supply. In this configuration, the LDOVOUT pin should be left floating; it must not be connected to the DCVDD pin. The LDO1 regulator is not used in this case, and must be disabled at all times.

For recommended use of the Sleep / Wake-Up functions (see “Low Power Sleep Configuration”), it is assumed that DCVDD is powered from the output of LDO1. In this case, Sleep mode is selected when LDO1 is disabled, causing the DCVDD supply to be removed. Note that the AVDD, DBVDD1, and LDOVDD supplies must be present throughout the Sleep mode duration.

If DCVDD is powered externally (not from LDO1), then the ISOLATE_DCVDD1 register bit must be controlled as described in Table 113 when selecting WM8998 Sleep mode. In this case, Sleep mode is selected by setting the ISOLATE_DCVDD1 register bit, and then removing the DCVDD supply. For applications where DCVDD is powered externally, only the AVDD and DBVDD1 supplies are required in Sleep mode.

An internal pull-down resistor is enabled by default on the LDOENA pin. This is configurable using the LDO1ENA_PD register bit. A pull-up resistor is also available, as described in Table 113. When the

pull-up and pull-down resistors are both enabled, the WM8998 provides a 'bus keeper' function on the LDOENA pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (eg. if the signal is tri-stated).

If DCVDD is powered from LDO1, then a logic '1' must be applied to the LDOENA pin during power-up, to enable LDO1. The LDO must also be enabled using the LDOENA pin following a Hardware Reset or Software Reset, to allow the device to re-start. (It is recommended that the LDOENA pin is asserted before any reset, and is held at logic '1' until after the reset is complete; this ensures the Write Sequencer memory contents are retained, and also allows faster reset time.)

For normal operation following Power-On Reset (POR), Hardware Reset, or Software Reset, LDO1 must be enabled using the hardware or software controls described above. Note that when the LDO1_ENA bit is set to 1, the LDOENA pin has no effect and may be de-asserted - the LDO is then under software control, allowing Sleep mode to be selected under register control, including via the Control Write Sequencer.

See "Power-On Reset (POR)" and "Hardware Reset, Software Reset, Wake-Up, and Device ID" for details of WM8998 Resets. See also "Low Power Sleep Configuration" for details of the Sleep / Wake-up functions.

The LDO1 Regulator circuit is illustrated in Figure 75. The associated register control bits are described in Table 113.

Note that a decoupling capacitor is recommended. Refer to the "Applications Information" section for recommended external components.

BLOCK DIAGRAM AND CONTROL REGISTERS

The Charge Pump and Regulator circuits are illustrated in Figure 75. Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to the "Applications Information" section for recommended external components.

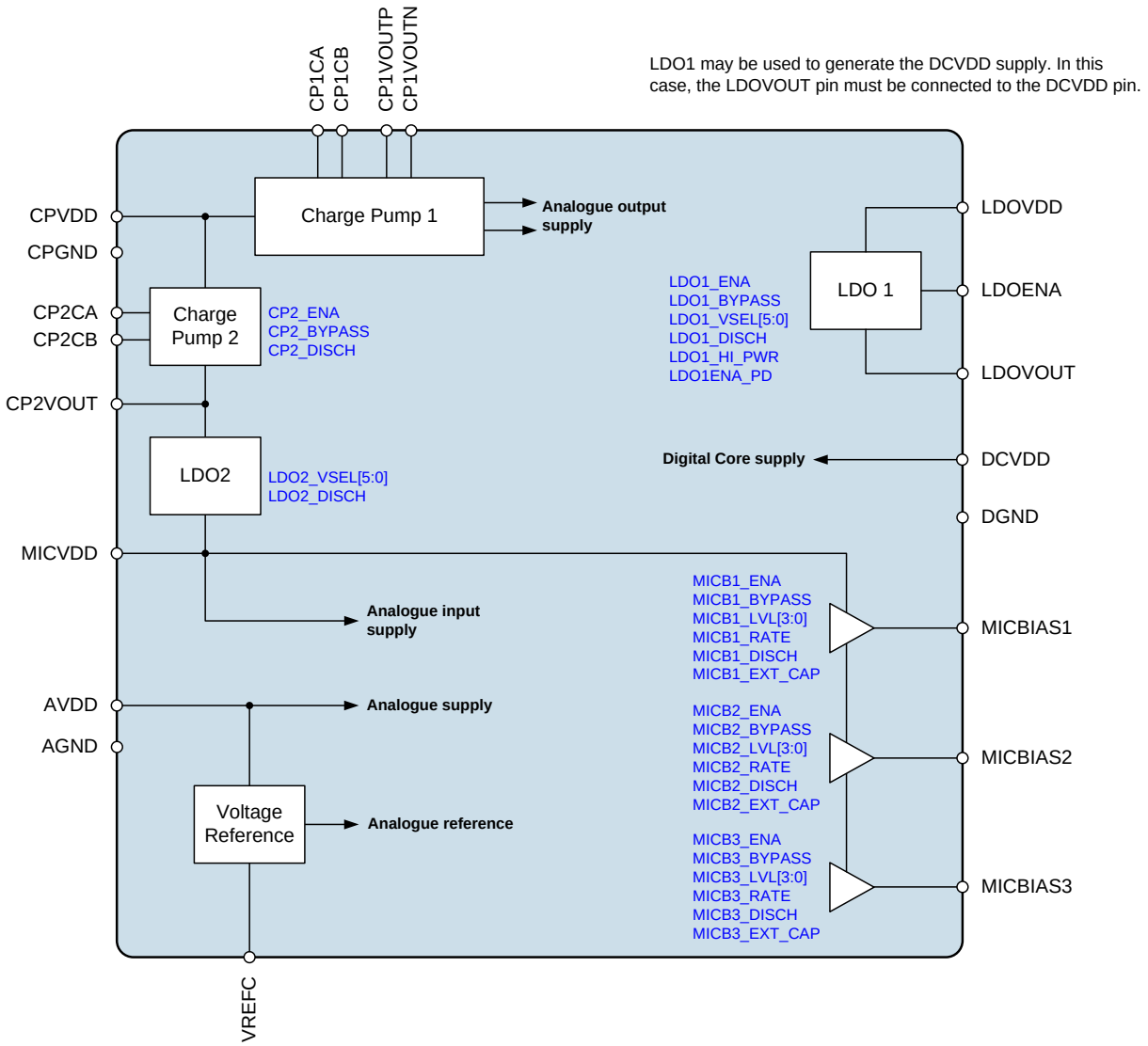


Figure 75 Charge Pumps and Regulators

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R512 (0200h) Mic Charge Pump 1	2	CP2_DISCH	1	Charge Pump 2 Discharge 0 = CP2VOUT floating when disabled 1 = CP2VOUT discharged when disabled
	1	CP2_BYPASS	1	Charge Pump 2 and LDO2 Bypass Mode 0 = Normal 1 = Bypass mode In Bypass mode, CPVDD is connected directly to MICVDD. Note that CP2_ENA must also be set.
	0	CP2_ENA	0	Charge Pump 2 and LDO2 Control (Provides analogue input and MICVDD supplies) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R528 (0210h) LDO1 Control 1	10:5	LDO1_VSEL [5:0]	06h	LDO1 Output Voltage Select Controls the LDO1 output voltage when LDO1_HI_PWR=0. 00h = 0.9V 01h = 0.95V 02h = 1.0V 03h = 1.05V 04h = 1.1V 05h = 1.15V 06h = 1.2V 07h to 3Fh = Reserved
	2	LDO1_DISCH	1	LDO1 Discharge 0 = LDOVOUT floating when disabled 1 = LDOVOUT discharged when disabled
	1	LDO1_BYPASS	0	LDO1 Bypass Mode 0 = Normal 1 = Bypass mode In Bypass mode, LDOVDD is connected directly to LDOVOUT. Note that LDO1_ENA must also be set.
	0	LDO1_ENA	0	LDO1 Control 0 = Disabled 1 = Enabled
R530 (0212h) LDO1 Control 2	0	LDO1_HI_PWR	1	LDO1 Output Voltage Control 0 = Set by LDO1_VSEL 1 = 1.8V
R531 (0213h) LDO2 Control 1	10:5	LDO2_VSEL [5:0]	1Ah	LDO2 Output Voltage Select 00h = 1.7V 01h = 1.75V 02h = 1.8V 03h = 1.85V … (50mV steps) 1Dh = 3.15V 1Eh = 3.2V 1Fh = 3.3V 20h to 3Fh = Reserved (See Table 114 for voltage range)
	2	LDO2_DISCH	1	LDO2 Discharge 0 = MICVDD floating when disabled 1 = MICVDD discharged when disabled
R536 (218h) Mic Bias Ctrl 1	15	MICB1_EXT_CAP	0	Microphone Bias 1 External Capacitor (when MICB1_BYPASS = 0). Configures the MICBIAS1 regulator according to the specified capacitance connected to the MICBIAS1 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB1_LVL [3:0]	Dh	Microphone Bias 1 Voltage Control (when MICB1_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB1_RATE	0	Microphone Bias 1 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	MICB1_DISCH	1	Microphone Bias 1 Discharge 0 = MICBIAS1 floating when disabled 1 = MICBIAS1 discharged when disabled
	1	MICB1_BYPASS	1	Microphone Bias 1 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled
R537 (219h) Mic Bias Ctrl 2	15	MICB2_EXT_CAP	0	Microphone Bias 2 External Capacitor (when MICB2_BYPASS = 0). Configures the MICBIAS2 regulator according to the specified capacitance connected to the MICBIAS2 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB2_LVL [3:0]	Dh	Microphone Bias 2 Voltage Control (when MICB2_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB2_RATE	0	Microphone Bias 2 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB2_DISCH	1	Microphone Bias 2 Discharge 0 = MICBIAS2 floating when disabled 1 = MICBIAS2 discharged when disabled
	1	MICB2_BYPASS	1	Microphone Bias 2 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled
R538 (21Ah) Mic Bias Ctrl 3	15	MICB3_EXT_CAP	0	Microphone Bias 3 External Capacitor (when MICB3_BYPASS = 0). Configures the MICBIAS3 regulator according to the specified capacitance connected to the MICBIAS3 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB3_LVL [3:0]	Dh	Microphone Bias 3 Voltage Control (when MICB3_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB3_RATE	0	Microphone Bias 3 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB3_DISCH	1	Microphone Bias 3 Discharge 0 = MICBIAS3 floating when disabled 1 = MICBIAS3 discharged when disabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	MICB3_BYPASS	1	Microphone Bias 3 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB3_ENA	0	Microphone Bias 3 Enable 0 = Disabled 1 = Enabled
R715 (02CBh) Isolation control	0	ISOLATE_DCVDD1	0	Always-On power domain isolate control Set this bit to 1 to isolate the 'Always-On' domain from the DCVDD pin. If DCVDD is powered externally (not from LDO1), this bit must be set before selecting Sleep mode (ie. before removing the external DCVDD supply). If DCVDD is powered from LDO1, then there is no requirement to set this bit. This bit is automatically reset to 0 following a Wake-up transition (from Sleep mode).
R3104 (0C20h) Misc Pad Ctrl 1	15	LDO1ENA_PD	1	LDOENA Pull-Down Control 0 = Disabled 1 = Enabled Note - when LDO1ENA_PD and LDO1ENA_PU are both set to '1', then a 'bus keeper' function is enabled on the LDOENA pin.
	14	LDO1ENA_PU	0	LDOENA Pull-Up Control 0 = Disabled 1 = Enabled Note - when LDO1ENA_PD and LDO1ENA_PU are both set to '1', then a 'bus keeper' function is enabled on the LDOENA pin.

Table 113 Charge Pump and LDO Control Registers

LDO2_VSEL [5:0]	LDO2 OUTPUT	LDO2_VSEL [5:0]	LDO2 OUTPUT
00h	1.70V	10h	2.50V
01h	1.75V	11h	2.55V
02h	1.80V	12h	2.60V
03h	1.85V	13h	2.65V
04h	1.90V	14h	2.70V
05h	1.95V	15h	2.75V
06h	2.00V	16h	2.80V
07h	2.05V	17h	2.85V
08h	2.10V	18h	2.90V
09h	2.15V	19h	2.95V
0Ah	2.20V	1Ah	3.00V
0Bh	2.25V	1Bh	3.05V
0Ch	2.30V	1Ch	3.10V
0Dh	2.35V	1Dh	3.15V
0Eh	2.40V	1Eh	3.20V
0Fh	2.45V	1Fh	3.30V

Table 114 LDO2 Voltage Control

THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTION

The WM8998 incorporates thermal protection functions, and also provides short-circuit detection on the Class D speaker output paths, as described below.

The temperature sensor detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature sensor is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”. A two-stage indication is provided, via the SPK_OVERHEAT_WARN_EINTn and SPK_OVERHEAT_EINTn interrupts.

If the upper temperature threshold (SPK_OVERHEAT_EINTn) is exceeded, then the Class D speaker outputs will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

The short circuit detection function for the Class D speaker outputs is triggered when the respective output drivers are enabled (using the register bits described in Table 52). If a short circuit is detected at this time, then the enable will be unsuccessful, and the respective output driver will not be enabled.

The Class D speaker short circuit detection provides inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

If the Class D speaker short circuit condition is detected, then the respective driver(s) will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

To enable the Class D speaker outputs following a short circuit detection, the host processor must disable and re-enable the output driver(s). Note that the short circuit status bits will always be cleared when the drivers are disabled.

The Thermal Shutdown and Short Circuit protection status flags can be output directly on a GPIO pin as an external indication of the associated events. See “General Purpose Input / Output” to configure a GPIO pin for this function.

POWER-ON RESET (POR)

The WM8998 will remain in the reset state until AVDD, DBVDD1 and DCVDD are all above their respective reset thresholds. Note that specified device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section.

Refer to “Recommended Operating Conditions” for the WM8998 power-up sequencing requirements.

If DCVDD is powered from LDO1, then the DCVDD supply must be enabled using the LDOENA pin for the initial power-up. Note that subsequent interruption to DCVDD should only be permitted as part of a control sequence for entering Sleep mode.

After the initial power-up, the Power-On Reset will be re-scheduled following an interruption to the DBVDD1 or AVDD supplies. Note that the AVDD supply must always be maintained whenever the DCVDD supply is present.

If the WM8998 SLIMbus component is in its operational state, then it must be reset prior to scheduling a Power-On Reset. See “SLIMbus Interface Control” for details of the SLIMbus reset control messages.

Following Power-On Reset (POR), a Boot Sequence is executed. The BOOT_DONE_STS register is asserted on completion of the Boot Sequence, as described in Table 115. Control register writes should not be attempted until the BOOT_DONE_STS register has been asserted.

The BOOT_DONE_STS signal is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”. Under default register conditions, a falling edge on the $\overline{IRQ}$ pin will indicate completion of the Boot Sequence.

The BOOT_DONE_STS signal can also generate a GPIO output, providing an external indication of the Boot Sequence. See “General Purpose Input / Output” to configure a GPIO pin for this function.

For details of the Boot Sequence, see “Control Write Sequencer”.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3363 (0D23h) Interrupt Raw Status 5	8	BOOT_DONE_STS	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.

Table 115 Device Boot-Up Status

Following Power-On Reset (POR), Hardware Reset, Software Reset, or Wake-Up (from Sleep mode), a sequence of device initialisation writes must be executed, as detailed in Table 116.

The host system should ensure that the WM8998 is ready before attempting these (or any other) Control Register writes: the initialisation settings should be written after the BOOT_DONE_STS bit has been asserted (also indicated by a falling edge of the $\overline{IRQ}$ pin).

WM8998 INITIALISATION	
1	Write 0x0014 to Register R529 (0x0211)
2	Write 0x0064 to Register R622 (0x026E)
3	Write 0x00EA to Register R623 (0x026F)
4	Write 0x1F16 to Register R624 (0x0270)
5	Write 0x2080 to Register R1040 (0x0410)
6	Write 0x2080 to Register R1048 (0x0418)
7	Write 0x2080 to Register R1056 (0x0420)
8	Write 0xC759 to Register R1089 (0x0441)
9	Write 0x2A08 to Register R1090 (0x0442)
10	Write 0x5CFA to Register R1091 (0x0443)
11	Write 0x080E to Register R1150 (0x047E)
12	Write 0x1120 to Register R1208 (0x04B8)
13	Write 0x0E0D to Register R1252 (0x04E4)
14	Write 0x0E0D to Register R1253 (0x04E5)
15	Write 0x0E0D to Register R1254 (0x04E6)
16	Write 0x060E to Register R1259 (0x04EB)

Table 116 Device Initialisation Register Settings

The WM8998 is in Sleep mode when AVDD and DBVDD1 are present, and DCVDD is below its reset threshold. (Note that specific control requirements are also applicable for entering Sleep mode, as described in “Low Power Sleep Configuration”.)

In Sleep mode, most of the Digital Core (and control registers) are held in reset; selected functions and control registers are maintained via an ‘Always-On’ internal supply domain. See “Low Power Sleep Configuration” for details of the ‘Always-On’ functions.

See “Hardware Reset, Software Reset, Wake-Up, and Device ID” for details of the Wake-Up transition (exit from Sleep mode).

Table 117 describes the default status of the WM8998 digital I/O pins on completion of Power-On Reset, prior to any register writes. The same default conditions are also applicable on completion of a Hardware Reset or Software Reset (see “Hardware Reset, Software Reset, Wake-Up, and Device ID”).

The same default conditions are applicable following a Wake-Up transition, except for the GPIO5, IRQ, LDOENA, MCLK2 and $\overline{\text{RESET}}$ pins. These are ‘Always-On’ pins whose configuration is unchanged in Sleep mode and during a Wake-Up transition.

Note that the default conditions described in Table 117 will not be valid if modified by the Boot Sequence or by a ‘Wake-Up’ control sequence. See “Control Write Sequencer” for details of these functions.

PIN NO	NAME	TYPE	RESET STATUS
MICVDD power domain			
C1	IN1LN / DMICCLK1	Analogue Input / Digital Output	Analogue input
C3	IN1RN / DMICDAT1	Analogue input / Digital Input	Analogue input
B1	IN2N / DMICCLK2	Analogue Input / Digital Output	Analogue input
B2	IN2P / DMICDAT2	Analogue input / Digital Input	Analogue input
DBVDD1 power domain			
F7	ADDR	Digital Input	Digital input, Pull-down to DGND
J12	AIF1BCLK	Digital Input / Output	Digital input
H11	AIF1RXDAT	Digital Input	Digital input
F10	AIF1LRCLK	Digital Input / Output	Digital input
G10	AIF1TXDAT	Digital Output	Digital output
F9	GPIO1	Digital Input / Output	Digital input, Pull-down to DGND
E11	GPIO5	Digital Input / Output	Digital input, Pull-down to DGND
F11	$\overline{\text{IRQ}}$	Digital Output	Digital output
F13	LDOENA	Digital Input	Digital input, Pull-down to DGND
H12	MCLK1	Digital Input	Digital input
F12	MCLK2	Digital Input	Digital input
D9	$\overline{\text{RESET}}$	Digital Input	Digital input, Pull-up to DBVDD1
J11	SCLK	Digital Input	Digital input
F8	SDA	Digital Input / Output	Digital input
J13	SLIMCLK	Digital Input	Digital input
G11	SLIMDAT	Digital Input / Output	Digital input
H10	SPKCLK	Digital Output	Digital output
G9	SPKDAT	Digital Output	Digital output
DBVDD2 power domain			
J9	AIF2BCLK	Digital Input / Output	Digital input
G7	AIF2RXDAT	Digital Input	Digital input
H9	AIF2LRCLK	Digital Input / Output	Digital input
H8	AIF2TXDAT	Digital Output	Digital output
H7	GPIO2	Digital Input / Output	Digital input, Pull-down to DGND
G8	GPIO4	Digital Input / Output	Digital input, Pull-down to DGND
DBVDD3 power domain			
J6	AIF3BCLK	Digital Input / Output	Digital input
G5	AIF3RXDAT	Digital Input	Digital input
H5	AIF3LRCLK	Digital Input / Output	Digital input
F5	AIF3TXDAT	Digital Output	Digital output
G4	GPIO3	Digital Input / Output	Digital input, Pull-down to DGND

Table 117 WM8998 Digital I/O Status in Reset

Note that the dual function IN1LN/DMICCLK1, IN1RN/DMICDAT1, IN2N/DMICCLK2 and IN2P/DMICDAT2 pins default to their respective analogue input functions after Power-On Reset is completed. The analogue input functions are referenced to the MICVDD power domain.

HARDWARE RESET, SOFTWARE RESET, WAKE-UP, AND DEVICE ID

The WM8998 provides a Hardware Reset function, which is executed whenever the $\overline{\text{RESET}}$ input is asserted (logic 0). The $\overline{\text{RESET}}$ input is active low and is referenced to the DBVDD1 power domain.

A Hardware Reset causes most of the WM8998 control registers to be reset to their default states. Note that the Control Write Sequencer memory contents are retained during Hardware Reset (assuming the conditions noted below).

An internal pull-up resistor is enabled by default on the $\overline{\text{RESET}}$ pin; this can be configured using the RESET_PU register bit. A pull-down resistor is also available, as described in Table 118. When the pull-up and pull-down resistors are both enabled, the WM8998 provides a 'bus keeper' function on the $\overline{\text{RESET}}$ pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (eg. if the signal is tri-stated).

If the WM8998 SLIMbus component is in its operational state, then it must be reset prior to scheduling a Hardware Reset. See "SLIMbus Interface Control" for details of the SLIMbus reset control messages.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3104 (0C20h) Misc Pad Ctrl 1	1	RESET_PU	1	RESET Pull-up enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.
	0	RESET_PD	0	RESET Pull-down enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.

Table 118 Reset Pull-Up Configuration

A Software Reset is executed by writing any value to register R0. A Software Reset causes most of the WM8998 control registers to be reset to their default states. Note that the Control Write Sequencer memory contents are retained during Software Reset (assuming the conditions noted below).

A Wake-Up transition (from Sleep mode) is similar to a Software Reset, but selected functions and control registers are maintained via an 'Always-On' internal supply domain. The 'Always-On' registers are not reset during Wake-Up. See "Low Power Sleep Configuration" for details of the 'Always-On' functions.

The Control Write Sequencer memory contents are retained during Hardware Reset, Software Reset or Sleep mode; these registers are only reset following a Power-On Reset (POR).

If DCVDD is powered from LDO1, it is recommended that the LDOENA pin is asserted (logic 1) before Hardware Reset or Software Reset, as this enables a faster reset time.

Following Hardware Reset, Software Reset or Wake-Up (from Sleep mode), a Boot Sequence is executed. The BOOT_DONE_STS register (see Table 115) is de-asserted during Hardware Reset, Software Reset and in Sleep mode. The BOOT_DONE_STS register is asserted on completion of the boot-up sequence. Control register writes should not be attempted until the BOOT_DONE_STS register has been asserted.

The BOOT_DONE_STS signal is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts".

The BOOT_DONE_STS signal can also generate a GPIO output, providing an external indication of the Boot Sequence. See "General Purpose Input / Output" to configure a GPIO pin for this function.

For details of the Boot Sequence, see "Control Write Sequencer".

Following Power-On Reset (POR), Hardware Reset, Software Reset, or Wake-Up (from Sleep mode), a sequence of device initialisation writes must be executed, as detailed in Table 119.

The host system should ensure that the WM8998 is ready before attempting these (or any other) Control Register writes: the initialisation settings should be written after the BOOT_DONE_STS bit has been asserted (also indicated by a falling edge of the $\overline{IRQ}$ pin).

WM8998 INITIALISATION	
1	Write 0x0014 to Register R529 (0x0211)
2	Write 0x0064 to Register R622 (0x026E)
3	Write 0x00EA to Register R623 (0x026F)
4	Write 0x1F16 to Register R624 (0x0270)
5	Write 0x2080 to Register R1040 (0x0410)
6	Write 0x2080 to Register R1048 (0x0418)
7	Write 0x2080 to Register R1056 (0x0420)
8	Write 0xC759 to Register R1089 (0x0441)
9	Write 0x2A08 to Register R1090 (0x0442)
10	Write 0x5CFA to Register R1091 (0x0443)
11	Write 0x080E to Register R1150 (0x047E)
12	Write 0x1120 to Register R1208 (0x04B8)
13	Write 0x0E0D to Register R1252 (0x04E4)
14	Write 0x0E0D to Register R1253 (0x04E5)
15	Write 0x0E0D to Register R1254 (0x04E6)
16	Write 0x060E to Register R1259 (0x04EB)

Table 119 Device Initialisation Register Settings

The status of the WM8998 digital I/O pins following Hardware Reset, Software Reset or Wake-Up is described in the “Power-On Reset (POR)” section.

The Device ID can be read back from Register R0. The Hardware Revision can be read back from Register R1.

The Software Revision can be read back from Register R2. The Software Revision code is incremented if software driver compatibility or software feature support is changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Software Reset	15:0	SW_RST_DEV_ID [15:0]	6349h	Writing to this register resets all registers to their default state. Reading from this register will indicate Device ID 6349h.
R1 (0001h) Hardware Revision	7:0	HW_REVISION [7:0]		Hardware Device revision. (incremented for every new revision of the device)
R2 (0002h) Software Revision	7:0	SW_REVISION [7:0]		Software Device revision. (incremented if software driver compatibility or software feature support is changed)

Table 120 Device Reset and ID

REGISTER MAP

The WM8998 control registers are listed below. Note that only the register addresses described here should be accessed; writing to other addresses may result in undefined behaviour. Register bits that are not documented should not be changed from the default values.

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset	SW_RST_DEV_ID [15:0]																6349h
R1 (1h)	Hardware Revision	0	0	0	0	0	0	0	0	HW_REVISION [7:0]								0000h
R2 (2h)	Software Revision	0	0	0	0	0	0	0	0	SW_REVISION [7:0]								0000h
R9 (9h)	Ctrl IF I2C1 CFG 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	I2C1_AUTO_INC [1:0]		0001h
R11 (Bh)	Ctrl IF I2C1 CFG 2	0	0	0	0	0	0	0	0	0	I2C1_DEV_ID [6:0]							001Ah
R22 (16h)	Write Sequencer Ctrl 0	0	0	0	0	WSEQ_ABORT	WSEQ_START	WSEQ_ENA	WSEQ_START_INDEX [8:0]									0000h
R23 (17h)	Write Sequencer Ctrl 1	0	0	0	0	0	0	WSEQ_BUSY	WSEQ_CURRENT_INDEX [8:0]									0000h
R24 (18h)	Write Sequencer Ctrl 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WSEQ_BOOT_START	WSEQ_LOAD_MEM	0000h
R32 (20h)	Tone Generator 1	0	TONE_RATE [3:0]				0	TONE_OFFSET [1:0]		0	0	TONE2_OVD	TONE1_OVD	0	0	TONE2_ENA	TONE1_ENA	0000h
R33 (21h)	Tone Generator 2	TONE1_LVL [15:0]																1000h
R34 (22h)	Tone Generator 3	0	0	0	0	0	0	0	0	TONE1_LVL [7:0]								0000h
R35 (23h)	Tone Generator 4	TONE2_LVL [15:0]																1000h
R36 (24h)	Tone Generator 5	0	0	0	0	0	0	0	0	TONE2_LVL [7:0]								0000h
R48 (30h)	PWM Drive 1	0	PWM_RATE [3:0]				PWM_CLK_SEL [2:0]			0	0	PWM2_OVD	PWM1_OVD	0	0	PWM2_ENA	PWM1_ENA	0000h
R49 (31h)	PWM Drive 2	0	0	0	0	0	0	PWM1_LVL [9:0]										0100h
R50 (32h)	PWM Drive 3	0	0	0	0	0	0	PWM2_LVL [9:0]										0100h
R64 (40h)	Wake control	0	0	0	0	0	0	0	0	WKUP_MICD_CLAMP_FALL	WKUP_MICD_CLAMP_RISE	WKUP_GP5_FALL	WKUP_GP5_RISE	WKUP_JD1_FALL	WKUP_JD1_RISE	0	0	0000h
R65 (41h)	Sequence control	0	0	0	0	0	0	0	0	WSEQ_ENA_MICD_CLAMP_FALL	WSEQ_ENA_MICD_CLAMP_RISE	WSEQ_ENA_GP5_FALL	WSEQ_ENA_GP5_RISE	WSEQ_ENA_JD1_FALL	WSEQ_ENA_JD1_RISE	0	0	0000h
R97 (61h)	Sample Rate Sequence Select 1	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0]									01FFh
R98 (62h)	Sample Rate Sequence Select 2	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0]									01FFh
R99 (63h)	Sample Rate Sequence	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0]									01FFh

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
	Select 3																	
R100 (64h)	Sample Rate Sequence Select 4	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0]									01FFh
R102 (66h)	Always On Triggers Sequence Select 1	0	0	0	0	0	0	0	WSEQ_MICD_CLAMP_RISE_INDEX [8:0]									01FFh
R103 (67h)	Always On Triggers Sequence Select 2	0	0	0	0	0	0	0	WSEQ_MICD_CLAMP_FALL_INDEX [8:0]									01FFh
R104 (68h)	Always On Triggers Sequence Select 3	0	0	0	0	0	0	0	WSEQ_GP5_RISE_INDEX [8:0]									01FFh
R105 (69h)	Always On Triggers Sequence Select 4	0	0	0	0	0	0	0	WSEQ_GP5_FALL_INDEX [8:0]									01FFh
R106 (6Ah)	Always On Triggers Sequence Select 5	0	0	0	0	0	0	0	WSEQ_JD1_RISE_INDEX [8:0]									01FFh
R107 (6Bh)	Always On Triggers Sequence Select 6	0	0	0	0	0	0	0	WSEQ_JD1_FALL_INDEX [8:0]									01FFh
R110 (6Eh)	Trigger Sequence Select 32	0	0	0	0	0	0	0	WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0]									01FFh
R111 (6Fh)	Trigger Sequence Select 33	0	0	0	0	0	0	0	WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0]									01FFh
R144 (90h)	Haptics Control 1	0	HAP_RATE [3:0]				0	0	0	0	0	0	ONESHOT_TRIG	HAP_CTRL [1:0]		HAP_ACT	0	0000h
R145 (91h)	Haptics Control 2	0	LRA_FREQ [14:0]															7FFFh
R146 (92h)	Haptics phase 1 intensity	0	0	0	0	0	0	0	0	PHASE1_INTENSITY [7:0]								0000h
R147 (93h)	Haptics phase 1 duration	0	0	0	0	0	0	0	PHASE1_DURATION [8:0]									0000h
R148 (94h)	Haptics phase 2 intensity	0	0	0	0	0	0	0	0	PHASE2_INTENSITY [7:0]								0000h
R149 (95h)	Haptics phase 2 duration	0	0	0	0	0	PHASE2_DURATION [10:0]											0000h
R150 (96h)	Haptics phase 3 intensity	0	0	0	0	0	0	0	0	PHASE3_INTENSITY [7:0]								0000h
R151 (97h)	Haptics phase 3 duration	0	0	0	0	0	0	0	PHASE3_DURATION [8:0]									0000h
R152 (98h)	Haptics Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ONESHOT_STS	0000h
R256 (100h)	Clock 32k 1	0	0	0	0	0	0	0	0	0	CLK_32K_ENA	0	0	0	0	CLK_32K_SRC [1:0]		0002h
R257 (101h)	System Clock 1	SYSCLK_FRA	0	0	0	0	SYSCLK_FREQ [2:0]			0	SYSCLK_ENA	0	0	SYSCLK_SRC [3:0]				0304h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		C																
R258 (102h)	Sample rate 1	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_1 [4:0]					0011h
R259 (103h)	Sample rate 2	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_2 [4:0]					0011h
R260 (104h)	Sample rate 3	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_3 [4:0]					0011h
R266 (10Ah)	Sample rate 1 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_1_STS [4:0]					0000h
R267 (10Bh)	Sample rate 2 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_2_STS [4:0]					0000h
R268 (10Ch)	Sample rate 3 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_3_STS [4:0]					0000h
R274 (112h)	Async clock 1	0	0	0	0	0	ASYNC_CLK_FREQ [2:0]			0	ASYNC_CLK_ENA	0	0	ASYNC_CLK_SRC [3:0]				0305h
R275 (113h)	Async sample rate 1	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_1 [4:0]					0011h
R276 (114h)	Async sample rate 2	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_2 [4:0]					0011h
R283 (11Bh)	Async sample rate 1 status	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_1_STS [4:0]					0000h
R284 (11Ch)	Async sample rate 2 status	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_2_STS [4:0]					0000h
R329 (149h)	Output system clock	OPCLK_ENA	0	0	0	0	0	0	0	OPCLK_DIV [4:0]					OPCLK_SEL [2:0]			0000h
R330 (14Ah)	Output async clock	OPCLK_ASYNC_ENA	0	0	0	0	0	0	0	OPCLK_ASYNC_DIV [4:0]					OPCLK_ASYNC_SEL [2:0]			0000h
R338 (152h)	Rate Estimator 1	0	0	0	0	0	0	0	0	0	0	0	TRIG_ON_STARTUP	LRCLK_SRC [2:0]			RATE_EST_ENA	0000h
R339 (153h)	Rate Estimator 2	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_A [4:0]					0000h
R340 (154h)	Rate Estimator 3	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_B [4:0]					0000h
R341 (155h)	Rate Estimator 4	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_C [4:0]					0000h
R342 (156h)	Rate Estimator 5	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_D [4:0]					0000h
R353 (161h)	Dynamic Frequency Scaling 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SUBSYS_MAX_FREQ	0000h
R369 (171h)	FLL1 Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL1_FREERUN	FLL1_ENA	0002h
R370 (172h)	FLL1 Control 2	FLL1_CTRL_UPD	0	0	0	0	0	FLL1_N [9:0]										0008h
R371 (173h)	FLL1 Control 3	FLL1_THETA [15:0]																0018h
R372 (174h)	FLL1 Control 4	FLL1_LAMBDA [15:0]																007Dh
R373 (175h)	FLL1 Control 5	0	0	0	0	FLL1_FRATIO [3:0]				0	0	0	0	FLL1_OUTDIV [2:0]			0	0004h
R374 (176h)	FLL1 Control 6	0	0	0	0	0	0	0	0	FLL1_REFCLK_DIV [1:0]		0	0	FLL1_REFCLK_SRC [3:0]				0000h
R375 (177h)	FLL1 Loop Filter Test 1	FLL1_FRC_INTEG_UPD	0	0	0	FLL1_FRC_INTEG_VAL [11:0]												0181h
R376 (178h)	FLL1 NCO Test 0	FLL1_INTEG_	0	0	0	FLL1_INTEG [11:0]												0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		VALID																
R377 (179h)	FLL1 Control 7	0	0	0	0	0	0	0	0	0	0	FLL1_GAIN [3:0]				0	0	0000h
R385 (181h)	FLL1 Synchroniser 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL1_SYNC_ENA	0000h
R386 (182h)	FLL1 Synchroniser 2	0	0	0	0	0	0	FLL1_SYNC_N [9:0]										0000h
R387 (183h)	FLL1 Synchroniser 3	FLL1_SYNC_THETA [15:0]																0000h
R388 (184h)	FLL1 Synchroniser 4	FLL1_SYNC_LAMBDA [15:0]																0000h
R389 (185h)	FLL1 Synchroniser 5	0	0	0	0	0	FLL1_SYNC_FRATIO [2:0]			0	0	0	0	0	0	0	0	0000h
R390 (186h)	FLL1 Synchroniser 6	0	0	0	0	0	0	0	0	FLL1_SYNCCLK_DIV [1:0]		0	0	FLL1_SYNCCLK_SRC [3:0]				0000h
R391 (187h)	FLL1 Synchroniser 7	0	0	0	0	0	0	0	0	0	0	FLL1_SYNC_GAIN [3:0]				0	FLL1_SYNC_DFSAT	0001h
R393 (189h)	FLL1 Spread Spectrum	0	0	0	0	0	0	0	0	0	0	FLL1_SS_AMPL [1:0]		FLL1_SS_FREQ [1:0]		FLL1_SS_SEL [1:0]		0000h
R394 (18Ah)	FLL1 GPIO Clock	0	0	0	0	0	0	0	0	FLL1_GPCLK_DIV [6:0]							FLL1_GPCLK_ENA	0004h
R401 (191h)	FLL2 Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL2_FREERUN	FLL2_ENA	0000h
R402 (192h)	FLL2 Control 2	FLL2_CTRL_UPD	0	0	0	0	0	FLL2_N [9:0]										0008h
R403 (193h)	FLL2 Control 3	FLL2_THETA [15:0]																0018h
R404 (194h)	FLL2 Control 4	FLL2_LAMBDA [15:0]																007Dh
R405 (195h)	FLL2 Control 5	0	0	0	0	FLL2_FRATIO [3:0]				0	0	0	0	FLL2_OUTDIV [2:0]			0	0004h
R406 (196h)	FLL2 Control 6	0	0	0	0	0	0	0	0	FLL2_REFCLK_DIV [1:0]		0	0	FLL2_REFCLK_SRC [3:0]				0000h
R407 (197h)	FLL2 Loop Filter Test 1	FLL2_FRC_INTEG_UPD	0	0	0	FLL2_FRC_INTEG_VAL [11:0]												0000h
R408 (198h)	FLL2 NCO Test 0	FLL2_INTEG_VALID	0	0	0	FLL2_INTEG [11:0]												0000h
R409 (199h)	FLL2 Control 7	0	0	0	0	0	0	0	0	0	0	FLL2_GAIN [3:0]				0	0	0000h
R417 (1A1h)	FLL2 Synchroniser 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL2_SYNC_ENA	0000h
R418 (1A2h)	FLL2 Synchroniser 2	0	0	0	0	0	0	FLL2_SYNC_N [9:0]										0000h
R419 (1A3h)	FLL2 Synchroniser 3	FLL2_SYNC_THETA [15:0]																0000h
R420 (1A4h)	FLL2 Synchroniser 4	FLL2_SYNC_LAMBDA [15:0]																0000h
R421 (1A5h)	FLL2 Synchroniser 5	0	0	0	0	0	FLL2_SYNC_FRATIO [2:0]			0	0	0	0	0	0	0	0	0000h
R422 (1A6h)	FLL2 Synchroniser 6	0	0	0	0	0	0	0	0	FLL2_SYNCCLK_DIV [1:0]		0	0	FLL2_SYNCCLK_SRC [3:0]				0000h
R423 (1A7h)	FLL2 Synchroniser 7	0	0	0	0	0	0	0	0	0	0	FLL2_SYNC_GAIN [3:0]				0	FLL2_SYNC_	0001h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
																	DFSAT	
R425 (1A9h)	FLL2 Spread Spectrum	0	0	0	0	0	0	0	0	0	0	FLL2_SS_AMPL [1:0]		FLL2_SS_FREQ [1:0]		FLL2_SS_SEL [1:0]		0000h
R426 (1AAh)	FLL2 GPIO Clock	0	0	0	0	0	0	0	0	FLL2_GPCLK_DIV [6:0]							FLL2_GPCLK_ENA	0004h
R512 (200h)	Mic Charge Pump 1	0	0	0	0	0	0	0	0	0	0	0	0	0	CP2_DISCH	CP2_BYPASS	CP2_ENA	0006h
R528 (210h)	LDO1 Control 1	0	0	0	0	0	LDO1_VSEL [5:0]						1	0	LDO1_DISCH	LDO1_BYPASS	LDO1_ENA	00D4h
R530 (212h)	LDO1 Control 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LDO1_HI_PWR	0001h
R531 (213h)	LDO2 Control 1	0	0	0	0	0	LDO2_VSEL [5:0]						0	0	LDO2_DISCH	0	0	0344h
R536 (218h)	Mic Bias Ctrl 1	MICB1_EXT_CAP	0	0	0	0	0	0	MICB1_LVL [3:0]				0	MICB1_RATE	MICB1_DISCH	MICB1_BYPASS	MICB1_ENA	01A6h
R537 (219h)	Mic Bias Ctrl 2	MICB2_EXT_CAP	0	0	0	0	0	0	MICB2_LVL [3:0]				0	MICB2_RATE	MICB2_DISCH	MICB2_BYPASS	MICB2_ENA	01A6h
R538 (21Ah)	Mic Bias Ctrl 3	MICB3_EXT_CAP	0	0	0	0	0	0	MICB3_LVL [3:0]				0	MICB3_RATE	MICB3_DISCH	MICB3_BYPASS	MICB3_ENA	01A6h
R659 (293h)	Accessory Detect Mode 1	0	0	ACCDET_SRC	0	0	0	0	0	1	0	0	0	0	ACCDET_MODE [2:0]			0080h
R667 (29Bh)	Headphone Detect 1	0	0	0	0	0	HP_IMPEDANCE_RANGE [1:0]		0	HP_HOLDTIME [2:0]			HP_CLK_DIV [1:0]		0	0	HP_POLL	0000h
R668 (29Ch)	Headphone Detect 2	HP_DONE	HP_LVL [14:0]															0000h
R674 (2A2h)	Micd Clamp control	0	0	0	0	0	0	0	0	0	0	0	0	MICD_CLAMP_MODE [3:0]				0000h
R675 (2A3h)	Mic Detect 1	MICD_BIAS_STARTTIME [3:0]			MICD_RATE [3:0]					0	0	MICD_BIAS_SRC [1:0]		0	0	MICD_DBTIME	MICD_ENA	1102h
R676 (2A4h)	Mic Detect 2	0	MICDET_HOLD_TIME [1:0]		0	0	0	0	0	MICD_LVL_SEL [7:0]								009Fh
R677 (2A5h)	Mic Detect 3	0	0	0	0	0	MICD_LVL [8:0]									MICD_VALID	MICD_STS	0000h
R683 (2ABh)	Mic Detect 4	MICDET_ADCVAL_DIFF [7:0]								0	MICDET_ADCVAL [6:0]							0000h
R715 (2CBh)	Isolation control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISOLATE_DCVDD1	0000h
R723 (2D3h)	Jack detect analogue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	JD1_ENA	0000h
R768 (300h)	Input Enables	0	0	0	0	0	0	0	0	0	0	0	0	IN2_ENA	0	IN1L_ENA	IN1R_ENA	0000h
R769 (301h)	Input Enables Status	0	0	0	0	0	0	0	0	0	0	0	0	IN2_ENA_STS	0	IN1L_ENA_STS	IN1R_ENA_STS	0000h
R776 (308h)	Input Rate	0	IN_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R777 (309h)	Input Volume Ramp	0	0	0	0	0	0	0	0	0	IN_VD_RAMP [2:0]			0	IN_VI_RAMP [2:0]			0022h
R780 (30Ch)	HPF Control	0	0	0	0	0	0	0	0	0	0	0	0	0	IN_HPF_CUT [2:0]			0002h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R784 (310h)	IN1L Control	IN1L_HPF	IN1_OSR [1:0]		IN1_DMIC_SUP [1:0]		IN1_MODE	0	0	IN1L_PGA_VOL [6:0]							0	2080h
R785 (311h)	ADC Digital Volume 1L	0	IN1L_SRC [1:0]		0	0	0	IN_VU	IN1L_MUTE	IN1L_VOL [7:0]								0180h
R786 (312h)	DMIC1L Control	0	0	0	0	0	0	0	0	0	0	IN1L_DMIC_DLY [5:0]						0000h
R788 (314h)	IN1R Control	IN1R_HPF	0	0	0	0	0	0	0	IN1R_PGA_VOL [6:0]							0	0080h
R789 (315h)	ADC Digital Volume 1R	0	IN1R_SRC [1:0]		0	0	0	IN_VU	IN1R_MUTE	IN1R_VOL [7:0]								0180h
R790 (316h)	DMIC1R Control	0	0	0	0	0	0	0	0	0	0	IN1R_DMIC_DLY [5:0]						0000h
R792 (318h)	IN2L Control	IN2_HPF	IN2_OSR [1:0]		IN2_DMIC_SUP [1:0]		IN2_MODE	0	0	IN2_PGA_VOL [6:0]							0	2080h
R793 (319h)	ADC Digital Volume 2L	0	IN2_SRC [1:0]		0	0	0	IN_VU	IN2_MUTE	IN2_VOL [7:0]								0180h
R794 (31Ah)	DMIC2L Control	0	0	0	0	0	0	0	0	0	0	IN2_DMIC_DLY [5:0]						0000h
R1024 (400h)	Output Enables 1	0	0	0	0	0	0	OUT5L_ENA	OUT5R_ENA	SPKOUTL_ENA	SPKOUTR_ENA	EP_ENA	0	LINEL_ENA	LINER_ENA	HPL_ENA	HPR_ENA	0000h
R1025 (401h)	Output Status 1	0	0	0	0	0	0	OUT5L_ENA_STS	OUT5R_ENA_STS	OUT4L_ENA_STS	OUT4R_ENA_STS	0	0	0	0	0	0	0000h
R1030 (406h)	Raw Output Status 1	0	0	0	0	0	0	0	0	0	0	OUT3_ENA_STS	0	OUT2L_ENA_STS	OUT2R_ENA_STS	OUT1L_ENA_STS	OUT1R_ENA_STS	0000h
R1032 (408h)	Output Rate 1	0	OUT_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R1033 (409h)	Output Volume Ramp	0	0	0	0	0	0	0	0	0	OUT_VD_RAMP [2:0]			0	OUT_VI_RAMP [2:0]			0022h
R1040 (410h)	Output Path Config 1L	0	0	OUT1_OSR	OUT1_MONO	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R1041 (411h)	DAC Digital Volume 1L	0	0	0	0	0	0	OUT_VU	OUT1L_MUTE	OUT1L_VOL [7:0]								0180h
R1043 (413h)	Noise Gate Select 1L	0	0	0	0	OUT1L_NGATE_SRC [11:0]												0001h
R1045 (415h)	DAC Digital Volume 1R	0	0	0	0	0	0	OUT_VU	OUT1R_MUTE	OUT1R_VOL [7:0]								0180h
R1047 (417h)	Noise Gate Select 1R	0	0	0	0	OUT1R_NGATE_SRC [11:0]												0002h
R1048 (418h)	Output Path Config 2L	0	0	OUT2_OSR	OUT2_MONO	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R1049 (419h)	DAC Digital Volume 2L	0	0	0	0	0	0	OUT_VU	OUT2L_MUTE	OUT2L_VOL [7:0]								0180h
R1051 (41Bh)	Noise Gate Select 2L	0	0	0	0	OUT2L_NGATE_SRC [11:0]												0004h
R1053 (41Dh)	DAC Digital Volume 2R	0	0	0	0	0	0	OUT_VU	OUT2R_MUTE	OUT2R_VOL [7:0]								0180h
R1055 (41Fh)	Noise Gate Select 2R	0	0	0	0	OUT2R_NGATE_SRC [11:0]												0008h
R1057 (421h)	DAC Digital Volume 3L	0	0	0	0	0	0	OUT_VU	OUT3_MUTE	OUT3_VOL [7:0]								0180h
R1059 (423h)	Noise Gate Select 3L	0	0	0	0	OUT3_NGATE_SRC [11:0]												0010h
R1064 (428h)	Output Path Config 4L	0	0	OUT4_OSR	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R1065 (429h)	DAC Digital Volume 4L	0	0	0	0	0	0	OUT_VU	OUT4L_MUTE	OUT4L_VOL [7:0]								0180h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1067 (42Bh)	Noise Gate Select 4L	OUT4L_NGATE_SRC [11:0]																0040h
R1069 (42Dh)	DAC Digital Volume 4R	0	0	0	0	0	0	OUT_VU	OUT4R_MUTE	OUT4R_VOL [7:0]								0180h
R1071 (42Fh)	Noise Gate Select 4R	OUT4R_NGATE_SRC [11:0]																0080h
R1072 (430h)	Output Path Config 5L	0	0	OUT5_OSR	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R1073 (431h)	DAC Digital Volume 5L	0	0	0	0	0	0	OUT_VU	OUT5L_MUTE	OUT5L_VOL [7:0]								0180h
R1075 (433h)	Noise Gate Select 5L	OUT5L_NGATE_SRC [11:0]																0100h
R1077 (435h)	DAC Digital Volume 5R	0	0	0	0	0	0	OUT_VU	OUT5R_MUTE	OUT5R_VOL [7:0]								0180h
R1079 (437h)	Noise Gate Select 5R	OUT5R_NGATE_SRC [11:0]																0200h
R1104 (450h)	DAC AEC Control 1	0	0	0	0	0	0	0	0	0	0	AEC1_LOOPBACK_SRC [3:0]				AEC1_ENA_STS	AEC1_LOOPBACK_ENA	0000h
R1105 (451h)	DAC AEC Control 2	0	0	0	0	0	0	0	0	0	0	AEC2_LOOPBACK_SRC [3:0]				AEC2_ENA_STS	AEC2_LOOPBACK_ENA	0000h
R1112 (458h)	Noise Gate Control	0	0	0	0	0	0	0	0	0	0	NGATE_HOLD [1:0]		NGATE_THR [2:0]			NGATE_ENA	0000h
R1168 (490h)	PDM SPK1 CTRL 1	0	0	SPK1R_MUTE	SPK1L_MUTE	0	0	0	SPK1_MUTE_ENDIAN	SPK1_MUTE_SEQ [7:0]								0069h
R1169 (491h)	PDM SPK1 CTRL 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SPK1_FMT	0000h
R1280 (500h)	AIF1 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF1_BCLK_INV	AIF1_BCLK_FRC	AIF1_BCLK_MSTR	AIF1_BCLK_FREQ [4:0]					000Ch
R1281 (501h)	AIF1 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF1TX_DAT_TRI	0	1	0	0	0	0008h
R1282 (502h)	AIF1 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1_LRCLK_INV	AIF1_LRCLK_FRC	AIF1_LRCLK_MSTR	0000h
R1283 (503h)	AIF1 Rate Ctrl	0	AIF1_RATE [3:0]			0	0	0	0	0	AIF1_TRI	0	0	0	0	0	0	0000h
R1284 (504h)	AIF1 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1_FMT [2:0]			0000h
R1286 (506h)	AIF1 Rx BCLK Rate	0	0	0	AIF1_BCPF [12:0]													0040h
R1287 (507h)	AIF1 Frame Ctrl 1	0	0	AIF1TX_WL [5:0]						AIF1TX_SLOT_LEN [7:0]								1818h
R1288 (508h)	AIF1 Frame Ctrl 2	0	0	AIF1RX_WL [5:0]						AIF1RX_SLOT_LEN [7:0]								1818h
R1289 (509h)	AIF1 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF1TX1_SLOT [5:0]						0000h
R1290 (50Ah)	AIF1 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF1TX2_SLOT [5:0]						0001h
R1291 (50Bh)	AIF1 Frame Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF1TX3_SLOT [5:0]						0002h
R1292	AIF1 Frame Ctrl	0	0	0	0	0	0	0	0	0	0	AIF1TX4_SLOT [5:0]						0003h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(50Ch)	6																	
R1293 (50Dh)	AIF1 Frame Ctrl 7	0	0	0	0	0	0	0	0	0	0	AIF1TX5_SLOT [5:0]						0004h
R1294 (50Eh)	AIF1 Frame Ctrl 8	0	0	0	0	0	0	0	0	0	0	AIF1TX6_SLOT [5:0]						0005h
R1297 (511h)	AIF1 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF1RX1_SLOT [5:0]						0000h
R1298 (512h)	AIF1 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF1RX2_SLOT [5:0]						0001h
R1299 (513h)	AIF1 Frame Ctrl 13	0	0	0	0	0	0	0	0	0	0	AIF1RX3_SLOT [5:0]						0002h
R1300 (514h)	AIF1 Frame Ctrl 14	0	0	0	0	0	0	0	0	0	0	AIF1RX4_SLOT [5:0]						0003h
R1301 (515h)	AIF1 Frame Ctrl 15	0	0	0	0	0	0	0	0	0	0	AIF1RX5_SLOT [5:0]						0004h
R1302 (516h)	AIF1 Frame Ctrl 16	0	0	0	0	0	0	0	0	0	0	AIF1RX6_SLOT [5:0]						0005h
R1305 (519h)	AIF1 Tx Enables	0	0	0	0	0	0	0	0	0	0	AIF1TX6_ENA	AIF1TX5_ENA	AIF1TX4_ENA	AIF1TX3_ENA	AIF1TX2_ENA	AIF1TX1_ENA	0000h
R1306 (51Ah)	AIF1 Rx Enables	0	0	0	0	0	0	0	0	0	0	AIF1RX6_ENA	AIF1RX5_ENA	AIF1RX4_ENA	AIF1RX3_ENA	AIF1RX2_ENA	AIF1RX1_ENA	0000h
R1344 (540h)	AIF2 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF2_BCLK_INV	AIF2_BCLK_FRC	AIF2_BCLK_MSTR	AIF2_BCLK_FREQ [4:0]					000Ch
R1345 (541h)	AIF2 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF2TX_DAT_TRI	0	1	0	0	0	0008h
R1346 (542h)	AIF2 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2_LRCLK_INV	AIF2_LRCLK_FRC	AIF2_LRCLK_MSTR	0000h
R1347 (543h)	AIF2 Rate Ctrl	0	AIF2_RATE [3:0]				0	0	0	0	AIF2_TRI	0	0	0	0	0	0	0000h
R1348 (544h)	AIF2 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2_FMT [2:0]			0000h
R1350 (546h)	AIF2 Rx BCLK Rate	0	0	0	AIF2_BCPF [12:0]													0040h
R1351 (547h)	AIF2 Frame Ctrl 1	0	0	AIF2TX_WL [5:0]						AIF2TX_SLOT_LEN [7:0]								1818h
R1352 (548h)	AIF2 Frame Ctrl 2	0	0	AIF2RX_WL [5:0]						AIF2RX_SLOT_LEN [7:0]								1818h
R1353 (549h)	AIF2 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF2TX1_SLOT [5:0]						0000h
R1354 (54Ah)	AIF2 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF2TX2_SLOT [5:0]						0001h
R1355 (54Bh)	AIF2 Frame Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF2TX3_SLOT [5:0]						0002h
R1356 (54Ch)	AIF2 Frame Ctrl 6	0	0	0	0	0	0	0	0	0	0	AIF2TX4_SLOT [5:0]						0003h
R1357 (54Dh)	AIF2 Frame Ctrl 7	0	0	0	0	0	0	0	0	0	0	AIF2TX5_SLOT [5:0]						0004h
R1358 (54Eh)	AIF2 Frame Ctrl 8	0	0	0	0	0	0	0	0	0	0	AIF2TX6_SLOT [5:0]						0005h
R1361 (551h)	AIF2 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF2RX1_SLOT [5:0]						0000h
R1362 (552h)	AIF2 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF2RX2_SLOT [5:0]						0001h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1363 (553h)	AIF2 Frame Ctrl 13	0	0	0	0	0	0	0	0	0	0	AIF2RX3_SLOT [5:0]						0002h
R1364 (554h)	AIF2 Frame Ctrl 14	0	0	0	0	0	0	0	0	0	0	AIF2RX4_SLOT [5:0]						0003h
R1365 (555h)	AIF2 Frame Ctrl 15	0	0	0	0	0	0	0	0	0	0	AIF2RX5_SLOT [5:0]						0004h
R1366 (556h)	AIF2 Frame Ctrl 16	0	0	0	0	0	0	0	0	0	0	AIF2RX6_SLOT [5:0]						0005h
R1369 (559h)	AIF2 Tx Enables	0	0	0	0	0	0	0	0	0	0	AIF2TX6_ENA	AIF2TX5_ENA	AIF2TX4_ENA	AIF2TX3_ENA	AIF2TX2_ENA	AIF2TX1_ENA	0000h
R1370 (55Ah)	AIF2 Rx Enables	0	0	0	0	0	0	0	0	0	0	AIF2RX6_ENA	AIF2RX5_ENA	AIF2RX4_ENA	AIF2RX3_ENA	AIF2RX2_ENA	AIF2RX1_ENA	0000h
R1408 (580h)	AIF3 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF3_BCLK_INV	AIF3_BCLK_FRC	AIF3_BCLK_MSTR	AIF3_BCLK_FREQ [4:0]					000Ch
R1409 (581h)	AIF3 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF3TX_DAT_TRI	0	1	0	0	0	0008h
R1410 (582h)	AIF3 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3_LRCLK_INV	AIF3_LRCLK_FRC	AIF3_LRCLK_MSTR	0000h
R1411 (583h)	AIF3 Rate Ctrl	0	AIF3_RATE [3:0]				0	0	0	0	AIF3_TRI	0	0	0	0	0	0	0000h
R1412 (584h)	AIF3 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3_FMT [2:0]			0000h
R1414 (586h)	AIF3 Rx BCLK Rate	0	0	0	AIF3_BCPF [12:0]													0040h
R1415 (587h)	AIF3 Frame Ctrl 1	0	0	AIF3TX_WL [5:0]						AIF3TX_SLOT_LEN [7:0]								1818h
R1416 (588h)	AIF3 Frame Ctrl 2	0	0	AIF3RX_WL [5:0]						AIF3RX_SLOT_LEN [7:0]								1818h
R1417 (589h)	AIF3 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF3TX1_SLOT [5:0]						0000h
R1418 (58Ah)	AIF3 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF3TX2_SLOT [5:0]						0001h
R1425 (591h)	AIF3 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF3RX1_SLOT [5:0]						0000h
R1426 (592h)	AIF3 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF3RX2_SLOT [5:0]						0001h
R1433 (599h)	AIF3 Tx Enables	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3TX2_ENA	AIF3TX1_ENA	0000h
R1434 (59Ah)	AIF3 Rx Enables	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3RX2_ENA	AIF3RX1_ENA	0000h
R1474 (5C2h)	SPD1 TX Control	0	0	SPD1_VAL2	SPD1_VAL1	0	0	0	0	SPD1_RATE [3:0]				0	0	0	SPD1_ENA	0000h
R1475 (5C3h)	SPD1 TX Channel Status 1	SPD1_CATCODE [7:0]								SPD1_CHSTMODE [1:0]		SPD1_PREEMPH [2:0]			SPD1_NOCOPY	SPD1_NOAUDIO	SPD1_PRO	0000h
R1476 (5C4h)	SPD1 TX Channel Status 2	SPD1_FREQ [3:0]				SPD1_CHNUM2 [3:0]				SPD1_CHNUM1 [3:0]				SPD1_SRCNUM [3:0]				0B01h
R1477 (5C5h)	SPD1 TX Channel Status 3	0	0	0	0	SPD1_ORGSAMP [3:0]				SPD1_TXWL [2:0]			SPD1_MAXWL	SPD1_CS31_30 [1:0]		SPD1_CLKACU [1:0]		0000h
R1490 (5D2h)	SLIMbus RX Ports0	0	0	SLIMRX2_PORT_ADDR [5:0]						0	0	SLIMRX1_PORT_ADDR [5:0]						0100h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1491 (5D3h)	SLIMbus RX Ports1	0	0	SLIMRX4_PORT_ADDR [5:0]						0	0	SLIMRX3_PORT_ADDR [5:0]						0302h
R1494 (5D6h)	SLIMbus TX Ports0	0	0	SLIMTX2_PORT_ADDR [5:0]						0	0	SLIMTX1_PORT_ADDR [5:0]						0908h
R1495 (5D7h)	SLIMbus TX Ports1	0	0	SLIMTX4_PORT_ADDR [5:0]						0	0	SLIMTX3_PORT_ADDR [5:0]						0B0Ah
R1496 (5D8h)	SLIMbus TX Ports2	0	0	SLIMTX6_PORT_ADDR [5:0]						0	0	SLIMTX5_PORT_ADDR [5:0]						0D0Ch
R1507 (5E3h)	SLIMbus Framer Ref Gear	0	0	0	0	0	0	0	0	0	0	0	0	SLIMCLK_REF_GEAR [3:0]				0004h
R1509 (5E5h)	SLIMbus Rates 1	0	SLIMRX2_RATE [3:0]				0	0	0	0	SLIMRX1_RATE [3:0]				0	0	0	0000h
R1510 (5E6h)	SLIMbus Rates 2	0	SLIMRX4_RATE [3:0]				0	0	0	0	SLIMRX3_RATE [3:0]				0	0	0	0000h
R1513 (5E9h)	SLIMbus Rates 5	0	SLIMTX2_RATE [3:0]				0	0	0	0	SLIMTX1_RATE [3:0]				0	0	0	0000h
R1514 (5EAh)	SLIMbus Rates 6	0	SLIMTX4_RATE [3:0]				0	0	0	0	SLIMTX3_RATE [3:0]				0	0	0	0000h
R1515 (5EBh)	SLIMbus Rates 7	0	SLIMTX6_RATE [3:0]				0	0	0	0	SLIMTX5_RATE [3:0]				0	0	0	0000h
R1525 (5F5h)	SLIMbus RX Channel Enable	0	0	0	0	0	0	0	0	0	0	0	0	SLIMRX4_ENA	SLIMRX3_ENA	SLIMRX2_ENA	SLIMRX1_ENA	0000h
R1526 (5F6h)	SLIMbus TX Channel Enable	0	0	0	0	0	0	0	0	0	0	SLIMTX6_ENA	SLIMTX5_ENA	SLIMTX4_ENA	SLIMTX3_ENA	SLIMTX2_ENA	SLIMTX1_ENA	0000h
R1527 (5F7h)	SLIMbus RX Port Status	0	0	0	0	0	0	0	0	0	0	0	0	SLIMRX4_PORT_STS	SLIMRX3_PORT_STS	SLIMRX2_PORT_STS	SLIMRX1_PORT_STS	0000h
R1528 (5F8h)	SLIMbus TX Port Status	0	0	0	0	0	0	0	0	0	0	SLIMTX6_PORT_STS	SLIMTX5_PORT_STS	SLIMTX4_PORT_STS	SLIMTX3_PORT_STS	SLIMTX2_PORT_STS	SLIMTX1_PORT_STS	0000h
R1600 (640h)	PWM1MIX Input 1 Source	PWM1MIX_STS1	0	0	0	0	0	0	0	PWM1MIX_SRC1 [7:0]								0000h
R1601 (641h)	PWM1MIX Input 1 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL1 [6:0]							0	0080h
R1602 (642h)	PWM1MIX Input 2 Source	PWM1MIX_STS2	0	0	0	0	0	0	0	PWM1MIX_SRC2 [7:0]								0000h
R1603 (643h)	PWM1MIX Input 2 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL2 [6:0]							0	0080h
R1604 (644h)	PWM1MIX Input 3 Source	PWM1MIX_STS3	0	0	0	0	0	0	0	PWM1MIX_SRC3 [7:0]								0000h
R1605 (645h)	PWM1MIX Input 3 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL3 [6:0]							0	0080h
R1606 (646h)	PWM1MIX Input 4 Source	PWM1MIX_STS4	0	0	0	0	0	0	0	PWM1MIX_SRC4 [7:0]								0000h
R1607 (647h)	PWM1MIX Input 4 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL4 [6:0]							0	0080h
R1608 (648h)	PWM2MIX Input 1 Source	PWM2MIX_STS1	0	0	0	0	0	0	0	PWM2MIX_SRC1 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1609 (649h)	PWM2MIX Input 1 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL1 [6:0]							0	0080h
R1610 (64Ah)	PWM2MIX Input 2 Source	PWM2MIX_STS2	0	0	0	0	0	0	0	PWM2MIX_SRC2 [7:0]								0000h
R1611 (64Bh)	PWM2MIX Input 2 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL2 [6:0]							0	0080h
R1612 (64Ch)	PWM2MIX Input 3 Source	PWM2MIX_STS3	0	0	0	0	0	0	0	PWM2MIX_SRC3 [7:0]								0000h
R1613 (64Dh)	PWM2MIX Input 3 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL3 [6:0]							0	0080h
R1614 (64Eh)	PWM2MIX Input 4 Source	PWM2MIX_STS4	0	0	0	0	0	0	0	PWM2MIX_SRC4 [7:0]								0000h
R1615 (64Fh)	PWM2MIX Input 4 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL4 [6:0]							0	0080h
R1664 (680h)	OUT1LMIX Input 1 Source	OUT1LMIX_STS1	0	0	0	0	0	0	0	OUT1LMIX_SRC1 [7:0]								0000h
R1665 (681h)	OUT1LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL1 [6:0]							0	0080h
R1666 (682h)	OUT1LMIX Input 2 Source	OUT1LMIX_STS2	0	0	0	0	0	0	0	OUT1LMIX_SRC2 [7:0]								0000h
R1667 (683h)	OUT1LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL2 [6:0]							0	0080h
R1668 (684h)	OUT1LMIX Input 3 Source	OUT1LMIX_STS3	0	0	0	0	0	0	0	OUT1LMIX_SRC3 [7:0]								0000h
R1669 (685h)	OUT1LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL3 [6:0]							0	0080h
R1670 (686h)	OUT1LMIX Input 4 Source	OUT1LMIX_STS4	0	0	0	0	0	0	0	OUT1LMIX_SRC4 [7:0]								0000h
R1671 (687h)	OUT1LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL4 [6:0]							0	0080h
R1672 (688h)	OUT1RMIX Input 1 Source	OUT1RMIX_STS1	0	0	0	0	0	0	0	OUT1RMIX_SRC1 [7:0]								0000h
R1673 (689h)	OUT1RMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL1 [6:0]							0	0080h
R1674 (68Ah)	OUT1RMIX Input 2 Source	OUT1RMIX_STS2	0	0	0	0	0	0	0	OUT1RMIX_SRC2 [7:0]								0000h
R1675 (68Bh)	OUT1RMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL2 [6:0]							0	0080h
R1676 (68Ch)	OUT1RMIX Input 3 Source	OUT1RMIX_STS3	0	0	0	0	0	0	0	OUT1RMIX_SRC3 [7:0]								0000h
R1677 (68Dh)	OUT1RMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL3 [6:0]							0	0080h
R1678 (68Eh)	OUT1RMIX Input 4 Source	OUT1RMIX_STS4	0	0	0	0	0	0	0	OUT1RMIX_SRC4 [7:0]								0000h
R1679 (68Fh)	OUT1RMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL4 [6:0]							0	0080h
R1680	OUT2LMIX	OUT2L	0	0	0	0	0	0	0	OUT2LMIX_SRC1 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(690h)	Input 1 Source	MIX_STS1																
R1681 (691h)	OUT2LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT2LMIX_VOL1 [6:0]							0	0080h
R1682 (692h)	OUT2LMIX Input 2 Source	OUT2LMIX_STS2	0	0	0	0	0	0	0	OUT2LMIX_SRC2 [7:0]								0000h
R1683 (693h)	OUT2LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT2LMIX_VOL2 [6:0]							0	0080h
R1684 (694h)	OUT2LMIX Input 3 Source	OUT2LMIX_STS3	0	0	0	0	0	0	0	OUT2LMIX_SRC3 [7:0]								0000h
R1685 (695h)	OUT2LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT2LMIX_VOL3 [6:0]							0	0080h
R1686 (696h)	OUT2LMIX Input 4 Source	OUT2LMIX_STS4	0	0	0	0	0	0	0	OUT2LMIX_SRC4 [7:0]								0000h
R1687 (697h)	OUT2LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT2LMIX_VOL4 [6:0]							0	0080h
R1688 (698h)	OUT2RMIX Input 1 Source	OUT2RMIX_STS1	0	0	0	0	0	0	0	OUT2RMIX_SRC1 [7:0]								0000h
R1689 (699h)	OUT2RMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT2RMIX_VOL1 [6:0]							0	0080h
R1690 (69Ah)	OUT2RMIX Input 2 Source	OUT2RMIX_STS2	0	0	0	0	0	0	0	OUT2RMIX_SRC2 [7:0]								0000h
R1691 (69Bh)	OUT2RMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT2RMIX_VOL2 [6:0]							0	0080h
R1692 (69Ch)	OUT2RMIX Input 3 Source	OUT2RMIX_STS3	0	0	0	0	0	0	0	OUT2RMIX_SRC3 [7:0]								0000h
R1693 (69Dh)	OUT2RMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT2RMIX_VOL3 [6:0]							0	0080h
R1694 (69Eh)	OUT2RMIX Input 4 Source	OUT2RMIX_STS4	0	0	0	0	0	0	0	OUT2RMIX_SRC4 [7:0]								0000h
R1695 (69Fh)	OUT2RMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT2RMIX_VOL4 [6:0]							0	0080h
R1696 (6A0h)	OUT3LMIX Input 1 Source	OUT3MIX_STS1	0	0	0	0	0	0	0	OUT3MIX_SRC1 [7:0]								0000h
R1697 (6A1h)	OUT3LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT3MIX_VOL1 [6:0]							0	0080h
R1698 (6A2h)	OUT3LMIX Input 2 Source	OUT3MIX_STS2	0	0	0	0	0	0	0	OUT3MIX_SRC2 [7:0]								0000h
R1699 (6A3h)	OUT3LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT3MIX_VOL2 [6:0]							0	0080h
R1700 (6A4h)	OUT3LMIX Input 3 Source	OUT3MIX_STS3	0	0	0	0	0	0	0	OUT3MIX_SRC3 [7:0]								0000h
R1701 (6A5h)	OUT3LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT3MIX_VOL3 [6:0]							0	0080h
R1702 (6A6h)	OUT3LMIX Input 4 Source	OUT3MIX_STS4	0	0	0	0	0	0	0	OUT3MIX_SRC4 [7:0]								0000h
R1703	OUT3LMIX	0	0	0	0	0	0	0	0	OUT3MIX_VOL4 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(6A7h)	Input 4 Volume																	
R1712 (6B0h)	OUT4LMIX Input 1 Source	OUT4LMIX_STS1	0	0	0	0	0	0	0	OUT4LMIX_SRC1 [7:0]								0000h
R1713 (6B1h)	OUT4LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL1 [6:0]							0	0080h
R1714 (6B2h)	OUT4LMIX Input 2 Source	OUT4LMIX_STS2	0	0	0	0	0	0	0	OUT4LMIX_SRC2 [7:0]								0000h
R1715 (6B3h)	OUT4LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL2 [6:0]							0	0080h
R1716 (6B4h)	OUT4LMIX Input 3 Source	OUT4LMIX_STS3	0	0	0	0	0	0	0	OUT4LMIX_SRC3 [7:0]								0000h
R1717 (6B5h)	OUT4LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL3 [6:0]							0	0080h
R1718 (6B6h)	OUT4LMIX Input 4 Source	OUT4LMIX_STS4	0	0	0	0	0	0	0	OUT4LMIX_SRC4 [7:0]								0000h
R1719 (6B7h)	OUT4LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL4 [6:0]							0	0080h
R1720 (6B8h)	OUT4RMIX Input 1 Source	OUT4RMIX_STS1	0	0	0	0	0	0	0	OUT4RMIX_SRC1 [7:0]								0000h
R1721 (6B9h)	OUT4RMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT4RMIX_VOL1 [6:0]							0	0080h
R1722 (6BAh)	OUT4RMIX Input 2 Source	OUT4RMIX_STS2	0	0	0	0	0	0	0	OUT4RMIX_SRC2 [7:0]								0000h
R1723 (6BBh)	OUT4RMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT4RMIX_VOL2 [6:0]							0	0080h
R1724 (6BCh)	OUT4RMIX Input 3 Source	OUT4RMIX_STS3	0	0	0	0	0	0	0	OUT4RMIX_SRC3 [7:0]								0000h
R1725 (6BDh)	OUT4RMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT4RMIX_VOL3 [6:0]							0	0080h
R1726 (6BEh)	OUT4RMIX Input 4 Source	OUT4RMIX_STS4	0	0	0	0	0	0	0	OUT4RMIX_SRC4 [7:0]								0000h
R1727 (6BFh)	OUT4RMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT4RMIX_VOL4 [6:0]							0	0080h
R1728 (6C0h)	OUT5LMIX Input 1 Source	OUT5LMIX_STS1	0	0	0	0	0	0	0	OUT5LMIX_SRC1 [7:0]								0000h
R1729 (6C1h)	OUT5LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT5LMIX_VOL1 [6:0]							0	0080h
R1730 (6C2h)	OUT5LMIX Input 2 Source	OUT5LMIX_STS2	0	0	0	0	0	0	0	OUT5LMIX_SRC2 [7:0]								0000h
R1731 (6C3h)	OUT5LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT5LMIX_VOL2 [6:0]							0	0080h
R1732 (6C4h)	OUT5LMIX Input 3 Source	OUT5LMIX_STS3	0	0	0	0	0	0	0	OUT5LMIX_SRC3 [7:0]								0000h
R1733 (6C5h)	OUT5LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT5LMIX_VOL3 [6:0]							0	0080h
R1734 (6C6h)	OUT5LMIX Input 4 Source	OUT5LMIX_S	0	0	0	0	0	0	0	OUT5LMIX_SRC4 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		TS4																
R1735 (6C7h)	OUT5LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT5LMIX_VOL4 [6:0]							0	0080h
R1736 (6C8h)	OUT5RMIX Input 1 Source	OUT5RMIX_STS1	0	0	0	0	0	0	0	OUT5RMIX_SRC1 [7:0]								0000h
R1737 (6C9h)	OUT5RMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT5RMIX_VOL1 [6:0]							0	0080h
R1738 (6CAh)	OUT5RMIX Input 2 Source	OUT5RMIX_STS2	0	0	0	0	0	0	0	OUT5RMIX_SRC2 [7:0]								0000h
R1739 (6CBh)	OUT5RMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT5RMIX_VOL2 [6:0]							0	0080h
R1740 (6CCh)	OUT5RMIX Input 3 Source	OUT5RMIX_STS3	0	0	0	0	0	0	0	OUT5RMIX_SRC3 [7:0]								0000h
R1741 (6CDh)	OUT5RMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT5RMIX_VOL3 [6:0]							0	0080h
R1742 (6CEh)	OUT5RMIX Input 4 Source	OUT5RMIX_STS4	0	0	0	0	0	0	0	OUT5RMIX_SRC4 [7:0]								0000h
R1743 (6CFh)	OUT5RMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT5RMIX_VOL4 [6:0]							0	0080h
R1792 (700h)	AIF1TX1MIX Input 1 Source	AIF1TX1MIX_STS1	0	0	0	0	0	0	0	AIF1TX1MIX_SRC1 [7:0]								0000h
R1793 (701h)	AIF1TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL1 [6:0]							0	0080h
R1794 (702h)	AIF1TX1MIX Input 2 Source	AIF1TX1MIX_STS2	0	0	0	0	0	0	0	AIF1TX1MIX_SRC2 [7:0]								0000h
R1795 (703h)	AIF1TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL2 [6:0]							0	0080h
R1796 (704h)	AIF1TX1MIX Input 3 Source	AIF1TX1MIX_STS3	0	0	0	0	0	0	0	AIF1TX1MIX_SRC3 [7:0]								0000h
R1797 (705h)	AIF1TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL3 [6:0]							0	0080h
R1798 (706h)	AIF1TX1MIX Input 4 Source	AIF1TX1MIX_STS4	0	0	0	0	0	0	0	AIF1TX1MIX_SRC4 [7:0]								0000h
R1799 (707h)	AIF1TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL4 [6:0]							0	0080h
R1800 (708h)	AIF1TX2MIX Input 1 Source	AIF1TX2MIX_STS1	0	0	0	0	0	0	0	AIF1TX2MIX_SRC1 [7:0]								0000h
R1801 (709h)	AIF1TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL1 [6:0]							0	0080h
R1802 (70Ah)	AIF1TX2MIX Input 2 Source	AIF1TX2MIX_STS2	0	0	0	0	0	0	0	AIF1TX2MIX_SRC2 [7:0]								0000h
R1803 (70Bh)	AIF1TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL2 [6:0]							0	0080h
R1804 (70Ch)	AIF1TX2MIX Input 3 Source	AIF1TX2MIX_STS3	0	0	0	0	0	0	0	AIF1TX2MIX_SRC3 [7:0]								0000h
R1805 (70Dh)	AIF1TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL3 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1806 (70Eh)	AIF1TX2MIX Input 4 Source	AIF1TX2MIX_STS4	0	0	0	0	0	0	0	AIF1TX2MIX_SRC4 [7:0]								0000h
R1807 (70Fh)	AIF1TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL4 [6:0]							0	0080h
R1808 (710h)	AIF1TX3MIX Input 1 Source	AIF1TX3MIX_STS1	0	0	0	0	0	0	0	AIF1TX3MIX_SRC1 [7:0]								0000h
R1809 (711h)	AIF1TX3MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL1 [6:0]							0	0080h
R1810 (712h)	AIF1TX3MIX Input 2 Source	AIF1TX3MIX_STS2	0	0	0	0	0	0	0	AIF1TX3MIX_SRC2 [7:0]								0000h
R1811 (713h)	AIF1TX3MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL2 [6:0]							0	0080h
R1812 (714h)	AIF1TX3MIX Input 3 Source	AIF1TX3MIX_STS3	0	0	0	0	0	0	0	AIF1TX3MIX_SRC3 [7:0]								0000h
R1813 (715h)	AIF1TX3MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL3 [6:0]							0	0080h
R1814 (716h)	AIF1TX3MIX Input 4 Source	AIF1TX3MIX_STS4	0	0	0	0	0	0	0	AIF1TX3MIX_SRC4 [7:0]								0000h
R1815 (717h)	AIF1TX3MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL4 [6:0]							0	0080h
R1816 (718h)	AIF1TX4MIX Input 1 Source	AIF1TX4MIX_STS1	0	0	0	0	0	0	0	AIF1TX4MIX_SRC1 [7:0]								0000h
R1817 (719h)	AIF1TX4MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL1 [6:0]							0	0080h
R1818 (71Ah)	AIF1TX4MIX Input 2 Source	AIF1TX4MIX_STS2	0	0	0	0	0	0	0	AIF1TX4MIX_SRC2 [7:0]								0000h
R1819 (71Bh)	AIF1TX4MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL2 [6:0]							0	0080h
R1820 (71Ch)	AIF1TX4MIX Input 3 Source	AIF1TX4MIX_STS3	0	0	0	0	0	0	0	AIF1TX4MIX_SRC3 [7:0]								0000h
R1821 (71Dh)	AIF1TX4MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL3 [6:0]							0	0080h
R1822 (71Eh)	AIF1TX4MIX Input 4 Source	AIF1TX4MIX_STS4	0	0	0	0	0	0	0	AIF1TX4MIX_SRC4 [7:0]								0000h
R1823 (71Fh)	AIF1TX4MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL4 [6:0]							0	0080h
R1824 (720h)	AIF1TX5MIX Input 1 Source	AIF1TX5MIX_STS1	0	0	0	0	0	0	0	AIF1TX5MIX_SRC1 [7:0]								0000h
R1825 (721h)	AIF1TX5MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL1 [6:0]							0	0080h
R1826 (722h)	AIF1TX5MIX Input 2 Source	AIF1TX5MIX_STS2	0	0	0	0	0	0	0	AIF1TX5MIX_SRC2 [7:0]								0000h
R1827 (723h)	AIF1TX5MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL2 [6:0]							0	0080h
R1828 (724h)	AIF1TX5MIX Input 3 Source	AIF1TX5MIX_STS3	0	0	0	0	0	0	0	AIF1TX5MIX_SRC3 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1829 (725h)	AIF1TX5MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL3 [6:0]							0	0080h
R1830 (726h)	AIF1TX5MIX Input 4 Source	AIF1TX5MIX_STS4	0	0	0	0	0	0	0	AIF1TX5MIX_SRC4 [7:0]								0000h
R1831 (727h)	AIF1TX5MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL4 [6:0]							0	0080h
R1832 (728h)	AIF1TX6MIX Input 1 Source	AIF1TX6MIX_STS1	0	0	0	0	0	0	0	AIF1TX6MIX_SRC1 [7:0]								0000h
R1833 (729h)	AIF1TX6MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL1 [6:0]							0	0080h
R1834 (72Ah)	AIF1TX6MIX Input 2 Source	AIF1TX6MIX_STS2	0	0	0	0	0	0	0	AIF1TX6MIX_SRC2 [7:0]								0000h
R1835 (72Bh)	AIF1TX6MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL2 [6:0]							0	0080h
R1836 (72Ch)	AIF1TX6MIX Input 3 Source	AIF1TX6MIX_STS3	0	0	0	0	0	0	0	AIF1TX6MIX_SRC3 [7:0]								0000h
R1837 (72Dh)	AIF1TX6MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL3 [6:0]							0	0080h
R1838 (72Eh)	AIF1TX6MIX Input 4 Source	AIF1TX6MIX_STS4	0	0	0	0	0	0	0	AIF1TX6MIX_SRC4 [7:0]								0000h
R1839 (72Fh)	AIF1TX6MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL4 [6:0]							0	0080h
R1856 (740h)	AIF2TX1MIX Input 1 Source	AIF2TX1MIX_STS1	0	0	0	0	0	0	0	AIF2TX1MIX_SRC1 [7:0]								0000h
R1857 (741h)	AIF2TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL1 [6:0]							0	0080h
R1858 (742h)	AIF2TX1MIX Input 2 Source	AIF2TX1MIX_STS2	0	0	0	0	0	0	0	AIF2TX1MIX_SRC2 [7:0]								0000h
R1859 (743h)	AIF2TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL2 [6:0]							0	0080h
R1860 (744h)	AIF2TX1MIX Input 3 Source	AIF2TX1MIX_STS3	0	0	0	0	0	0	0	AIF2TX1MIX_SRC3 [7:0]								0000h
R1861 (745h)	AIF2TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL3 [6:0]							0	0080h
R1862 (746h)	AIF2TX1MIX Input 4 Source	AIF2TX1MIX_STS4	0	0	0	0	0	0	0	AIF2TX1MIX_SRC4 [7:0]								0000h
R1863 (747h)	AIF2TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL4 [6:0]							0	0080h
R1864 (748h)	AIF2TX2MIX Input 1 Source	AIF2TX2MIX_STS1	0	0	0	0	0	0	0	AIF2TX2MIX_SRC1 [7:0]								0000h
R1865 (749h)	AIF2TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL1 [6:0]							0	0080h
R1866 (74Ah)	AIF2TX2MIX Input 2 Source	AIF2TX2MIX_STS2	0	0	0	0	0	0	0	AIF2TX2MIX_SRC2 [7:0]								0000h
R1867 (74Bh)	AIF2TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL2 [6:0]							0	0080h
R1868	AIF2TX2MIX	AIF2TX	0	0	0	0	0	0	0	AIF2TX2MIX_SRC3 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(74Ch)	Input 3 Source	2MIX_STS3																
R1869 (74Dh)	AIF2TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL3 [6:0]							0	0080h
R1870 (74Eh)	AIF2TX2MIX Input 4 Source	AIF2TX2MIX_STS4	0	0	0	0	0	0	0	AIF2TX2MIX_SRC4 [7:0]								0000h
R1871 (74Fh)	AIF2TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL4 [6:0]							0	0080h
R1872 (750h)	AIF2TX3MIX Input 1 Source	AIF2TX3MIX_STS1	0	0	0	0	0	0	0	AIF2TX3MIX_SRC1 [7:0]								0000h
R1873 (751h)	AIF2TX3MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL1 [6:0]							0	0080h
R1874 (752h)	AIF2TX3MIX Input 2 Source	AIF2TX3MIX_STS2	0	0	0	0	0	0	0	AIF2TX3MIX_SRC2 [7:0]								0000h
R1875 (753h)	AIF2TX3MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL2 [6:0]							0	0080h
R1876 (754h)	AIF2TX3MIX Input 3 Source	AIF2TX3MIX_STS3	0	0	0	0	0	0	0	AIF2TX3MIX_SRC3 [7:0]								0000h
R1877 (755h)	AIF2TX3MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL3 [6:0]							0	0080h
R1878 (756h)	AIF2TX3MIX Input 4 Source	AIF2TX3MIX_STS4	0	0	0	0	0	0	0	AIF2TX3MIX_SRC4 [7:0]								0000h
R1879 (757h)	AIF2TX3MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL4 [6:0]							0	0080h
R1880 (758h)	AIF2TX4MIX Input 1 Source	AIF2TX4MIX_STS1	0	0	0	0	0	0	0	AIF2TX4MIX_SRC1 [7:0]								0000h
R1881 (759h)	AIF2TX4MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL1 [6:0]							0	0080h
R1882 (75Ah)	AIF2TX4MIX Input 2 Source	AIF2TX4MIX_STS2	0	0	0	0	0	0	0	AIF2TX4MIX_SRC2 [7:0]								0000h
R1883 (75Bh)	AIF2TX4MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL2 [6:0]							0	0080h
R1884 (75Ch)	AIF2TX4MIX Input 3 Source	AIF2TX4MIX_STS3	0	0	0	0	0	0	0	AIF2TX4MIX_SRC3 [7:0]								0000h
R1885 (75Dh)	AIF2TX4MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL3 [6:0]							0	0080h
R1886 (75Eh)	AIF2TX4MIX Input 4 Source	AIF2TX4MIX_STS4	0	0	0	0	0	0	0	AIF2TX4MIX_SRC4 [7:0]								0000h
R1887 (75Fh)	AIF2TX4MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL4 [6:0]							0	0080h
R1888 (760h)	AIF2TX5MIX Input 1 Source	AIF2TX5MIX_STS1	0	0	0	0	0	0	0	AIF2TX5MIX_SRC1 [7:0]								0000h
R1889 (761h)	AIF2TX5MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL1 [6:0]							0	0080h
R1890 (762h)	AIF2TX5MIX Input 2 Source	AIF2TX5MIX_STS2	0	0	0	0	0	0	0	AIF2TX5MIX_SRC2 [7:0]								0000h
R1891	AIF2TX5MIX	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL2 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(763h)	Input 2 Volume																	
R1892 (764h)	AIF2TX5MIX Input 3 Source	AIF2TX5MIX_STS3	0	0	0	0	0	0	0	AIF2TX5MIX_SRC3 [7:0]								0000h
R1893 (765h)	AIF2TX5MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL3 [6:0]							0	0080h
R1894 (766h)	AIF2TX5MIX Input 4 Source	AIF2TX5MIX_STS4	0	0	0	0	0	0	0	AIF2TX5MIX_SRC4 [7:0]								0000h
R1895 (767h)	AIF2TX5MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL4 [6:0]							0	0080h
R1896 (768h)	AIF2TX6MIX Input 1 Source	AIF2TX6MIX_STS1	0	0	0	0	0	0	0	AIF2TX6MIX_SRC1 [7:0]								0000h
R1897 (769h)	AIF2TX6MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL1 [6:0]							0	0080h
R1898 (76Ah)	AIF2TX6MIX Input 2 Source	AIF2TX6MIX_STS2	0	0	0	0	0	0	0	AIF2TX6MIX_SRC2 [7:0]								0000h
R1899 (76Bh)	AIF2TX6MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL2 [6:0]							0	0080h
R1900 (76Ch)	AIF2TX6MIX Input 3 Source	AIF2TX6MIX_STS3	0	0	0	0	0	0	0	AIF2TX6MIX_SRC3 [7:0]								0000h
R1901 (76Dh)	AIF2TX6MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL3 [6:0]							0	0080h
R1902 (76Eh)	AIF2TX6MIX Input 4 Source	AIF2TX6MIX_STS4	0	0	0	0	0	0	0	AIF2TX6MIX_SRC4 [7:0]								0000h
R1903 (76Fh)	AIF2TX6MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL4 [6:0]							0	0080h
R1920 (780h)	AIF3TX1MIX Input 1 Source	AIF3TX1MIX_STS1	0	0	0	0	0	0	0	AIF3TX1MIX_SRC1 [7:0]								0000h
R1921 (781h)	AIF3TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL1 [6:0]							0	0080h
R1922 (782h)	AIF3TX1MIX Input 2 Source	AIF3TX1MIX_STS2	0	0	0	0	0	0	0	AIF3TX1MIX_SRC2 [7:0]								0000h
R1923 (783h)	AIF3TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL2 [6:0]							0	0080h
R1924 (784h)	AIF3TX1MIX Input 3 Source	AIF3TX1MIX_STS3	0	0	0	0	0	0	0	AIF3TX1MIX_SRC3 [7:0]								0000h
R1925 (785h)	AIF3TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL3 [6:0]							0	0080h
R1926 (786h)	AIF3TX1MIX Input 4 Source	AIF3TX1MIX_STS4	0	0	0	0	0	0	0	AIF3TX1MIX_SRC4 [7:0]								0000h
R1927 (787h)	AIF3TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL4 [6:0]							0	0080h
R1928 (788h)	AIF3TX2MIX Input 1 Source	AIF3TX2MIX_STS1	0	0	0	0	0	0	0	AIF3TX2MIX_SRC1 [7:0]								0000h
R1929 (789h)	AIF3TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL1 [6:0]							0	0080h
R1930 (78Ah)	AIF3TX2MIX Input 2 Source	AIF3TX2MIX_	0	0	0	0	0	0	0	AIF3TX2MIX_SRC2 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		STS2																
R1931 (78Bh)	AIF3TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL2 [6:0]							0	0080h
R1932 (78Ch)	AIF3TX2MIX Input 3 Source	AIF3TX2MIX_STS3	0	0	0	0	0	0	0	AIF3TX2MIX_SRC3 [7:0]								0000h
R1933 (78Dh)	AIF3TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL3 [6:0]							0	0080h
R1934 (78Eh)	AIF3TX2MIX Input 4 Source	AIF3TX2MIX_STS4	0	0	0	0	0	0	0	AIF3TX2MIX_SRC4 [7:0]								0000h
R1935 (78Fh)	AIF3TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL4 [6:0]							0	0080h
R1984 (7C0h)	SLIMTX1MIX Input 1 Source	SLIMTX1MIX_STS	0	0	0	0	0	0	0	SLIMTX1MIX_SRC [7:0]								0000h
R1985 (7C1h)	SLIMTX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX1MIX_VOL [6:0]							0	0080h
R1992 (7C8h)	SLIMTX2MIX Input 1 Source	SLIMTX2MIX_STS	0	0	0	0	0	0	0	SLIMTX2MIX_SRC [7:0]								0000h
R1993 (7C9h)	SLIMTX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX2MIX_VOL [6:0]							0	0080h
R2000 (7D0h)	SLIMTX3MIX Input 1 Source	SLIMTX3MIX_STS	0	0	0	0	0	0	0	SLIMTX3MIX_SRC [7:0]								0000h
R2001 (7D1h)	SLIMTX3MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX3MIX_VOL [6:0]							0	0080h
R2008 (7D8h)	SLIMTX4MIX Input 1 Source	SLIMTX4MIX_STS	0	0	0	0	0	0	0	SLIMTX4MIX_SRC [7:0]								0000h
R2009 (7D9h)	SLIMTX4MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX4MIX_VOL [6:0]							0	0080h
R2016 (7E0h)	SLIMTX5MIX Input 1 Source	SLIMTX5MIX_STS	0	0	0	0	0	0	0	SLIMTX5MIX_SRC [7:0]								0000h
R2017 (7E1h)	SLIMTX5MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX5MIX_VOL [6:0]							0	0080h
R2024 (7E8h)	SLIMTX6MIX Input 1 Source	SLIMTX6MIX_STS	0	0	0	0	0	0	0	SLIMTX6MIX_SRC [7:0]								0000h
R2025 (7E9h)	SLIMTX6MIX Input 1 Volume	0	0	0	0	0	0	0	0	SLIMTX6MIX_VOL [6:0]							0	0080h
R2048 (800h)	SPDIF1TX1MIX Input 1 Source	SPDIF1TX1_STS	0	0	0	0	0	0	0	SPDIF1TX1MIX_SRC [7:0]								0000h
R2049 (801h)	SPDIF1TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	SPDIF1TX1MIX_VOL [6:0]							0	0080h
R2056 (808h)	SPDIF1TX2MIX Input 1 Source	SPDIF1TX2_STS	0	0	0	0	0	0	0	SPDIF1TX2MIX_SRC [7:0]								0000h
R2057 (809h)	SPDIF1TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	SPDIF1TX2MIX_VOL [6:0]							0	0080h
R2176 (880h)	EQ1MIX Input 1 Source	EQ1MIX_STS	0	0	0	0	0	0	0	EQ1MIX_SRC [7:0]								0000h
R2177 (881h)	EQ1MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ1MIX_VOL [6:0]							0	0080h
R2184	EQ2MIX Input 1	EQ2MI	0	0	0	0	0	0	0	EQ2MIX_SRC [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(888h)	Source	X_STS																
R2185 (889h)	EQ2MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ2MIX_VOL [6:0]							0	0080h
R2192 (890h)	EQ3MIX Input 1 Source	EQ3MIX_STS	0	0	0	0	0	0	0	EQ3MIX_SRC [7:0]								0000h
R2193 (891h)	EQ3MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ3MIX_VOL [6:0]							0	0080h
R2200 (898h)	EQ4MIX Input 1 Source	EQ4MIX_STS	0	0	0	0	0	0	0	EQ4MIX_SRC [7:0]								0000h
R2201 (899h)	EQ4MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ4MIX_VOL [6:0]							0	0080h
R2240 (8C0h)	DRC1LMIX Input 1 Source	DRC1LMIX_STS	0	0	0	0	0	0	0	DRC1LMIX_SRC [7:0]								0000h
R2241 (8C1h)	DRC1LMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC1LMIX_VOL [6:0]							0	0080h
R2248 (8C8h)	DRC1RMIX Input 1 Source	DRC1RMIX_STS	0	0	0	0	0	0	0	DRC1RMIX_SRC [7:0]								0000h
R2249 (8C9h)	DRC1RMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC1RMIX_VOL [6:0]							0	0080h
R2304 (900h)	HPLP1MIX Input 1 Source	LHPF1MIX_STS1	0	0	0	0	0	0	0	LHPF1MIX_SRC1 [7:0]								0000h
R2305 (901h)	HPLP1MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL1 [6:0]							0	0080h
R2306 (902h)	HPLP1MIX Input 2 Source	LHPF1MIX_STS2	0	0	0	0	0	0	0	LHPF1MIX_SRC2 [7:0]								0000h
R2307 (903h)	HPLP1MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL2 [6:0]							0	0080h
R2308 (904h)	HPLP1MIX Input 3 Source	LHPF1MIX_STS3	0	0	0	0	0	0	0	LHPF1MIX_SRC3 [7:0]								0000h
R2309 (905h)	HPLP1MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL3 [6:0]							0	0080h
R2310 (906h)	HPLP1MIX Input 4 Source	LHPF1MIX_STS4	0	0	0	0	0	0	0	LHPF1MIX_SRC4 [7:0]								0000h
R2311 (907h)	HPLP1MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL4 [6:0]							0	0080h
R2312 (908h)	HPLP2MIX Input 1 Source	LHPF2MIX_STS1	0	0	0	0	0	0	0	LHPF2MIX_SRC1 [7:0]								0000h
R2313 (909h)	HPLP2MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL1 [6:0]							0	0080h
R2314 (90Ah)	HPLP2MIX Input 2 Source	LHPF2MIX_STS2	0	0	0	0	0	0	0	LHPF2MIX_SRC2 [7:0]								0000h
R2315 (90Bh)	HPLP2MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL2 [6:0]							0	0080h
R2316 (90Ch)	HPLP2MIX Input 3 Source	LHPF2MIX_STS3	0	0	0	0	0	0	0	LHPF2MIX_SRC3 [7:0]								0000h
R2317 (90Dh)	HPLP2MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL3 [6:0]							0	0080h
R2318 (90Eh)	HPLP2MIX Input 4 Source	LHPF2MIX_S	0	0	0	0	0	0	0	LHPF2MIX_SRC4 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		TS4																
R2319 (90Fh)	HPLP2MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL4 [6:0]							0	0080h
R2320 (910h)	HPLP3MIX Input 1 Source	LHPF3MIX_STS1	0	0	0	0	0	0	0	LHPF3MIX_SRC1 [7:0]								0000h
R2321 (911h)	HPLP3MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL1 [6:0]							0	0080h
R2322 (912h)	HPLP3MIX Input 2 Source	LHPF3MIX_STS2	0	0	0	0	0	0	0	LHPF3MIX_SRC2 [7:0]								0000h
R2323 (913h)	HPLP3MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL2 [6:0]							0	0080h
R2324 (914h)	HPLP3MIX Input 3 Source	LHPF3MIX_STS3	0	0	0	0	0	0	0	LHPF3MIX_SRC3 [7:0]								0000h
R2325 (915h)	HPLP3MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL3 [6:0]							0	0080h
R2326 (916h)	HPLP3MIX Input 4 Source	LHPF3MIX_STS4	0	0	0	0	0	0	0	LHPF3MIX_SRC4 [7:0]								0000h
R2327 (917h)	HPLP3MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL4 [6:0]							0	0080h
R2328 (918h)	HPLP4MIX Input 1 Source	LHPF4MIX_STS1	0	0	0	0	0	0	0	LHPF4MIX_SRC1 [7:0]								0000h
R2329 (919h)	HPLP4MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL1 [6:0]							0	0080h
R2330 (91Ah)	HPLP4MIX Input 2 Source	LHPF4MIX_STS2	0	0	0	0	0	0	0	LHPF4MIX_SRC2 [7:0]								0000h
R2331 (91Bh)	HPLP4MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL2 [6:0]							0	0080h
R2332 (91Ch)	HPLP4MIX Input 3 Source	LHPF4MIX_STS3	0	0	0	0	0	0	0	LHPF4MIX_SRC3 [7:0]								0000h
R2333 (91Dh)	HPLP4MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL3 [6:0]							0	0080h
R2334 (91Eh)	HPLP4MIX Input 4 Source	LHPF4MIX_STS4	0	0	0	0	0	0	0	LHPF4MIX_SRC4 [7:0]								0000h
R2335 (91Fh)	HPLP4MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL4 [6:0]							0	0080h
R2688 (A80h)	ASRC1LMIX Input 1 Source	ASRC1LMIX_STS	0	0	0	0	0	0	0	ASRC1L_SRC [7:0]								0000h
R2696 (A88h)	ASRC1RMIX Input 1 Source	ASRC1RMIX_STS	0	0	0	0	0	0	0	ASRC1R_SRC [7:0]								0000h
R2704 (A90h)	ASRC2LMIX Input 1 Source	ASRC2LMIX_STS	0	0	0	0	0	0	0	ASRC2L_SRC [7:0]								0000h
R2712 (A98h)	ASRC2RMIX Input 1 Source	ASRC2RMIX_STS	0	0	0	0	0	0	0	ASRC2R_SRC [7:0]								0000h
R2816 (B00h)	ISRC1DEC1MIX Input 1 Source	ISRC1DEC1MIX_S	0	0	0	0	0	0	0	ISRC1DEC1_SRC [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		TS																
R2824 (B08h)	ISRC1DEC2MIX Input 1 Source	ISRC1DEC2MIX_STS	0	0	0	0	0	0	0	ISRC1DEC2_SRC [7:0]								0000h
R2832 (B10h)	ISRC1DEC3MIX Input 1 Source	ISRC1DEC3MIX_STS	0	0	0	0	0	0	0	ISRC1DEC3_SRC [7:0]								0000h
R2840 (B18h)	ISRC1DEC4MIX Input 1 Source	ISRC1DEC4MIX_STS	0	0	0	0	0	0	0	ISRC1DEC4_SRC [7:0]								0000h
R2848 (B20h)	ISRC1INT1MIX Input 1 Source	ISRC1INT1MIX_STS	0	0	0	0	0	0	0	ISRC1INT1_SRC [7:0]								0000h
R2856 (B28h)	ISRC1INT2MIX Input 1 Source	ISRC1INT2MIX_STS	0	0	0	0	0	0	0	ISRC1INT2_SRC [7:0]								0000h
R2864 (B30h)	ISRC1INT3MIX Input 1 Source	ISRC1INT3MIX_STS	0	0	0	0	0	0	0	ISRC1INT3_SRC [7:0]								0000h
R2872 (B38h)	ISRC1INT4MIX Input 1 Source	ISRC1INT4MIX_STS	0	0	0	0	0	0	0	ISRC1INT4_SRC [7:0]								0000h
R2880 (B40h)	ISRC2DEC1MIX Input 1 Source	ISRC2DEC1MIX_STS	0	0	0	0	0	0	0	ISRC2DEC1_SRC [7:0]								0000h
R2888 (B48h)	ISRC2DEC2MIX Input 1 Source	ISRC2DEC2MIX_STS	0	0	0	0	0	0	0	ISRC2DEC2_SRC [7:0]								0000h
R2912 (B60h)	ISRC2INT1MIX Input 1 Source	ISRC2INT1MIX_STS	0	0	0	0	0	0	0	ISRC2INT1_SRC [7:0]								0000h
R2920 (B68h)	ISRC2INT2MIX Input 1 Source	ISRC2INT2MIX_STS	0	0	0	0	0	0	0	ISRC2INT2_SRC [7:0]								0000h
R3072 (C00h)	GPIO1 CTRL	GP1_DIR	GP1_PU	GP1_PD	0	GP1_LVL	GP1_POL	GP1_OP_CFG	GP1_DB	0	GP1_FN [6:0]							A101h
R3073 (C01h)	GPIO2 CTRL	GP2_DIR	GP2_PU	GP2_PD	0	GP2_LVL	GP2_POL	GP2_OP_CFG	GP2_DB	0	GP2_FN [6:0]							A101h
R3074 (C02h)	GPIO3 CTRL	GP3_DIR	GP3_PU	GP3_PD	0	GP3_LVL	GP3_POL	GP3_OP_CFG	GP3_DB	0	GP3_FN [6:0]							A101h
R3075 (C03h)	GPIO4 CTRL	GP4_DIR	GP4_PU	GP4_PD	0	GP4_LVL	GP4_POL	GP4_OP_CFG	GP4_DB	0	GP4_FN [6:0]							A101h
R3076 (C04h)	GPIO5 CTRL	GP5_DIR	GP5_PU	GP5_PD	0	GP5_LVL	GP5_POL	GP5_OP_CFG	GP5_DB	0	GP5_FN [6:0]							A101h
R3087 (C0Fh)	IRQ CTRL 1	0	0	0	0	0	IRQ_POL	IRQ_OP_CFG	0	0	0	0	0	0	0	0	0	0400h
R3088 (C10h)	GPIO Debounce Config	GP_DBTIME [3:0]				0	0	0	0	0	0	0	0	0	0	0	0	1000h
R3096 (C18h)	GP Switch 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW1_MODE [1:0]		0000h
R3104 (C20h)	Misc Pad Ctrl 1	LDO1ENA_PD	LDO1ENA_PU	MCLK2_PD	0	0	0	0	0	0	0	0	0	0	0	RESET_PU	RESET_PD	8002h
R3105	Misc Pad Ctrl 2	0	0	0	MCLK1	0	0	0	0	0	0	0	0	0	0	0	ADDR_	0001h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(C21h)					_PD												PD	
R3106 (C22h)	Misc Pad Ctrl 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DMICDAT2_PD	DMICDAT1_PD	0000h
R3107 (C23h)	Misc Pad Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF1LRCLK_PU	AIF1LRCLK_PD	AIF1BCLK_PU	AIF1BCLK_PD	AIF1RXDAT_PU	AIF1RXDAT_PD	0000h
R3108 (C24h)	Misc Pad Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF2LRCLK_PU	AIF2LRCLK_PD	AIF2BCLK_PU	AIF2BCLK_PD	AIF2RXDAT_PU	AIF2RXDAT_PD	0000h
R3109 (C25h)	Misc Pad Ctrl 6	0	0	0	0	0	0	0	0	0	0	AIF3LRCLK_PU	AIF3LRCLK_PD	AIF3BCLK_PU	AIF3BCLK_PD	AIF3RXDAT_PU	AIF3RXDAT_PD	0000h
R3328 (D00h)	Interrupt Status 1	0	0	0	0	0	0	0	0	0	0	0	0	GP4_EINT1	GP3_EINT1	GP2_EINT1	GP1_EINT1	0000h
R3329 (D01h)	Interrupt Status 2	SPKR_DISABLE_DONE_EINT1	SPKL_DISABLE_DONE_EINT1	SPKR_ENABLE_DONE_EINT1	SPKL_ENABLE_DONE_EINT1	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3330 (D02h)	Interrupt Status 3	SPK_OVERHEAT_WARN_EINT1	SPK_OVERHEAT_EINT1	HPDET_EINT1	MICDET_EINT1	WSEQ_DONE_EINT1	0	DRC1_SIG_DET_EINT1	ASRC2_LOCK_EINT1	ASRC1_LOCK_EINT1	UNDERCLOCKED_EINT1	OVERCLOCKED_EINT1	0	FLL2_LOCK_EINT1	FLL1_LOCK_EINT1	CLKGEN_ERR_EINT1	CLKGEN_ERR_ASYNC_EINT1	0000h
R3331 (D03h)	Interrupt Status 4	AIF3_ERR_EINT1	AIF2_ERR_EINT1	AIF1_ERR_EINT1	CTRLIF_ERR_EINT1	MIXER_DROPPED_SAMPLE_EINT1	ASYNC_CLK_ENA_LOW_EINT1	SYSCLK_ENA_LOW_EINT1	ISRC1_CFG_ERR_EINT1	ISRC2_CFG_ERR_EINT1	0	0	0	LINER_ENABLE_DONE_EINT1	LINEL_ENABLE_DONE_EINT1	HPR_ENABLE_DONE_EINT1	HPL_ENABLE_DONE_EINT1	0000h
R3332 (D04h)	Interrupt Status 5	0	EP_ENABLE_DONE_EINT1	EP_DISABLE_DONE_EINT1	LINER_DISABLE_DONE_EINT1	LINEL_DISABLE_DONE_EINT1	HPR_DISABLE_DONE_EINT1	HPL_DISABLE_DONE_EINT1	BOOT_DONE_EINT1	0	0	0	0	ASRC_CFG_ERR_EINT1	0	FLL2_CLOCK_OK_EINT1	FLL1_CLOCK_OK_EINT1	0000h
R3333 (D05h)	Interrupt Status 6	0	SPK_SHUTDOWN_EINT1	SPKR_SHORT_EINT1	SPKL_SHORT_EINT1	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3336 (D08h)	Interrupt Status 1 Mask	0	0	0	0	0	0	0	0	0	0	0	0	IM_GP4_EINT1	IM_GP3_EINT1	IM_GP2_EINT1	IM_GP1_EINT1	000Fh
R3337 (D09h)	Interrupt Status 2 Mask	IM_SPKR_DISABLE_DONE_EINT1	IM_SPKL_DISABLE_DONE_EINT1	IM_SPKR_ENABLE_DONE_EINT1	IM_SPKL_ENABLE_DONE_EINT1	0	0	0	0	0	0	0	0	0	0	0	0	F000h
R3338 (D0Ah)	Interrupt Status 3 Mask	IM_SPK_OVERHEAT_WARN_EINT1	IM_SPK_OVERHEAT_EINT1	IM_HPDET_EINT1	IM_MICDET_EINT1	IM_WSEQ_DONE_EINT1	0	IM_DRC1_SIG_DET_EINT1	IM_ASRC2_LOCK_EINT1	IM_ASRC1_LOCK_EINT1	IM_UNDERCLOCKED_EINT1	IM_OVERCLOCKED_EINT1	0	IM_FLL2_LOCK_EINT1	IM_FLL1_LOCK_EINT1	IM_CLKGEN_ERR_EINT1	IM_CLKGEN_ERR_ASYNC_EINT1	FBEFh
R3339 (D0Bh)	Interrupt Status 4 Mask	IM_AIF3_ERR_EINT1	IM_AIF2_ERR_EINT1	IM_AIF1_ERR_EINT1	IM_CTRLIF_ERR_EINT1	IM_MIXER_DROPPED_SAMPLE_EINT1	IM_ASYNC_CLK_ENA_LOW_EINT1	IM_SYSCLK_ENA_LOW_EINT1	IM_ISRC1_CFG_ERR_EINT1	IM_ISRC2_CFG_ERR_EINT1	0	0	0	IM_LINER_ENABLE_DONE_EINT1	IM_LINEL_ENABLE_DONE_EINT1	IM_HPR_ENABLE_DONE_EINT1	IM_HPL_ENABLE_DONE_EINT1	FF8Fh

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3340 (D0Ch)	Interrupt Status 5 Mask	0	IM_EP_ENABLE_DONE_EINT1	IM_EP_ENABLE_DONE_EINT1	IM_LINER_DISABLE_DONE_EINT1	IM_LINEL_DISABLE_DONE_EINT1	IM_HPR_DISABLE_DONE_EINT1	IM_HPL_DISABLE_DONE_EINT1	IM_BOOT_DONE_EINT1	0	0	0	0	IM_ASRC_CFG_ERR_EINT1	0	IM_FLL2_CLOCK_OK_EINT1	IM_FLL1_CLOCK_OK_EINT1	7E0Bh
R3341 (D0Dh)	Interrupt Status 6 Mask	0	IM_SPK_SHUTDOWN_EINT1	IM_SPKR_SHORT_EINT1	IM_SPKL_SHORT_EINT1	0	0	0	0	0	0	0	0	0	0	0	0	7000h
R3343 (D0Fh)	Interrupt Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ1	0000h
R3344 (D10h)	IRQ2 Status 1	0	0	0	0	0	0	0	0	0	0	0	0	GP4_EINT2	GP3_EINT2	GP2_EINT2	GP1_EINT2	0000h
R3345 (D11h)	IRQ2 Status 2	SPKR_DISABLE_DONE_EINT2	SPKL_DISABLE_DONE_EINT2	SPKR_ENABLE_DONE_EINT2	SPKL_ENABLE_DONE_EINT2	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3346 (D12h)	IRQ2 Status 3	SPK_OVERHEAT_WARN_EINT2	SPK_OVERHEAT_EINT2	HPDET_EINT2	MICDET_EINT2	WSEQ_DONE_EINT2	0	DRC1_SIG_DET_EINT2	ASRC2_LOCK_EINT2	ASRC1_LOCK_EINT2	UNDERCLOCKED_EINT2	OVERCLOCKED_EINT2	0	FLL2_LOCK_EINT2	FLL1_LOCK_EINT2	CLKGEN_ERR_EINT2	CLKGEN_ERR_ASYNC_EINT2	0000h
R3347 (D13h)	IRQ2 Status 4	AIF3_ERR_EINT2	AIF2_ERR_EINT2	AIF1_ERR_EINT2	CTRLIF_ERR_EINT2	MIXER_DROPPED_SAMPLE_EINT2	ASYNC_CLK_ENA_LOW_EINT2	SYSCLK_ENA_LOW_EINT2	ISRC1_CFG_ERR_EINT2	ISRC2_CFG_ERR_EINT2	0	0	0	LINER_ENABLE_DONE_EINT2	LINEL_ENABLE_DONE_EINT2	HPR_ENABLE_DONE_EINT2	HPL_ENABLE_DONE_EINT2	0000h
R3348 (D14h)	IRQ2 Status 5	0	EP_ENABLE_DONE_EINT2	EP_DISABLE_DONE_EINT2	LINER_DISABLE_DONE_EINT2	LINEL_DISABLE_DONE_EINT2	HPR_DISABLE_DONE_EINT2	HPL_DISABLE_DONE_EINT2	BOOT_DONE_EINT2	0	0	0	0	ASRC_CFG_ERR_EINT2	0	FLL2_CLOCK_OK_EINT2	FLL1_CLOCK_OK_EINT2	0000h
R3349 (D15h)	IRQ2 Status 6	0	SPK_SHUTDOWN_EINT2	SPKR_SHORT_EINT2	SPKL_SHORT_EINT2	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3352 (D18h)	IRQ2 Status 1 Mask	0	0	0	0	0	0	0	0	0	0	0	0	IM_GP4_EINT2	IM_GP3_EINT2	IM_GP2_EINT2	IM_GP1_EINT2	000Fh
R3353 (D19h)	IRQ2 Status 2 Mask	IM_SPKR_DISABLE_DONE_EINT	IM_SPKL_DISABLE_DONE_EINT2	IM_SPKR_ENABLE_DONE_EINT2	IM_SPKL_ENABLE_DONE_EINT2	0	0	0	0	0	0	0	0	0	0	0	0	F000h
R3354 (D1Ah)	IRQ2 Status 3 Mask	IM_SPK_OVERHEAT_WARN_EINT2	IM_SPK_OVERHEAT_EINT2	IM_HPDET_EINT2	IM_MICDET_EINT2	IM_WSEQ_DONE_EINT2	0	IM_DRC1_SIG_DET_EINT2	IM_ASRC2_LOCK_EINT2	IM_ASRC1_LOCK_EINT2	IM_UNDERCLOCKED_EINT2	IM_OVERCLOCKED_EINT2	0	IM_FLL2_LOCK_EINT2	IM_FLL1_LOCK_EINT2	IM_CLKGEN_ERR_EINT2	IM_CLKGEN_ERR_ASYNC_EINT2	FBEFh
R3355 (D1Bh)	IRQ2 Status 4 Mask	IM_AIF3_ERR_EINT2	IM_AIF2_ERR_EINT2	IM_AIF1_ERR_EINT2	IM_CTRLIF_ERR_EINT2	IM_MIXER_DROPPED_SAMPLE_EINT2	IM_ASYNC_CLK_ENA_LOW_EINT2	IM_SYSCLK_ENA_LOW_EINT2	IM_ISRC1_CFG_ERR_EINT2	IM_ISRC2_CFG_ERR_EINT2	0	0	0	IM_LINER_ENABLE_DONE_EINT2	IM_LINEL_ENABLE_DONE_EINT2	IM_HPR_ENABLE_DONE_EINT2	IM_HPL_ENABLE_DONE_EINT2	FF8Fh
R3356	IRQ2 Status 5	0	IM_EP	IM_EP	IM_LIN	IM_LIN	IM_HP	IM_HP	IM_BO	0	0	0	0	IM_AS	0	IM_FLL	IM_FLL	7E0Bh

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(D1Ch)	Mask		_ENABLE_DONE_EINT2	_ENABLE_DONE_EINT2	ER_DISABLE_DONE_EINT2	EL_DISABLE_DONE_EINT2	R_DISABLE_DONE_EINT2	L_DISABLE_DONE_EINT2	OT_DONE_EINT2					RC_CFG_ERR_EINT2		2_CLOCK_OK_EINT2	1_CLOCK_OK_EINT2	
R3357 (D1Dh)	IRQ2 Status 6 Mask	0	IM_SPK_SHUTDOWN_EINT2	IM_SPKR_SHORT_EINT2	IM_SPKL_SHORT_EINT2	0	0	0	0	0	0	0	0	0	0	0	0	7000h
R3359 (D1Fh)	IRQ2 Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ2	0000h
R3360 (D20h)	Interrupt Raw Status 1	SPKR_DISABLE_DONE_STS	SPKL_DISABLE_DONE_STS	SPKR_ENABLE_DONE_STS	SPKL_ENABLE_DONE_STS	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3361 (D21h)	Interrupt Raw Status 2	SPK_OVERHEAT_WARN_STS	SPK_OVERHEAT_STS	0	0	WSEQ_DONE_STS	0	DRC1_SIG_DET_STS	ASRC2_LOCK_STS	ASRC1_LOCK_STS	UNDERCLOCKED_STS	OVERCLOCKED_STS	0	FLL2_LOCK_STS	FLL1_LOCK_STS	CLKGEN_ERR_STS	CLKGEN_ERR_ASYNC_STS	0000h
R3362 (D22h)	Interrupt Raw Status 3	AIF3_ERR_STS	AIF2_ERR_STS	AIF1_ERR_STS	CTRLIF_ERR_STS	MIXER_DROPPED_SAMPLE_STS	ASYNC_CLK_ENA_LOW_STS	SYSCLK_ENA_LOW_STS	ISRC1_CFG_ERR_STS	ISRC2_CFG_ERR_STS	0	0	0	LINER_ENABLE_DONE_STS	LINEL_ENABLE_DONE_STS	HPR_ENABLE_DONE_STS	HPL_ENABLE_DONE_STS	0000h
R3363 (D23h)	Interrupt Raw Status 4	0	EP_ENABLE_DONE_STS	EP_DISABLE_DONE_STS	LINER_DISABLE_DONE_STS	LINEL_DISABLE_DONE_STS	HPR_DISABLE_DONE_STS	HPL_DISABLE_DONE_STS	BOOT_DONE_STS	0	0	0	0	ASRC_CFG_ERR_STS	0	FLL2_CLOCK_OK_STS	FLL1_CLOCK_OK_STS	0000h
R3364 (D24h)	Interrupt Raw Status 5	0	PWM_OVERCLOCKED_STS	FX_CORE_OVERCLOCKED_STS	DAC_SYS_OVERCLOCKED_STS	DAC_WARP_OVERCLOCKED_STS	ADC_OVERCLOCKED_STS	MIXER_OVERCLOCKED_STS	0	AIF3_ASYNC_OVERCLOCKED_STS	AIF2_ASYNC_OVERCLOCKED_STS	AIF1_ASYNC_OVERCLOCKED_STS	0	AIF3_SYNC_OVERCLOCKED_STS	AIF2_SYNC_OVERCLOCKED_STS	AIF1_SYNC_OVERCLOCKED_STS	PAD_CTRL_OVERCLOCKED_STS	0000h
R3365 (D25h)	Interrupt Raw Status 6	SLIMBUS_SUBSYS_OVERCLOCKED_STS	SLIMBUS_ASYNC_OVERCLOCKED_STS	SLIMBUS_SYNC_OVERCLOCKED_STS	ASRC_ASYNC_SYS_OVERCLOCKED_STS	ASRC_ASYNC_WARP_OVERCLOCKED_STS	ASRC_SYNC_SYS_OVERCLOCKED_STS	ASRC_SYNC_WARP_OVERCLOCKED_STS	0	0	0	0	0	0	0	ISRC2_OVERCLOCKED_STS	ISRC1_OVERCLOCKED_STS	0000h
R3366 (D26h)	Interrupt Raw Status 7	SPDIF_SYNC_OVERCLOCKED_STS	0	0	0	0	AIF3_UNDERCLOCKED_STS	AIF2_UNDERCLOCKED_STS	AIF1_UNDERCLOCKED_STS	0	ISRC2_UNDERCLOCKED_STS	ISRC1_UNDERCLOCKED_STS	FX_UNDERCLOCKED_STS	ASRC_UNDERCLOCKED_STS	DAC_UNDERCLOCKED_STS	ADC_UNDERCLOCKED_STS	MIXER_UNDERCLOCKED_STS	0000h
R3368 (D28h)	Interrupt Raw Status 8	0	SPK_SHUTDOWN_STS	SPKR_SHORT_STS	SPKL_SHORT_STS	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3392 (D40h)	IRQ Pin Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ2_STS	IRQ1_STS	0000h
R3408 (D50h)	AOD wkup and trig	0	0	0	0	0	0	0	0	MICD_CLAMP_FALL_TRI	MICD_CLAMP_RISE_TRI	GP5_FALL_TRIG_STS	GP5_RISE_TRIG_STS	JD1_FALL_TRIG_STS	JD1_RISE_TRIG_STS	0	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
										G_STS	G_STS							
R3409 (D51h)	AOD IRQ1	0	0	0	0	0	0	0	0	MICD_CLAMP_FALL_EINT1	MICD_CLAMP_RISE_EINT1	GP5_FALL_EINT1	GP5_RISE_EINT1	JD1_FALL_EINT1	JD1_RISE_EINT1	0	0	0000h
R3410 (D52h)	AOD IRQ2	0	0	0	0	0	0	0	0	MICD_CLAMP_FALL_EINT2	MICD_CLAMP_RISE_EINT2	GP5_FALL_EINT2	GP5_RISE_EINT2	JD1_FALL_EINT2	JD1_RISE_EINT2	0	0	0000h
R3411 (D53h)	AOD IRQ Mask IRQ1	0	0	0	0	0	0	0	0	IM_MICD_CLAMP_FALL_EINT1	IM_MICD_CLAMP_RISE_EINT1	IM_GP5_FALL_EINT1	IM_GP5_RISE_EINT1	IM_JD1_FALL_EINT1	IM_JD1_RISE_EINT1	0	0	00FCh
R3412 (D54h)	AOD IRQ Mask IRQ2	0	0	0	0	0	0	0	0	IM_MICD_CLAMP_FALL_EINT2	IM_MICD_CLAMP_RISE_EINT2	IM_GP5_FALL_EINT2	IM_GP5_RISE_EINT2	IM_JD1_FALL_EINT2	IM_JD1_RISE_EINT2	0	0	00FCh
R3413 (D55h)	AOD IRQ Raw Status	0	0	0	0	0	0	0	0	0	0	0	0	MICD_CLAMP_STS	GP5_STS	0	JD1_STS	0000h
R3414 (D56h)	Jack detect debounce	0	0	0	0	0	0	0	0	0	0	0	0	MICD_CLAMP_DB	0	0	JD1_DB	0000h
R3584 (E00h)	FX_Ctrl1	0	FX_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3585 (E01h)	FX_Ctrl2	FX_STS [11:0]												0	0	0	0	0000h
R3600 (E10h)	EQ1_1	EQ1_B1_GAIN [4:0]					EQ1_B2_GAIN [4:0]					EQ1_B3_GAIN [4:0]					EQ1_ENA	6318h
R3601 (E11h)	EQ1_2	EQ1_B4_GAIN [4:0]					EQ1_B5_GAIN [4:0]					0	0	0	0	0	EQ1_B1_MODE	6300h
R3602 (E12h)	EQ1_3	EQ1_B1_A [15:0]																0FC8h
R3603 (E13h)	EQ1_4	EQ1_B1_B [15:0]																03FEh
R3604 (E14h)	EQ1_5	EQ1_B1_PG [15:0]																00E0h
R3605 (E15h)	EQ1_6	EQ1_B2_A [15:0]																1EC4h
R3606 (E16h)	EQ1_7	EQ1_B2_B [15:0]																F136h
R3607 (E17h)	EQ1_8	EQ1_B2_C [15:0]																0409h
R3608 (E18h)	EQ1_9	EQ1_B2_PG [15:0]																04CCh
R3609 (E19h)	EQ1_10	EQ1_B3_A [15:0]																1C9Bh
R3610 (E1Ah)	EQ1_11	EQ1_B3_B [15:0]																F337h
R3611 (E1Bh)	EQ1_12	EQ1_B3_C [15:0]																040Bh
R3612 (E1Ch)	EQ1_13	EQ1_B3_PG [15:0]																0CBBh

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3613 (E1Dh)	EQ1_14	EQ1_B4_A [15:0]																16F8h
R3614 (E1Eh)	EQ1_15	EQ1_B4_B [15:0]																F7D9h
R3615 (E1Fh)	EQ1_16	EQ1_B4_C [15:0]																040Ah
R3616 (E20h)	EQ1_17	EQ1_B4_PG [15:0]																1F14h
R3617 (E21h)	EQ1_18	EQ1_B5_A [15:0]																058Ch
R3618 (E22h)	EQ1_19	EQ1_B5_B [15:0]																0563h
R3619 (E23h)	EQ1_20	EQ1_B5_PG [15:0]																4000h
R3620 (E24h)	EQ1_21	EQ1_B1_C [15:0]																0B75h
R3622 (E26h)	EQ2_1	EQ2_B1_GAIN [4:0]					EQ2_B2_GAIN [4:0]					EQ2_B3_GAIN [4:0]					EQ2_ENA	6318h
R3623 (E27h)	EQ2_2	EQ2_B4_GAIN [4:0]					EQ2_B5_GAIN [4:0]					0	0	0	0	0	EQ2_B1_MODE	6300h
R3624 (E28h)	EQ2_3	EQ2_B1_A [15:0]																0FC8h
R3625 (E29h)	EQ2_4	EQ2_B1_B [15:0]																03FEh
R3626 (E2Ah)	EQ2_5	EQ2_B1_PG [15:0]																00E0h
R3627 (E2Bh)	EQ2_6	EQ2_B2_A [15:0]																1EC4h
R3628 (E2Ch)	EQ2_7	EQ2_B2_B [15:0]																F136h
R3629 (E2Dh)	EQ2_8	EQ2_B2_C [15:0]																0409h
R3630 (E2Eh)	EQ2_9	EQ2_B2_PG [15:0]																04CCh
R3631 (E2Fh)	EQ2_10	EQ2_B3_A [15:0]																1C9Bh
R3632 (E30h)	EQ2_11	EQ2_B3_B [15:0]																F337h
R3633 (E31h)	EQ2_12	EQ2_B3_C [15:0]																040Bh
R3634 (E32h)	EQ2_13	EQ2_B3_PG [15:0]																0CBBh
R3635 (E33h)	EQ2_14	EQ2_B4_A [15:0]																16F8h
R3636 (E34h)	EQ2_15	EQ2_B4_B [15:0]																F7D9h
R3637 (E35h)	EQ2_16	EQ2_B4_C [15:0]																040Ah
R3638 (E36h)	EQ2_17	EQ2_B4_PG [15:0]																1F14h
R3639 (E37h)	EQ2_18	EQ2_B5_A [15:0]																058Ch
R3640 (E38h)	EQ2_19	EQ2_B5_B [15:0]																0563h
R3641 (E39h)	EQ2_20	EQ2_B5_PG [15:0]																4000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3642 (E3Ah)	EQ2_21	EQ2_B1_C [15:0]																0B75h
R3644 (E3Ch)	EQ3_1	EQ3_B1_GAIN [4:0]					EQ3_B2_GAIN [4:0]					EQ3_B3_GAIN [4:0]					EQ3_ENA	6318h
R3645 (E3Dh)	EQ3_2	EQ3_B4_GAIN [4:0]					EQ3_B5_GAIN [4:0]					0	0	0	0	0	EQ3_B1_MODE	6300h
R3646 (E3Eh)	EQ3_3	EQ3_B1_A [15:0]																0FC8h
R3647 (E3Fh)	EQ3_4	EQ3_B1_B [15:0]																03FEh
R3648 (E40h)	EQ3_5	EQ3_B1_PG [15:0]																00E0h
R3649 (E41h)	EQ3_6	EQ3_B2_A [15:0]																1EC4h
R3650 (E42h)	EQ3_7	EQ3_B2_B [15:0]																F136h
R3651 (E43h)	EQ3_8	EQ3_B2_C [15:0]																0409h
R3652 (E44h)	EQ3_9	EQ3_B2_PG [15:0]																04CCh
R3653 (E45h)	EQ3_10	EQ3_B3_A [15:0]																1C9Bh
R3654 (E46h)	EQ3_11	EQ3_B3_B [15:0]																F337h
R3655 (E47h)	EQ3_12	EQ3_B3_C [15:0]																040Bh
R3656 (E48h)	EQ3_13	EQ3_B3_PG [15:0]																0CBBh
R3657 (E49h)	EQ3_14	EQ3_B4_A [15:0]																16F8h
R3658 (E4Ah)	EQ3_15	EQ3_B4_B [15:0]																F7D9h
R3659 (E4Bh)	EQ3_16	EQ3_B4_C [15:0]																040Ah
R3660 (E4Ch)	EQ3_17	EQ3_B4_PG [15:0]																1F14h
R3661 (E4Dh)	EQ3_18	EQ3_B5_A [15:0]																058Ch
R3662 (E4Eh)	EQ3_19	EQ3_B5_B [15:0]																0563h
R3663 (E4Fh)	EQ3_20	EQ3_B5_PG [15:0]																4000h
R3664 (E50h)	EQ3_21	EQ3_B1_C [15:0]																0B75h
R3666 (E52h)	EQ4_1	EQ4_B1_GAIN [4:0]					EQ4_B2_GAIN [4:0]					EQ4_B3_GAIN [4:0]					EQ4_ENA	6318h
R3667 (E53h)	EQ4_2	EQ4_B4_GAIN [4:0]					EQ4_B5_GAIN [4:0]					0	0	0	0	0	EQ4_B1_MODE	6300h
R3668 (E54h)	EQ4_3	EQ4_B1_A [15:0]																0FC8h
R3669 (E55h)	EQ4_4	EQ4_B1_B [15:0]																03FEh
R3670 (E56h)	EQ4_5	EQ4_B1_PG [15:0]																00E0h
R3671	EQ4_6	EQ4_B2_A [15:0]																1EC4h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
(E57h)																		
R3672 (E58h)	EQ4_7	EQ4_B2_B [15:0]																F136h
R3673 (E59h)	EQ4_8	EQ4_B2_C [15:0]																0409h
R3674 (E5Ah)	EQ4_9	EQ4_B2_PG [15:0]																04CCh
R3675 (E5Bh)	EQ4_10	EQ4_B3_A [15:0]																1C9Bh
R3676 (E5Ch)	EQ4_11	EQ4_B3_B [15:0]																F337h
R3677 (E5Dh)	EQ4_12	EQ4_B3_C [15:0]																040Bh
R3678 (E5Eh)	EQ4_13	EQ4_B3_PG [15:0]																0CBBh
R3679 (E5Fh)	EQ4_14	EQ4_B4_A [15:0]																16F8h
R3680 (E60h)	EQ4_15	EQ4_B4_B [15:0]																F7D9h
R3681 (E61h)	EQ4_16	EQ4_B4_C [15:0]																040Ah
R3682 (E62h)	EQ4_17	EQ4_B4_PG [15:0]																1F14h
R3683 (E63h)	EQ4_18	EQ4_B5_A [15:0]																058Ch
R3684 (E64h)	EQ4_19	EQ4_B5_B [15:0]																0563h
R3685 (E65h)	EQ4_20	EQ4_B5_PG [15:0]																4000h
R3686 (E66h)	EQ4_21	EQ4_B1_C [15:0]																0B75h
R3712 (E80h)	DRC1 ctrl1	DRC1_SIG_DET_RMS [4:0]					DRC1_SIG_DET_PK [1:0]		DRC1_NG_ENA	DRC1_SIG_DET_MODE	DRC1_SIG_DET	DRC1_KNEE2_OP_ENA	DRC1_QR	DRC1_ANTICLIP	DRC1_WSEQ_SIG_DET_ENA	DRC1L_ENA	DRC1R_ENA	0018h
R3713 (E81h)	DRC1 ctrl2	0	0	0	DRC1_ATK [3:0]				DRC1_DCY [3:0]				DRC1_MINGAIN [2:0]			DRC1_MAXGAIN [1:0]		0933h
R3714 (E82h)	DRC1 ctrl3	DRC1_NG_MINGAIN [3:0]				DRC1_NG_EXP [1:0]		DRC1_QR_THR [1:0]		DRC1_QR_DCY [1:0]		DRC1_HI_COMP [2:0]			DRC1_LO_COMP [2:0]			0018h
R3715 (E83h)	DRC1 ctrl4	0	0	0	0	0	DRC1_KNEE_IP [5:0]						DRC1_KNEE_OP [4:0]					0000h
R3716 (E84h)	DRC1 ctrl5	0	0	0	0	0	0	DRC1_KNEE2_IP [4:0]					DRC1_KNEE2_OP [4:0]					0000h
R3776 (EC0h)	HPLPF1_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF1_MODE	LHPF1_ENA	0000h
R3777 (EC1h)	HPLPF1_2	LHPF1_COEFF [15:0]																0000h
R3780 (EC4h)	HPLPF2_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF2_MODE	LHPF2_ENA	0000h
R3781 (EC5h)	HPLPF2_2	LHPF2_COEFF [15:0]																0000h
R3784 (EC8h)	HPLPF3_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF3_MODE	LHPF3_ENA	0000h

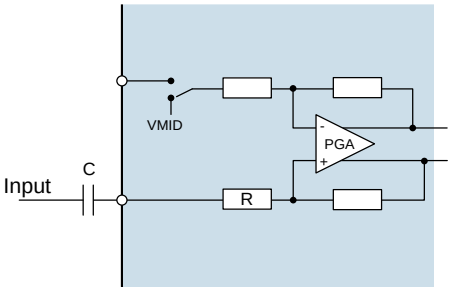
REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3785 (EC9h)	HPLPF3_2	LHPF3_COEFF [15:0]																0000h
R3788 (ECCh)	HPLPF4_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF4_MODE	LHPF4_ENA	0000h
R3789 (ECDh)	HPLPF4_2	LHPF4_COEFF [15:0]																0000h
R3808 (EE0h)	ASRC_ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	ASRC2L_ENA	ASRC2R_ENA	ASRC1L_ENA	ASRC1R_ENA	0000h
R3809 (EE1h)	ASRC_STATUS	0	0	0	0	0	0	0	0	0	0	0	0	ASRC2L_ENA_STS	ASRC2R_ENA_STS	ASRC1L_ENA_STS	ASRC1R_ENA_STS	0000h
R3810 (EE2h)	ASRC_RATE1	0	ASRC_RATE1 [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3811 (EE3h)	ASRC_RATE2	0	ASRC_RATE2 [3:0]				0	0	0	0	0	0	0	0	0	0	0	4000h
R3824 (EF0h)	ISRC 1 CTRL 1	0	ISRC1_FSH [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3825 (EF1h)	ISRC 1 CTRL 2	0	ISRC1_FSL [3:0]				0	0	0	0	0	0	0	0	0	0	1	0001h
R3826 (EF2h)	ISRC 1 CTRL 3	ISRC1_INT1_ENA	ISRC1_INT2_ENA	ISRC1_INT3_ENA	ISRC1_INT4_ENA	0	0	ISRC1_DEC1_ENA	ISRC1_DEC2_ENA	ISRC1_DEC3_ENA	ISRC1_DEC4_ENA	0	0	0	0	0	ISRC1_NOTCH_ENA	0000h
R3827 (EF3h)	ISRC 2 CTRL 1	0	ISRC2_FSH [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3828 (EF4h)	ISRC 2 CTRL 2	0	ISRC2_FSL [3:0]				0	0	0	0	0	0	0	0	0	0	1	0001h
R3829 (EF5h)	ISRC 2 CTRL 3	ISRC2_INT1_ENA	ISRC2_INT2_ENA	0	0	0	0	ISRC2_DEC1_ENA	ISRC2_DEC2_ENA	0	0	0	0	0	0	0	ISRC2_NOTCH_ENA	0000h
R12288 (3000h)	WSEQ Sequence 1	WSEQ_DATA_WIDTH0 [2:0] *(O)*			WSEQ_ADDR0 [12:0] *(O)*													0225h
R12289 (3001h)	WSEQ Sequence 2	WSEQ_DELAY0 [3:0] *(O)*				WSEQ_DATA_START0 [3:0] *(O)*				WSEQ_DATA0 [7:0] *(O)*								0001h
R12290 (3002h)	WSEQ Sequence 3	WSEQ_DATA_WIDTH1 [2:0] *(O)*			WSEQ_ADDR1 [12:0] *(O)*													0000h
R12291 (3003h)	WSEQ Sequence 4	WSEQ_DELAY1 [3:0] *(O)*				WSEQ_DATA_START1 [3:0] *(O)*				WSEQ_DATA1 [7:0] *(O)*								0003h
		(similar for WSEQ_ADDR2 … WSEQ_ADDR254*)*																
R12798 (31FEh)	WSEQ Sequence 511	WSEQ_DATA_WIDTH255 [2:0] *(O)*			WSEQ_ADDR255 [12:0] *(O)*													0000h
R12799 (31FFh)	WSEQ Sequence 512	WSEQ_DELAY255 [3:0] *(O)*				WSEQ_DATA_START255 [3:0] *(O)*				WSEQ_DATA255 [7:0] *(O)*								0000h

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

ANALOGUE INPUT PATHS

The WM8998 provides up to 6 analogue audio input paths. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each analogue input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the impedance of the input pin. The circuit is illustrated in Figure 76.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 76 Audio Input Path DC Blocking Capacitor

In accordance with the WM8998 input pin resistance (see "Electrical Characteristics"), it is recommended that a 1µF capacitance for all input connections will give good results in most cases, with a 3dB cut-off frequency around 13Hz.

Ceramic capacitors are suitable, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a single-ended line or microphone input connection. For a differential input connection, a DC blocking capacitor is required on both input pins.

The external connections for single-ended and differential microphones, incorporating the WM8998 microphone bias circuit, are shown later in the "Microphone Bias Circuit" section - see Figure 77.

DIGITAL MICROPHONE INPUT PATHS

The WM8998 provides up to 3 digital microphone input paths. The DMICDAT1 pin carries two multiplexed channels of audio data; the DMICDAT2 pin supports a single channel of audio data. These interfaces are clocked using the respective DMICCLK1 or DMICCLK2 pin.

The external connections for digital microphones, incorporating the WM8998 microphone bias circuit, are shown later in the "Microphone Bias Circuit" section - see Figure 79.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

When two microphones are connected to a single DMICDAT pin, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The WM8998 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting. Integrated pull-down resistors can be enabled on the DMICDAT pins if required.

The voltage reference for each digital microphone interface is selectable. It is important that the selected reference for the WM8998 interface is compatible with the applicable configuration of the external microphone.

MICROPHONE BIAS CIRCUIT

The WM8998 is designed to interface easily with up to 6 analogue microphones or up to 3 digital microphones.

Each microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones); these can be provided by the MICBIAS1, MICBIAS2 or MICBIAS3 regulators on the WM8998.

Note that the MICVDD pin can also be used (instead of MICBIASn) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

Analogue microphones may be connected in single-ended or differential configurations, as illustrated in Figure 77. The differential configuration provides better performance due to its rejection of common-mode noise; the single-ended method provides a reduction in external component count.

A bias resistor is required when using an electret condenser microphone (ECM). The bias resistor should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the WM8998 is not exceeded.

A 2.2kΩ bias resistor is recommended; this provides compatibility with a wide range of microphone components.

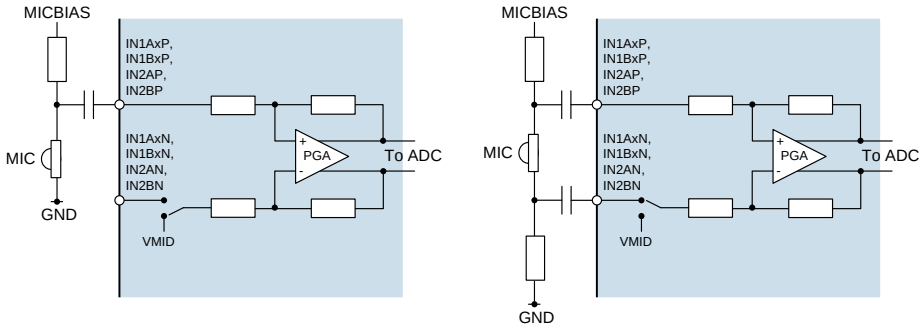


Figure 77 Single-Ended and Differential Analogue Microphone Connections

Analogue MEMS microphones can be connected to the WM8998 as illustrated in Figure 78. In this configuration, the MICBIAS generators provide a low-noise supply for the microphones; a bias resistor is not required.

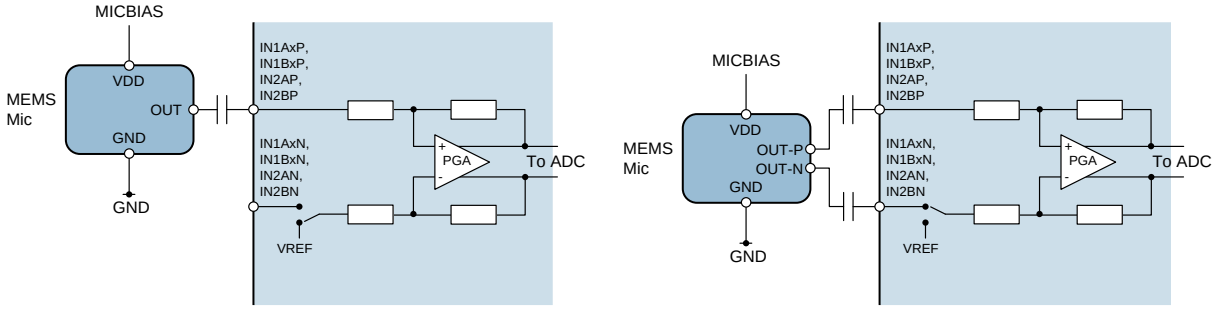


Figure 78 Single-Ended and Differential Analogue Microphone Connections

Digital microphone connection to the WM8998 is illustrated in Figure 79.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

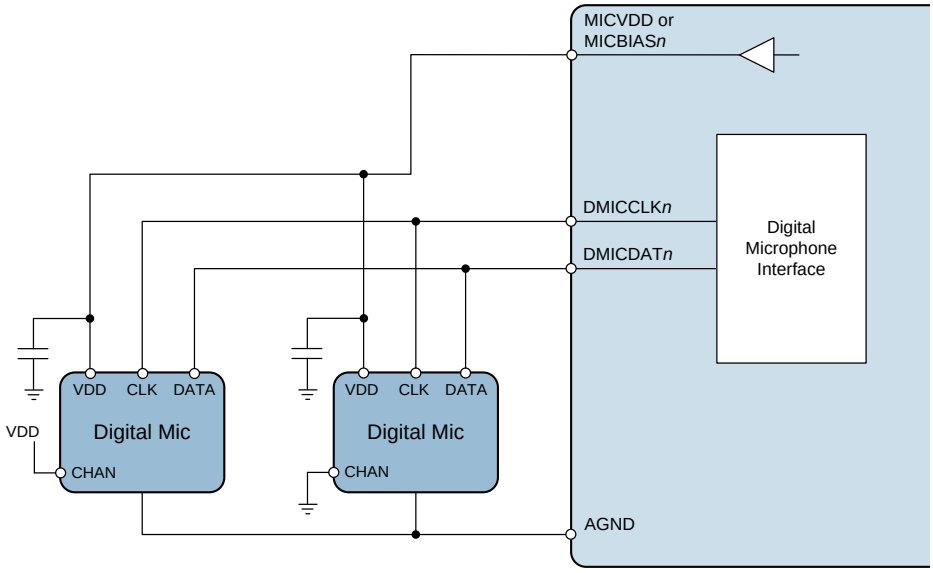


Figure 79 Digital Microphone Connection

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. See “Charge Pumps, Regulators and Voltage Reference” for details of the MICBIAS generators.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required (eg. for digital microphone supply decoupling). The compatible load conditions are detailed in the “Electrical Characteristics” section.

If the capacitive load on MICBIAS1, MICBIAS2 or MICBIAS3 exceeds the specified conditions for Regulator mode (eg. due to a decoupling capacitor or long PCB trace), then the respective generator must be configured in Bypass mode.

The maximum output current for each MICBIAS*n* pin is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode. The MICBIAS output voltage can be adjusted using register control in Regulator mode.

HEADPHONE/LINE/EARPIECE DRIVER OUTPUT PATH

The WM8998 provides stereo headphone, stereo line, and mono earpiece output drivers. These outputs are all ground-referenced, allowing direct connection to the external load(s). There is no requirement for DC blocking capacitors.

In single-ended (default) configuration, the headphone and line outputs comprise 4 independently controlled output channels, for up to 2 stereo outputs. In mono (BTL) mode, the drivers support up to 2 differential outputs.

The headphone and line outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pins must be connected to ground for normal operation of the respective outputs.

The feedback pins should be connected to GND close to the respective headphone/line jack, as illustrated in Figure 80. In mono (differential) mode, the feedback pin(s) should be connected to the ground plane that is physically closest to the earpiece output PCB tracks.

The mono earpiece output is supported on the EPOUTP and EPOUTN pins. The output configuration is differential (BTL), suitable for direct connection to an external earpiece or hearing coil load.

Typical headphone, line, and earpiece connections are illustrated in Figure 80.

It is recommended to ensure that the electrical characteristics of the PCB traces for each output pair are closely matched. This is particularly important to matching the two traces of a differential (BTL) output.

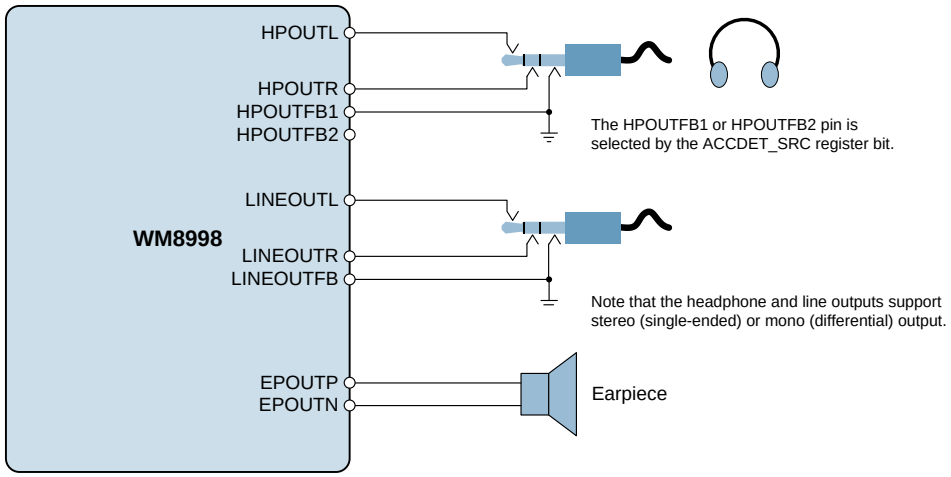


Figure 80 Headphone, Line, and Earpiece Connection

It is common for ESD diodes to be wired to pins that link to external connectors. This provides protection from potentially harmful ESD effects. In a typical application, ESD diodes would be recommended for the headphone and line output paths (HPOUT and LINEOUT), when used as external headphone or line output.

The HPOUT and LINEOUT outputs are ground-referenced, and the respective voltages may swing between +1.8V and -1.8V. The ESD diode configuration must be carefully chosen.

The recommended ESD diode configuration for these ground-referenced outputs is illustrated in Figure 81. The 'back-to-back' arrangement is necessary in order to prevent clipping and distortion of the output signal.

Note that similar care is required when connecting the WM8998 outputs to external circuits that provide input path ESD protection - the configuration on those input circuits must be correctly designed to accommodate ground-referenced signals.

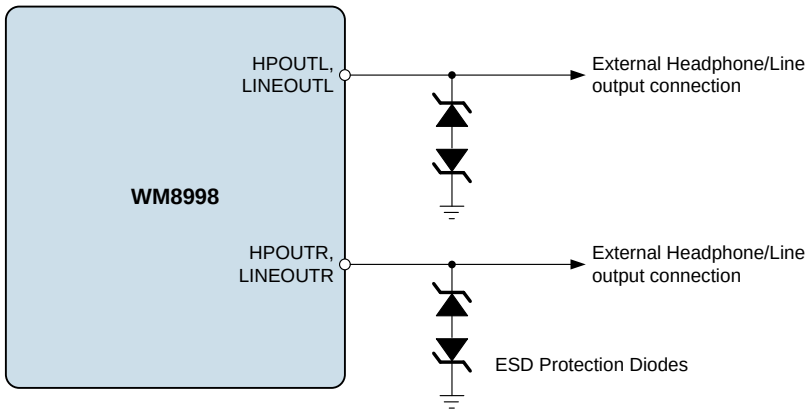


Figure 81 ESD Diode Configuration for External Output Connections

SPEAKER DRIVER OUTPUT PATH

The WM8998 incorporates two Class D speaker drivers, offering high amplifier efficiency at large signal levels. As the Class D output is a pulse width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The efficiency of the speaker drivers is affected by the series resistance between the WM8998 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 82. This resistance should be as low as possible to maximise efficiency.

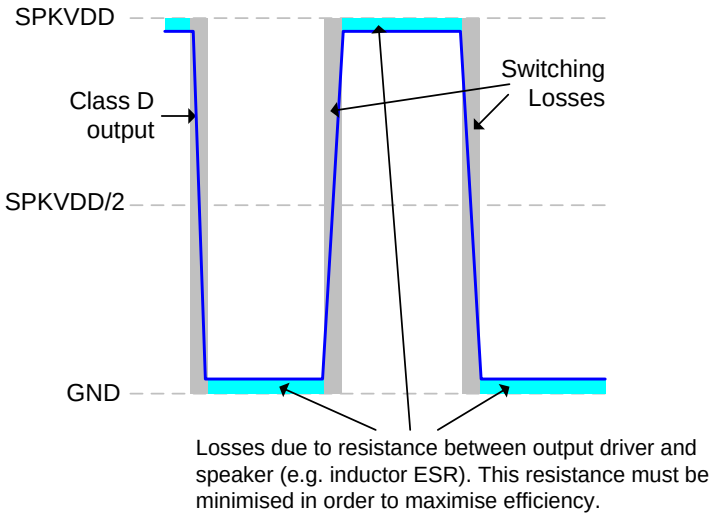


Figure 82 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC or 1st order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a 2nd order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimises power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximises both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is illustrated in Figure 83.

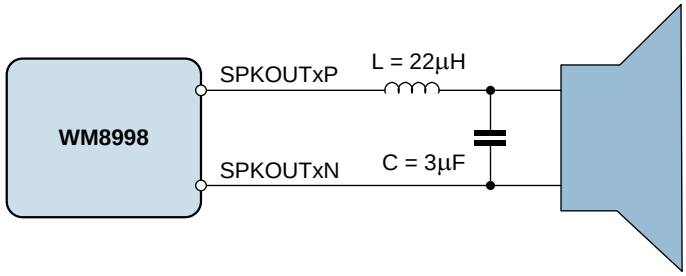


Figure 83 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 84. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.

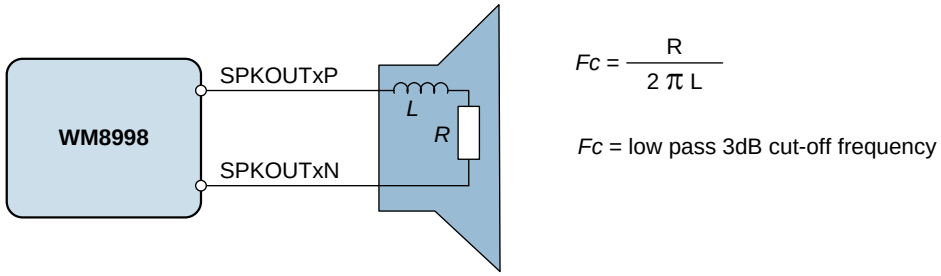


Figure 84 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2 \pi Fc} = \frac{8\Omega}{2 \pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20µH to 100µH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the WM8998 operate at much higher frequencies than is recommended for most speakers and it must be ensured that the cut-off frequency is low enough to protect the speaker.

POWER SUPPLY / REFERENCE DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations ('spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling ('bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8998, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply and voltage reference decoupling capacitors for WM8998 are detailed below in Table 121.

POWER SUPPLY	DECOUPLING CAPACITOR
LDOVDD, DBVDD1, DBVDD2, DBVDD3, AVDD	0.1μF ceramic (see Note)
CPVDD	4.7μF ceramic
MICVDD	4.7μF ceramic
DCVDD	4.7μF ceramic
SPKVDDL, SPKVDDR	4.7μF ceramic
VREFC	1.0μF ceramic

Table 121 Power Supply Decoupling Capacitors

Note: 0.1μF is required with 4.7μF a guide to the total required power rail capacitance.

All decoupling capacitors should be placed as close as possible to the WM8998 device. The connection between AGND, the AVDD decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND balls of the WM8998.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

CHARGE PUMP COMPONENTS

The WM8998 incorporates two Charge Pump circuits, identified as CP1 and CP2.

CP1 generates the CP1VOUTP and CP1VOUTN supply rails for the ground-referenced headphone drivers; CP2 generates the CP2VOUT supply rail for the microphone bias (MICBIAS) regulators.

Decoupling capacitors are required on each of the Charge Pump outputs. A fly-back capacitor is also required for each Charge Pump.

The recommended Charge Pump capacitors for WM8998 are detailed below in Table 122.

DESCRIPTION	CAPACITOR
CP1VOUTP decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1VOUTN decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1 fly-back (connect between CP1CA and CP1CB)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.
CP2VOUT decoupling	Required capacitance is 1.0µF at 3.6V. Suitable component typically 4.7µF.
CP2 fly-back (connect between CP2CA and CP2CB)	Required capacitance is 220nF at 2V. Suitable component typically 470nF.

Table 122 Charge Pump External Capacitors

Ceramic capacitors are recommended for these Charge Pump requirements. Note that, due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. Ceramic capacitors with X5R dielectric are recommended.

The positioning of the Charge Pump capacitors is important, particularly the fly-back capacitors. These capacitors should be placed as close as possible to the WM8998. The component choice and positioning of the CP1 components are more critical than those of CP2, due to the higher output power requirements of CP1.

EXTERNAL ACCESSORY DETECTION COMPONENTS

The external accessory detection circuit measures jack insertion using the JACKDET pin. The insertion switch status is detected using an internal pull-up resistor circuit on the JACKDET pin.

Microphone detection and key-button press detection is supported using the MICDETn pins. The applicable MICDET pin should be connected to one of the MICBIASn outputs, via a 2.2kΩ bias resistor, as described in the “Microphone Bias Circuit” section. Note that, when using the External Accessory Detection function, the MICBIASn resistor must be 2.2kΩ +/-2%.

A recommended circuit configuration, including headphone output and microphone connections, is shown in Figure 85. See “Analogue Input Paths” for details of the DC-blocking microphone input capacitor selection.

The recommended external components and connections for microphone / push-button detection are illustrated in Figure 86.

Note that, when using the Microphone Detect circuit, it is recommended to use the IN2B analogue microphone input paths, to ensure best immunity to electrical transients arising from the external accessory.

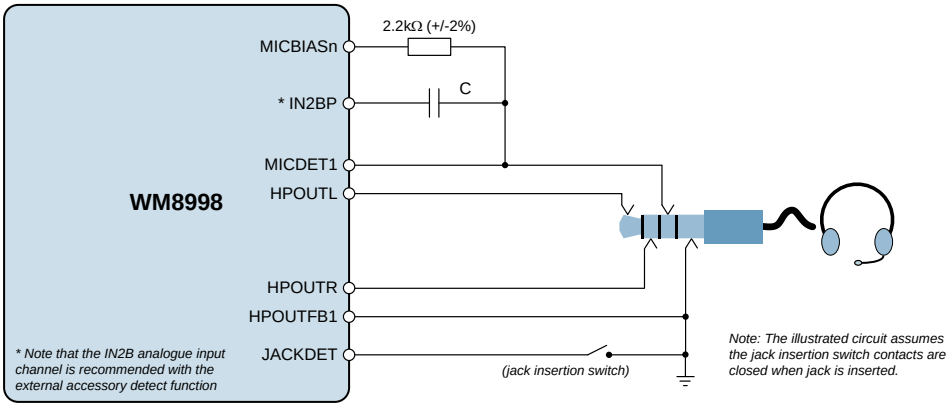


Figure 85 External Accessory Detection

The accessory detection circuit measures the impedance of an external load connected to one of the MICDET pins.

The microphone detection circuit uses MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 as a reference. The applicable source is configured using the MICD_BIAS_SRC register.

The WM8998 can detect the presence of a typical microphone and up to 6 push-buttons, using the components shown in Figure 86. When the microphone detection circuit is enabled, then each of the push-buttons shown will cause a different bit within the MICD_LVL register to be set.

The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required. A measured external impedance of 75Ω will cause the MICD_LVL [3] bit to be set.

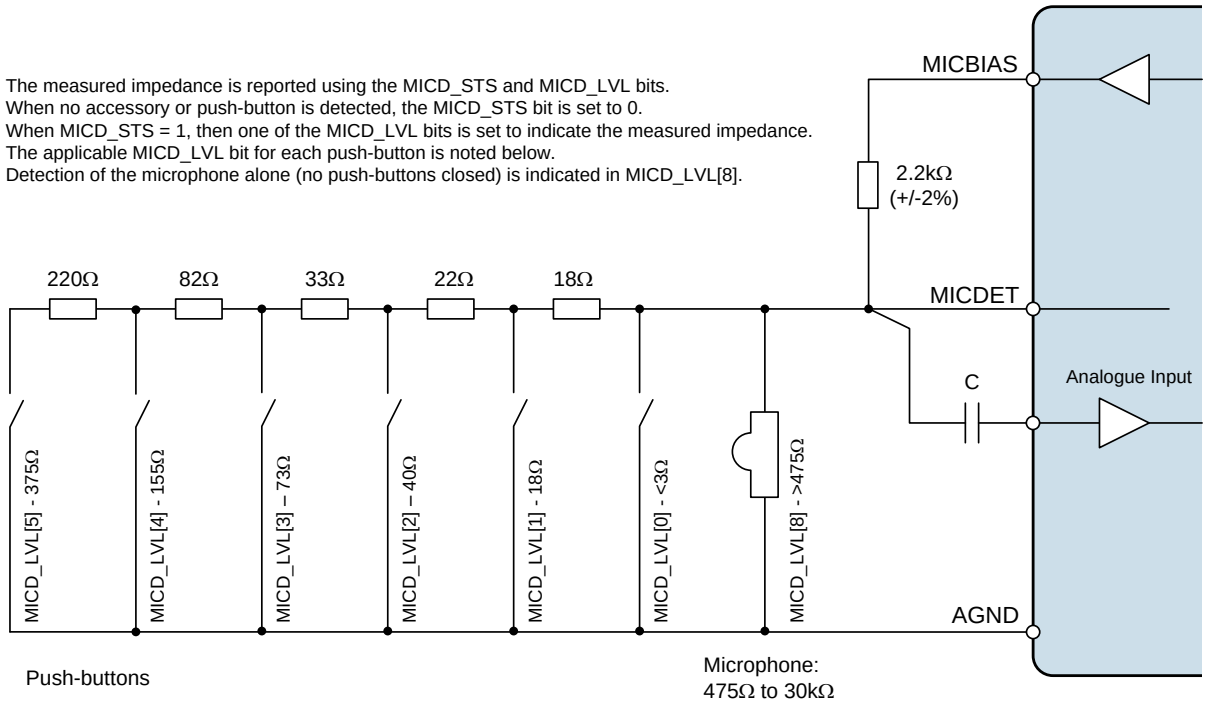
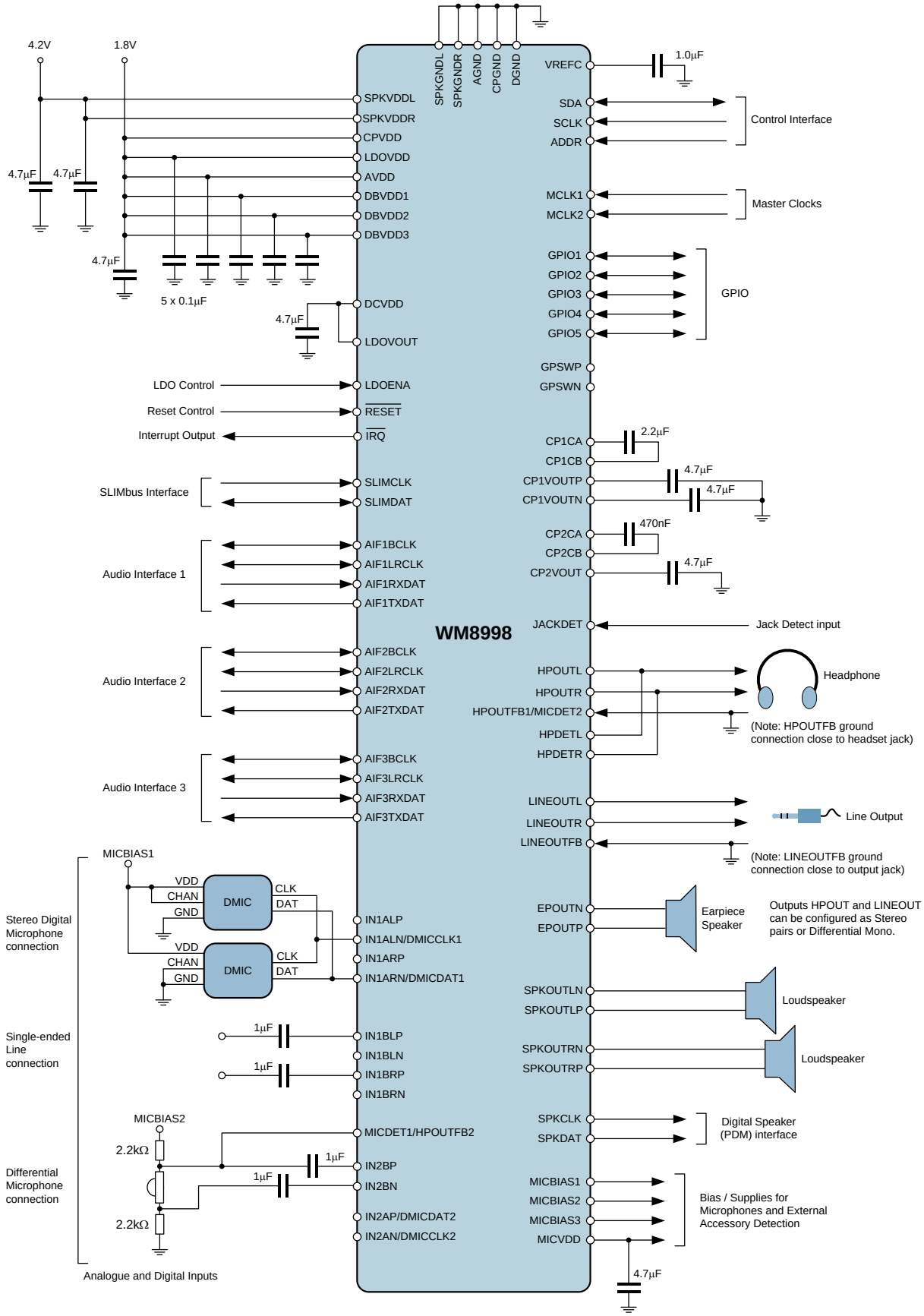


Figure 86 External Accessory Detect Connection

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM



RESETS SUMMARY

The contents of Table 123 provide a summary of the WM8998 registers and other programmable memory under different reset conditions. The associated events and conditions are listed below.

- A Power-On Reset occurs when AVDD or DBVDD1 is below its respective reset threshold. (Note that DCVDD is also required for initial start-up; subsequent interruption to DCVDD should only be permitted as part of a control sequence for entering Sleep mode.)
- A Hardware Reset occurs when the $\overline{\text{RESET}}$ input is asserted (logic 0).
- A Software Reset occurs when register R0 is written to.
- Sleep Mode is selected when LDO1 is disabled. (LDO1 can be controlled using the LDO1_ENA register bit, or using the LDOENA pin; both of these controls must be de-asserted to disable the LDO.) Note that the AVDD, DBVDD1 and LDOVDD supplies must be present, and the LDOENA pin held low. It is assumed that DCVDD is supplied by LDO1.

	ALWAYS-ON REGISTERS	OTHER REGISTERS	CONTROL SEQUENCER MEMORY
Power-On Reset	Reset	Reset	Reset
Hardware Reset	Reset	Reset	Retained
Software Reset	Reset	Reset	Retained
Sleep Mode	Retained	Reset	Retained

Table 123 Memory Reset Summary

See “Low Power Sleep Configuration” for details of the ‘Always-On’ registers.

DIGITAL AUDIO INTERFACE CLOCKING CONFIGURATIONS

The digital audio interfaces (AIF1, AIF2, AIF3) can be configured in Master or Slave modes. In all applications, it is important that the system clocking configuration is correctly designed. Incorrect clock configurations will lead to audible clicks arising from dropped or repeated audio samples; this is caused by the inherent tolerances of multiple asynchronous system clocks.

To ensure reliable clocking of the audio interface functions, it is a requirement that the external interface clocks (eg. BCLK, LRCLK) are derived from the same clock source as SYSCLK (or ASYNCCLK, where applicable).

In AIF Master mode, the external BCLK and LRCLK signals are generated by the WM8998 and synchronisation of these signals with SYSCLK (or ASYNCCLK) is ensured. In this case, clocking of the AIF is typically derived from the MCLK1 or MCLK2 inputs, either directly or via one of the Frequency Locked Loop (FLL) circuits. It is also possible to use a different interface (AIFn or SLIMbus) to provide the reference clock to which the AIF Master can be synchronised.

In AIF Slave mode, the external BCLK and LRCLK signals are generated by another device, as inputs to the WM8998. In this case, it must be ensured that the applicable system clock (SYSCLK or ASYNCCLK) is generated from a source that is synchronised to the external BCLK and LRCLK inputs.

In a typical Slave mode application, the BCLK input is selected as the clock reference, using the FLL to perform frequency shifting. It is also possible to use the MCLK1 or MCLK2 inputs, but only if the selected clock is synchronised externally to the BCLK and LRCLK inputs. The SLIMbus interface can also provide the clock reference, via one of the FLLs, provided that the BCLK and LRCLK signals are externally synchronised with the SLIMCLK input.

The valid AIF clocking configurations are listed in Table 124 for AIF Master and AIF Slave modes.

The applicable system clock (SYSCLK or ASYNCCLK) depends on the AIFn_RATE setting for the relevant digital audio interface; if AIFn_RATE < 1000, then SYSCLK is applicable; if AIFn_RATE ≥ 1000, then ASYNCCLK is applicable.

AIF MODE	CLOCKING CONFIGURATION
AIF Master Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface (BCLK, LRCLK, SLIMCLK) as FLLn source.
AIF Slave Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects BCLK as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface (eg. SLIMCLK) as FLLn source, provided the other interface is externally synchronised to the BCLK input.

Table 124 Audio Interface (AIF) Clocking Confgurations

In each case, the SYSCLK (ASYNCCLK) frequency must be a valid ratio to the LRCLK frequency; the supported clocking rates are defined by the SYSCLK_FREQ (ASYNC_CLK_FREQ) and SAMPLE_RATE_n (ASYNC_SAMPLE_RATE_n) registers.

The valid AIF clocking configurations are illustrated in Figure 87 to Figure 93 below. Note that, where MCLK1 is illustrated as the clock source, it is equally possible to select MCLK2 as the clock source. Similarly, in cases where FLL1 is illustrated, it is equally possible to select FLL2.

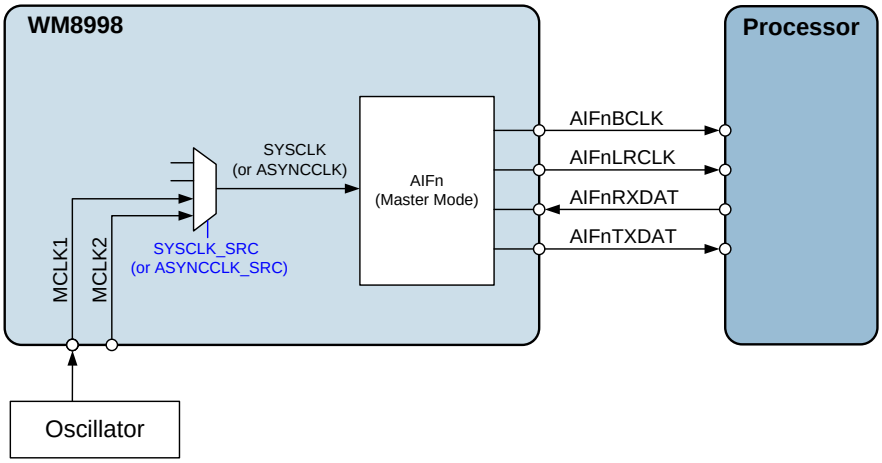


Figure 87 AIF Master Mode, using MCLK as Reference

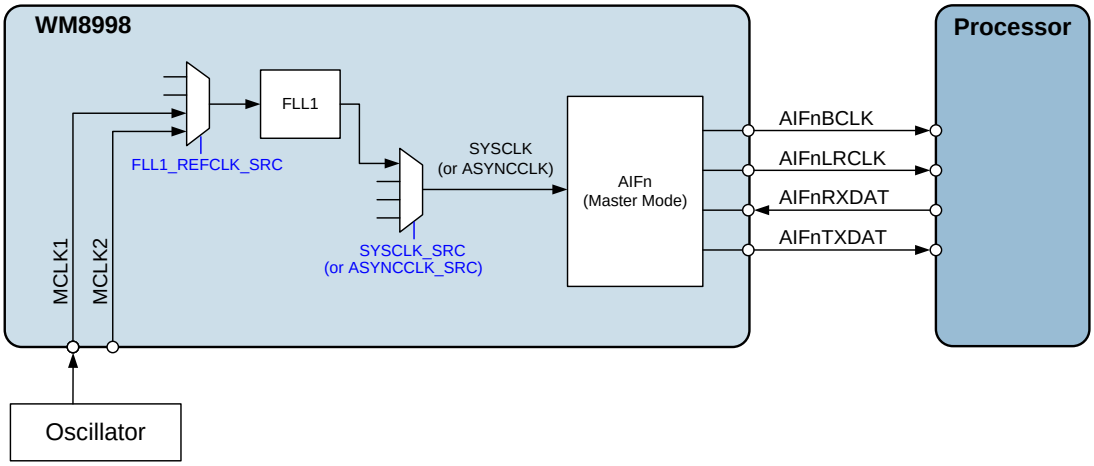


Figure 88 AIF Master Mode, using MCLK and FLL as Reference

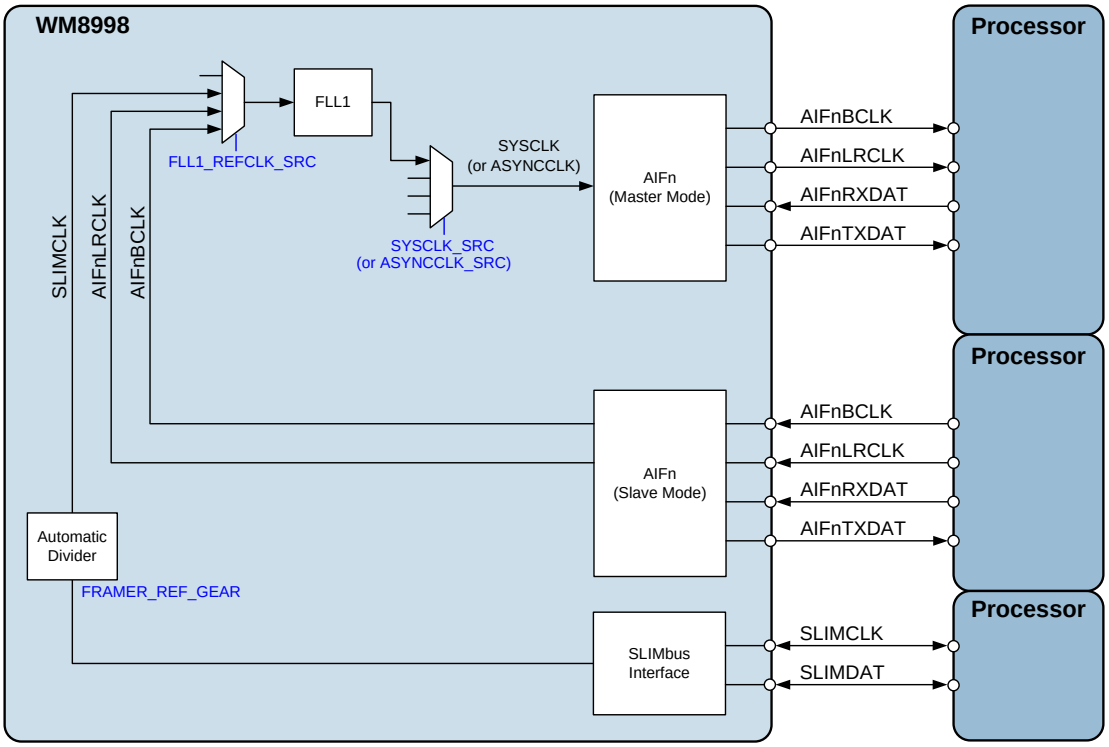


Figure 89 AIF Master Mode, using another Interface as Reference

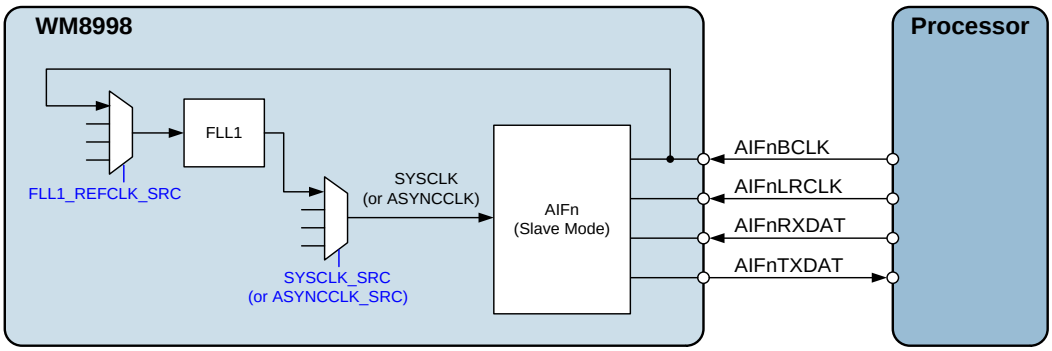


Figure 90 AIF Slave Mode, using BCLK and FLL as Reference

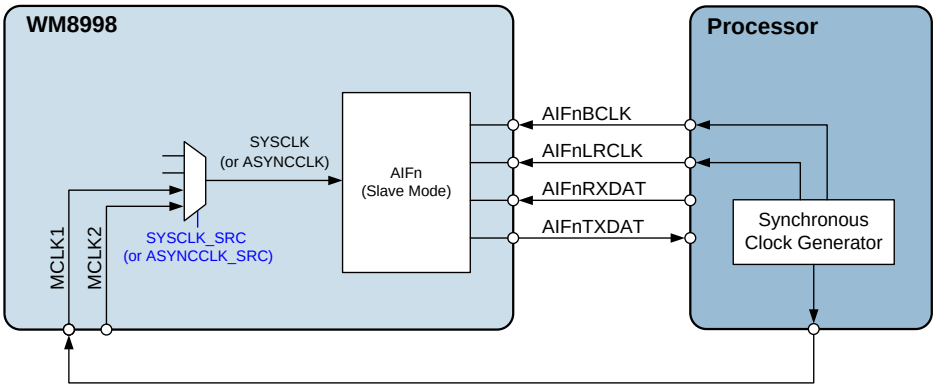


Figure 91 AIF Slave Mode, using MCLK as Reference

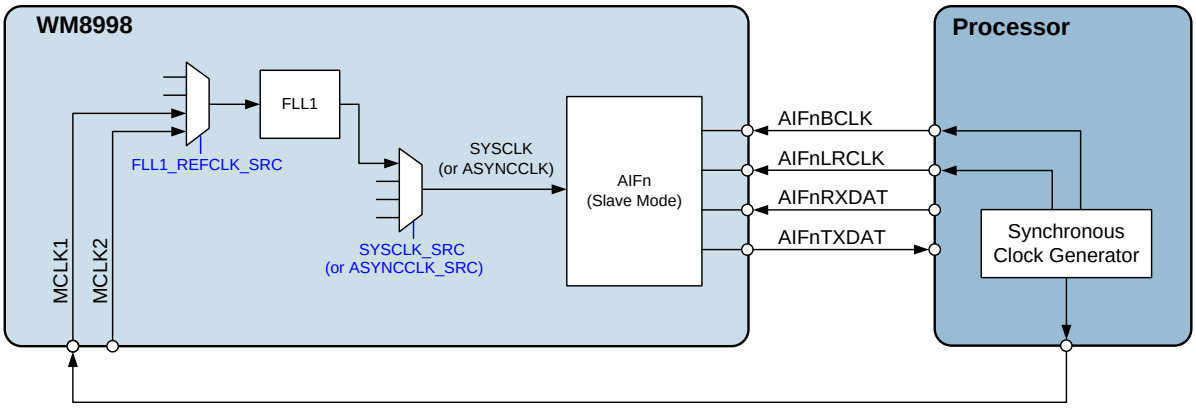


Figure 92 AIF Slave Mode, using MCLK and FLL as Reference

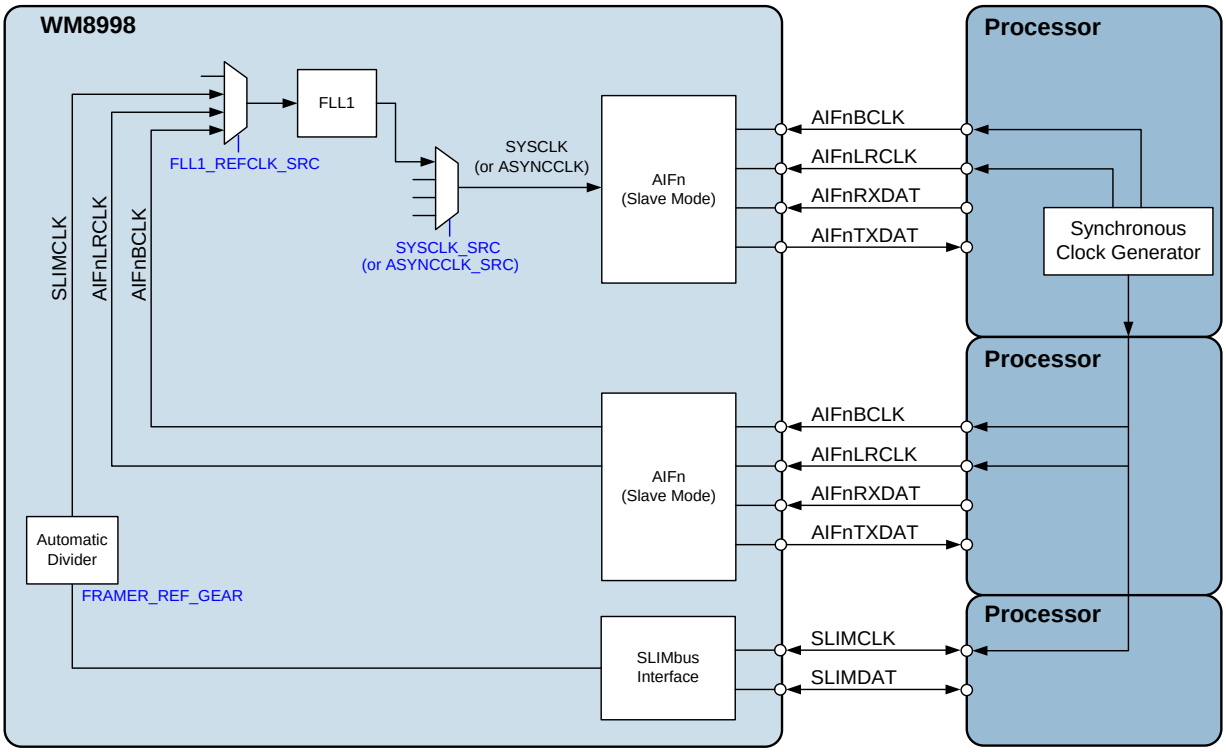


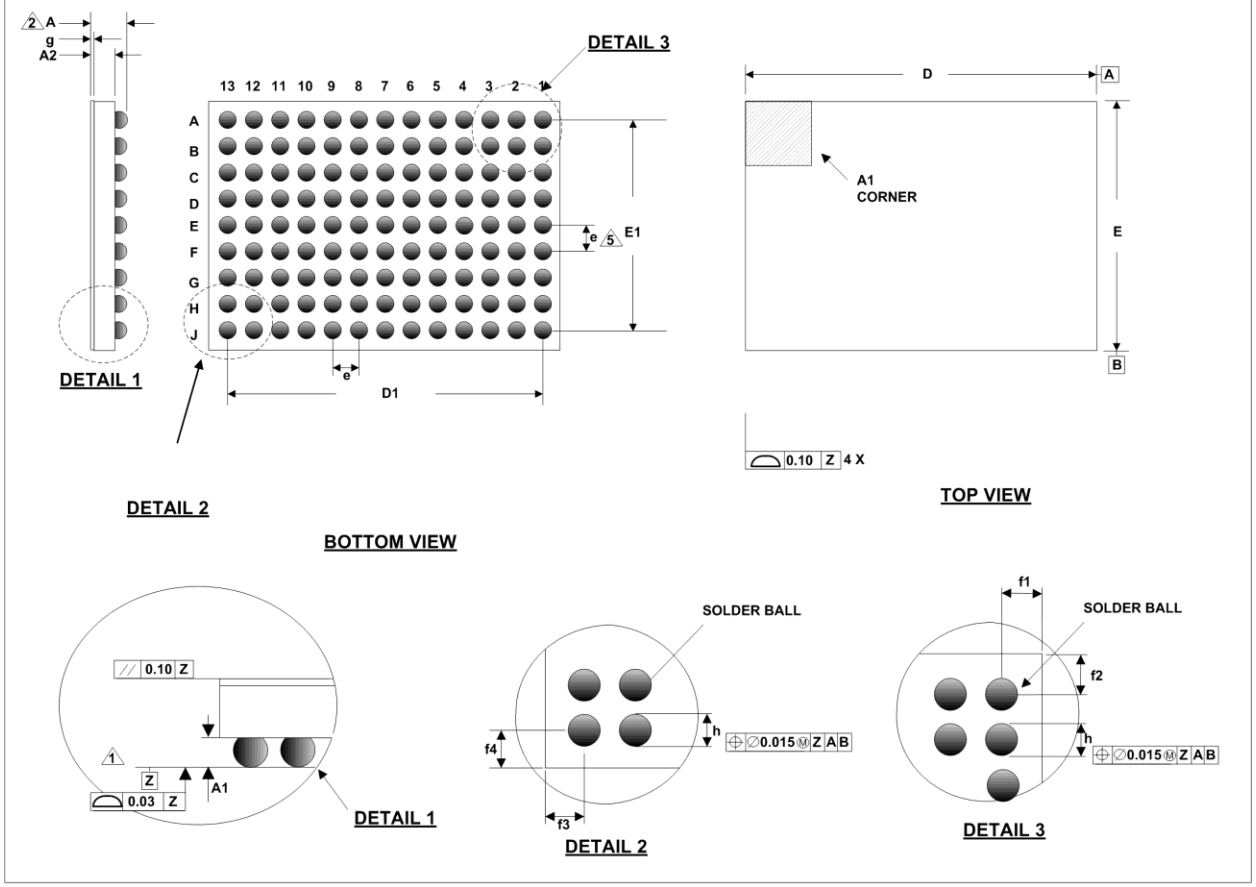
Figure 93 AIF Slave Mode, using another Interface as Reference

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8998 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

B: 117 BALL W-CSP PACKAGE 5.348 x 4.088 x 0.574 mm BODY, 0.40 mm BALL PITCH **DM128.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.538	0.574	0.610	
A1	0.165	0.199	0.232	
A2	0.356	0.376	0.396	
D	5.323	5.348	5.373	
D1		4.80 BSC		
E	4.063	4.088	4.113	
E1		3.20 BSC		
e		0.40 BSC		5
f1		0.274 BSC		
f2		0.444 BSC		
f3		0.274 BSC		
f4		0.444 BSC		
g		0.022		
h	0.212	0.262	0.312	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
02/01/14	1.0	First Release.		
14/01/14	2.0	Reel Quantity changed		PH
25/02/14	2.0	Digital Speaker (PDM) output added. Additional notes on SLIMbus Value Map & Information Map. Clarification of the TRIG_ON_STARTUP (automatic sample rate detection) behaviour. IN1 / IN3 input pins changed to IN1A / IN1B. IN2 / IN4 input pins changed to IN2A / IN2B. SLIMbus Timing information added.		PH
25/03/14	2.0	Updated Electrical Characteristics		SS
14/05/14	2.1	Recommended DBVDD1 operating range updated - 1.7V to 1.9V. SLIMCLK_REF_GEAR description updated.	13 136	PH
21/05/14	2.2	Updates to Charge Pump configuration requirements, according to HPOUT or EPOUT load condition. Electrical Characteristics and Reset Thresholds updated. Thermal characteristics added. Control logic affecting 'on-the-fly' AIF configuration described. SLIMbus description for control register access updated. Added 'Initialisation Sequence' definition - required after Power-Up, Reset, or Wake-Up.	15, 140, 142 16-23 25 108-119 134-135 235, 255, 256, 259	PH
26/06/14	3.0	Product Status updated to Pre-Production	All	JMacDs
15/10/14	4.0	Clarification to the AEC Loopback path description Clarification of LDOENA & LDOVDD pin requirements Electrical Characteristics updated Typical Performance data added Clarification of Sleep Mode control requirements when using external DCVDD (not LDO1) Bus-keeper function on GPIO pins is removed	2, 140, 151 9, 249 16-18 26-27 176 179-180	PH
09/01/17	4.1	Clarification of DCVDD, GPSWN, GPSWP voltage limits Clarification of PDM input/output digital signal levels. Electrical Characteristics updated. Correction to PWMn_LVL description. Sample Rate control requirements updated (*RATE, *FSL, *FSH). ASRC sample rate restrictions added. Clarification of SLIMbus requirements for different TP options. Clocking required for FLL Interrupt. FLL configuration and example settings updated. Correction to FLLn_SS_SEL description. Noted constraints for using WSEQ_START to trigger WSEQ.	12, 21 14, 16, 50, 147 15 86, 87, 190 88-103 96, 98, 211 128, 129 197 222-237 234 242	PH

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