



**THE DATASHEET OF  
AD5623RBRMZ-3**



## FEATURES

Low power, smallest pin-compatible, dual *nano*DAC

**AD5663R:** 16 bits

**AD5643R:** 14 bits

**AD5623R:** 12 bits

User-selectable external or internal reference

External reference default

On-chip 1.25 V/2.5 V, 5 ppm/°C reference

10-lead MSOP and 3 mm × 3 mm LFCSP

2.7 V to 5.5 V power supply

Guaranteed monotonic by design

Power-on reset to zero scale

Per channel power-down

Serial interface up to 50 MHz

Hardware LDAC and CLR functions

## APPLICATIONS

Process control

Data acquisition systems

Portable battery-powered instruments

Digital gain and offset adjustment

Programmable voltage and current sources

Programmable attenuators

## GENERAL DESCRIPTION

The [AD5623R/AD5643R/AD5663R](#), members of the *nano*DAC® family, are low power, dual 12-, 14-, and 16-bit buffered voltage-out digital-to-analog converters (DAC) that operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design.

The [AD5623R/AD5643R/AD5663R](#) have an on-chip reference. The [AD5623R-3/AD5643R-3/AD5663R-3](#) have a 1.25 V, 5 ppm/°C reference, giving a full-scale output of 2.5 V; and the [AD5623R-5/AD5643R-5/AD5663R-5](#) have a 2.5 V, 5 ppm/°C reference, giving a full-scale output of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference; and all devices can be operated from a single 2.7 V to 5.5 V supply. The internal reference is turned on by writing to the DAC.

The parts incorporate a power-on reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode.

Rev. G

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## FUNCTIONAL BLOCK DIAGRAM

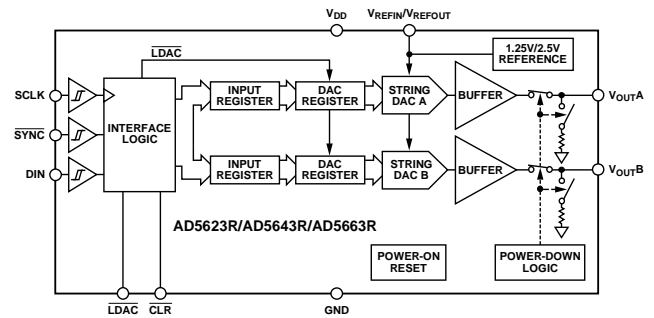


Figure 1.

Table 1. Related Devices

Part No.	Description
<a href="#">AD5663</a>	2.7 V to 5.5 V, dual 16-bit <i>nano</i> DAC, with external reference

The low power consumption of this part in normal operation makes it ideally suited to portable, battery-operated equipment.

The [AD5623R/AD5643R/AD5663R](#) use a versatile, 3-wire serial interface that operates at clock rates up to 50 MHz, and they are compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing to be achieved.

## PRODUCT HIGHLIGHTS

1. Dual 12-, 14-, and 16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP.
4. Low power; typically consumes 0.6 mW at 3 V and 1.25 mW at 5 V.
5. 4.5 μs maximum settling time for the [AD5623R](#).

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**4/06—Revision 0: Initial Version**

## SPECIFICATIONS

## AD5623R-5/AD5643R-5/AD5663R-5

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ;  $R_L = 2\text{ k}\Omega$  to GND;  $C_L = 200\text{ pF}$  to GND;  $V_{REFIN} = V_{DD}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter	A Grade <sup>1</sup>			B Grade <sup>1</sup>			Unit	Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
STATIC PERFORMANCE <sup>2</sup>								
AD5663R								
Resolution				16			Bits	Guaranteed monotonic by design
Relative Accuracy					$\pm 8$	$\pm 16$	LSB	
Differential Nonlinearity						$\pm 1$	LSB	
AD5643R								
Resolution				14			Bits	Guaranteed monotonic by design
Relative Accuracy					$\pm 2$	$\pm 4$	LSB	
Differential Nonlinearity						$\pm 0.5$	LSB	
AD5623R								
Resolution				12			Bits	Guaranteed monotonic by design
Relative Accuracy		$\pm 1$	$\pm 2$		$\pm 0.5$	$\pm 1$	LSB	
Differential Nonlinearity			$\pm 1$			$\pm 0.25$	LSB	
Zero-Scale Error		+2	+10		+2	+10	mV	All 0s loaded to DAC register
Offset Error		$\pm 1$	$\pm 10$		$\pm 1$	$\pm 10$	mV	
Full-Scale Error		-0.1	$\pm 1$		-0.1	$\pm 1$	% of FSR	All 1s loaded to DAC register
Gain Error			$\pm 1.5$			$\pm 1.5$	% of FSR	
Zero-Scale Error Drift		$\pm 2$			$\pm 2$		$\mu\text{V}/^\circ\text{C}$	
Gain Temperature Coefficient		$\pm 2.5$			$\pm 2.5$		ppm	Of FSR/ $^\circ\text{C}$
DC Power Supply Rejection Ratio		-100			-100		dB	DAC code = midscale; $V_{DD} = 5\text{ V} \pm 10\%$
DC Crosstalk (External Reference)								
		10			10		$\mu\text{V}$	Due to full-scale output change; $R_L = 2\text{ k}\Omega$ to GND or $V_{DD}$
		10			10		$\mu\text{V}/\text{mA}$	Due to load current change
		5			5		$\mu\text{V}$	Due to powering down (per channel)
DC Crosstalk (Internal Reference)								
		25			25		$\mu\text{V}$	Due to full-scale output change; $R_L = 2\text{ k}\Omega$ to GND or $V_{DD}$
		20			20		$\mu\text{V}/\text{mA}$	Due to load current change
		10			10		$\mu\text{V}$	Due to powering down (per channel)
OUTPUT CHARACTERISTICS <sup>3</sup>								
Output Voltage Range	0		$V_{DD}$	0		$V_{DD}$	V	
Capacitive Load Stability								
		2			2		nF	$R_L = \infty$
		10			10		nF	$R_L = 2\text{ k}\Omega$
DC Output Impedance		0.5			0.5		$\Omega$	
Short-Circuit Current		30			30		mA	$V_{DD} = 5\text{ V}$
Power-Up Time		4			4		$\mu\text{s}$	Coming out of power-down mode; $V_{DD} = 5\text{ V}$
REFERENCE INPUTS								
Reference Current		170	200		170	200	$\mu\text{A}$	$V_{REF} = V_{DD} = 5.5\text{ V}$
Reference Input Range	0.75		$V_{DD}$	0.75		$V_{DD}$	V	
Reference Input Impedance		26			26		k $\Omega$	

Parameter	A Grade <sup>1</sup>			B Grade <sup>1</sup>			Unit	Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
REFERENCE OUTPUT								
Output Voltage	2.495		2.505	2.495		2.505	V	At ambient
Reference Temperature Coefficient <sup>3</sup>		±10			±5	±10	ppm/°C	MSOP package models
		±10			±10		ppm/°C	LFCSP package models
Output Impedance		7.5			7.5		kΩ	
LOGIC INPUTS <sup>3</sup>								
Input Current			±2			±2	μA	All digital inputs
Input Low Voltage (V <sub>INL</sub> )			0.8			0.8	V	V <sub>DD</sub> = 5 V
Input High Voltage (V <sub>INH</sub> )	2			2			V	V <sub>DD</sub> = 5 V
Pin Capacitance		3			3		pF	DIN, SCLK, and SYNC
		19			19		pF	LDAC and CLR
POWER REQUIREMENTS								
V <sub>DD</sub>	4.5		5.5	4.5		5.5	V	
I <sub>DD</sub> (Normal Mode) <sup>4</sup>								V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND
V <sub>DD</sub> = 4.5 V to 5.5 V		0.25	0.45		0.25	0.45	mA	Internal reference off
V <sub>DD</sub> = 4.5 V to 5.5 V		0.8	1		0.8	1	mA	Internal reference on
I <sub>DD</sub> (All Power-Down Modes) <sup>5</sup>								
V <sub>DD</sub> = 4.5 V to 5.5 V		0.48	1		0.48	1	μA	V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND

<sup>1</sup> Temperature range: A, B grade = -40°C to +105°C.

<sup>2</sup> Linearity calculated using a reduced code range: [AD5663R](#) (Code 512 to Code 65,024), [AD5643R](#) (Code 128 to Code 16,256), and [AD5623R](#) (Code 32 to Code 4064). Output unloaded.

<sup>3</sup> Guaranteed by design and characterization, not production tested.

<sup>4</sup> Interface inactive. All DACs active. DAC outputs unloaded.

<sup>5</sup> Both DACs powered down.

## AD5623R-3/AD5643R-3/AD5663R-3

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ;  $R_L = 2\text{ k}\Omega\text{ to GND}$ ;  $C_L = 200\text{ pF to GND}$ ;  $V_{REFIN} = V_{DD}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 3.

Parameter	B Grade <sup>1</sup>			Unit	Conditions/Comments
	Min	Typ	Max		
STATIC PERFORMANCE <sup>2</sup>					
AD5663R					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5643R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5623R					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Scale Error		+2	+10	mV	All 0s loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		-0.1	±1	% of FSR	All 1s loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Scale Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		-100		dB	DAC code = midscale; $V_{DD} = 3\text{ V} \pm 10\%$
DC Crosstalk (External Reference)		10		μV	Due to full-scale output change; $R_L = 2\text{ k}\Omega\text{ to GND or }V_{DD}$
		10		μV/mA	Due to load current change
		5		μV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		μV	Due to full-scale output change; $R_L = 2\text{ k}\Omega\text{ to GND or }V_{DD}$
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS <sup>3</sup>					
Output Voltage Range	0		$V_{DD}$	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	$R_L = 2\text{ k}\Omega$
DC Output Impedance		0.5		Ω	
Short Circuit Current		30		mA	$V_{DD} = 3\text{ V}$
Power-Up Time		4		μs	Coming out of power-down mode; $V_{DD} = 3\text{ V}$
REFERENCE INPUTS					
Reference Current		170	200	μA	$V_{REF} = V_{DD} = 3.6\text{ V}$
Reference Input Range	0.75		$V_{DD}$	V	
Reference Input Impedance		26		kΩ	
REFERENCE OUTPUT					
Output Voltage	1.247		1.253	V	At ambient
Reference Temperature Coefficient <sup>3</sup>		±5	±15	ppm/°C	MSOP package models
		±10		ppm/°C	LFCSP package models
Output Impedance		7.5		kΩ	

Parameter	B Grade <sup>1</sup>			Unit	Conditions/Comments
	Min	Typ	Max		
LOGIC INPUTS <sup>3</sup>					
Input Current			±2	μA	All digital inputs
V <sub>INL</sub> , Input Low Voltage			0.8	V	V <sub>DD</sub> = 3 V
V <sub>INH</sub> , Input High Voltage	2			V	V <sub>DD</sub> = 3 V
Pin Capacitance		3		pF	DIN, SCLK, and $\overline{\text{SYNC}}$
		19		pF	$\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$
POWER REQUIREMENTS					
V <sub>DD</sub>	2.7		3.6	V	
I <sub>DD</sub> (Normal Mode) <sup>4</sup>					V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND
V <sub>DD</sub> = 2.7 V to 3.6 V		200	425	μA	Internal reference off
V <sub>DD</sub> = 2.7 V to 3.6 V		800	900	μA	Internal reference on
I <sub>DD</sub> (All Power-Down Modes) <sup>5</sup>					
V <sub>DD</sub> = 2.7 V to 3.6 V		0.2	1	μA	V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND

<sup>1</sup> Temperature range: B grade = -40°C to +105°C.

<sup>2</sup> Linearity calculated using a reduced code range: AD5663R (Code 512 to Code 65,024), AD5643R (Code 128 to Code 16,256), and AD5623R (Code 32 to Code 4064). Output unloaded.

<sup>3</sup> Guaranteed by design and characterization, not production tested.

<sup>4</sup> Interface inactive. All DACs active. DAC outputs unloaded.

<sup>5</sup> Both DACs powered down.

## AC CHARACTERISTICS

V<sub>DD</sub> = 2.7 V to 5.5 V; R<sub>L</sub> = 2 kΩ to GND; C<sub>L</sub> = 200 pF to GND; V<sub>REFIN</sub> = V<sub>DD</sub>; all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 4.

Parameter <sup>1,2</sup>	Min	Typ	Max	Unit	Conditions/Comments <sup>3</sup>
Output Voltage Settling Time					
AD5623R		3	4.5	μs	¼ to ¾ scale settling to ±0.5 LSB
AD5643R		3.5	5	μs	¼ to ¾ scale settling to ±0.5 LSB
AD5663R		4	7	μs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/μs	
Digital-to-Analog Glitch Impulse		10		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.1		nV-sec	
Reference Feedthrough		-90		dB	V <sub>REF</sub> = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	External reference
		4		nV-sec	Internal reference
DAC-to-DAC Crosstalk		1		nV-sec	External reference
		4		nV-sec	Internal reference
Multiplying Bandwidth		340		kHz	V <sub>REF</sub> = 2 V ± 0.1 V p-p
Total Harmonic Distortion		-80		dB	V <sub>REF</sub> = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		μV p-p	0.1 Hz to 10 Hz

<sup>1</sup> Guaranteed by design and characterization, not production tested.

<sup>2</sup> See the Terminology section.

<sup>3</sup> Temperature range: A, B grade = -40°C to +105°C, typical at +25°C.

**TIMING CHARACTERISTICS**

All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .  $V_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

Table 5.

Parameter	Limit at $T_{MIN}, T_{MAX}$ $V_{DD} = 2.7 \text{ V}$ to $5.5 \text{ V}$	Unit	Conditions/Comments
$t_1^2$	20	ns min	SCLK cycle time
$t_2$	9	ns min	SCLK high time
$t_3$	9	ns min	SCLK low time
$t_4$	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
$t_5$	5	ns min	Data setup time
$t_6$	5	ns min	Data hold time
$t_7$	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
$t_8$	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
$t_9$	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
$t_{10}$	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore
$t_{11}$	10	ns min	$\overline{\text{LDAC}}$ pulse width low
$t_{12}$	15	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ rising edge
$t_{13}$	5	ns min	$\overline{\text{CLR}}$ pulse width low
$t_{14}$	0	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge
$t_{15}$	300	ns max	$\overline{\text{CLR}}$ pulse activation time

<sup>1</sup> Guaranteed by design and characterization, not production tested.

<sup>2</sup> Maximum SCLK frequency is 50 MHz at  $V_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ .

**TIMING DIAGRAM**

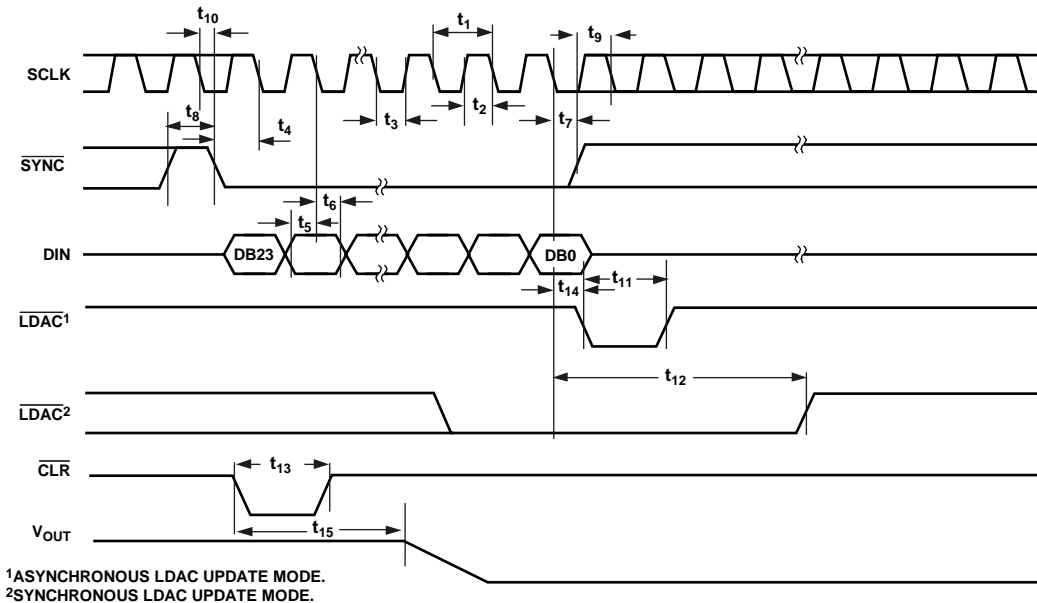


Figure 2. Serial Write Operation

05885E-002

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 6.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_{OUT}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
$V_{REFIN}/V_{REFOUT}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Digital Input Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_J$ max)	150°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
LFCSP Package (4-Layer Board)	
$\theta_{JA}$ Thermal Impedance	61°C/W
MSOP Package (4-Layer Board)	
$\theta_{JA}$ Thermal Impedance	142°C/W
$\theta_{JC}$ Thermal Impedance	43.7°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260(+0/-5)°C

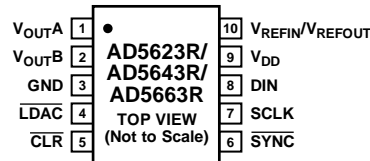
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. EXPOSED PAD TIED TO GND ON LFCSP PACKAGE.

05859-003

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>OUTA</sub>	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	V <sub>OUTB</sub>	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
3	GND	Ground. Reference point for all circuitry on the part.
4	LDAC	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
5	CLR	Asynchronous Clear Input. The CLR input is falling edge sensitive. While CLR is low, all LDAC pulses are ignored. When CLR is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the 24th falling edge of the next write to the part. If CLR is activated during a write sequence, the write is aborted.
6	SYNC	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless SYNC is taken high before this edge, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
8	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
9	V <sub>DD</sub>	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
10	V <sub>REFIN</sub> /V <sub>REFOUT</sub>	Common Reference Input/Reference Output. When the internal reference is selected, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is a reference input.

TYPICAL PERFORMANCE CHARACTERISTICS

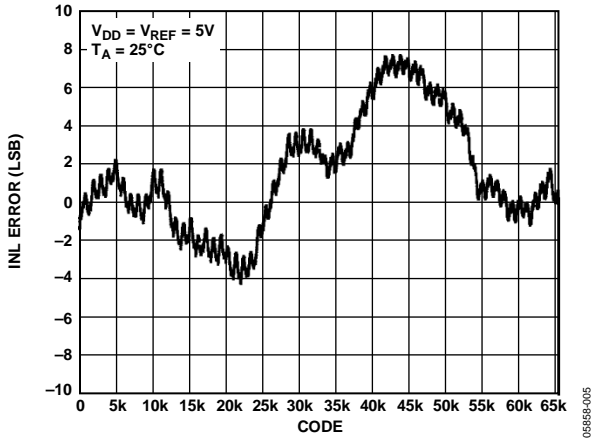


Figure 4. INL—AD5663R, External Reference

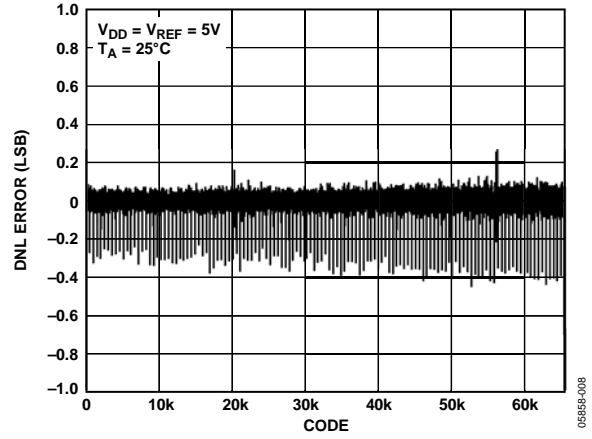


Figure 7. DNL—AD5663R, External Reference

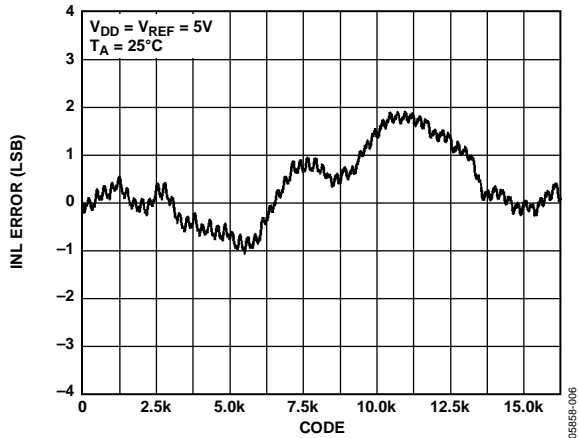


Figure 5. INL—AD5643R, External Reference

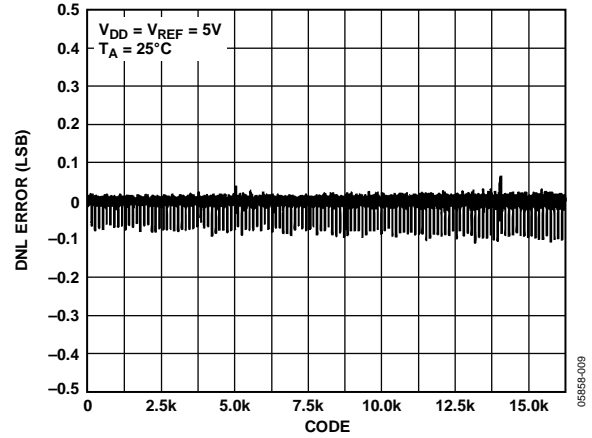


Figure 8. DNL—AD5643R, External Reference

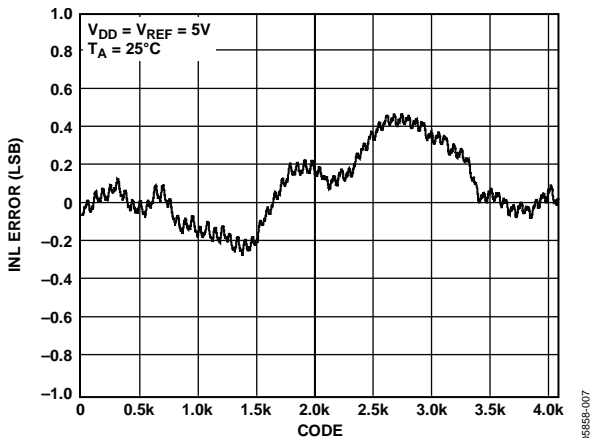


Figure 6. INL—AD5623R, External Reference

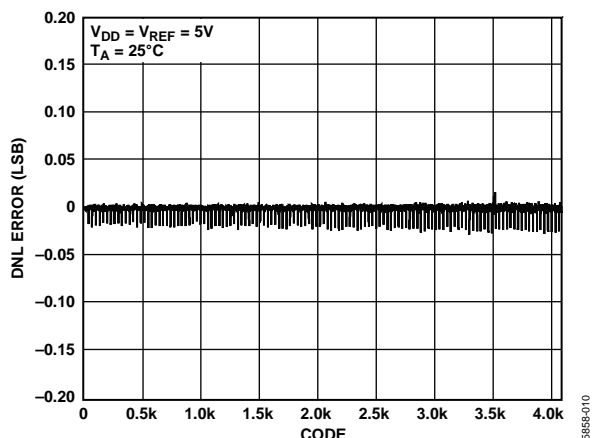


Figure 9. DNL—AD5623R, External Reference

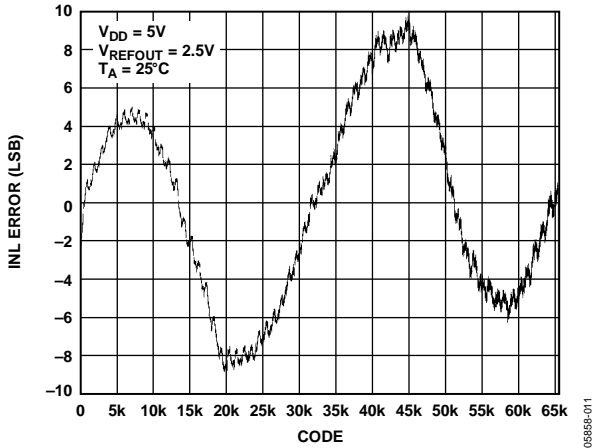


Figure 10. INL—AD5663R-5

05858-011

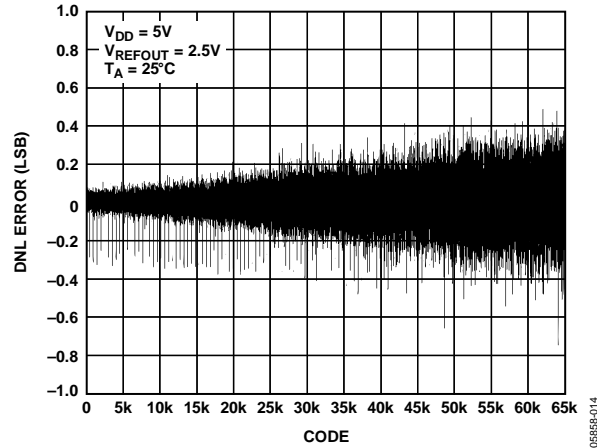


Figure 13. DNL—AD5663R-5

05858-014

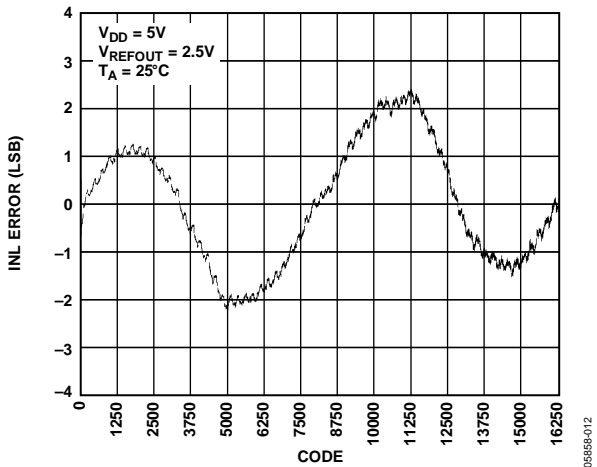


Figure 11. INL—AD5643R-5

05858-012

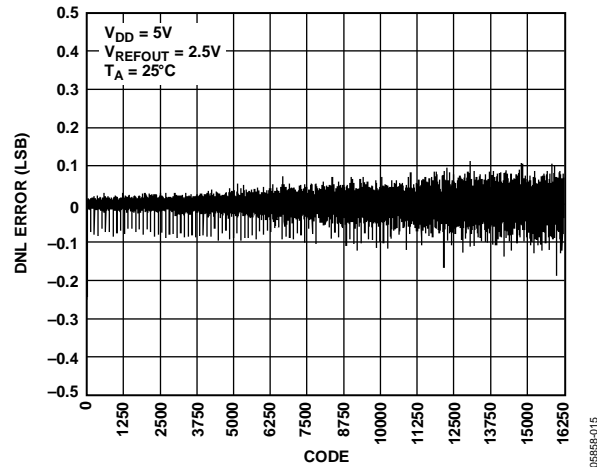


Figure 14. DNL—AD5643R-5

05858-015

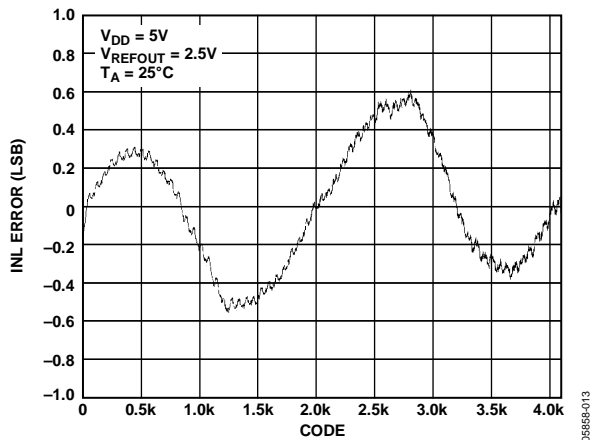


Figure 12. INL—AD5623R-5

05858-013

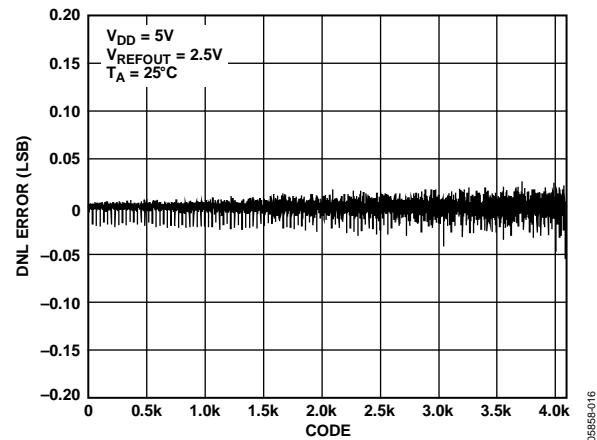


Figure 15. DNL—AD5623R-5

05858-016

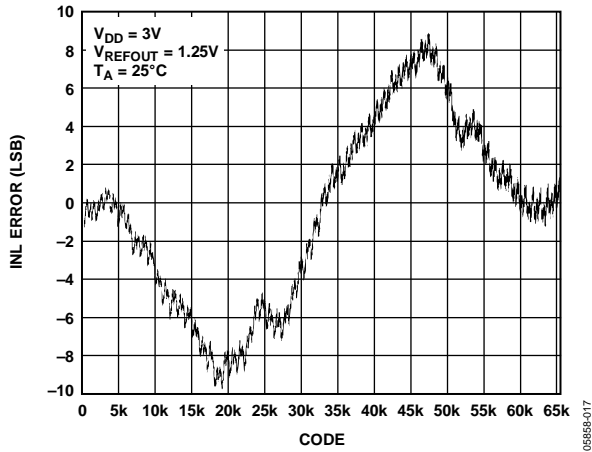


Figure 16. INL—AD5663R-3

05858-017

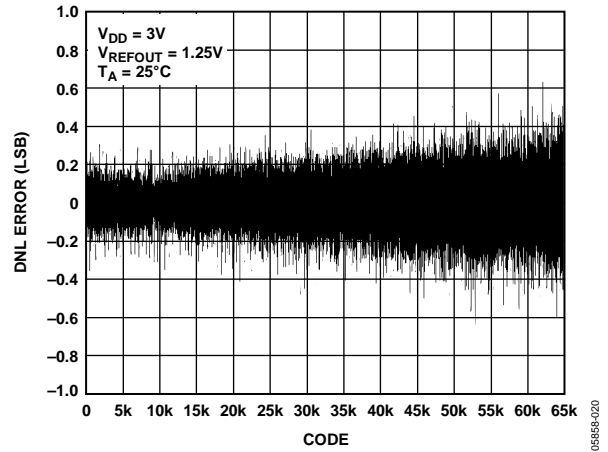


Figure 19. DNL—AD5663R-3

05858-020

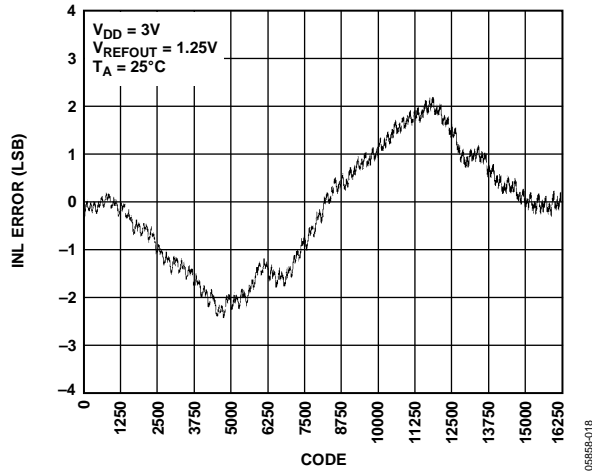


Figure 17. INL—AD5643R-3

05858-018

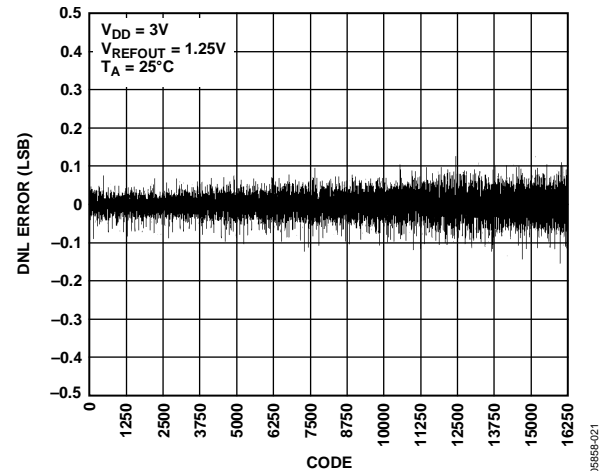


Figure 20. DNL—AD5643R-3

05858-021

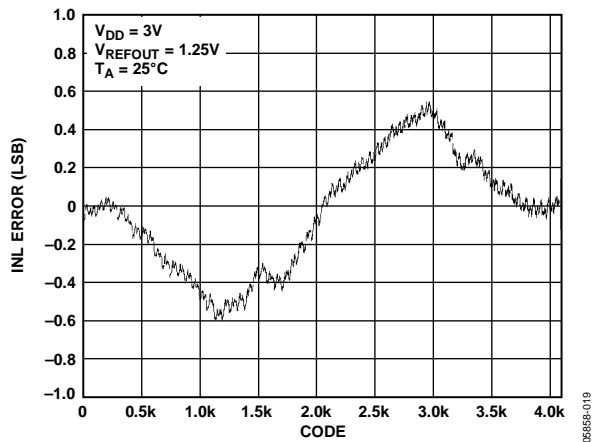


Figure 18. INL—AD5623R-3

05858-019

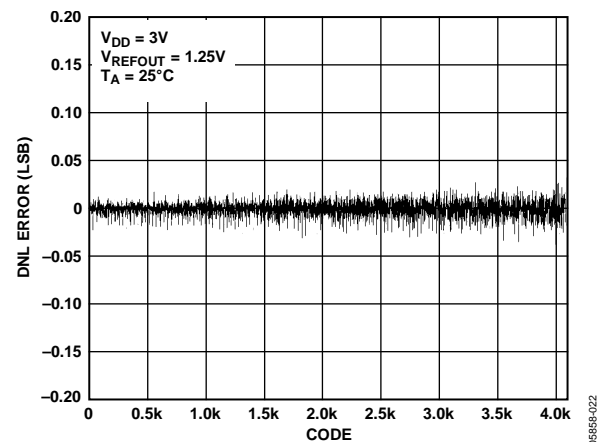


Figure 21. DNL—AD5623R-3

05858-022

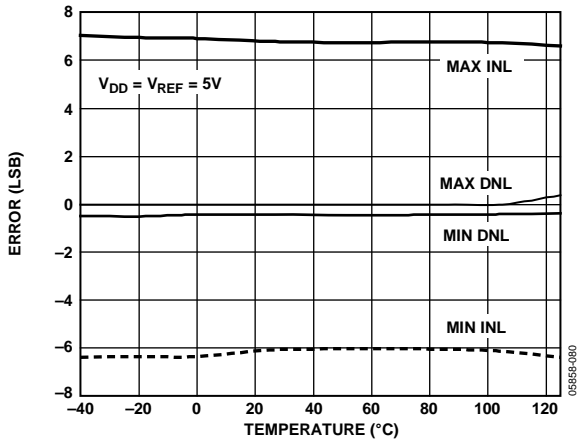


Figure 22. INL Error and DNL Error vs. Temperature

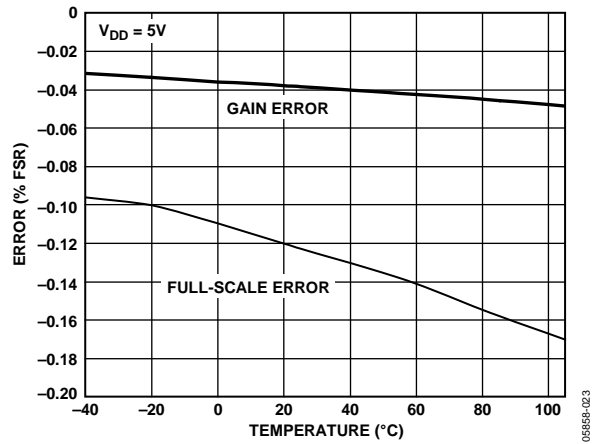


Figure 25. Gain Error and Full-Scale Error vs. Temperature

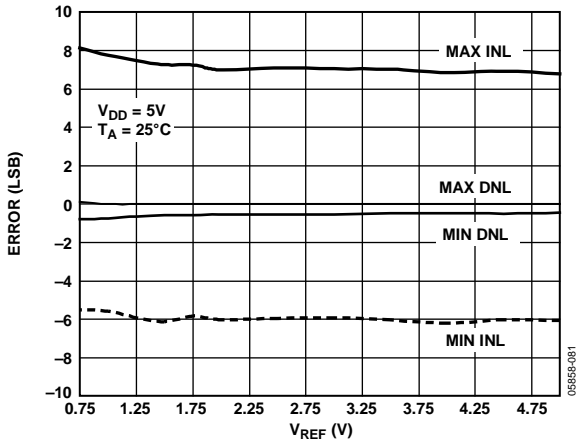


Figure 23. INL Error and DNL Error vs.  $V_{REF}$

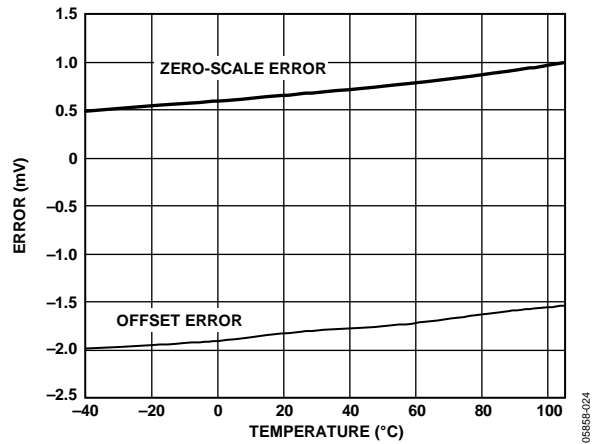


Figure 26. Zero-Scale Error and Offset Error vs. Temperature

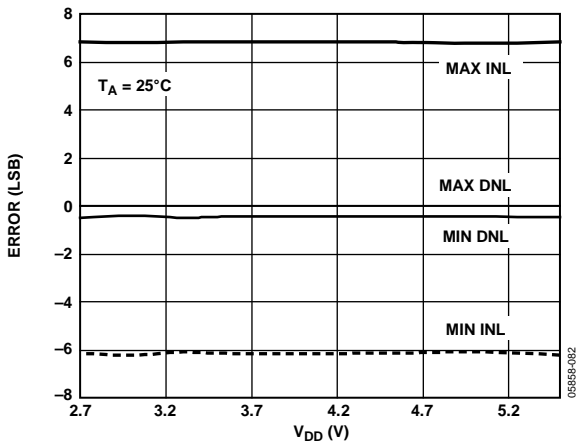


Figure 24. INL Error and DNL Error vs. Supply

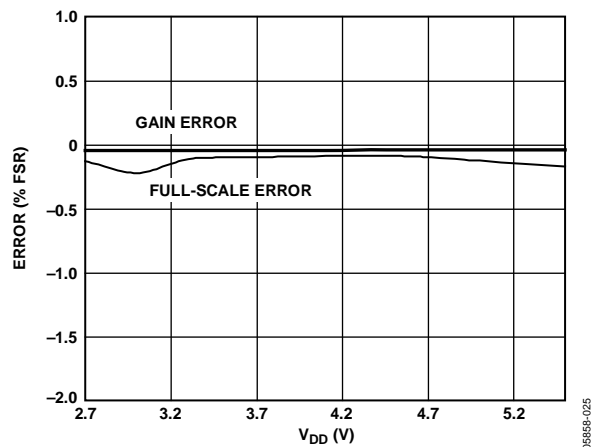


Figure 27. Gain Error and Full-Scale Error vs. Supply

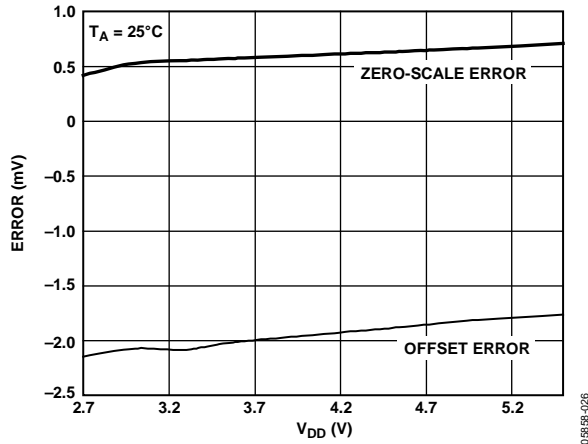


Figure 28. Zero-Scale Error and Offset Error vs. Supply

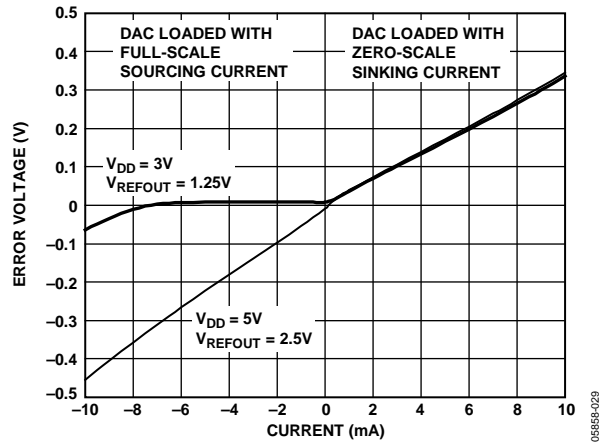


Figure 31. Headroom at Rails vs. Source and Sink

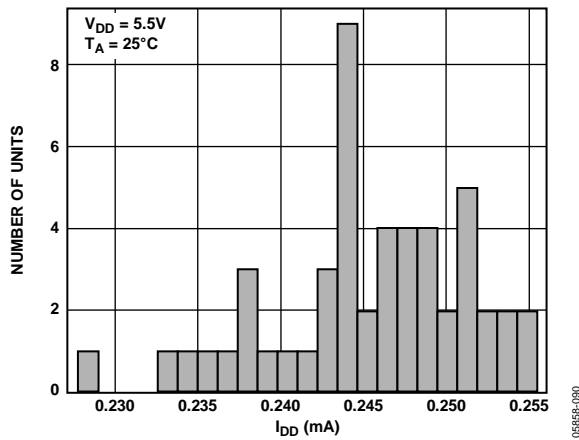


Figure 29.  $I_{DD}$  Histogram with External Reference

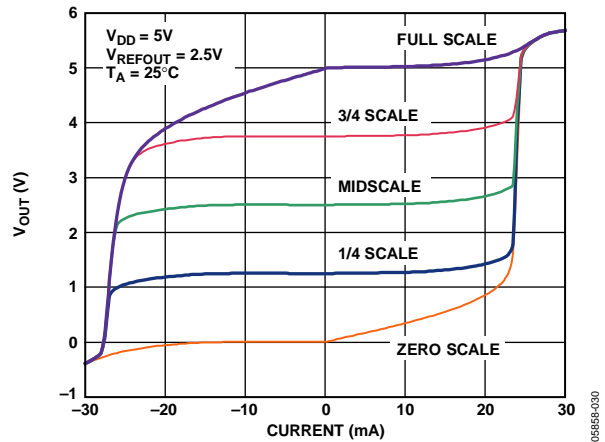


Figure 32. AD5623R-5/AD5643R-5/AD5663R-5 Source and Sink Capability

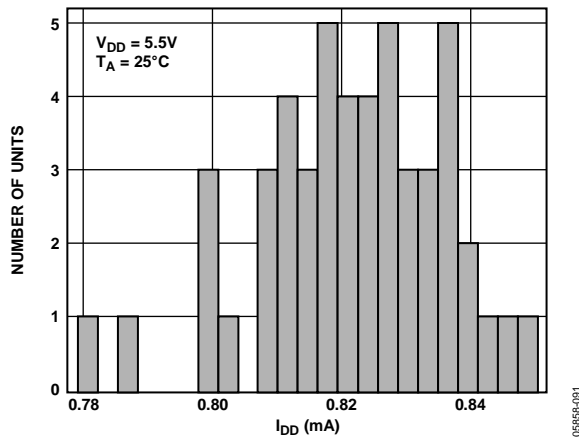


Figure 30.  $I_{DD}$  Histogram with Internal Reference

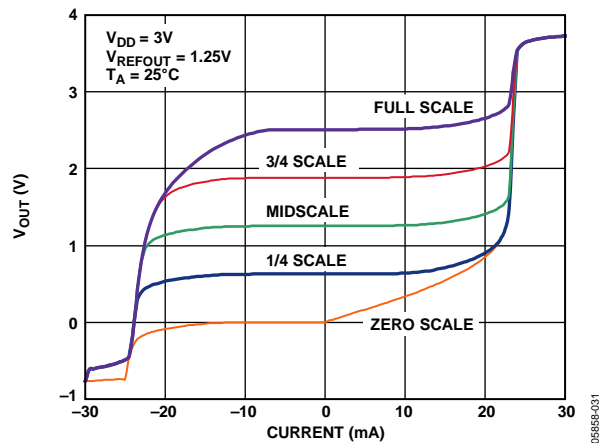


Figure 33. AD5623R-3/AD5643R-3/AD5663R-3 Source and Sink Capability

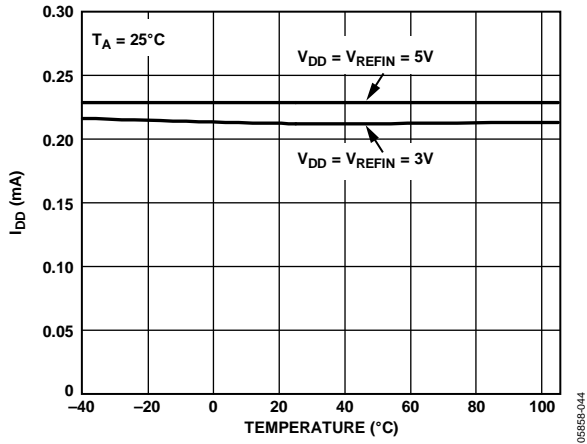


Figure 34. Supply Current vs. Temperature

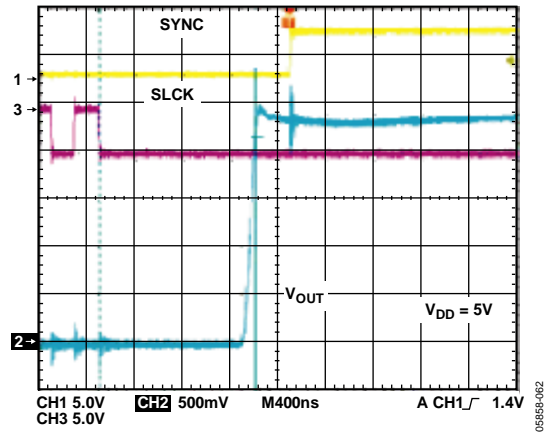


Figure 37. Exiting Power-Down to Midscale

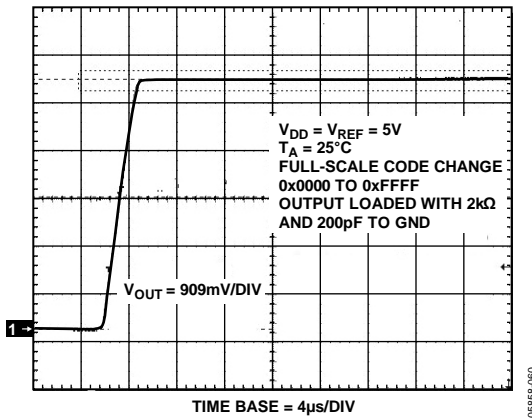


Figure 35. Full-Scale Settling Time, 5 V

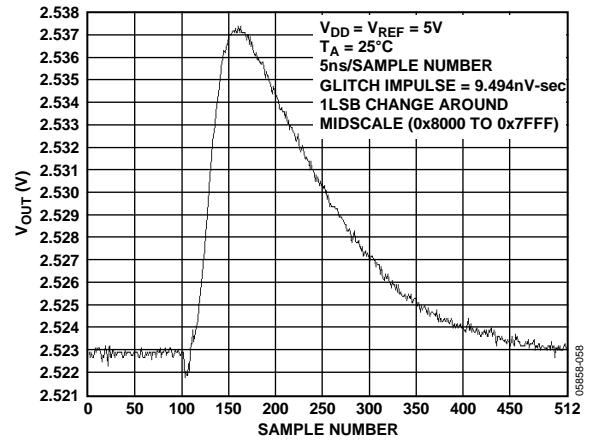


Figure 38. Digital-to-Analog Glitch Impulse (Negative)

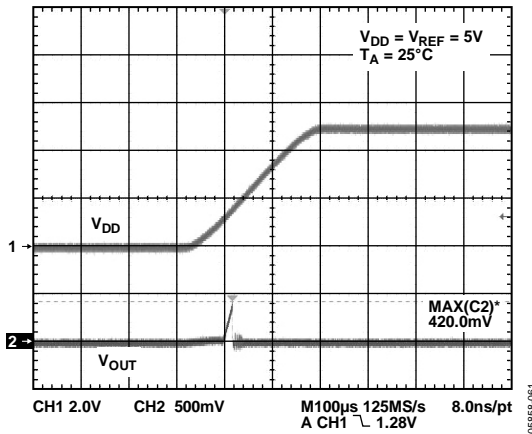


Figure 36. Power-On Reset to 0 V

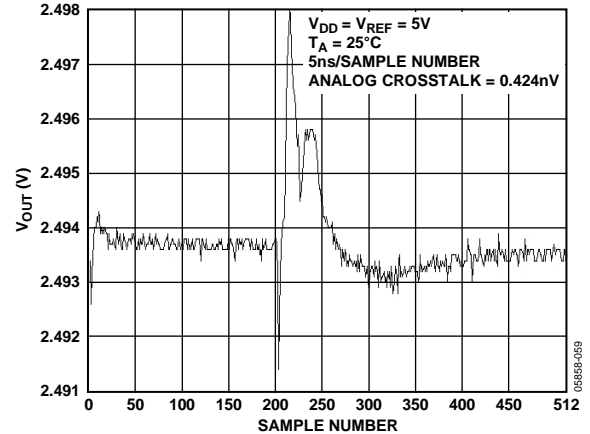


Figure 39. Analog Crosstalk, External Reference

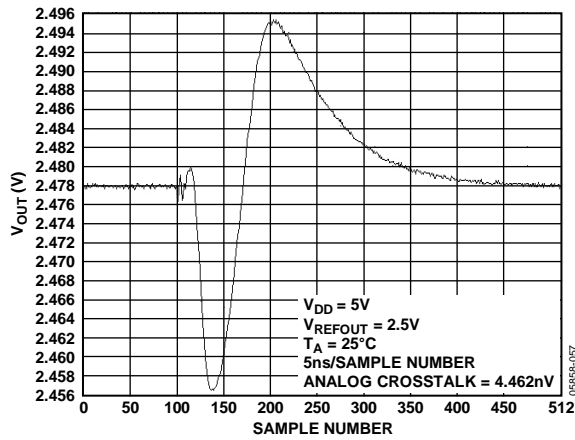


Figure 40. Analog Crosstalk, Internal Reference

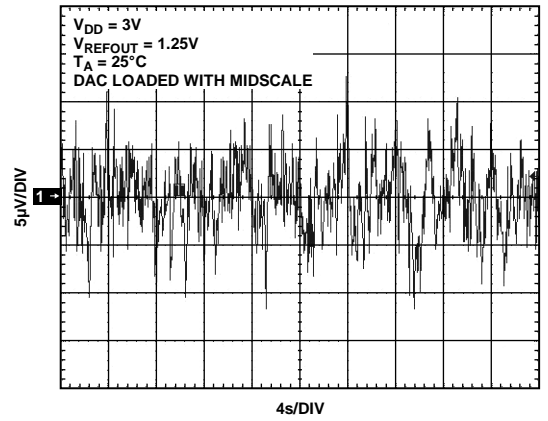


Figure 43. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

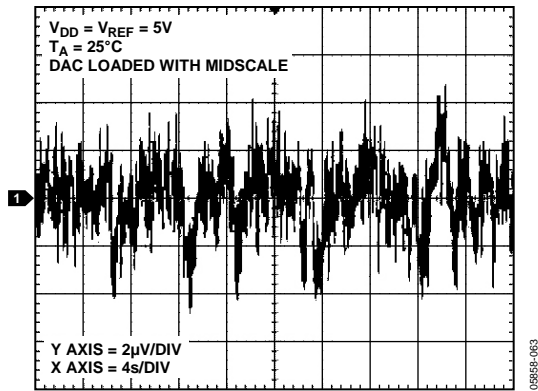


Figure 41. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

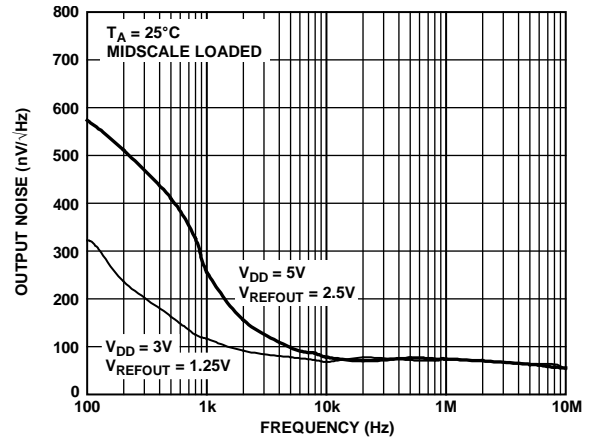


Figure 44. Noise Spectral Density, Internal Reference

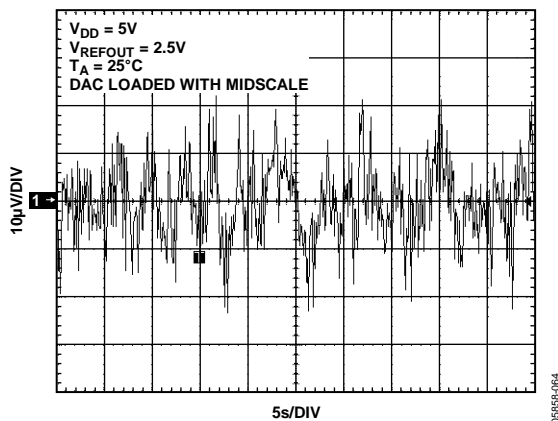


Figure 42. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

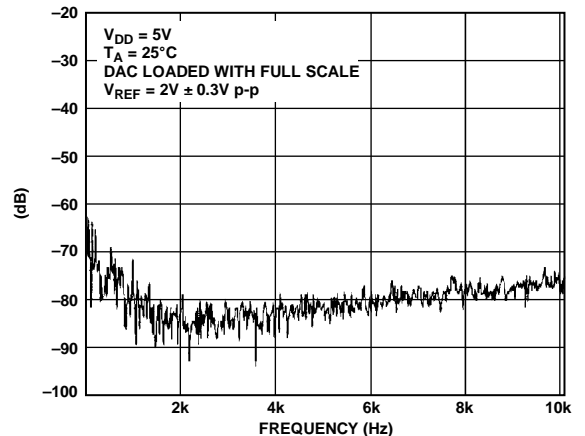


Figure 45. Total Harmonic Distortion

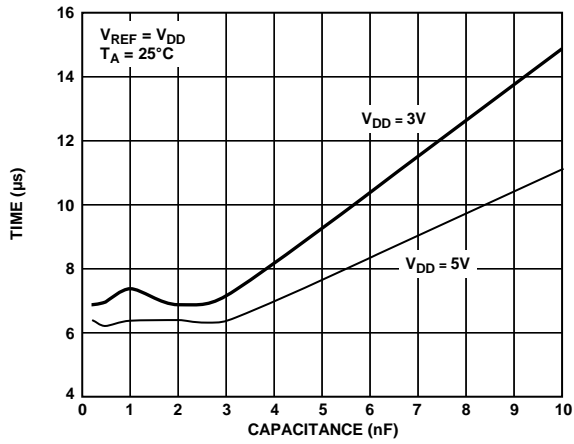


Figure 46. Settling Time vs. Capacitive Load

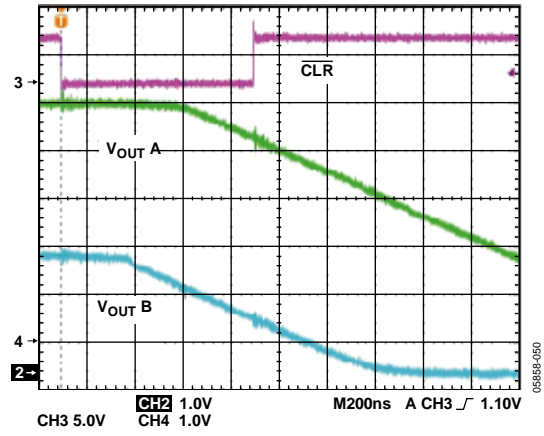


Figure 48. CLR Pulse Activation Time

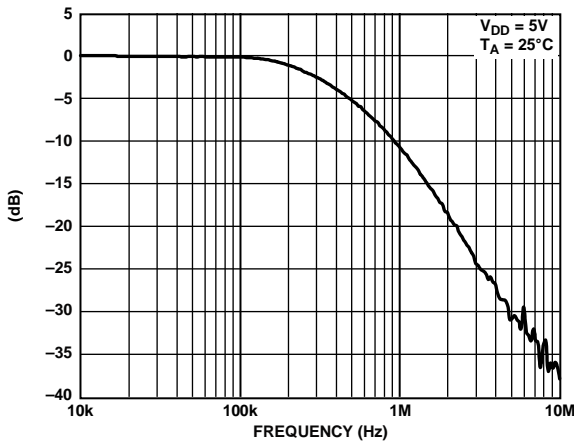


Figure 47. Multiplying Bandwidth

06859-089

06859-050

06859-089

## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 5.

### Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 9.

### Zero-Scale Error

Zero-scale error is the measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-scale error is always positive in the [AD5623R/AD5643R/AD5663R](#) because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-scale error is expressed in mV. A plot of zero-scale error vs. temperature is shown in Figure 26.

### Full-Scale Error

Full-scale error is the measurement of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be  $V_{DD} - 1$  LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature is shown in Figure 25.

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range.

### Zero-Scale Error Drift

Zero-scale error drift is the measurement of the change in zero-scale error with a change in temperature. It is expressed in microvolts/ $^{\circ}\text{C}$  ( $\mu\text{V}/^{\circ}\text{C}$ ).

### Gain Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/ $^{\circ}\text{C}$ .

### Offset Error

Offset error is a measure of the difference between  $V_{\text{OUT}}$  (actual) and  $V_{\text{OUT}}$  (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the [AD5623R/AD5643R/AD5663R](#) with code 512 loaded in the DAC register. It can be negative or positive.

### DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in  $V_{\text{OUT}}$  to a change in  $V_{\text{DD}}$  for full-scale output of the DAC. It is measured in dB.  $V_{\text{REF}}$  is held at 2 V, and  $V_{\text{DD}}$  is varied by  $\pm 10\%$ .

### Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a 1/4 to 3/4 full-scale input change and is measured from the 24th falling edge of SCLK.

### Digital-to-Analog Glitch Impulse

The impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 38.

### Digital Feedthrough

A measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, digital feedthrough is measured when the DAC output is not updated. It is specified in nV-sec, and it is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

### Reference Feedthrough

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is,  $\overline{\text{LDAC}}$  is high). It is expressed in decibels (dB).

### Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density ( $\text{nV}/\sqrt{\text{Hz}}$ ). It is measured by loading the DAC to midscale and measuring noise at the output. A plot of noise spectral density is shown in Figure 44.

### DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts ( $\mu\text{V}$ ).

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts/milliamperes ( $\mu\text{V}/\text{mA}$ ).

**Digital Crosstalk**

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nanovolts-second (nV-sec).

**Analog Crosstalk**

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping LDAC high. Then pulse LDAC low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nanovolts-second (nV-sec).

**DAC-to-DAC Crosstalk**

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with LDAC low and monitoring the output of another DAC. The energy of the glitch is expressed in nanovolts-second (nV-sec).

**Multiplying Bandwidth**

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

**Total Harmonic Distortion (THD)**

Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in decibels (dB).

## THEORY OF OPERATION

### DIGITAL-TO-ANALOG SECTION

The AD5623R/AD5643R/AD5663R DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 49 shows a block diagram of the DAC architecture.

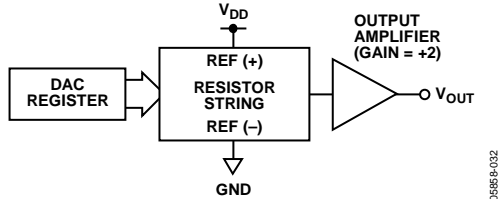


Figure 49. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left( \frac{D}{2^N} \right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left( \frac{D}{2^N} \right)$$

where:

$D$  is the decimal equivalent of the binary code that is loaded to the DAC register:

- 0 to 4095 for AD5623R (12-bit)
- 0 to 16,383 for AD5643R (14-bit)
- 0 to 65,535 for AD5663R (16-bit)

$N$  is the DAC resolution.

### RESISTOR STRING

The resistor string section is shown in Figure 50. It is simply a string of resistors, each of Value  $R$ . The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

### OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to  $V_{DD}$ . It can drive a load of 2 k $\Omega$  in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 31. The slew rate is 1.8 V/ $\mu$ s with a 1/4 to 3/4 full-scale settling time of 10  $\mu$ s.

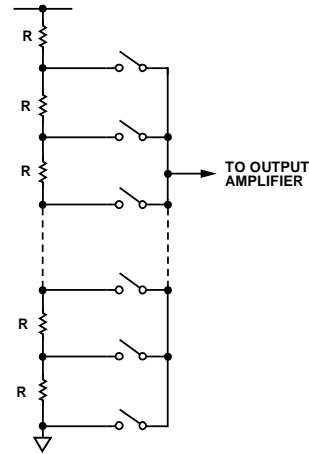


Figure 50. Resistor String

### INTERNAL REFERENCE

The AD5623R/AD5643R/AD5663R on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

The AD5623R-3/AD5643R-3/AD5663R-3 has a 1.25 V, 5 ppm/ $^{\circ}$ C reference, giving a full-scale output of 2.5 V. The AD5623R-5/AD5643R-5/AD5663R-5 has a 2.5 V, 5 ppm/ $^{\circ}$ C reference, giving a full-scale output of 5 V. The internal reference associated with each part is available at the  $V_{REFOUT}$  pin. A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between reference output and GND for reference stability.

### EXTERNAL REFERENCE

The  $V_{REFIN}$  pins on the AD5623R-3/AD5643R-3/AD5663R-3 and the AD5623R-5/AD5643R-5/AD5663R-5 allows the use of an external reference if the application requires it. The on-chip reference is off at power-up, and this is the default condition. The AD5623R-3/AD5643R-3/AD5663R-3 and the AD5623R-5/AD5643R-5/AD5663R-5 can be operated from a single 2.7 V to 5.5 V supply.

### SERIAL INTERFACE

The AD5623R/AD5643R/AD5663R have a 3-wire serial interface ( $\overline{SYNC}$ , SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as with most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the  $\overline{SYNC}$  line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5623R/AD5643R/AD5663R compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, for example, a change in DAC register contents and/or a change in the mode of operation.

At this stage, the SYNC line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence, so that a falling edge of SYNC can initiate the next write sequence.

Because the SYNC buffer draws more current when  $V_{IN} = 2 V$  than it does when  $V_{IN} = 0.8 V$ , SYNC should be idled low between write sequences for even lower power operation. As mentioned previously, it must, however, be brought high again just before the next write sequence.

**INPUT SHIFT REGISTER**

The input shift register is 24 bits wide (see Figure 52). The first two bits are don't cares. The next three are Command Bit C2 to Command Bit C0 (see Table 8), followed by the 3-bit DAC Address A2 to DAC Address A0 (see Table 9), and, finally, the 16-, 14-, and 12-bit data-word.

The data-word comprises the 16-, 14-, and 12-bit input codes, followed by zero, two, or four don't care bits, for the AD5663R, AD5643R, and AD5623R, respectively (see Figure 51, Figure 52, and Figure 53). The data bits are transferred to the DAC register on the 24th falling edge of SCLK.

**Table 8. Command Definition**

C2	C1	C0	Command
0	0	0	Write to Input Register <i>n</i>
0	0	1	Update DAC Register <i>n</i>
0	1	0	Write to Input Register <i>n</i> , update all (software LDAC)
0	1	1	Write to and update DAC Channel <i>n</i>
1	0	0	Power down DAC (power up)
1	0	1	Reset
1	1	0	LDAC register setup
1	1	1	Internal reference setup (on/off)

**Table 9. Address Command**

A2	A1	A0	ADDRESS (n)
0	0	0	DAC A
0	0	1	DAC B
0	1	0	Reserved
0	1	1	Reserved
1	1	1	All DACs

**SYNC INTERRUPT**

In a normal write sequence, the SYNC line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if SYNC is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 54).



Figure 51. AD5663R Input Shift Register Contents

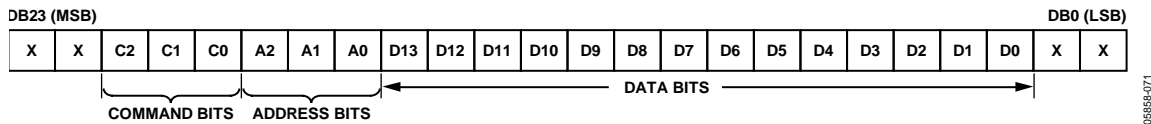


Figure 52. AD5643R Input Shift Register Contents

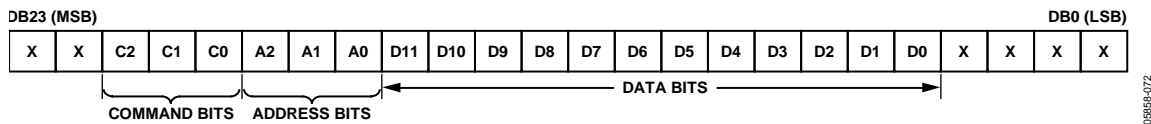


Figure 53. AD5623R Input Shift Register Contents

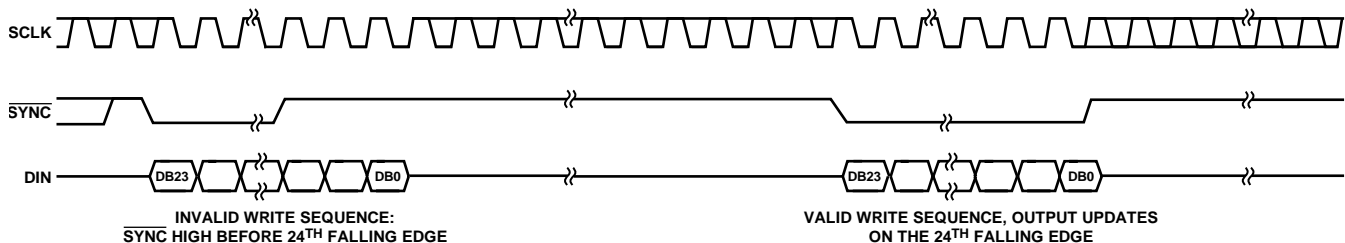


Figure 54. SYNC Interrupt Facility

**POWER-ON RESET**

The AD5623R/AD5643R/AD5663R contain a power-on reset circuit that controls the output voltage during power-up. The AD5623R/AD5643R/AD5663R DACs output power up to 0 V, and the output remains there until a valid write sequence is made to the DACs. This is useful in applications where it is important to know the state of the output of the DACs while they are in the process of powering up. Any events on  $\overline{\text{LDAC}}$  or  $\overline{\text{CLR}}$  during power-on reset are ignored.

**SOFTWARE RESET**

The AD5623R/AD5643R/AD5663R contain a software reset function. Command 101 is reserved for the software reset function (see Table 8). The software reset command contains two reset modes that are software-programmable by setting bit DB0 in the control register. Table 10 shows how the state of the bit corresponds to the mode of operation of the device. Table 12 shows the contents of the input shift register during the software reset mode of operation.

**Table 10. Software Reset Modes**

DB0	Registers Reset to Zero
0	DAC register Input register
1 (Power-on Reset)	DAC register Input register $\overline{\text{LDAC}}$ register Power-down register Internal reference setup register

After a full software reset (DB0 = 1), there must be a short time delay, approximately 5  $\mu\text{s}$ , to allow the reset to complete. During the reset, a low pulse can be observed on the  $\overline{\text{CLR}}$  line. If the next SPI transaction commences before the  $\overline{\text{CLR}}$  line returns high, that SPI transaction is ignored.

**POWER-DOWN MODES**

The AD5623R/AD5643R/AD5663R contain four separate modes of operation. Command 100 is reserved for the power-down function (see Table 8). These modes are software-programmable by setting Bit DB5 and Bit DB4 in the control register. Table 11 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC B and DAC A) can be powered down to the selected mode by setting the corresponding two bits (Bit DB1 and Bit DB0) to 1.

By executing the same Command 100, any combination of DACs can be powered up by setting Bit DB5 and Bit DB4 to normal operation mode.

Again, to select which combination of DAC channels to power up, set the corresponding bits (Bit DB1 and Bit DB0) to 1. See Table 13 for contents of the input shift register during power-down/power-up operation.

The DAC output powers up to the value in the input register while  $\overline{\text{LDAC}}$  is low. If  $\overline{\text{LDAC}}$  is high, the DAC output powers up to the value held in the DAC register before power-down.

**Table 11. Modes of Operation**

DB5	DB4	Operating Mode
0	0	Normal operation Power-down modes
0	1	1 k $\Omega$ to GND
1	0	100 k $\Omega$ to GND
1	1	Three-state

When both Bit DB1 and Bit DB2 are set to 0, the part works normally, with its normal power consumption of 250  $\mu\text{A}$  at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V (200 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 k $\Omega$  or 100 k $\Omega$  resistor or left open-circuited (three-state) (see Figure 55).

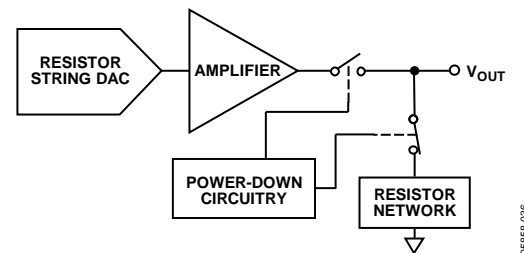


Figure 55. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4  $\mu\text{s}$  for both VDD = 5 V and VDD = 3 V (see Figure 37).

**Table 12. 24-Bit Input Shift Register Contents for Software Reset Command**

MSB								LSB
DB23 to DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0
x	1	0	1	X	X	X	X	1/0
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0)			Don't care	Determines software reset mode

Table 13. 24-Bit Input Shift Register Contents of Power Up/Down Function

MSB													LSB	
DB23 to DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB6	DB5	DB4	DB3	DB2	DB1	DB0	
x	1	0	0	X	X	X	X	PD1	PD0	X	X	DAC B	DAC A	
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0) Don't care			Don't care	Power-down mode		Don't care		Power down/Power up channel selection; set bit to 1 to select channel		

Table 14. 24-Bit Input Shift Register Contents for  $\overline{\text{LDAC}}$  Setup Command

MSB										LSB	
DB23 to DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB2	DB1	DB0		
x	1	1	0	X	X	X	X	DAC B	DAC A		
Don't care	Command bits (C2 to C0)			Address bits (A3 to A0) Don't care			Don't care	Set DAC to 0 or 1 for required mode of operation			

## LDAC FUNCTION

The AD5623R/AD5643R/AD5663R DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register, and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the  $\overline{\text{LDAC}}$  pin. When the  $\overline{\text{LDAC}}$  pin is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When  $\overline{\text{LDAC}}$  is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them. The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to one of the input registers individually and then, by bringing  $\overline{\text{LDAC}}$  low when writing to the other DAC input register, all outputs will update simultaneously.

These parts each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time  $\overline{\text{LDAC}}$  was brought low. Normally, when  $\overline{\text{LDAC}}$  is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5623R/AD5643R/AD5663R, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

The outputs of all DACs can be simultaneously updated, using the hardware  $\overline{\text{LDAC}}$  pin.

### Synchronous $\overline{\text{LDAC}}$

The DAC registers are updated after new data is read in on the falling edge of the 24th SCLK pulse.  $\overline{\text{LDAC}}$  can be permanently low or pulsed as shown in Figure 2.

### Asynchronous $\overline{\text{LDAC}}$

The outputs are not updated at the same time that the input registers are written to. When  $\overline{\text{LDAC}}$  goes low, the DAC registers are updated with the contents of the input register.

The  $\overline{\text{LDAC}}$  register gives the user full flexibility and control over the hardware  $\overline{\text{LDAC}}$  pin. This register allows the user to select which combination of channels to simultaneously update when the hardware  $\overline{\text{LDAC}}$  pin is executed. Setting the  $\overline{\text{LDAC}}$  bit register to 0 for a DAC channel means that the update of this channel is controlled by the  $\overline{\text{LDAC}}$  pin. If this bit is set to 1, this channel synchronously updates; that is, the DAC register is updated after new data is read in, regardless of the state of the  $\overline{\text{LDAC}}$  pin. It effectively sees the  $\overline{\text{LDAC}}$  pin as being pulled low. See Table 15 for the  $\overline{\text{LDAC}}$  register mode of operation. This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using Command 110 loads the 2-bit  $\overline{\text{LDAC}}$  register [DB1:DB0]. The default for each channel is 0; that is, the  $\overline{\text{LDAC}}$  pin works normally. Setting the bits to 1 means the DAC register is updated, regardless of the state of the  $\overline{\text{LDAC}}$  pin. See Table 14 for contents of the input shift register during the  $\overline{\text{LDAC}}$  register setup command.

Table 15.  $\overline{\text{LDAC}}$  Register Mode of Operation

LDAC Bits (DB1 to DB0)	$\overline{\text{LDAC}}$ Pin	$\overline{\text{LDAC}}$ Operation
0	1/0	Determined by $\overline{\text{LDAC}}$ pin
1	X = don't care	The DAC registers are updated after new data is read in on the falling edge of the 24th SCLK pulse.

**INTERNAL REFERENCE SETUP**

The on-chip reference is off at power-up by default. This reference can be turned on or off by setting a software programmable bit, DB0, in the control register. Table 16 shows how the state of the bit corresponds to the mode of operation. Command 111 is reserved for setting up the internal reference (see Table 8). See Table 16 for the contents of the input shift register during the internal reference setup command.

Table 16. Reference Setup Register

Internal Reference Setup Register (DB0)	Action
0	Reference off (default)
1	Reference on

Table 17. 32-Bit Input Shift Register Contents for Reference Setup Function

MSB								LSB
DB23 to DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0
X	1	1	1	X	X	X	X	1/0
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0)			Don't care	Reference setup register

## MICROPROCESSOR INTERFACING

### AD5623R/AD5643R/AD5663R to Blackfin® Microprocessors Interface

Figure 56 shows a serial interface between the AD5623R/AD5643R/AD5663R and a Blackfin microprocessor such as the ADSP-BF531. The ADSP-BF531 incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5623R/AD5643R/AD5663R, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5623R/AD5643R/AD5663R, while TSCLK0 drives the SCLK of the parts. The SYNC is driven from TFS0.

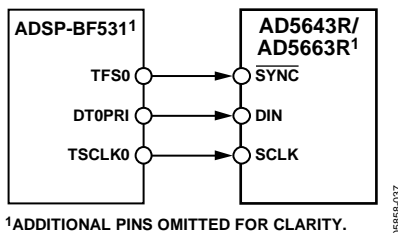


Figure 56. AD5623R/AD5643R/AD5663R to Blackfin ADSP-BF531 Interface

### AD5623R/AD5643R/AD5663R to 68HC11/68L11 Interface

Figure 57 shows a serial interface between the AD5623R/AD5643R/AD5663R and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5623R/AD5643R/AD5663R, and the MOSI output drives the serial data line of the DAC.

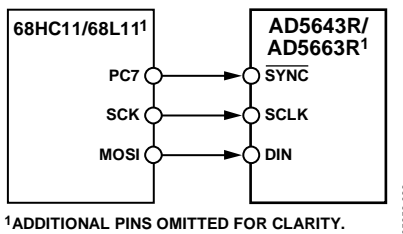


Figure 57. AD5623R/AD5643R/AD5663R to 68HC11/68L11 Interface

The SYNC signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 is configured with its CPOL bit as 0, and its CPHA bit as 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 is configured as described previously, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

Data is transmitted MSB first. To load data to the AD5623R/AD5643R/AD5663R, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

### AD5623R/AD5643R/AD5663R to 80C51/80L51 Interface

Figure 58 shows a serial interface between the AD5623R/AD5643R/AD5663R and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5623R/AD5643R/AD5663R, and RxD drives the serial data line of the part. The SYNC signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5623R/AD5643R/AD5663R, P3.3 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle.

The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5623R/AD5643R/AD5663R must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

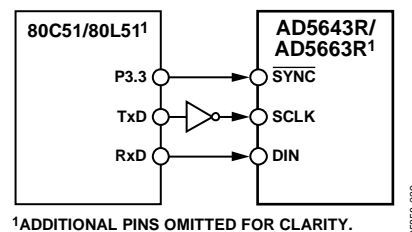


Figure 58. AD5623R/AD5643R/AD5663R to 80C51/80L51 Interface

### AD5623R/AD5643R/AD5663R to MICROWIRE Interface

Figure 59 shows an interface between the AD5623R/AD5643R/AD5663R and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5623R/AD5643R/AD5663R on the rising edge of the SK.

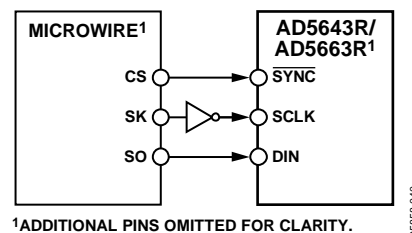


Figure 59. AD5623R/AD5643R/AD5663R to MICROWIRE Interface

## APPLICATIONS INFORMATION

### USING A REFERENCE AS A POWER SUPPLY

Because the supply current required by the [AD5623R/AD5643R/AD5663R](#) is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the parts (see Figure 60). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the [AD5623R/AD5643R/AD5663R](#). If the low dropout [REF195](#) is used, it must supply 500  $\mu$ A of current to the [AD5623R/AD5643R/AD5663R](#), with no load on the output of the DAC. When the DAC output is loaded, the [REF195](#) also needs to supply the current to the load. The total current required (with a 5 k $\Omega$  load on the DAC output) is

$$500 \mu\text{A} + (5 \text{ V} / 5 \text{ k}\Omega) = 1.5 \text{ mA}$$

The load regulation of the [REF195](#) is typically 2 ppm/mA, which results in a 3 ppm (15  $\mu$ V) error for the 1.5 mA current drawn from it. This corresponds to a 0.196 LSB error for the 16-bit [AD5663R](#).

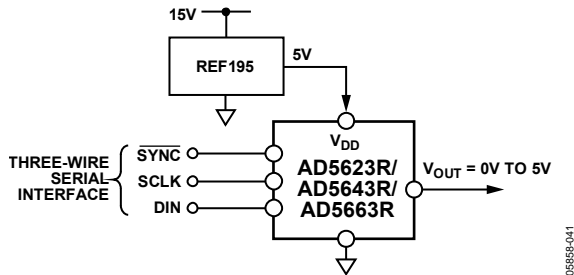


Figure 60. REF195 as Power Supply to the [AD5623R/AD5643R/AD5663R](#)

### BIPOLAR OPERATION USING THE AD5663R

The [AD5663R](#) has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 61. The circuit gives an output voltage range of  $\pm 5$  V. Rail-to-rail operation at the amplifier output is achievable using an [AD820](#) or an [OP295](#) as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[ V_{DD} \times \left( \frac{D}{65,536} \right) \times \left( \frac{R1 + R2}{R1} \right) - V_{DD} \times \left( \frac{R2}{R1} \right) \right]$$

where  $D$  represents the input code in decimal (0 to 65,535). With  $V_{DD} = 5$  V,  $R1 = R2 = 10$  k $\Omega$ ,

$$V_O = \left( \frac{10 \times D}{65,536} \right) - 5 \text{ V}$$

This is an output voltage range of  $\pm 5$  V, with 0x0000 corresponding to a  $-5$  V output, and 0xFFFF corresponding to a  $+5$  V output.

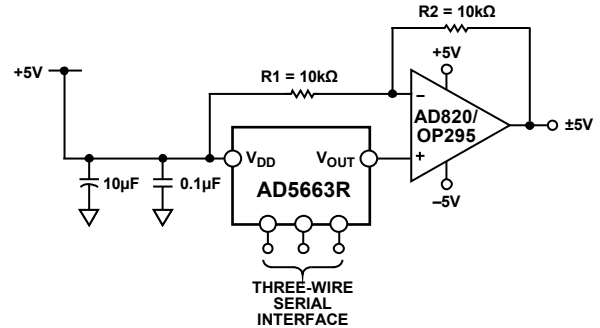


Figure 61. Bipolar Operation with the [AD5663R](#)

### USING THE AD5663R WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. *iCoupler*<sup>®</sup> provides isolation in excess of 2.5 kV. The [AD5663R](#) uses a 3-wire serial logic interface, so the [ADuM1300](#) 3-channel digital isolator provides the required isolation (see Figure 62). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the [AD5663R](#).

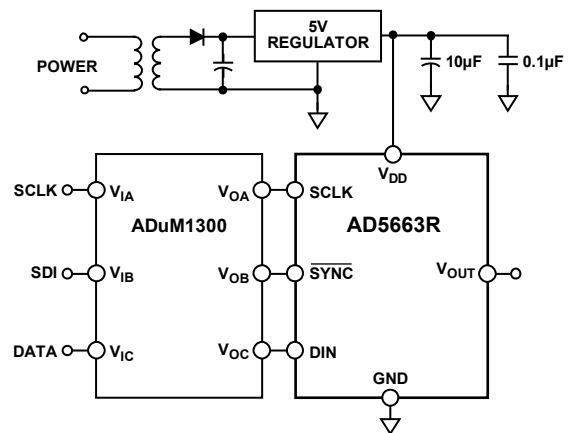


Figure 62. [AD5663R](#) with a Galvanically Isolated Interface

## POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the [AD5663R](#) should have separate analog and digital sections, each having its own area of the board.

If the [AD5663R](#) is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the [AD5663R](#).

The power supply to the [AD5663R](#) should be bypassed with 10  $\mu\text{F}$  and 0.1  $\mu\text{F}$  capacitors. The capacitors should be located as close as possible to the device, with the 0.1  $\mu\text{F}$  capacitor ideally right up against the device. The 10  $\mu\text{F}$  capacitors are the tantalum bead type. It is important that the 0.1  $\mu\text{F}$  capacitor have low effective series resistance (ESR) and effective series inductance (ESI), which is found, for example, in common ceramic types of capacitors.

This 0.1  $\mu\text{F}$  capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

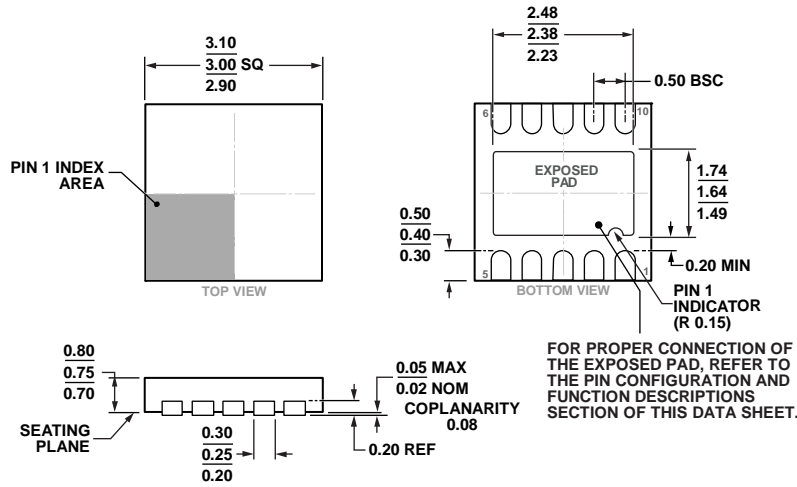
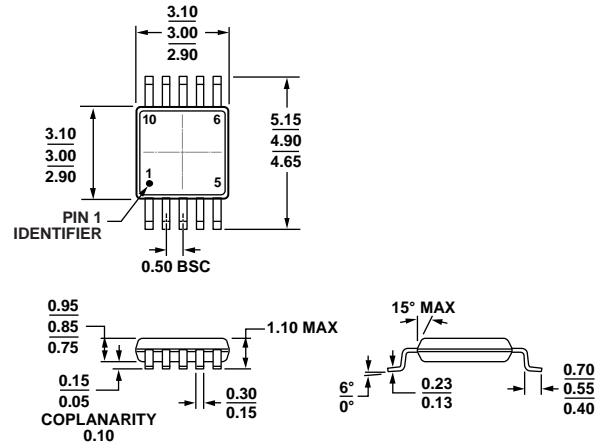


Figure 63. 10-Lead Lead Frame Chip Scale Package [LFCSP\_WD]  
 3 mm x 3 mm Body, Very Very Thin, Dual Lead  
 (CP-10-9)  
 Dimensions shown in millimeters

02-05-2013-C



COMPLIANT TO JEDEC STANDARDS MO-187-BA  
 Figure 64. 10-Lead Mini Small Outline Package [MSOP]  
 (RM-10)  
 Dimensions shown in millimeters

091705-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Accuracy	Internal Reference	Package Description	Package Option	Branding
AD5623RBCPZ-3R2	-40°C to +105°C	±1 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D85
AD5623RBCPZ-3REEL7	-40°C to +105°C	±1 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D85
AD5623RBCPZ-5REEL7	-40°C to +105°C	±1 LSB INL	2.5 V	10-Lead LFCSP_WD	CP-10-9	D86
AD5623RBRMZ-3	-40°C to +105°C	±1 LSB INL	1.25 V	10-Lead MSOP	RM-10	D85
AD5623RBRMZ-3REEL7	-40°C to +105°C	±1 LSB INL	1.25 V	10-Lead MSOP	RM-10	D85
AD5623RBRMZ-5	-40°C to +105°C	±1 LSB INL	2.5 V	10-Lead MSOP	RM-10	D86
AD5623RBRMZ-5REEL7	-40°C to +105°C	±1 LSB INL	2.5 V	10-Lead MSOP	RM-10	D86
AD5623RACPZ-5REEL7	-40°C to +105°C	±2 LSB INL	2.5 V	10-Lead LFCSP_WD	CP-10-9	DKB
AD5623RARMZ-5REEL7	-40°C to +105°C	±2 LSB INL	2.5 V	10-Lead MSOP	RM-10	DKP
AD5623RARMZ-5	-40°C to +105°C	±2 LSB INL	2.5 V	10-Lead MSOP	RM-10	DKP
AD5643RBRMZ-3	-40°C to +105°C	±4 LSB INL	1.25 V	10-Lead MSOP	RM-10	D81
AD5643RBRMZ-3REEL7	-40°C to +105°C	±4 LSB INL	1.25 V	10-Lead MSOP	RM-10	D81
AD5643RBRMZ-5	-40°C to +105°C	±4 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7Q
AD5643RBRMZ-5REEL7	-40°C to +105°C	±4 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7Q
AD5663RBCPZ-3R2	-40°C to +105°C	±16 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D7S
AD5663RBCPZ-3REEL7	-40°C to +105°C	±16 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D7S
AD5663RBCPZ-5REEL7	-40°C to +105°C	±16 LSB INL	2.5 V	10-Lead LFCSP_WD	CP-10-9	D7H
AD5663RBRMZ-3	-40°C to +105°C	±16 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7S
AD5663RBRMZ-3REEL7	-40°C to +105°C	±16 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7S
AD5663RBRMZ-5	-40°C to +105°C	±16 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7H
AD5663RBRMZ-5REEL7	-40°C to +105°C	±16 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7H
EVAL-AD5663REBZ				Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

## Looking for pricing, stock, or lifecycle information?

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-  Excess Inventory Management