THE DATASHEET OF

AD5621AKSZ-REEL7

2.7 V to 5.5 V, <100 µA, 8-/10-/12-Bit *nano*DAC, SPI Interface in LFCSP and SC70

Data Sheet

AD5601/AD5611/AD5621

FEATURES

- 6-lead SC70 and LFCSP packages
- Micropower operation: 100 µA maximum at 5 V
- Power-down typically to 0.2 µA at 3 V
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-on reset to 0 V with brownout detection
- 3 power-down functions
- Low power serial interface with Schmitt-triggered inputs
- On-chip output buffer amplifier, rail-to-rail operation
- $\overline{\text{SYNC}}$ interrupt facility
- Minimized zero-code error
- AD5601 buffered 8-bit DAC
  - B version: ±0.5 LSB INL
- AD5611 buffered 10-bit DAC
  - B version: ±0.5 LSB INL
  - A version: ±4 LSB INL
- AD5621 buffered 12-bit DAC
  - B version: ±1 LSB INL
  - A version: ±6 LSB INL

APPLICATIONS

- Voltage level setting
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

GENERAL DESCRIPTION

The AD5601/AD5611/AD5621, members of the *nano*DAC® family, are single, 8-/10-/12-bit, buffered voltage output DACs that operate from a single 2.7 V to 5.5 V supply, consuming typically 75 µA at 5 V. The parts come in tiny LFCSP and SC70 packages. Their on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5601/AD5611/AD5621 utilize a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards.

The reference for the AD5601/AD5611/AD5621 is derived from the power supply inputs and, therefore, gives the widest dynamic output range. The parts incorporate a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains there until a valid write to the device takes place.

The AD5601/AD5611/AD5621 contain a power-down feature that reduces current consumption to typically 0.2 µA at 3 V.

FUNCTIONAL BLOCK DIAGRAM

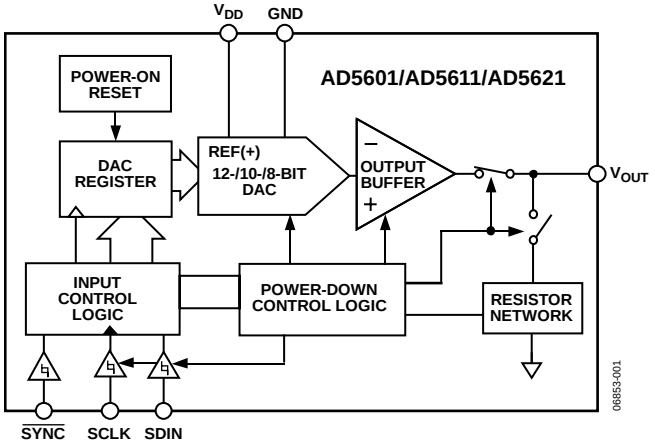

Figure 1.

Table 1. Related Devices

Part Number	Description
AD5641	2.7 V to 5.5 V, <100 µA, 14-bit *nano*DAC in SC70 and LFCSP packages

They also provide software-selectable output loads while in power-down mode. The parts are put into power-down mode over the serial interface.

The low power consumption of these parts in normal operation makes them ideally suited to portable battery-operated equipment. The combination of small package and low power makes these *nano*DAC devices ideal for level-setting requirements, such as generating bias or control voltages in space-constrained and power-sensitive applications.

PRODUCT HIGHLIGHTS

1. Available in 6-lead LFCSP and SC70 packages.
2. Low power, single-supply operation. The AD5601/AD5611/AD5621 operate from a single 2.7 V to 5.5 V supply with a maximum current consumption of 100 µA, making them ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a typical slew rate of 0.5 V/µs.
4. Reference is derived from the power supply.
5. High speed serial interface with clock speeds up to 30 MHz. Designed for very low power consumption. The interface powers up only during a write cycle.
6. Power-down capability. When powered down, the DAC typically consumes 0.2 µA at 3 V. Power-on reset with brownout detection.

Rev. I

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TABLE OF CONTENTS

REVISION HISTORY

4/2019—Rev. H to Rev. I

Changes to Table 2 ... 5
Change to Figure 16 ... 8
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 21

2/2016—Rev. G to Rev. H

Changes to Noise Parameter, Table 2 ... 3
Changes to Serial Interface Section ... 14

6/2013—Rev. F to Rev. G

Change to Ordering Guide ... 21

2/2012—Rev. E to Rev. F

Added 6-Lead LFCSP ... Universal
Changes to Features Section, General Description Section, Table 1, and Product Highlights Section ... 1
Changes to Table 4 ... 5
Added Figure 4; Renumbered Sequentially ... 6
Changes to Table 5 ... 6
Changes to Choosing a Reference as Power Supply for the AD5601/AD5611/AD5621 Section ... 18
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 21

7/2010—Rev. D to Rev. E

Changes to Figure 1 ... 1

5/2008—Rev. C to Rev. D

Changes to General Description Section ... 1
Changes to Table 2 ... 3
Changes to Choosing a Reference as Power Supply for the AD5601/AD5611/AD5621 Section ... 18
Changes to Ordering Guide ... 20

12/2007—Rev. B to Rev. C

Changes to Features ... 1
Changes to Table 2 ... 3
Changes to AD5601/AD5611/AD5621 to ADSP-2101 Interface Section ... 16
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

7/2005—Rev. A to Rev. B

Changes to Figure 48 ... 17
Changes to Galvanically Isolated Interface Section ... 19
Changes to Figure 52 ... 19

3/2005—Rev. 0 to Rev. A

Changes to Timing Characteristics ... 4
Changes to Absolute Maximum Ratings ... 5
Changes to Full Scale Error Section ... 7
Changes to Figure 20 ... 10
Changes to Theory of Operation ... 14
Changes to Power Down Modes ... 15

1/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range for A/B grades is −40°C to +125°C, typical at 25°C.

Table 2.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE								
AD5601								
Resolution				8			Bits	
Relative Accuracy[1] (INL)						±0.5	LSB	
Differential Nonlinearity (DNL)						±0.5	LSB	Guaranteed monotonic by design
AD5611								
Resolution	10						Bits	
Relative Accuracy[1] (INL)			±4			±0.5	LSB	
Differential Nonlinearity (DNL)			±0.5			±0.5	LSB	Guaranteed monotonic by design
AD5621								
Resolution	12						Bits	
Relative Accuracy[1] (INL)			±6			±1	LSB	
Differential Nonlinearity (DNL)			±0.5			±0.5	LSB	Guaranteed monotonic by design
Zero-Code Error		0.5	10		0.5	10	mV	All 0s loaded to DAC register
Full-Scale Error		±0.5			±0.5		mV	All 1s loaded to DAC register
Offset Error		±0.063	±10		±0.063	±10	mV	
Gain Error		±0.0004	±0.037		±0.0004	±0.037	%FSR	
Zero-Code Error Drift		5.0			5.0		µV/°C	
Gain Temperature Coefficient		2.0			2.0		ppm FSR/°C	
OUTPUT CHARACTERISTICS[2]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Output Voltage Settling Time		6	10		6	10	µs	Code ¼ scale to ¾ scale
Slew Rate		0.5			0.5		V/µs	
Capacitive Load Stability		470			470		pF	$R_L = \infty$
		1000			1000		pF	R_L = 2 kΩ
Output Noise Spectral Density		120			120		nV/√Hz	DAC code = midscale,1 kHz
Noise		2			2		µV rms	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth
Digital-to-Analog Glitch Impulse		5			5		nV-s	1 LSB change around major carry
Digital Feedthrough		0.2			0.2		nV-s	
Short-Circuit Current		15			15		mA	V_{DD} = 3 V/5 V
DC Output Impedance		0.5			0.5		Ω	
LOGIC INPUTS								
Input Current[3]			±2			±2	µA	
Input High Voltage, V_{INH}	1.8			1.8			V	V_{DD} = 4.7 V to 5.5 V
	1.4			1.4			V	V_{DD} = 2.7 V to 3.6 V
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 4.7 V to 5.5 V
			0.6			0.6	V	V_{DD} = 2.7 V to 3.6 V
Pin Input Capacitance		3			3		pF	

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} for Normal Mode								DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		75	100		75	100	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		60	90		60	90	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} for All Power-Down Modes								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.5			0.5		µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.2			0.2		µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY								
I_{OUT}/I_{DD}		96			96		%	I_{LOAD} = 2 mA and V_{DD} = ±5 V

[1] Linearity calculated using a reduced code range: AD5621 from Code 64 to Code 4032; AD5611 from Code 16 to Code 1008; AD5601 from Code 4 to Code 252.
[2] Guaranteed by design and characterization, not production tested.
[3] Total current flowing into all pins.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 2.

Table 3.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	33	ns min	SCLK cycle time
t_2	5	ns min	SCLK high time
t_3	5	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	20	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge ignored

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 30 MHz.

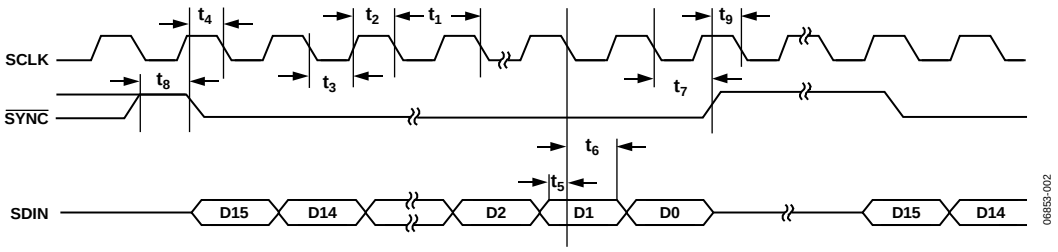


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A/B Grades)	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SC70 Package	
θ_{JA} Thermal Impedance	433.34°C/W
θ_{JC} Thermal Impedance	149.47°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD (Human Body Model)	2.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

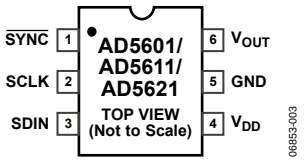


Figure 3. 6-Lead SC70 Pin Configuration

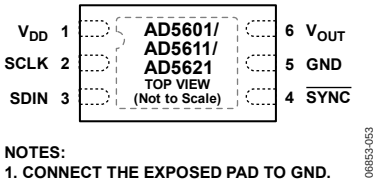


Figure 4. 6-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

SC70 Pin No.	LFCSP Pin No.	Mnemonic	Description
1	4	$\overline{\text{SYNC}}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the clocks that follow. The DAC is updated following the 16th clock cycle, unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC.
2	2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
3	3	SDIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
4	1	V_{DD}	Power Supply Input. The AD5601/AD5611/AD5621 can be operated from 2.7 V to 5.5 V. Decouple V_{DD} to GND.
5	5	GND	Ground. Ground reference point for all circuitry on the AD5601/AD5611/AD5621.
6	6	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
		EP	Exposed Pad. Connect to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

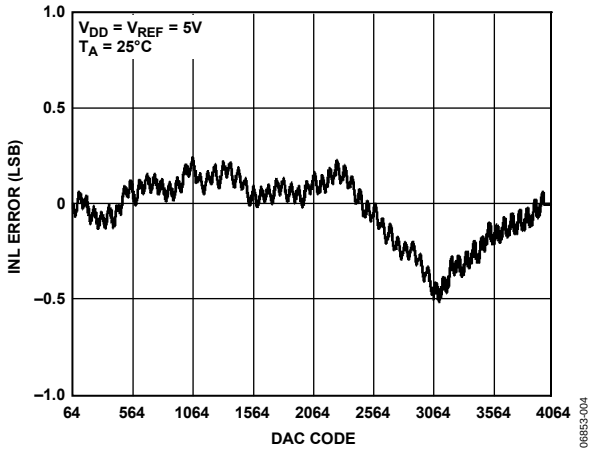


Figure 5. Typical AD5621 INL

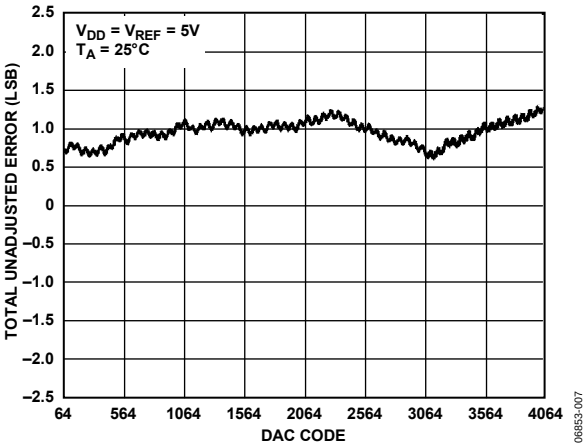


Figure 8. AD5621 Total Unadjusted Error (TUE)

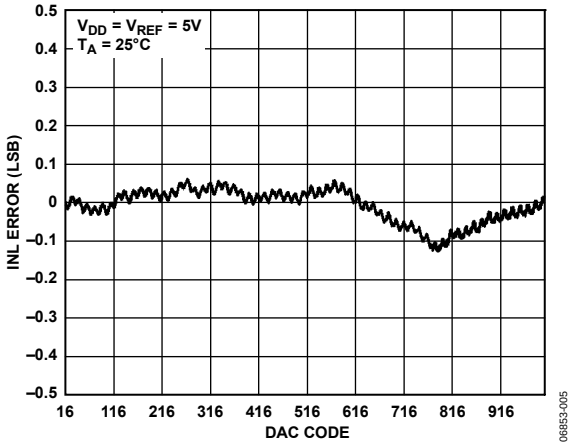


Figure 6. Typical AD5611 INL

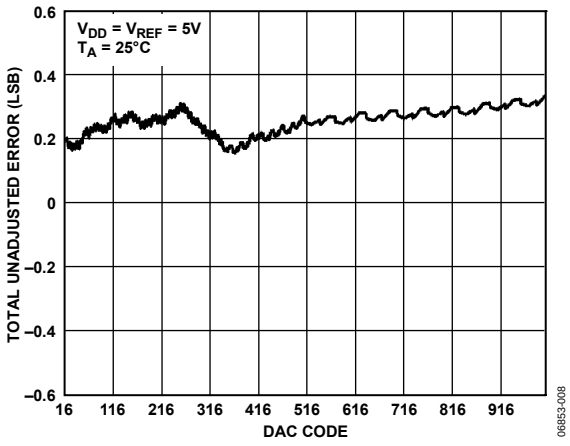


Figure 9. AD5611 Total Unadjusted Error (TUE)

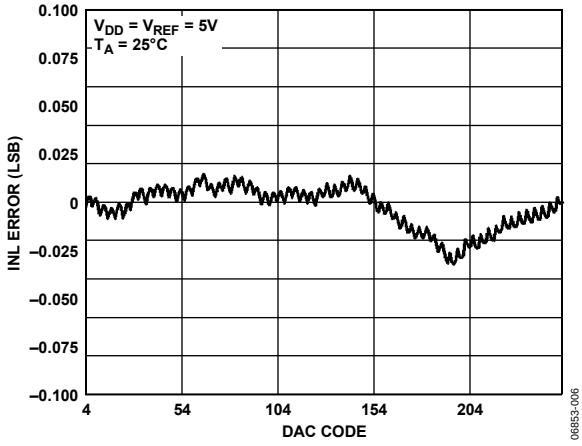


Figure 7. Typical AD5601 INL

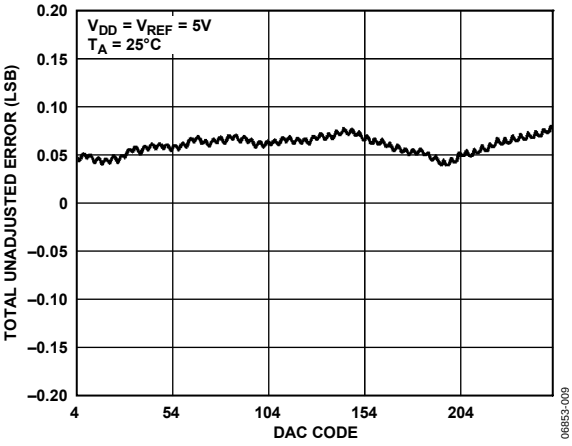


Figure 10. AD5601 Total Unadjusted Error (TUE)

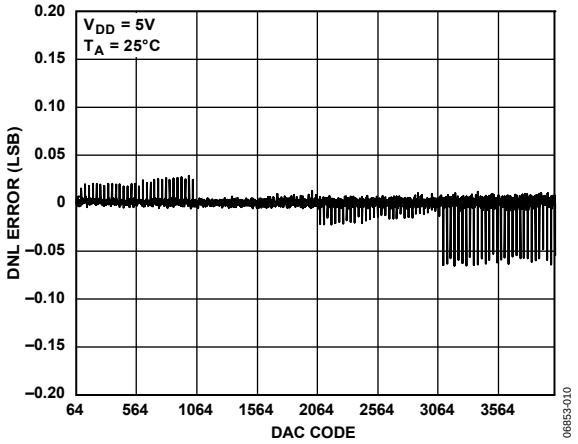


Figure 11. Typical AD5621 DNL

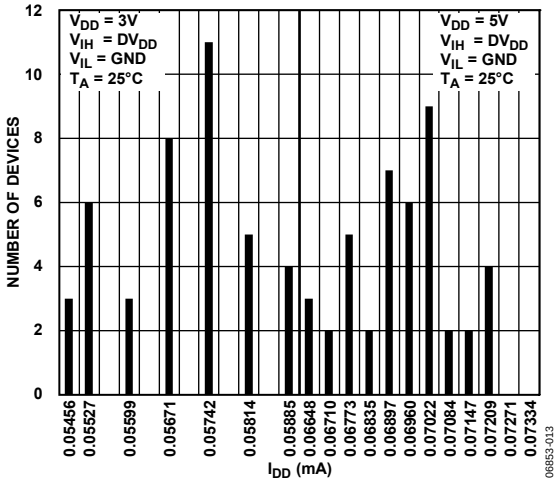


Figure 14. I_{DD} Histogram (3 V/5 V)

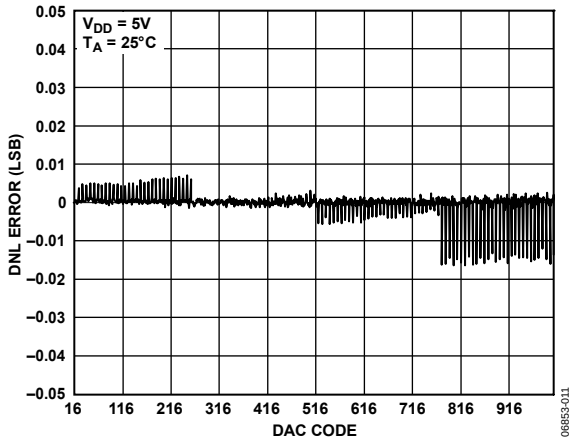


Figure 12. Typical AD5611 DNL

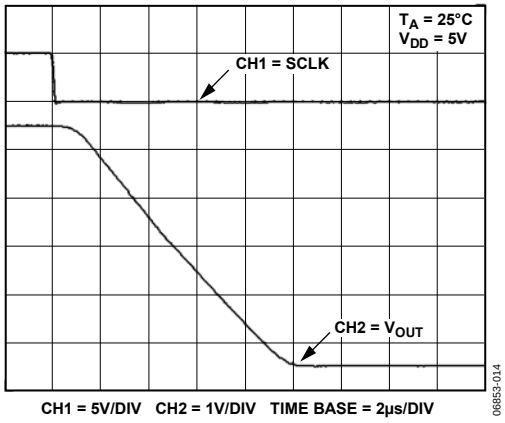


Figure 15. Full-Scale Settling Time

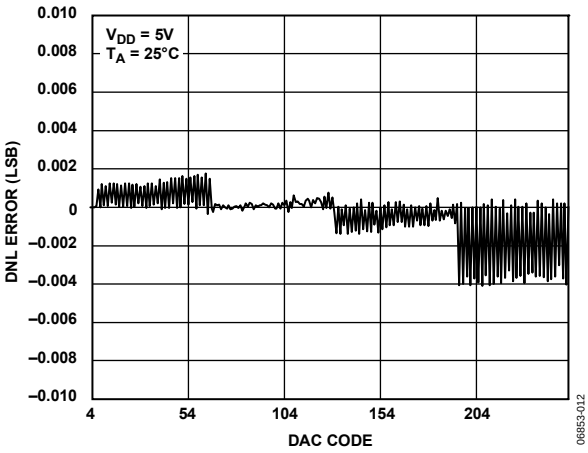


Figure 13. Typical AD5601 DNL

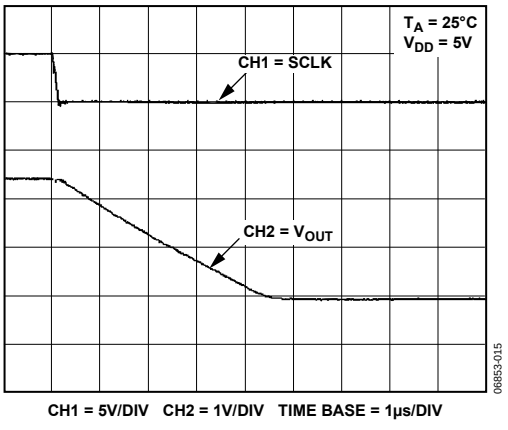


Figure 16. Half-Scale Settling Time

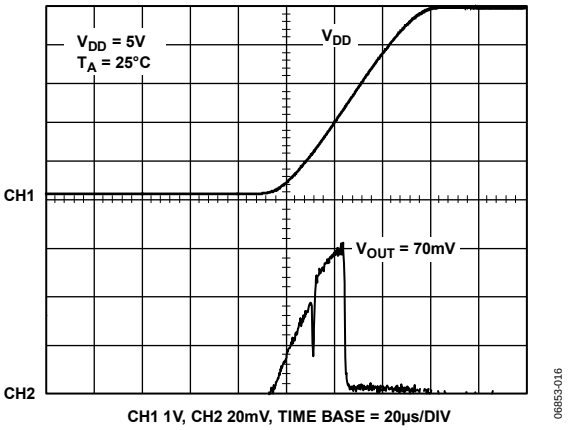


Figure 17. Power-On Reset to 0 V

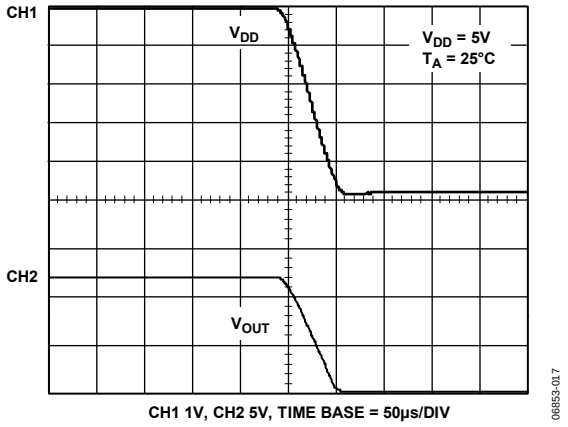


Figure 18. V_{DD} vs. V_{OUT}

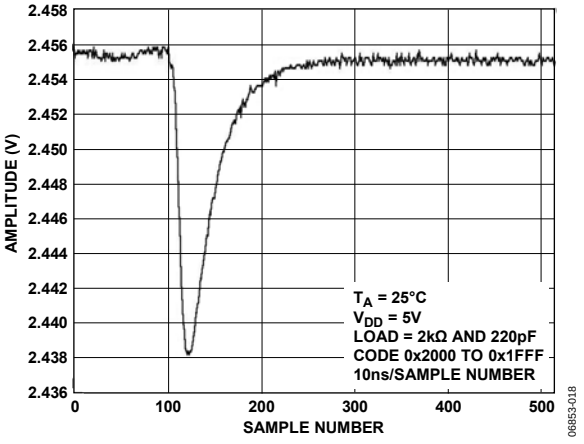


Figure 19. Digital-to-Analog Glitch Energy

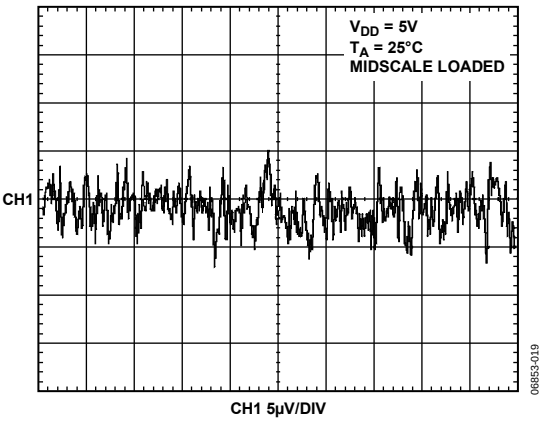


Figure 20. 1/f Noise, 0.1 Hz to 10 Hz Bandwidth

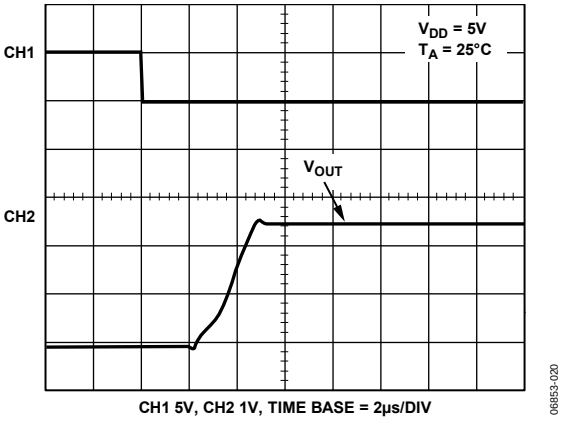


Figure 21. Exiting Power-Down Mode

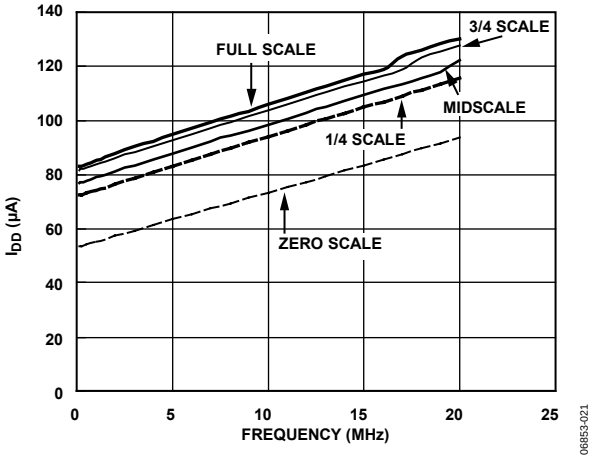


Figure 22. I_{DD} vs. SCLK vs. Code

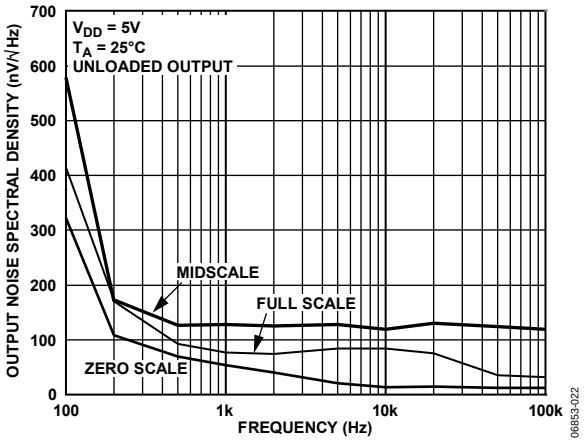


Figure 23. Noise Spectral Density

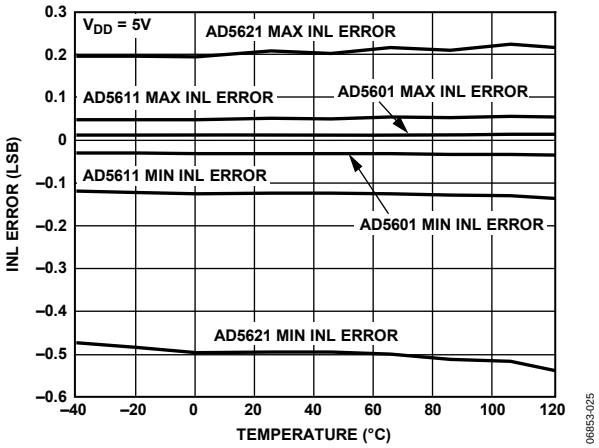


Figure 26. INL vs. Temperature (5 V)

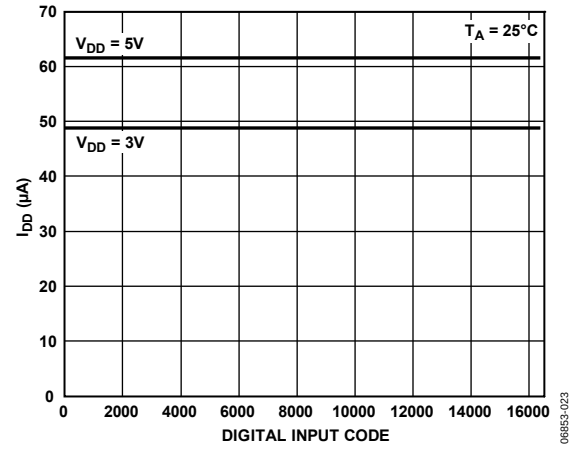


Figure 24. Supply Current vs. Digital Input Code

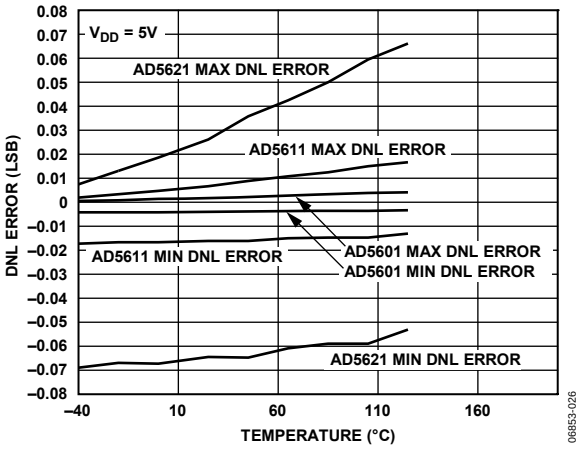


Figure 27. DNL vs. Temperature (5 V)

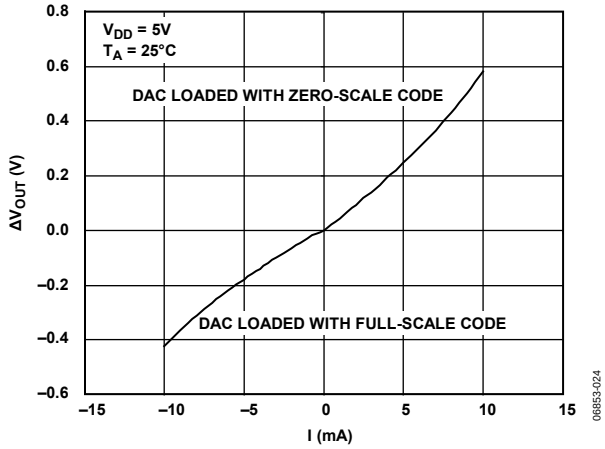


Figure 25. Sink and Source Capability

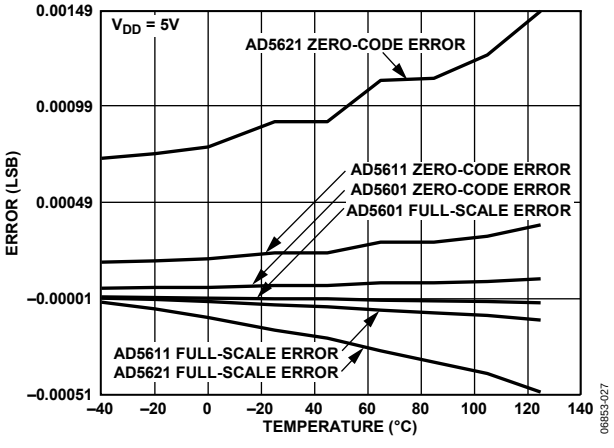


Figure 28. Zero-Code Error and Full-Scale Error vs. Temperature

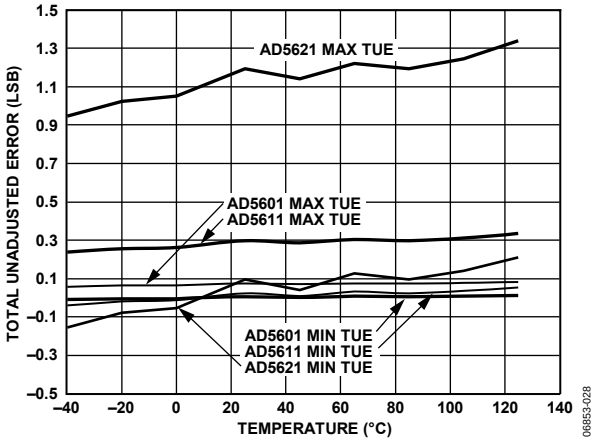


Figure 29. Total Unadjusted Error (TUE) vs. Temperature (5 V)

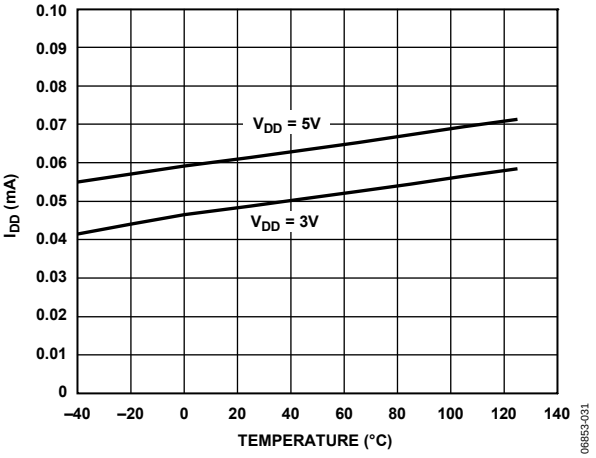


Figure 32. Supply Current vs. Temperature (3 V/5 V Supply)

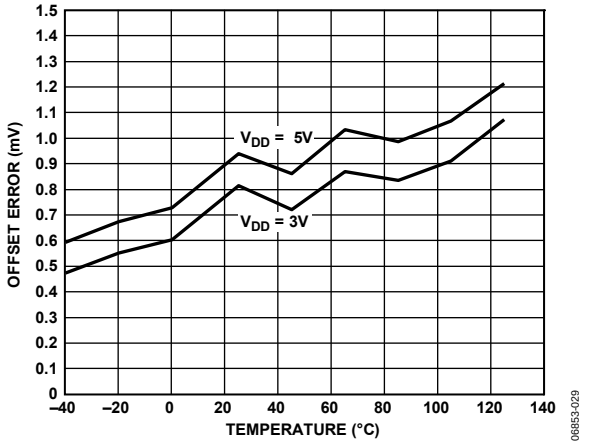


Figure 30. Offset Error vs. Temperature (3 V/5 V Supply)

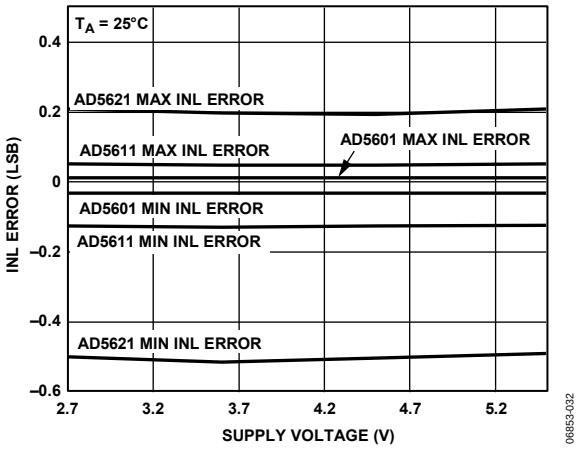


Figure 33. INL vs. Supply Voltage at 25°C

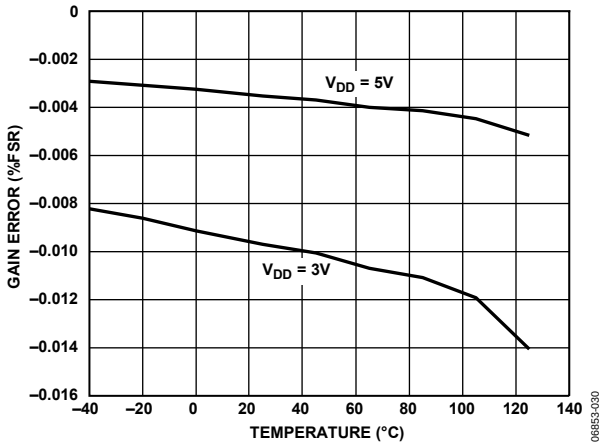


Figure 31. Gain Error vs. Temperature (3 V/5 V Supply)

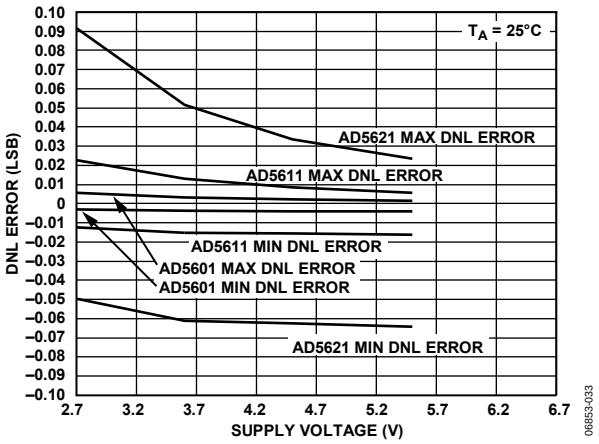


Figure 34. DNL vs. Supply Voltage at 25°C

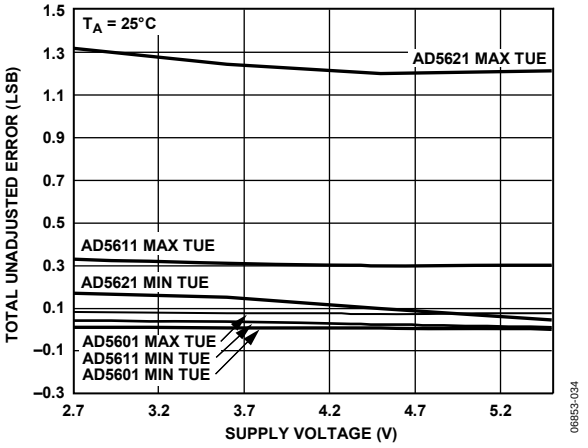


Figure 35. Total Unadjusted Error (TUE) vs. Supply Voltage at 25°C

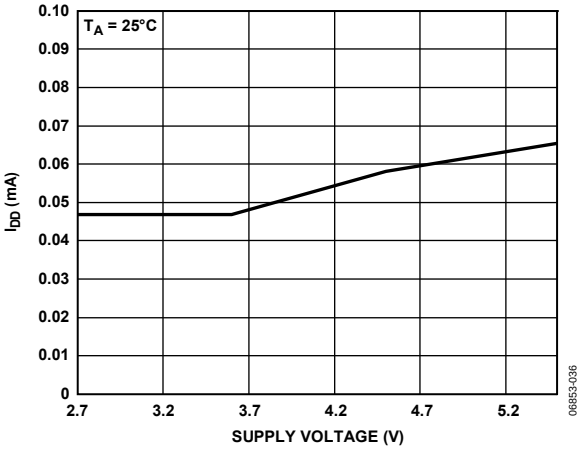


Figure 37. Supply Current vs. Supply Voltage at 25°C

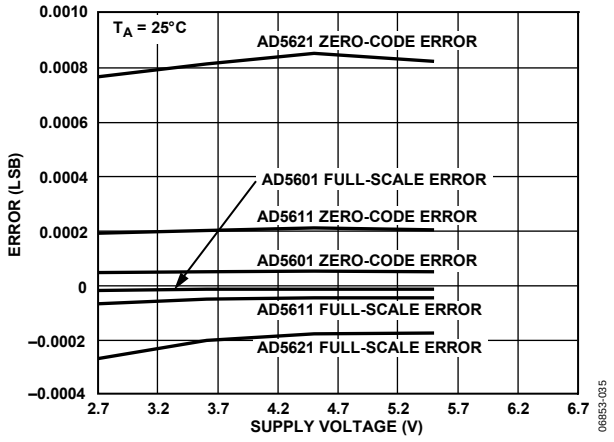


Figure 36. Zero-Code Error and Full-Scale Error vs. Supply Voltage at 25°C

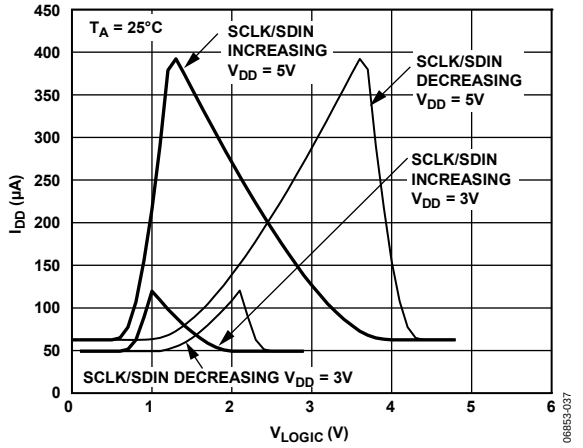


Figure 38. SCLK/SDIN vs. Logic Voltage

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. See Figure 5 to Figure 7 for plots of typical INL vs. code.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. See Figure 11 to Figure 13 for plots of typical DNL vs. code.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 V. The zero-code error is always positive in the AD5601/AD5611/AD5621 because the output of the DAC cannot go below 0 V. Zero-code error is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. See Figure 28 for a plot of zero-code error vs. temperature.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output is V_{DD} − 1 LSB. Full-scale error is expressed in mV. See Figure 28 for a plot of full-scale error vs. temperature.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percent of the full-scale range.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error, taking all the various errors into account. See Figure 8 to Figure 10 for plots of typical TUE vs. code.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x2000 to 0x1FFF). See Figure 19.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus—from all 0s to all 1s and vice versa.

THEORY OF OPERATION

DAC SECTION

The AD5601/AD5611/AD5621 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 39 is a block diagram of the DAC architecture.

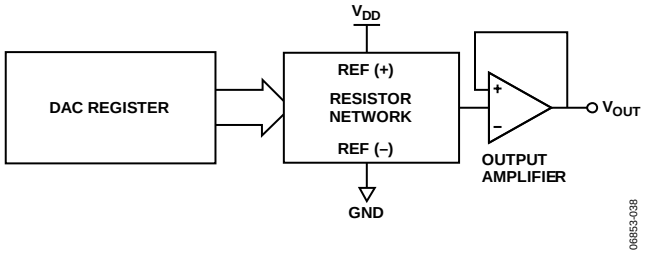


Figure 39. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{DD} \times \left(\frac{D}{2^n} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register.
n is the bit resolution of the DAC.

RESISTOR STRING

The resistor string structure is shown in Figure 40. It is simply a string of resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

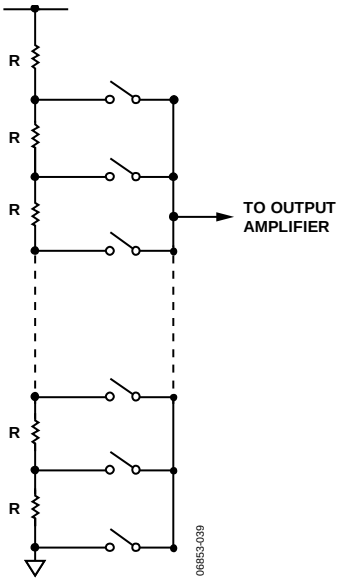


Figure 40. Resistor String Structure

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier are shown in Figure 25. The slew rate is 0.5 V/μs, with a half-scale settling time of 8 μs with the output loaded.

SERIAL INTERFACE

The AD5601/AD5611/AD5621 have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the SDIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5601/AD5611/AD5621 compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line can be kept low or brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

Because the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 1.8 V than it does when V_{IN} = 0.8 V, idle the $\overline{\text{SYNC}}$ buffer low between write sequences for even lower power operation of the device, as mentioned previously. However, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 41). The first two bits are control bits, which control the operating mode of the part (normal mode or any one of three power-down modes). For a complete description of the various modes, see the Power-Down Modes section. For the AD5621, the next 12 bits are the data bits, which are transferred to the DAC register on the 16th falling edge of SCLK. The information in the last two bits is ignored by the AD5621. See Figure 42 and Figure 43 for the AD5611 and AD5601 input shift register map.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 44).

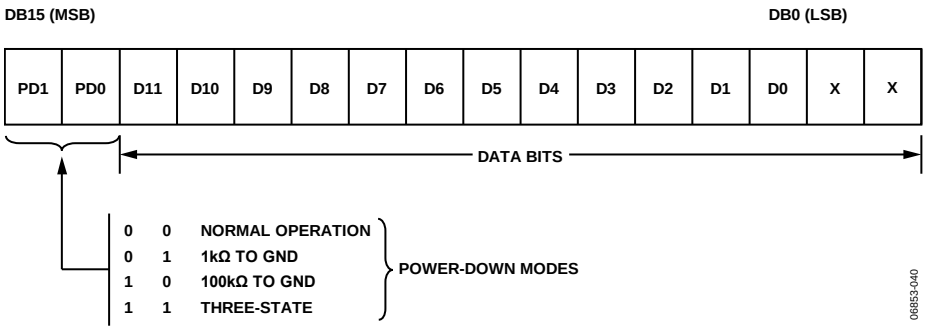


Figure 41. AD5621 Input Register Contents

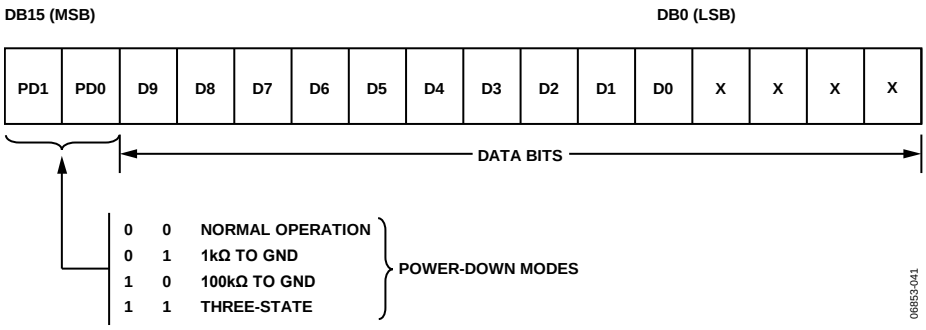


Figure 42. AD5611 Input Register Contents

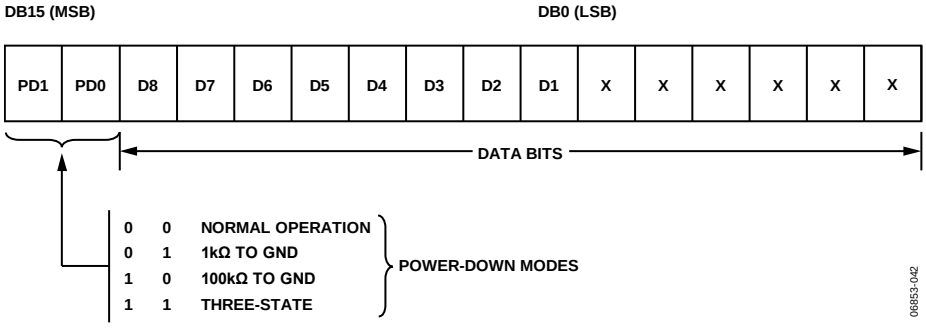


Figure 43. AD5601 Input Register Contents

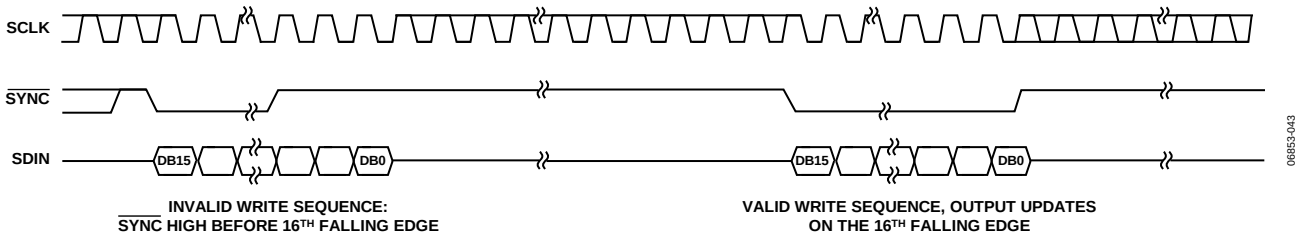


Figure 44. SYNC Interrupt Facility

POWER-ON RESET

The AD5601/AD5611/AD5621 contain a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with 0s and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications in which it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The AD5601/AD5611/AD5621 have four separate modes of operation. These modes are software-programmable by setting two bits (DB15 and DB14) in the control register. Table 6 shows how the state of the bits corresponds to the operating mode of the device.

Table 6. Operating Modes of the AD5601/AD5611/AD5621

DB15	DB14	Operating Mode
0	0	Normal operation
		Power-down modes:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

When both bits are set to 0, the part has normal power consumption of 100 μA maximum at 5 V. However, for the three power-down modes, the supply current falls to typically 0.2 μA at 3 V.

Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode.

There are three different options: the output is connected internally to GND through a 1 kΩ resistor or a 100 kΩ resistor, or the output is left open-circuited (three-stated). Figure 45 shows the output stage.

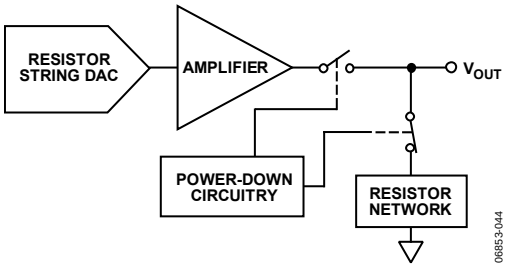


Figure 45. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are all shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 13 μs for V_{DD} = 5 V and 16 μs for V_{DD} = 3 V. See Figure 21 for a plot.

MICROPROCESSOR INTERFACING

AD5601/AD5611/AD5621 to ADSP-BF531 Interface

Figure 46 shows a serial interface between the AD5601/AD5611/AD5621 and the ADSP-BF531. The ADSP-BF531 processor has an integrated SPI port that can connect directly to the SPI pins of the AD5601/AD5611/AD5621.

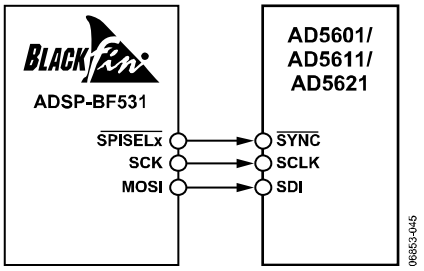
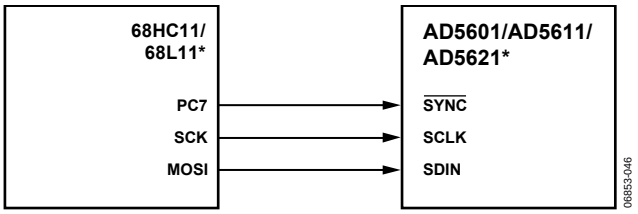


Figure 46. AD5601/AD5611/AD5621 to ADSP-BF531 Interface

AD5601/AD5611/AD5621 to 68HC11/68L11 Interface

Figure 47 shows a serial interface between the AD5601/AD5611/AD5621 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5601/AD5611/AD5621, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7). The setup conditions for proper operation of this interface are as follows: the 68HC11/68L11 must be configured so that the CPOL bit is 0 and the CPHA bit is 1. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is taken low (PC7). When the 68HC11/68L11 are configured as indicated, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5601/AD5611/AD5621, PC7 is left low after the first eight bits are transferred and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

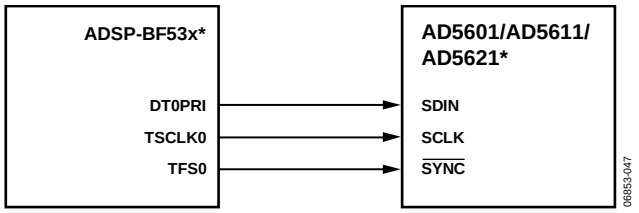


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 47. AD5601/AD5611/AD5621 to 68HC11/68L11 Interface

AD5601/AD5611/AD5621 to Blackfin® ADSP-BF53x Interface

Figure 48 shows a serial interface between the AD5601/AD5611/AD5621 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5601/AD5611/AD5621, the setup for the interface is as follows: DT0PRI drives the SDIN pin of the AD5601/AD5611/AD5621, while TSCLK0 drives the SCLK of the part. The $\overline{\text{SYNC}}$ is driven from TFS0.

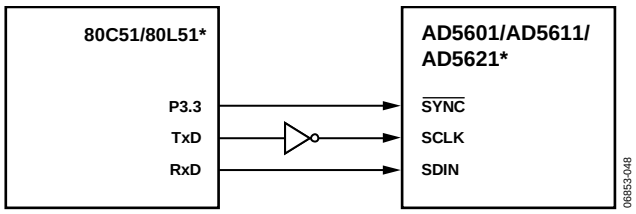


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 48. AD5601/AD5611/AD5621 to Blackfin ADSP-BF53x Interface

AD5601/AD5611/AD5621 to 80C51/80L51 Interface

Figure 49 shows a serial interface between the AD5601/AD5611/AD5621 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5601/AD5611/AD5621, while RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5601/AD5611/AD5621, P3.3 is taken low. The 80C51/80L51 transmit data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data LSB first. The AD5601/AD5611/AD5621 require data with the MSB as the first bit received. The 80C51/80L51 transmit routine must take this into account.

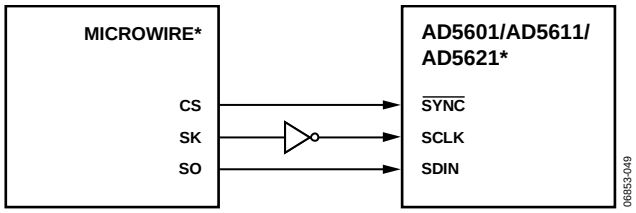


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 49. AD5601/AD5611/AD5621 to 80C51/80L51 Interface

AD5601/AD5611/AD5621 to MICROWIRE Interface

Figure 50 shows an interface between the AD5601/AD5611/AD5621 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5601/AD5611/AD5621 on the rising edge of the SK.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 50. AD5601/AD5611/AD5621 to MICROWIRE Interface

APPLICATIONS INFORMATION

CHOOSING A REFERENCE AS POWER SUPPLY FOR THE AD5601/AD5611/AD5621

The AD5601/AD5611/AD5621 come in tiny LFCSP and SC70 packages with less than a 100 µA supply current. Because of this, the choice of reference depends on the application requirements. For applications with space-saving requirements, the ADR02 is recommended. It is available in an SC70 package and has excellent drift at 9 ppm/°C (3 ppm/°C in the R-8 package) and provides very good noise performance at 3.4 µV p-p in the 0.1 Hz to 10 Hz range.

Because the supply current required by the AD5601/AD5611/AD5621 is extremely low, the parts are ideal for low supply applications. The ADR395 voltage reference is recommended in this case. It requires less than 100 µA of quiescent current and can, therefore, drive multiple DACs in one system, if required. It also provides very good noise performance at 8 µV p-p in the 0.1 Hz to 10 Hz range.

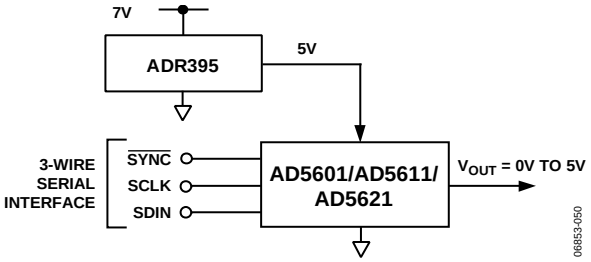


Figure 51. ADR395 as Power Supply to the AD5601/AD5611/AD5621

Some recommended precision references for use as supplies to the AD5601/AD5611/AD5621 are listed in Table 7.

Table 7. Precision References for the AD5601/AD5611/AD5621

Part No.	Initial Accuracy (mV max)	Temp Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)
ADR435	±2	3 (R-8)	8
ADR425	±2	3 (R-8)	3.4
ADR02	±3	3 (R-8)	10
ADR02	±3	3 (SC70)	10
ADR395	±5	9 (TSOT-23)	8

BIPOLAR OPERATION USING THE AD5601/AD5611/AD5621

The AD5601/AD5611/AD5621 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit shown in Figure 52. The circuit in Figure 52 gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

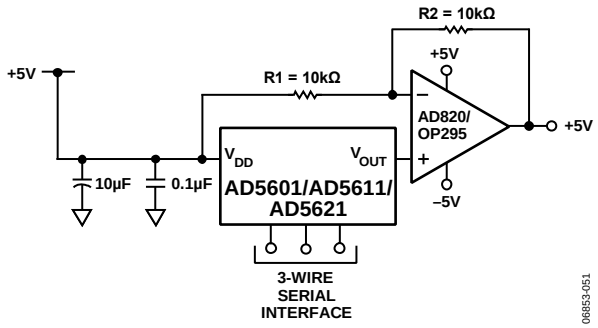


Figure 52. Bipolar Operation with the AD5601/AD5611/AD5621

The output voltage for any input code can be calculated as

$$V_{OUT} = \left[V_{DD} \times \left(\frac{D}{2^N} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal ($0 - 2^N$).

With V_{DD} = 5 V, R1 = R2 = 10 kΩ

$$V_{OUT} = \left(\frac{10 \times D}{2^N} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output and 0x3FFF corresponding to a +5 V output.

USING THE AD5601/AD5611/AD5621 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. Because the AD5601/AD5611/AD5621 use a 3-wire serial logic interface, the ADuM1300 3-channel digital isolator provides the required isolation (see Figure 53). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5601/AD5611/AD5621.

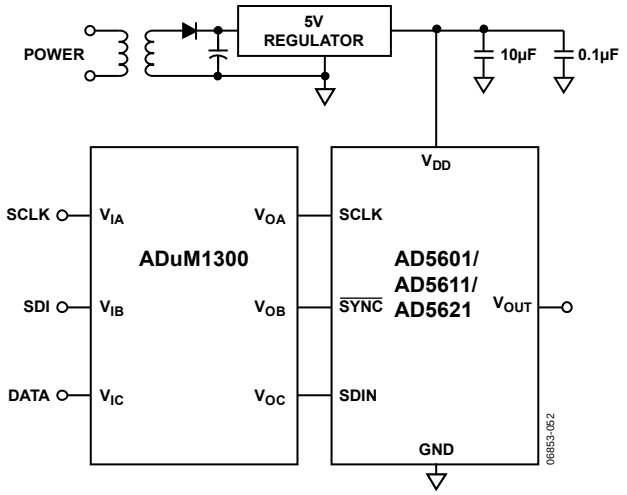


Figure 53. AD5601/AD5611/AD5621 with a Galvanically Isolated Interface

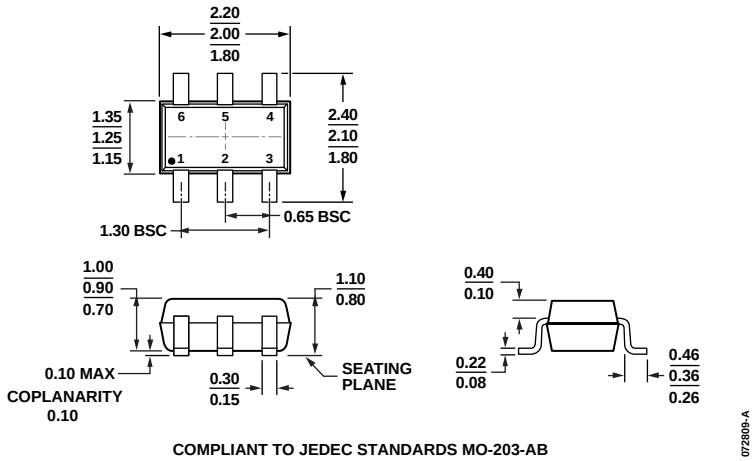
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The PCB containing the AD5601/AD5611/AD5621 must have separate analog and digital sections, each having its own area of the board. If the AD5601/AD5611/AD5621 are in a system where other devices require an AGND-to-DGND connection, the connection must be made at one point only. This ground point must be as close as possible to the AD5601/AD5611/AD5621.

Bypass the power supply to the AD5601/AD5611/AD5621 with 10 µF and 0.1 µF capacitors. The capacitors must be physically as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and effective series inductance (ESI), such as in common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

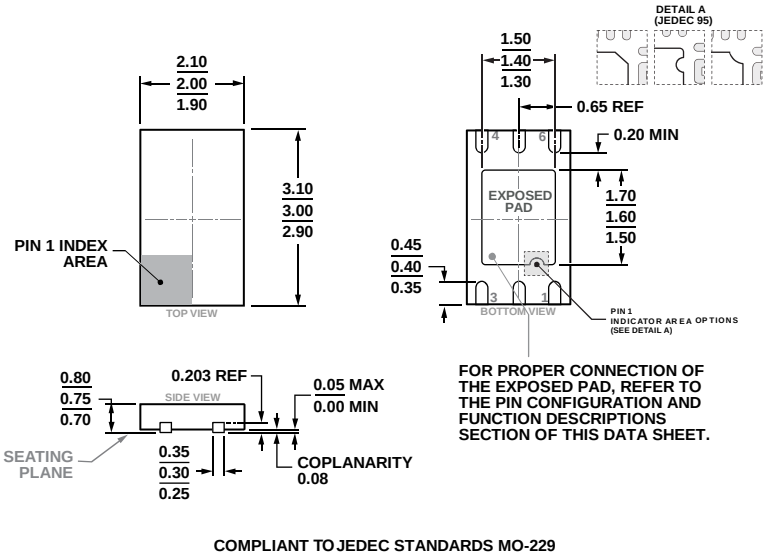
The power supply line itself must have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 54. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229

Figure 55. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2.00 × 3.00 mm Body and 0.75 mm Package Height
(CP-6-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	INL	Package Description	Package Option	Branding
AD5601BKSZ-500RL7	–40°C to +125°C	±0.5 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3V
AD5601BKSZ-REEL7	–40°C to +125°C	±0.5 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3V
AD5601BCPZ-RL7	–40°C to +125°C	±0.5 LSB	6-Lead Lead Frame Chip Scale Package [LFCSP]	CP-6-5	89
AD5611AKSZ-500RL7	–40°C to +125°C	±4.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3U
AD5611AKSZ-REEL7	–40°C to +125°C	±4.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3U
AD5611ACPZ-RL7	–40°C to +125°C	±4.0 LSB	6-Lead Lead Frame Chip Scale Package[LFCSP]	CP-6-5	8B
AD5611BKSZ-500RL7	–40°C to +125°C	±0.5 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3T
AD5611BKSZ-REEL7	–40°C to +125°C	±0.5 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3T
AD5621AKSZ-500RL7	–40°C to +125°C	±6.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3S
AD5621AKSZ-REEL7	–40°C to +125°C	±6.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3S
AD5621ACPZ-RL7	–40°C to +125°C	±6.0 LSB	6-Lead Lead Frame Chip Scale Package[LFCSP]	CP-6-5	D3S
AD5621BKSZ-500RL7	–40°C to +125°C	±1.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3R
AD5621BKSZ-REEL7	–40°C to +125°C	±1.0 LSB	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3R
EVAL-AD5621EBZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

Looking for pricing, stock, or lifecycle information?

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- View AD5621AKSZ-REEL7 on WIN SOURCE
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