



**THE DATASHEET OF
W2RF002RF**



LED Control IC W2RF002RF

Most Suitable IC for Controlling LED Effects within Applications

- Free-running PWM gradation control, with up to 1,024 levels, enables the representation of beautiful fade-in and fade-out effects.
- CPU load can be reduced by controlling lighting gradation and speed.
- Up to 49 pieces of this IC can be connected on the same serial bus communication line. Device group setting is also possible.
- 24 Line Outputs are contained in the 7 x 7 mm package.
- Use with Omron's W2RV005RM Constant Current IC to directly drive multiple LED's in series.
- RoHS Compliant



Ordering Information

| Description | Model |
|----------------|-----------|
| LED Control IC | W2RF002RF |

Specifications

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Rating |
|---|-------------------|---------------------------------------|
| Supply Voltage | V _{DD} | -0.3 to 7.0 V |
| Input Voltage | V _{IN} | -0.3 to V _{DD} + 0.3 ≤ 7.0 V |
| Communication Output Voltage (SCL-O, SDA-O) | V _{SOUT} | -0.3 to V _{DD} + 0.3 ≤ 7.0 V |
| Driving Output Voltage | V _{DOUT} | -0.3 to 20 V |
| Driving Output Current/pin (See note 1) | I _{DOUT} | 50 mA (when V _{DD} = 5.0 V) |
| | | 30 mA (when V _{DD} = 3.3 V) |
| Power Dissipation | P _d | 1.19 W (See note 2) |
| Operating Temperature | T _{OPR} | -20 to 85 °C |
| Storage Temperature | T _{STG} | -40 to 150 °C |

Note: 1. Take the power consumption and power dissipation rating into consideration.

- 2.** When implemented on a standard board (70 x 70 x 1.6 mm, Cu 3%, Single-sided glass epoxy board). The value reduces at a rate of about 9.52 mW/°C when the IC is used at Ta = 25°C or higher.

Recommended Operating Conditions

| Item | Symbol | Rating |
|---|-------------------|-------------------------|
| Supply Voltage | V _{DD} | 3.0 to 5.5 V |
| Input Voltage | V _{IN} | 0 to V _{DD} V |
| Communication Output Current (SCL-O, SDA-O) | I _{SOUT} | -10 to 10 mA |
| Communication Clock Frequency (SCL-I) | f _{SCL} | Max. 5 MHz (See note 1) |

Note: 1. Take the timing characteristics into consideration.

DC Electrical Characteristics (Ta = 25°C, V_{DD} = 5V)

| Item | Symbol | Condition | Spec. | | | Unit | Applicable terminal |
|---|------------------|--|-----------------------|------|-----------------------|------|---|
| | | | Min. | Typ. | Max. | | |
| High-level Input Voltage | V _{IH} | --- | V _{DD} x 0.7 | --- | --- | V | SDA-I, SCL-I, $\overline{\text{RST}}$, INV, ADRA0 to 2, ADRB0 to 2 |
| Low-level Input Voltage | V _{IL} | --- | --- | --- | V _{DD} x 0.3 | V | |
| High-level Communication Output Voltage | V _{SOH} | I _{OUT} = -10 mA | V _{DD} - 0.5 | --- | --- | V | SDA-O, SCL-O |
| Low-level Communication Output Voltage | V _{SOL} | I _{OUT} = 10 mA | --- | --- | 0.5 | V | |
| Driving Output Voltage 1 | V _{DO1} | I _{OUT} = 50 mA | --- | 0.27 | 0.60 | V | OUTA0 to 7 OUTB0 to 7 OUTC0 to 7 |
| Driving Output Voltage 2 | V _{DO2} | I _{OUT} = 20 mA | --- | 0.10 | 0.22 | V | |
| Driving Output Leakage Current | I _{DOZ} | V _{OUT} = 5 V | --- | --- | 1.0 | μA | |
| Operating Current Consumption | I _{DD} | Total Output: I _{OUT} = 50 mA | --- | 3.2 | 5.3 | mA | V _{DD} |

Timing Characteristics (Ta = 25°C, V_{DD} = 5V)

| Item | Symbol | Condition | Spec. | | | Unit | Applicable terminal |
|---------------------------------|------------------|-----------|-------|------|------|------|--|
| | | | Min. | Typ. | Max. | | |
| Driving Output PWM Cycle | T _{PWM} | --- | 3.88 | 4.00 | 4.12 | ms | OUTA0 to 7 OUTB0 to 7 OUTC0 to 7 |
| Communication Clock Pulse Width | t _{SCL} | --- | 100 | --- | --- | ns | SCL-I |
| Setup Time | t _{SET} | --- | 50 | --- | --- | ns | SDA-I, SCL-I |
| Hold Time | t _{HLD} | --- | 50 | --- | --- | ns | |

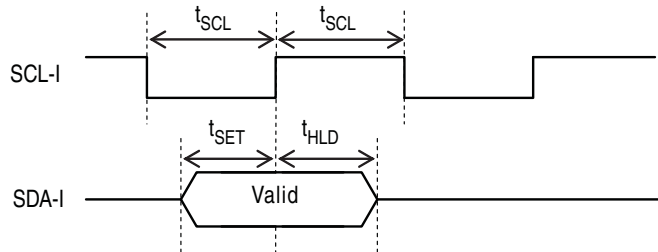
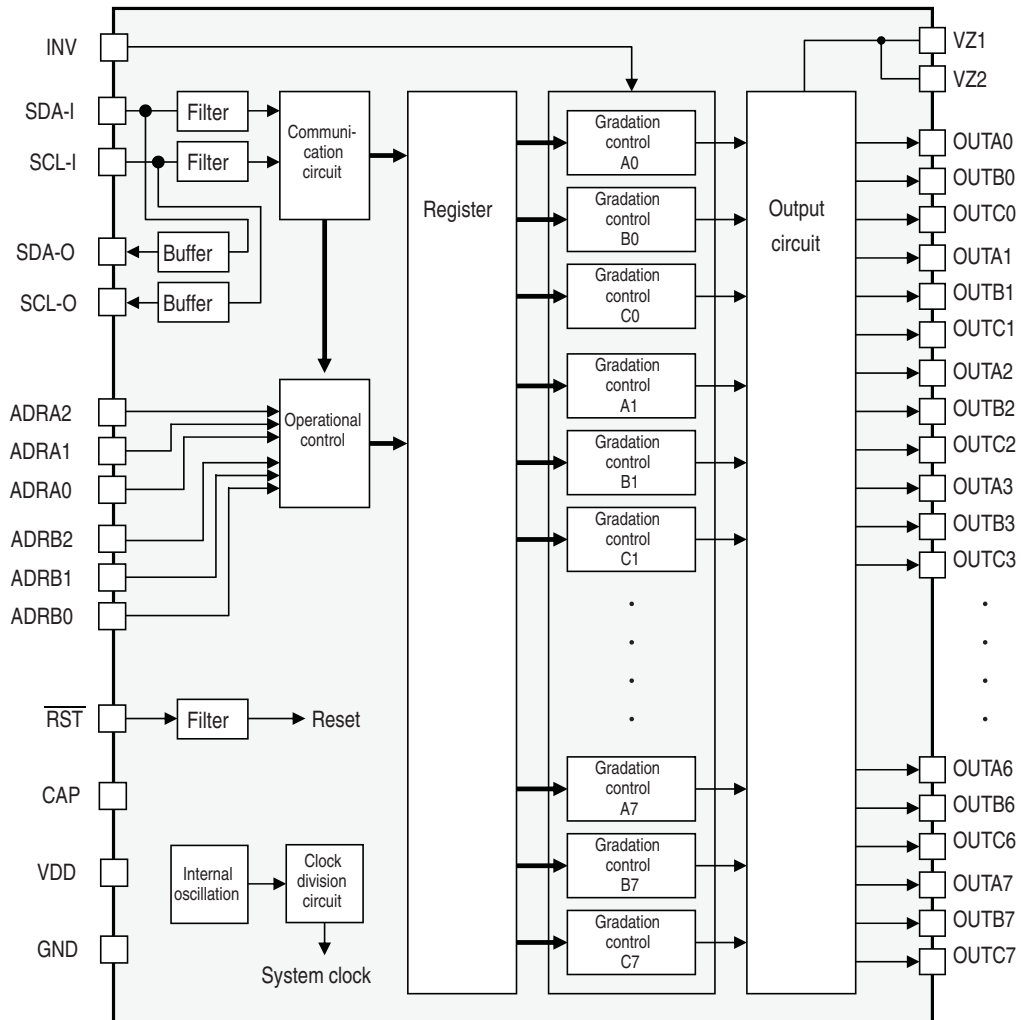


Fig. 1 Input timing waveforms

Engineering Data

Block Diagram



Terminal Designation

| Terminal Number | Terminal Name | Description | I/O | Logic | Function |
|-----------------|-------------------------|---------------------------------|-------|--|-----------------------|
| 1 | SDA-I | Serial data input | I | | CMOS, filter |
| 2 | SCL-I | Serial clock input | I | | |
| 3 | $\overline{\text{RST}}$ | Reset (See note 1) | I | L: Reset | CMOS, filter, pull-up |
| 4 | V _{DD} | Power source | P | | |
| 5 | CAP | Capacitor (See note 2) | - - - | | |
| 6 | GND | Ground | P | | |
| 7 | ADRA2 | Device address A2 | I | Refer to Operaton section (See note 4) | CMOS |
| 8 | ADRA1 | Device address A1 | I | | |
| 9 | ADRA0 | Device address A0 | I | | |
| 10 | ADRB2 | Device address B2 | I | | |
| 11 | ADRB1 | Device address B1 | I | | |
| 12 | ADRB0 | Device address B0 | I | | |
| 13 | INV | Output inversion | I | | |
| 14 | GND | Ground | P | | |
| 15 | OUTA0 | Output A0 | O | | N-ch open drain |
| 16 | OUTB0 | Output B0 | O | | |
| 17 | OUTC0 | Output C0 | O | | |
| 18 | OUTA1 | Output A1 | O | | |
| 19 | OUTB1 | Output B1 | O | | |
| 20 | OUTC1 | Output C1 | O | | |
| 21 | VZ1 | Output protection 1(See note 3) | - - - | | |
| 22 | GND | Ground | P | | |
| 23 | OUTA2 | Output A2 | O | | N-ch open drain |
| 24 | OUTB2 | Output B2 | O | | |
| 25 | OUTC2 | Output C2 | O | | |
| 26 | OUTA3 | Output A3 | O | | |
| 27 | OUTB3 | Output B3 | O | | |
| 28 | OUTC3 | Output C3 | O | | |
| 29 | GND | Ground | P | | |
| 30 | OUTA4 | Output A4 | O | | N-ch open drain |
| 31 | OUTB4 | Output B4 | O | | |
| 32 | OUTC4 | Output C4 | O | | |
| 33 | OUTA5 | Output A5 | O | | |
| 34 | OUTB5 | Output B5 | O | | |
| 35 | OUTC5 | Output C5 | O | | |
| 36 | GND | Ground | P | | |
| 37 | VZ2 | Output protection 2(See note 3) | - - - | | |
| 38 | OUTA6 | Output A6 | O | | N-ch open drain |
| 39 | OUTB6 | Output B6 | O | | |
| 40 | OUTC6 | Output C6 | O | | |
| 41 | OUTA7 | Output A7 | O | | |
| 42 | OUTB7 | Output B7 | O | | |
| 43 | OUTC7 | Output C7 | O | | |
| 44 | GND | Ground | P | | |
| 45 | TST1 | Not used (See note 4) | - - - | | |
| 46 | TST2 | Not used (See note 4) | - - - | | |
| 47 | SDA-O | Serial data buffer output | O | | CMOS |
| 48 | SCL-O | Serial clock buffer output | O | | |

- Note:**
1. The $\overline{\text{RST}}$ terminal is connected to an internal 100 k Ω pull-up resistor. When this terminal is not used, connect a 0.1 μF capacitor between the terminal and ground to prevent misoperation at power-on.
 2. Connect the CAP terminal to a capacitor for smoothing power supply. Connect a 0.1 μF capacitor between the terminal and GND.
 3. The VZ1 and VZ2 terminals are for driving output protection. Connect them to the power source of a driving system. When several driving system power supplies are used, connect the terminals to the highest potential among them. When these terminals are not used, leave them open.
 4. Always leave the TST1 and TST2 terminals open.
 5. Leave unused output terminals open.

Operation

■ Functional Overview

Receiving Commands

The IC receives commands with two-wire serial communication to control 24 LED lines. Commands are received in a 40-bits-per-command communication format.

Gradation Control

The lighting of the 24 LED lines is controlled individually or by group with 16-level lighting gradation and 32-level lighting speed. The exponential control of output duty cycle allows lighting gradation that matches the human visual characteristics. In addition, the specification of lighting speed allows fade-in and fade-out with up to 1,024 levels.

Number of Control Lines

The IC has two device address lines, each of which can be configured in seven ways by terminal configuration. This provides up to 49 patterns of device address configuration, allowing up to 1,176 lines to be controlled on the same communication line. Two device address lines can be combined to configure a device group.

■ Communication Specifications

Input signals to SDA-I and SCL-I are input via the filter circuit (0.1μs delay) to the communication circuit. An SDA-I signal that is input to the communication circuit is taken in as serial data at the rising edge of an SCL-I signal. When serial data is received in a different format from the communication format, the data will be invalid.

When the START signal, “11111111” is detected, the communication circuit takes in data as new serial data, whether it is on stand-by or in the middle of intake of serial data.

Input signals to SDA-I and SCL-I will be output via the asynchronous buffer to SDA-O and SCL-O without going through the filter circuit.

Communication Format

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|---------------------------------------|---|---|---|---|---|---|---|---|---------|------------------------------------|------------------|------------------|---------|----------------------------|----------------|---------|------------------------------|--------------------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|
| bit | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | | | |
| SCL-I | [Timing diagram showing SCL-I signal] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDA-I | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | | | | | | | 0 | | | | | | | | | | | | | | | | | | | | | 0 | X | X | X |
| Name | START | | | | | | | | | (Break) | Device ID | Device address A | Device address B | (Break) | Control | Output address | (Break) | Lighting speed | Lighting gradation | END | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | (Break) | Device selection data dvc_dat[7:0] | | | (Break) | Control data ctrl_dat[6:0] | | (Break) | Lighting data light_dat[8:0] | | | | | | | | | | | | | | | | | | | | | | | | | |

Description of Communication Format

| | | |
|-----------------------|--------------------|---|
| Device Selection Data | Device ID | Device-specific ID (Fixed to “00” for this IC) |
| | Device Address A | Specified with the ADRA0 to 2 terminals |
| | Device Address B | Specified with the ADRB0 to 2 terminals |
| Control Data | Control | Specifies control (data saving / immediate reflection) |
| | Output Address | Specifies the terminal to output (Individual specification and collective specification are possible) |
| Lighting Data | Lighting Speed | Specifies changing speed of free-running gradation control (32 levels) |
| | Lighting Gradation | Specifies the brightness of lighting (16 levels) |

■ Control Command

Device Selection Data (8 bits)

| Device selection data dvc_dat (7:0) | | | | | | | |
|-------------------------------------|---|------------------|-------|-------|------------------|-------|-------|
| Device ID | | Device Address A | | | Device Address B | | |
| 0 | 0 | ADRA2 | ADRA1 | ADRA0 | ADRB2 | ADRB1 | ADRB0 |

The device ID is fixed. The correspondence between the device addresses A and B and the setting terminals ADRA0 to 2 and ADRB0 to 2 is shown in the table. (Setting “L”...Data “0”. Setting “H”...Data “1”).

When ADRA0 to 2 = “111”, the device address A line is specified collectively, and when ADRB0 to 2 = “111”, the device address B line is specified collectively.

Because up to 7 addresses can be specified for each of device address A and device address B, their combination allows the specification of up to 49 addresses.

Control Data (7 bits)

| Control data ctrl_dat (6:0) | | | | | | |
|-----------------------------|----------------|----------|----------|----------|----------|----------|
| Control | Output Address | | | | | |
| ctrl | o_adr(5) | o_adr(4) | o_adr(3) | o_adr(2) | o_adr(1) | o_adr(0) |

The control signal, 'ctrl', activates the operational control shown in the following table.

- When ctrl = "0", latch operation is activated, in which data is only stored in latch registers and will not be reflected in the output.
- When ctrl = "1", load operation is activated, in which data is stored in the specified latch registers and the data of the latch registers in all addresses will be stored in the load registers.

| Control (ctrl) | Operational Control |
|----------------|---------------------|
| 0 | Latch |
| 1 | Load |

The output terminals in the following table are specified with the output address o_adr(5:0)

| Output Address o_adr (5:0) | | | | | | Output Terminal |
|----------------------------|-----|-----|-----|-----|-----|--|
| (5) | (4) | (3) | (2) | (1) | (0) | |
| 0 | 0 | 0 | 0 | 0 | 0 | OUTA0 |
| 0 | 0 | 0 | 0 | 0 | 1 | OUTA1 |
| 0 | 0 | 0 | 0 | 1 | 0 | OUTA2 |
| 0 | 0 | 0 | 0 | 1 | 1 | OUTA3 |
| 0 | 0 | 0 | 1 | 0 | 0 | OUTA4 |
| 0 | 0 | 0 | 1 | 0 | 1 | OUTA5 |
| 0 | 0 | 0 | 1 | 1 | 0 | OUTA6 |
| 0 | 0 | 0 | 1 | 1 | 1 | OUTA7 |
| 0 | 0 | 1 | 0 | 0 | 0 | OUTB0 |
| 0 | 0 | 1 | 0 | 0 | 1 | OUTB1 |
| 0 | 0 | 1 | 0 | 1 | 0 | OUTB2 |
| 0 | 0 | 1 | 0 | 1 | 1 | OUTB3 |
| 0 | 0 | 1 | 1 | 0 | 0 | OUTB4 |
| 0 | 0 | 1 | 1 | 0 | 1 | OUTB5 |
| 0 | 0 | 1 | 1 | 1 | 0 | OUTB6 |
| 0 | 0 | 1 | 1 | 1 | 1 | OUTB7 |
| 0 | 1 | 0 | 0 | 0 | 0 | OUTC0 |
| 0 | 1 | 0 | 0 | 0 | 1 | OUTC1 |
| 0 | 1 | 0 | 0 | 1 | 0 | OUTC2 |
| 0 | 1 | 0 | 0 | 1 | 1 | OUTC3 |
| 0 | 1 | 0 | 1 | 0 | 0 | OUTC4 |
| 0 | 1 | 0 | 1 | 0 | 1 | OUTC5 |
| 0 | 1 | 0 | 1 | 1 | 0 | OUTC6 |
| 0 | 1 | 0 | 1 | 1 | 1 | OUTC7 |
| 0 | 1 | 1 | 0 | 0 | 0 | OUTA0, OUTA2, OUTA4, OUTA6 |
| 0 | 1 | 1 | 0 | 0 | 1 | OUTA1, OUTA3, OUTA5, OUTA7 |
| 0 | 1 | 1 | 0 | 1 | 0 | OUTB0, OUTB2, OUTB4, OUTB6 |
| 0 | 1 | 1 | 0 | 1 | 1 | OUTB1, OUTB3, OUTB5, OUTB7 |
| 0 | 1 | 1 | 1 | 0 | 0 | OUTC0, OUTC2, OUTC4, OUTC6 |
| 0 | 1 | 1 | 1 | 0 | 1 | OUTC1, OUTC3, OUTC5, OUTC7 |
| 0 | 1 | 1 | 1 | 1 | 0 | OUTA0, OUTA2, OUTA4, OUTA6 OUTB0, OUTB2, OUTB4, OUTB6 OUTC0, OUTC2, OUTC4, OUTC6 |
| 0 | 1 | 1 | 1 | 1 | 1 | OUTA1, OUTA3, OUTA5, OUTA7 OUTB1, OUTB3, OUTB5, OUTB7 OUTC1, OUTC3, OUTC5, OUTC7 |

| Output Address o_adr (5:0) | | | | | | Output Terminal |
|----------------------------|-----|-----|-----|-----|-----|--|
| (5) | (4) | (3) | (2) | (1) | (0) | |
| 1 | 0 | 0 | 0 | 0 | 0 | OUTA0, OUTA1, OUTA4, OUTA5 |
| 1 | 0 | 0 | 0 | 0 | 1 | OUTA2, OUTA3, OUTA6, OUTA7 |
| 1 | 0 | 0 | 0 | 1 | 0 | OUTB0, OUTB1, OUTB4, OUTB5 |
| 1 | 0 | 0 | 0 | 1 | 1 | OUTB2, OUTB3, OUTB6, OUTB7 |
| 1 | 0 | 0 | 1 | 0 | 0 | OUTC0, OUTC1, OUTC4, OUTC5 |
| 1 | 0 | 0 | 1 | 0 | 1 | OUTC2, OUTC3, OUTC6, OUTC7 |
| 1 | 0 | 0 | 1 | 1 | 0 | OUTA0, OUTA1, OUTA4, OUTA5 OUTB0, OUTB1, OUTB4, OUTB5 OUTC0, OUTC1, OUTC4, OUTC5 |
| 1 | 0 | 0 | 1 | 1 | 1 | OUTA2, OUTA3, OUTA6, OUTA7 OUTB2, OUTB3, OUTB6, OUTB7 OUTC2, OUTC3, OUTC6, OUTC7 |
| 1 | 0 | 1 | 0 | 0 | 0 | OUTA0, OUTA1, OUTA2, OUTA3 |
| 1 | 0 | 1 | 0 | 0 | 1 | OUTA4, OUTA5, OUTA6, OUTA7 |
| 1 | 0 | 1 | 0 | 1 | 0 | OUTB0, OUTB1, OUTB2, OUTB3 |
| 1 | 0 | 1 | 0 | 1 | 1 | OUTB4, OUTB5, OUTB6, OUTB7 |
| 1 | 0 | 1 | 1 | 0 | 0 | OUTC0, OUTC1, OUTC2, OUTC3 |
| 1 | 0 | 1 | 1 | 0 | 1 | OUTC4, OUTC5, OUTC6, OUTC7 |
| 1 | 0 | 1 | 1 | 1 | 0 | OUTA0, OUTA1, OUTA2, OUTA3 OUTB0, OUTB1, OUTB2, OUTB3 OUTC0, OUTC1, OUTC2, OUTC3 |
| 1 | 0 | 1 | 1 | 1 | 1 | OUTA4, OUTA5, OUTA6, OUTA7 OUTB4, OUTB5, OUTB6, OUTB7 OUTC4, OUTC5, OUTC6, OUTC7 |
| 1 | 1 | 0 | 0 | 0 | 0 | OUTA0, OUTB0, OUTC0 |
| 1 | 1 | 0 | 0 | 0 | 1 | OUTA1, OUTB1, OUTC1 |
| 1 | 1 | 0 | 0 | 1 | 0 | OUTA2, OUTB2, OUTC2 |
| 1 | 1 | 0 | 0 | 1 | 1 | OUTA3, OUTB3, OUTC3 |
| 1 | 1 | 0 | 1 | 0 | 0 | OUTA4, OUTB4, OUTC4 |
| 1 | 1 | 0 | 1 | 0 | 1 | OUTA5, OUTB5, OUTC5 |
| 1 | 1 | 0 | 1 | 1 | 0 | OUTA6, OUTB6, OUTC6 |
| 1 | 1 | 0 | 1 | 1 | 1 | OUTA7, OUTB7, OUTC7 |
| 1 | 1 | 1 | 0 | 0 | 0 | (No terminal) |
| 1 | 1 | 1 | 0 | 0 | 1 | All OUTA |
| 1 | 1 | 1 | 0 | 1 | 0 | All OUTB |
| 1 | 1 | 1 | 0 | 1 | 1 | All OUTA, All OUTB |
| 1 | 1 | 1 | 1 | 0 | 0 | All OUTC |
| 1 | 1 | 1 | 1 | 0 | 1 | All OUTA, All OUTC |
| 1 | 1 | 1 | 1 | 1 | 0 | All OUTB, All OUTC |
| 1 | 1 | 1 | 1 | 1 | 1 | All OUTA, All OUTB, All OUTC |

Lighting Data (9 bits)

| Lighting data light_dat (8:0) | | | | | | | | |
|-------------------------------|--------|--------|--------|--------|--------------------|--------|--------|--------|
| Lighting speed | | | | | Lighting gradation | | | |
| spd(4) | spd(3) | spd(2) | spd(1) | spd(0) | brt(3) | brt(2) | brt(1) | brt(0) |

Lighting is controlled in each line with the values of the load registers. In lighting control, the gradation changes to the specified one at the specified lighting speed

The Lighting speed follows the table below.

The change time is specified with 5 bits;

| Lighting Speed spd(4:0) | | | | | Change time per 1/15 of brightness | Change time from 0/15 to 15/15 of brightness (and vice versa) |
|-------------------------|-----|-----|-----|-----|------------------------------------|---|
| (4) | (3) | (2) | (1) | (0) | | |
| 0 | 0 | 0 | 0 | 0 | Less than 60 μs | Less than 1 ms |
| 0 | 0 | 0 | 0 | 1 | 8.5 ms | 0.128 s |
| 0 | 0 | 0 | 1 | 0 | 10.7 ms | 0.160 s |
| 0 | 0 | 0 | 1 | 1 | 12.8 ms | 0.192 s |
| 0 | 0 | 1 | 0 | 0 | 14.9 ms | 0.224 s |
| 0 | 0 | 1 | 0 | 1 | 17.1 ms | 0.256 s |
| 0 | 0 | 1 | 1 | 0 | 21.3 ms | 0.320 s |
| 0 | 0 | 1 | 1 | 1 | 25.6 ms | 0.384 s |
| 0 | 1 | 0 | 0 | 0 | 29.9 ms | 0.448 s |
| 0 | 1 | 0 | 0 | 1 | 34.1 ms | 0.512 s |
| 0 | 1 | 0 | 1 | 0 | 42.7 ms | 0.640 s |
| 0 | 1 | 0 | 1 | 1 | 51.2 ms | 0.768 s |
| 0 | 1 | 1 | 0 | 0 | 59.7 ms | 0.896 s |
| 0 | 1 | 1 | 0 | 1 | 68.3 ms | 1.024 s |
| 0 | 1 | 1 | 1 | 0 | 85.3 ms | 1.280 s |
| 0 | 1 | 1 | 1 | 1 | 102 ms | 1.536 s |
| 1 | 0 | 0 | 0 | 0 | 119 ms | 1.792 s |
| 1 | 0 | 0 | 0 | 1 | 137 ms | 2.048 s |
| 1 | 0 | 0 | 1 | 0 | 171 ms | 2.560 s |
| 1 | 0 | 0 | 1 | 1 | 205 ms | 3.072 s |
| 1 | 0 | 1 | 0 | 0 | 239 ms | 3.584 s |
| 1 | 0 | 1 | 0 | 1 | 273 ms | 4.096 s |
| 1 | 0 | 1 | 1 | 0 | 341 ms | 5.120 s |
| 1 | 0 | 1 | 1 | 1 | 410 ms | 6.144 s |
| 1 | 1 | 0 | 0 | 0 | 478 ms | 7.168 s |
| 1 | 1 | 0 | 0 | 1 | 546 ms | 8.192 s |
| 1 | 1 | 0 | 1 | 0 | 683 ms | 10.24 s |
| 1 | 1 | 0 | 1 | 1 | 819 ms | 12.29 s |
| 1 | 1 | 1 | 0 | 0 | 956 ms | 14.34 s |
| 1 | 1 | 1 | 0 | 1 | 1,092 ms | 16.38 s |
| 1 | 1 | 1 | 1 | 0 | 1,365 ms | 20.48 s |
| 1 | 1 | 1 | 1 | 1 | 1,638 ms | 24.58 s |

Note: The change time per 1/15 of brightness represents the time required for a change from, for example, 10/15 to 11/15 of brightness.

The change time from 0/15 to 15/15 of brightness and vice versa represents the time required for a change from 0/15 of brightness (light OFF) to 15/15 of brightness (light completely ON). However, these times are median values and depend on the driving output PWM cycle.

The Lighting gradation follows the table below.

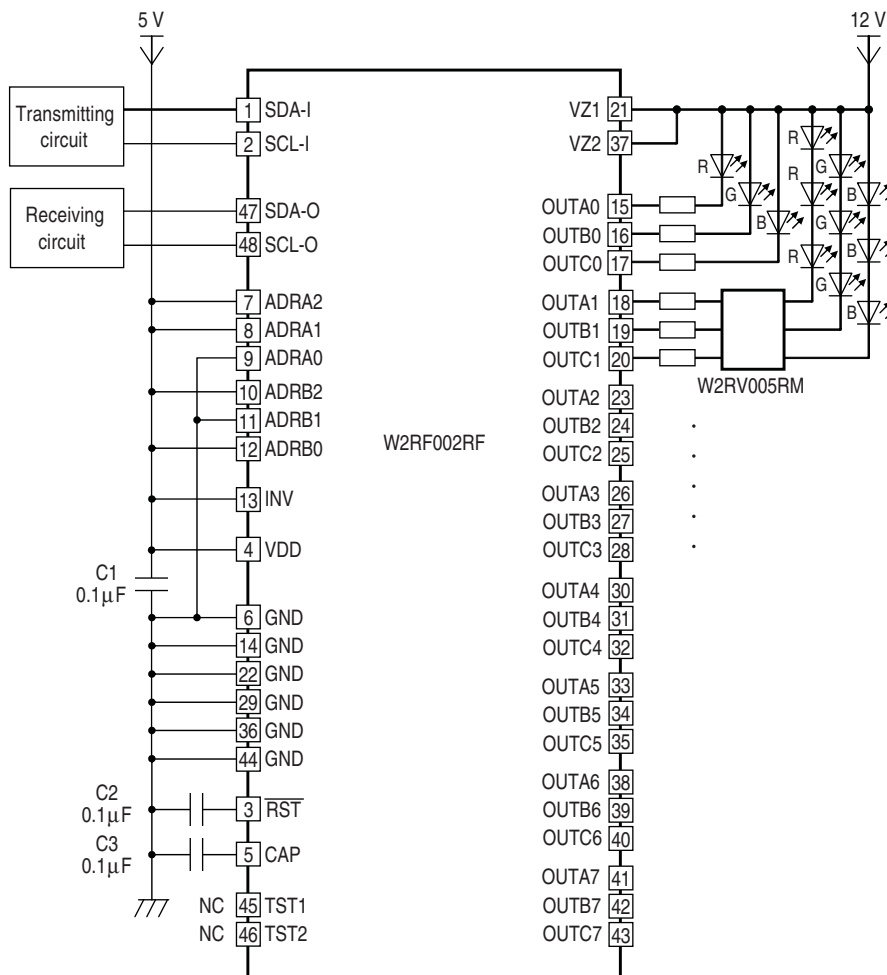
The brightness is specified with 4 bits;

| Lighting Gradation brt(3:0) | | | | Brightness | PWM duty ratio (reference) |
|-----------------------------|-----|-----|-----|-----------------------------|----------------------------|
| (3) | (2) | (1) | (0) | | |
| 0 | 0 | 0 | 0 | 0/15 (light OFF) | 0 % |
| 0 | 0 | 0 | 1 | 1/15 | 0.42 % |
| 0 | 0 | 1 | 0 | 2/15 | 0.84 % |
| 0 | 0 | 1 | 1 | 3/15 | 1.25 % |
| 0 | 1 | 0 | 0 | 4/15 | 1.78 % |
| 0 | 1 | 0 | 1 | 5/15 | 2.61 % |
| 0 | 1 | 1 | 0 | 6/15 | 3.76 % |
| 0 | 1 | 1 | 1 | 7/15 | 5.42 % |
| 1 | 0 | 0 | 0 | 8/15 | 7.96 % |
| 1 | 0 | 0 | 1 | 9/15 | 11.3 % |
| 1 | 0 | 1 | 0 | 10/15 | 16.7 % |
| 1 | 0 | 1 | 1 | 11/15 | 23.3 % |
| 1 | 1 | 0 | 0 | 12/15 | 35.2 % |
| 1 | 1 | 0 | 1 | 13/15 | 48.4 % |
| 1 | 1 | 1 | 0 | 14/15 | 73.4 % |
| 1 | 1 | 1 | 1 | 15/15 (Light completely ON) | 100 % |

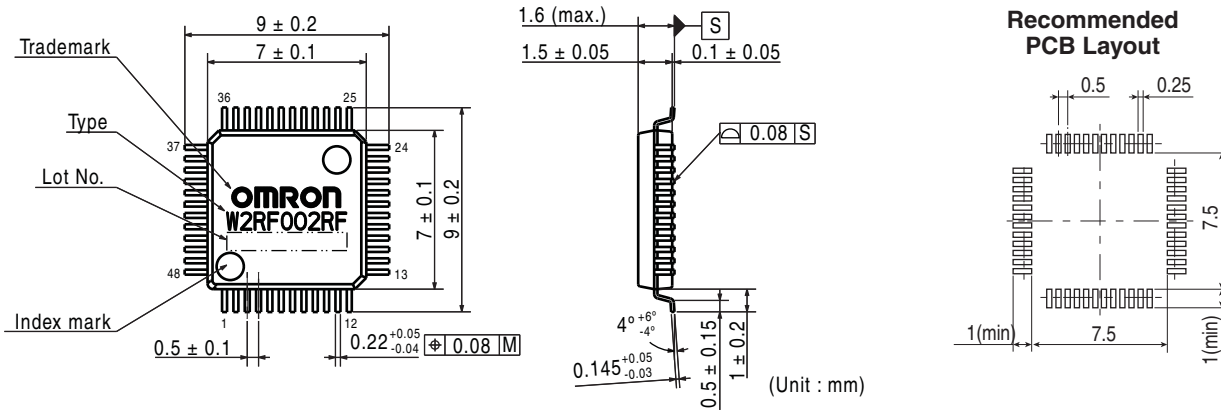
Functional Terminals/Setting Terminals

| | |
|----------------------|--|
| ADR terminals | The ADRA terminal and ADRB terminal set device address A and device address B, respectively. For "H" setting, connect the terminal to V_{DD} and for "L" setting, connect the terminal to GND |
| INV terminal | This terminal sets the polarity of OUT terminal. <ul style="list-style-type: none"> When the terminal is used with "L" as active (e.g., for directly driving an LED), connect the terminal to V_{DD} When the terminal is used with the "H" as active (e.g., for driving an LED with a driving transistor), connect the terminal to GND. |
| RST terminal | When the voltage of the RST terminal becomes "L", the internal circuit will be reset and the output will be open. |

Application Example



Dimensions

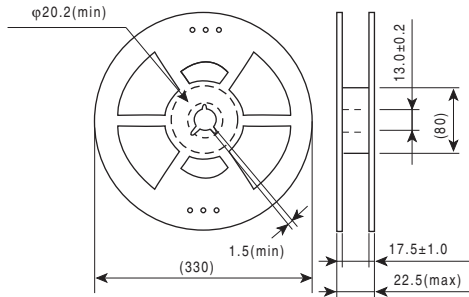


Tape Packaging

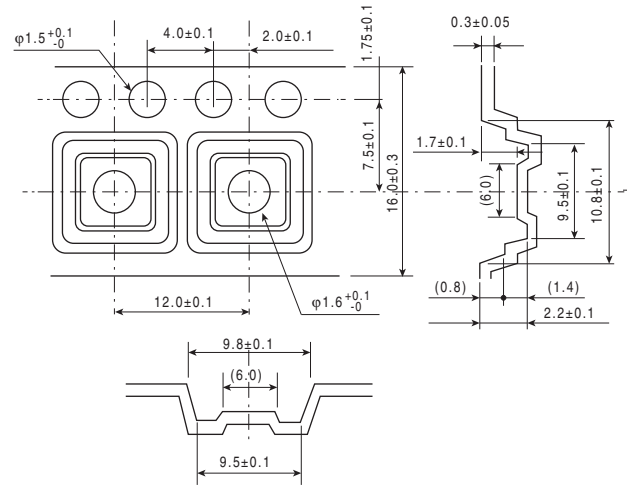
Packaging style: Embossed taping

Packaging quantity: 1,500 pcs/reel

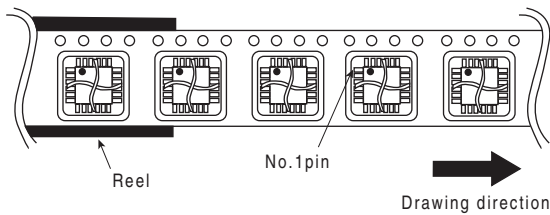
Reel Dimensions



Embossed Tape Dimensions



Direction of Insertion



Precautions for Use

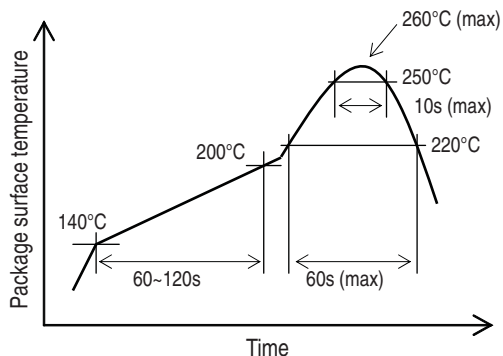
■ Correct Use

- The absolute maximum rating is the limit value which should not be exceeded even in a flash. Exceeding this value can cause deterioration of the characteristics or complete failure of the IC.
- Check the operation at the communication frequency to be used before using the device.
- Sufficiently take into consideration the static electricity, chattering and voltage of the input to be connected when determining each input circuit.
- Although the device contains an ESD protection circuit, static electricity that exceeds the function may damage the device. When handling the device, exercise due caution by, for example, grounding the human body.
- Due to potential damage, do not use product that has been dropped or that has come into contact with water.

■ Recommended Reflow Conditions

Allowable Temperature Profile Conditions

Product mounting method should be by Reflow and we recommend the following temperature profile. Reflow no more than two times, maximum.



Storage Conditions before Mounting

Moisture absorption by the plastic package will increase the possibility of faults, such as cracks; therefore, take enough care for storage.

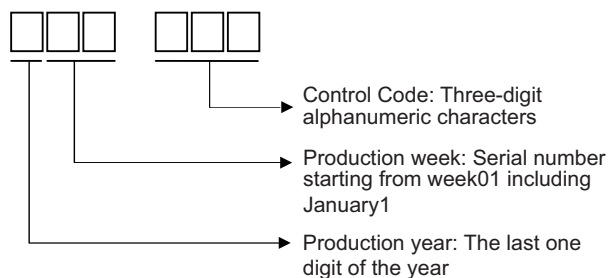
| Storage Conditions | Period |
|------------------------|----------|
| 5 to 30°C, 40 to 70%RH | One Year |

■ RoHS Directive Compliance

Models that are indicated as being RoHS compliant are free of the following six substances.

| | |
|----------------------|----------------|
| Lead: | 1,000 ppm max. |
| Mercury: | 1,000 ppm max. |
| Cadmium: | 100 ppm max. |
| Hexavalent chromium: | 1,000 ppm max. |
| PBB: | 1,000 ppm max. |
| PBDE: | 1,000 ppm max. |

■ Lot Code Indication



All sales are subject to Omron Electronic Components LLC standard terms and conditions of sale, which can be found at http://www.components.omron.com/components/web/webfiles.nsf/sales_terms.html

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
To convert millimeters into inches, multiply by 0.03937. To convert grams into ounces, multiply by 0.03527.

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