THE DATASHEET OF

AD5262BRUZ200

1-/2-Channel 15 V Digital Potentiometer

AD5260/AD5262

FEATURES

256 positions
AD5260: 1 channel
AD5262: 2 channels (independently programmable)
Potentiometer replacement
20 kΩ, 50 kΩ, 200 kΩ
Low temperature coefficient: 35 ppm/°C
4-wire, SPI-compatible serial data input
5 V to 15 V single-supply; ±5.5 V dual-supply operation
Power on midscale preset

APPLICATIONS

Mechanical potentiometer replacement
Instrumentation: gain, offset adjustment
Stereo channel audio level control
Programmable voltage-to-current conversion
Programmable filters, delays, time constants
Line impedance matching
Low resolution DAC replacement

GENERAL DESCRIPTION

The AD5260/AD5262 provide a single- or dual-channel, 256-position, digitally controlled variable resistor (VR) device.[1] These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5260/AD5262 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 20 Ω, 50 Ω, or 200 Ω has a nominal temperature coefficient of 35 ppm/°C. Unlike the majority of the digital potentiometers in the market, these devices can operate up to 15 V or ±5 V provided proper supply voltages are furnished.

Each VR has its own VR latch that holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register, which is loaded from a standard 3-wire serial-input digital interface. The AD5260 contains an 8-bit serial register whereas the AD5262 contains a 9-bit serial register. Each bit is clocked into the register on the positive edge of the CLK pin. The AD5262 address bit determines the corresponding VR latch to be loaded with the last eight bits of the data word during the positive edging of $\overline{CS}$ strobe. A serial data output pin at the opposite end of the serial register enables simple daisy-chaining in multiple VR applications without additional external decoding logic. An optional reset pin ($\overline{PR}$) forces the wiper to the midscale position by loading 0x80 into the VR latch.

The AD5260/AD5262 are available in thin surface-mount 14-lead TSSOP and 16-lead TSSOP packages. All parts are guaranteed to operate over the extended industrial temperature range of −40°C to +85°C.

[1] The terms digital potentiometers, VR, and RDAC are used interchangeably.

FUNCTIONAL BLOCK DIAGRAMS

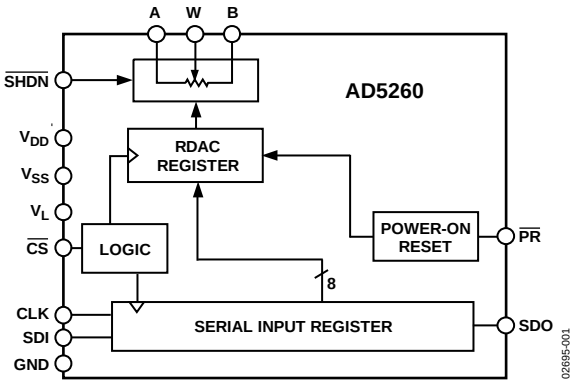

Figure 1. AD5260

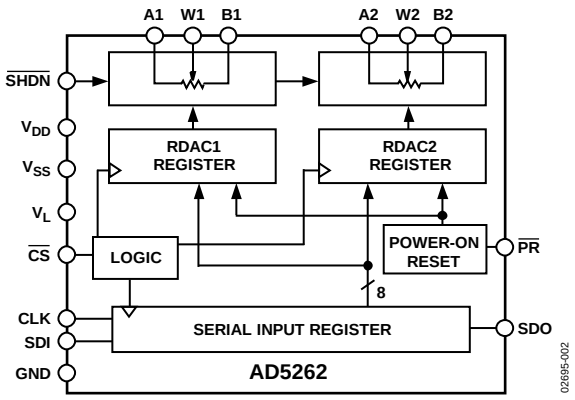

Figure 2. AD5262

Rev. A

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REVISION HISTORY

8/10—Rev. 0 to Rev. A

Updated Format ... Universal
Deleted Figure 1; Renumbered Sequentially ... 1
Changes to General Description Section ... 1
Changes to Conditions of Channel Resistance Matching (AD5262 only) Parameter, Voltage Divider Temperature Coefficient Parameter, Full-Scale Error Parameter, and Zero-Scale Error Parameter, Table 1 ... 3
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Deleted Potentiometer Family Selection Guide ... 18
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Updated Outline Dimensions ... 23
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3/02—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—20 kΩ, 50 kΩ, 200 kΩ VERSIONS

V_{DD} = +15 V, V_{SS} = 0 V, or V_{DD} = +5 V, V_{SS} = −5 V; V_L = +5 V; V_A = +5 V, V_B = 0 V, −40°C < T_A < +85°C, unless otherwise noted.
The AD5260/AD5262 contain 1968 transistors. Die size: 89 mil × 105 mil (9345 sq mil).

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE		Specifications apply to all VRs				
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±¼	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−1	±½	+1	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	Wiper = no connect		35		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{AB}		60	150	Ω
Channel Resistance Matching (AD5262 only)	$\Delta R_{WB}/R_{WB}$	Channel 1 and Channel 2 R_{WB}, D_X = 0x80		0.1		%
Resistance Drift	ΔR_{AB}			0.05		%
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE		Specifications apply to all VRs				
Resolution	N		8			Bits
Differential Nonlinearity[4]	DNL		−1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		−1	±1/2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = half scale		5		ppm/°C
Full-Scale Error	W_{FSE}	Code = full scale	−2	−1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0	1	2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Ax and Bx Capacitance[6]	$C_{A,B}$	f = 5 MHz, measured to GND, code = half scale		25		pF
Wx Capacitance[6]	C_W	f = 1 MHz, measured to GND, code = half scale		55		pF
Common-Mode Leakage Current	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
Shutdown Current[7]	I_{SHDN}				5	µA
DIGITAL INPUTS and OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_L = 3 V, V_{SS} = 0 V	2.1			V
Input Logic Low	V_{IL}	V_L = 3 V, V_{SS} = 0 V			0.6	V
Output Logic High (SDO)	V_{OH}	$R_{PULL-UP}$ = 2 kΩ to 5 V	4.9			V
Output Logic Low (SDO)	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current[8]	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_L		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	4.5		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±5.5	V
Logic Supply Current	I_L	V_L = 5 V			60	µA
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V			1	µA
Negative Supply Current	I_{SS}	V_{SS}= −5 V			1	µA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = −5 V			0.3	mW
Power Supply Sensitivity	PSS	ΔV_{DD}= +5 V, ±10%		0.003	0.01	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW	R_{AB} = 20 kΩ/50 kΩ/200 kΩ		310/130/30		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V_{RMS}, V_B = 0 V, f = 1 kHz, R_{AB} = 20 kΩ		0.014		%
V_W Settling Time	t_S	V_A = +5 V, V_B = −5 V, ±1 LSB error band, R_{AB} = 20 kΩ		5		µs
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V, measure V_W with adjacent RDAC making full-scale code change (AD5262 only)		1		nV-sec
Analog Crosstalk	C_{TA}	V_{A1} = V_{DD}, V_{B1} = 0 V, measure V_{W1} with V_{W2} = 5 V p-p at f = 10 kHz, R_{AB} = 20 kΩ/200 kΩ (AD5262 only)		–64		dB
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 20 kΩ, f = 1 kHz		13		nV/√Hz
INTERFACE TIMING CHARACTERISTICS[6, 12]		Specifications apply to all parts				
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns
CLK to SDO Propagation Delay[13]	t_{PD}	R_L = 1 kΩ, C_L< 20 pF	1		160	ns
$\overline{CS}$ Setup Time	t_{CSS}		5			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		20			ns
Reset Pulse Width	t_{RS}		50			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

[1] Typical values represent average readings at 25°C and V_{DD} = +5 V, V_{SS} = −5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W = V_{DD}/R for both V_{DD} = +5 V and V_{SS} = −5V.
[3] V_{AB} = V_{DD}, wiper = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the Ax terminals. All Ax terminals are open-circuit in shutdown mode.
[8] Worst-case supply current consumed when all logic-input levels set at 2.4 V, which is the standard characteristic of CMOS logic.
[9] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[10] All dynamic characteristics use V_{DD} = +5 V, V_{SS} = −5 V, V_L = +5 V.
[11] Measured at V_W where an adjacent V_W is making a full-scale voltage change.
[12] See Figure 5 for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_L = 5 V.
[13] Propagation delay depends on value of V_{DD}, R_L, and C_L.

TIMING DIAGRAMS

Table 2. AD5260 8-Bit Serial Data Word Format

Data							
B7 (MSB)	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0 (LSB)**
D7	D6	D5	D4	D3	D2	D1	D0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table 3. AD5262 9-Bit Serial Data Word Format

ADDR	Data							
B8	**B7 (MSB)**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0 (LSB)**
A0	D7	D6	D5	D4	D3	D2	D1	D0
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

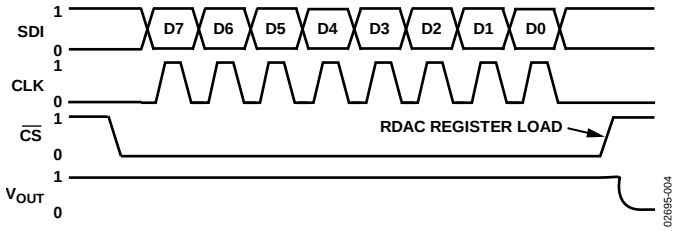


Figure 3. AD5260 Timing Diagram

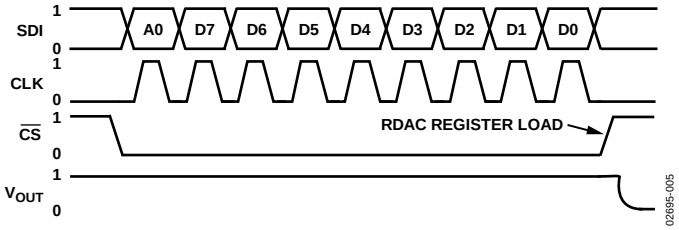


Figure 4. AD5262 Timing Diagram

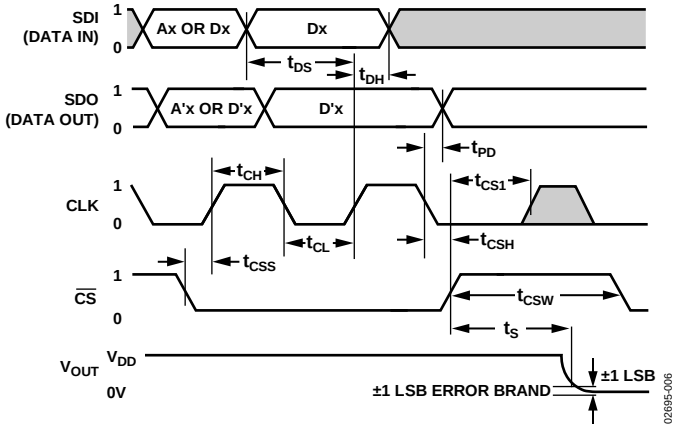


Figure 5. Detailed Timing Diagram

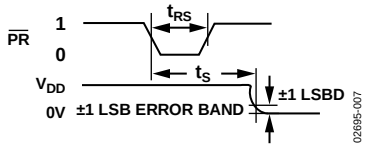


Figure 6. Preset Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A =25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +17 V
V_{SS} to GND	0 V to −7 V
V_{DD} to V_{SS}	17 V
V_L to GND	0 V to +7 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
A_X to B_X, A_X to W_X, B_X to W_X	
Intermittent[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	−0.3 V to V_L + 0.3 V, or +7 V (whichever is less)
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature ($T_{J\,MAX}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering,10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance[2] θ_{JA}	
14-Lead TSSOP	206°C/W
16-Lead TSSOP	150°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance setting.

[2] Package power dissipation = $(T_{J\,MAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

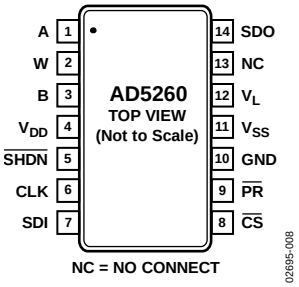


Figure 7. AD5260 Pin Configuration

Table 5. AD5260 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A	A Terminal.
2	W	Wiper Terminal.
3	B	B Terminal.
4	V_{DD}	Positive Power Supply. Specified for operation at both 5 V or 15 V (sum of $\|V_{DD}\| + \|V_{SS}\| \leq 15$ V).
5	$\overline{SHDN}$	Active Low Input. Terminal A, open-circuit. Shutdown controls variable resistor.
6	CLK	Serial Clock Input, Positive Edge Triggered.
7	SDI	Serial Data Input.
8	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data is loaded into the RDAC register.
9	$\overline{PR}$	Active Low Preset to Midscale. Sets RDAC registers to 0x80.
10	GND	Ground.
11	V_{SS}	Negative Power Supply. Specified for operation from 0 V to −5 V.
12	V_L	Logic Supply Voltage. Needs to be the same voltage as the digital logic controlling the AD5260.
13	NC	No Connect. Users should not connect anything other than a dummy pad on this pin.
14	SDO	Serial Data Output. Open-drain transistor requires a pull-up resistor.

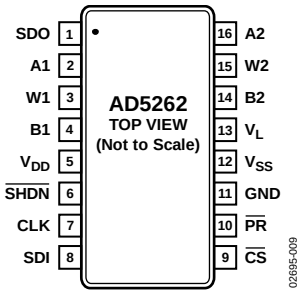


Figure 8. AD5262 Pin Configuration

Table 6. AD5262 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SDO	Serial Data Output. Open-drain transistor requires a pull-up resistor.
2	A1	A Terminal RDAC 1.
3	W1	Wiper RDAC 1, Address A0 = 0.
4	B1	B Terminal RDAC 1.
5	V_{DD}	Positive Power Supply. Specified for operation at both 5 V or 15 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| \leq 15$ V)
6	$\overline{SHDN}$	Active Low Input. Terminal A, open-circuit. Shutdown controls variable Resistor 1 through Resistor R2.
7	CLK	Serial Clock Input, Positive Edge Triggered.
8	SDI	Serial Data Input.
9	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the Address Bit A0, and loaded into the target RDAC register.
10	$\overline{PR}$	Active Low Preset to Midscale. Sets RDAC registers to 0x80.
11	GND	Ground.
12	V_{SS}	Negative Power Supply. Specified for operation at either 0 V or −5 V (sum of $\|V_{DD}\| + \|V_{SS}\| < 15$ V).
13	V_L	Logic Supply Voltage. Needs to be same voltage as the digital logic controlling the AD5262.
14	B2	B Terminal RDAC 2.
15	W2	Wiper RDAC 2, Address A0 = 1.
16	A2	A Terminal RDAC 2.

TYPICAL PERFORMANCE CHARACTERISTICS

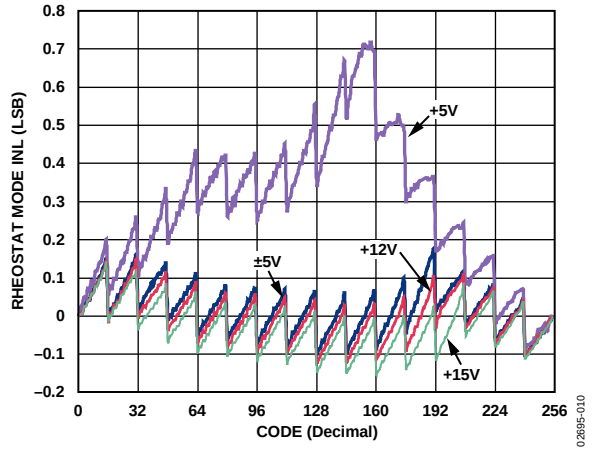


Figure 9. R-INL vs. Code vs. Supply Voltages

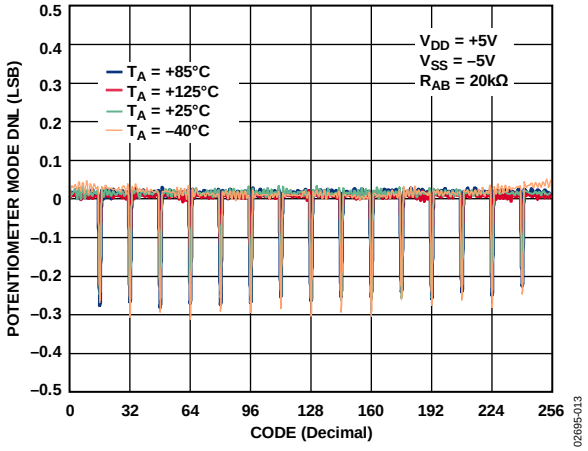


Figure 12. DNL vs. Code

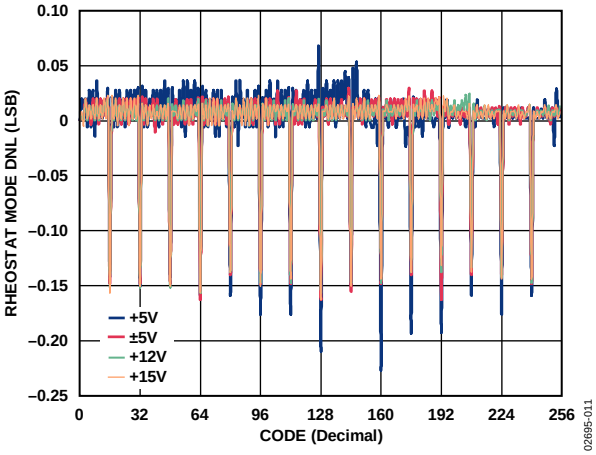


Figure 10. R-DNL vs. Code vs. Supply Voltages

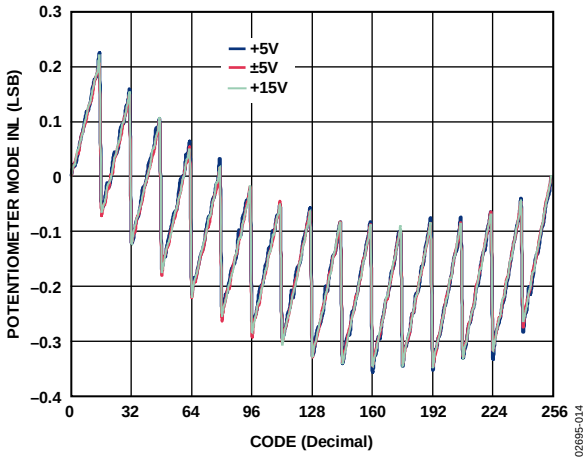


Figure 13. INL vs. Code vs. Supply Voltages

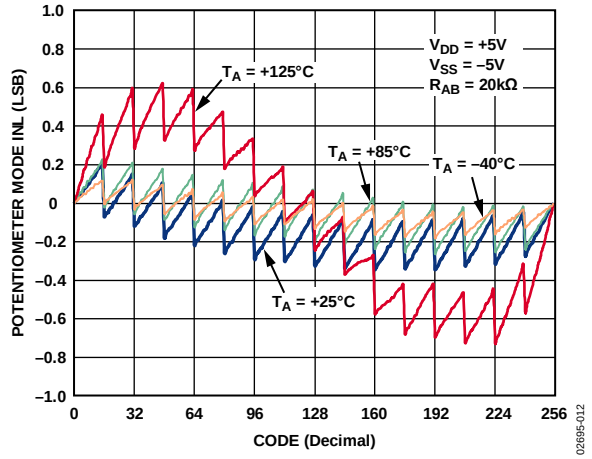


Figure 11. INL vs. Code

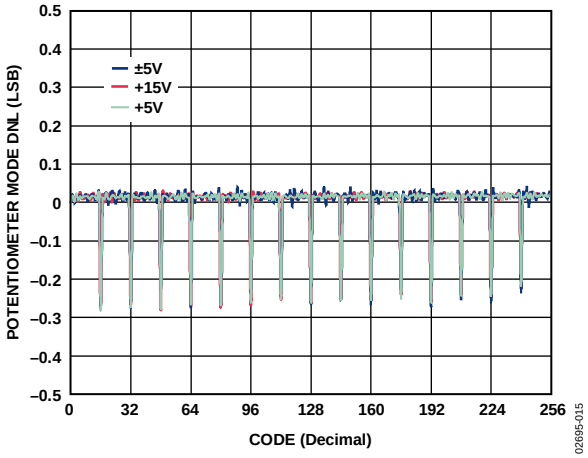


Figure 14. DNL vs. Code vs. Supply Voltages

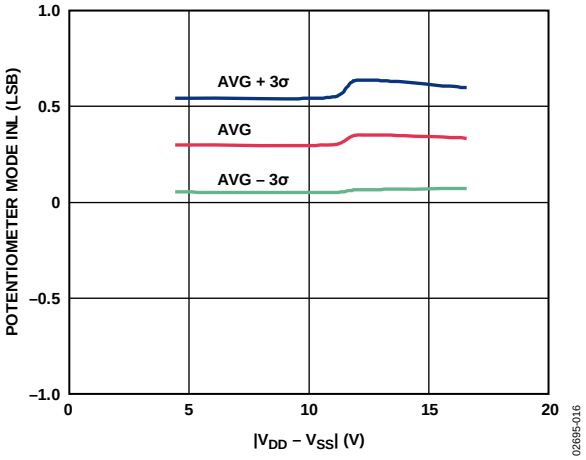


Figure 15. INL vs. Supply Voltages

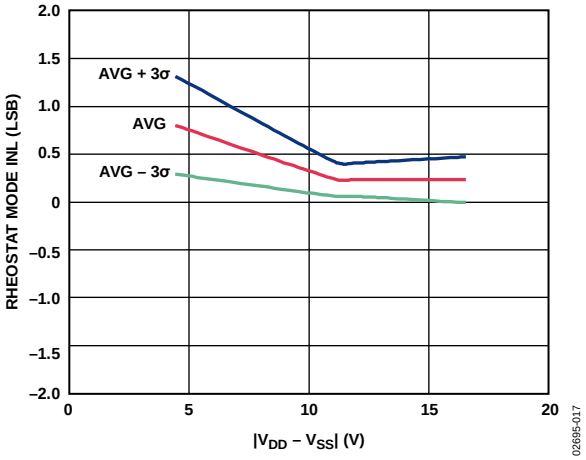


Figure 16. R-INL vs. Supply Voltages

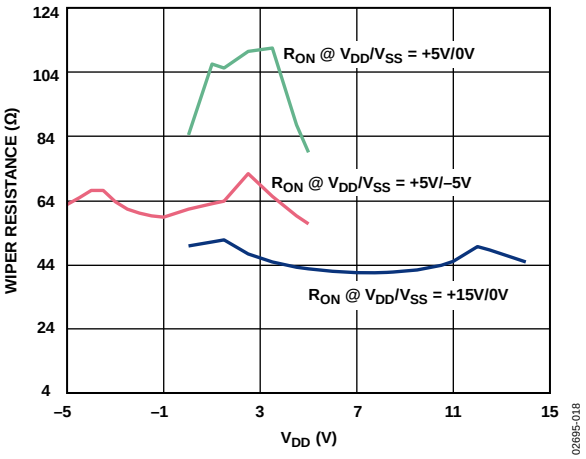


Figure 17. Wiper On Resistance vs. Bias Voltage

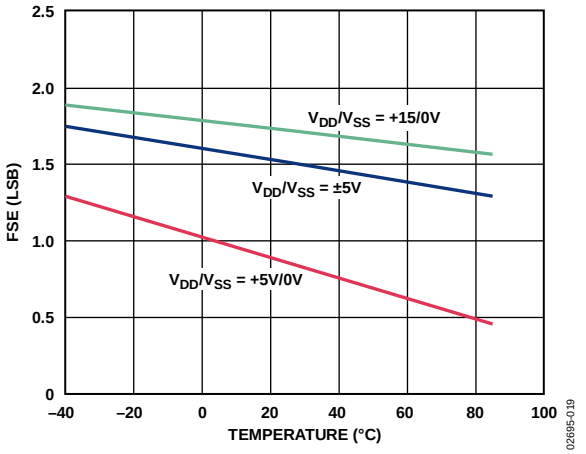


Figure 18. Full-Scale Error vs. Temperature

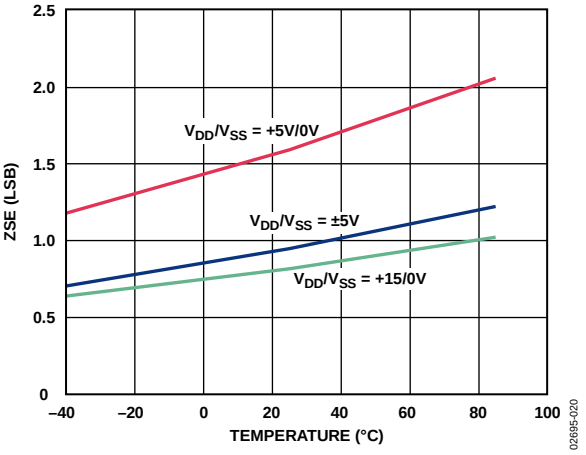


Figure 19. Zero-Scale Error vs. Temperature

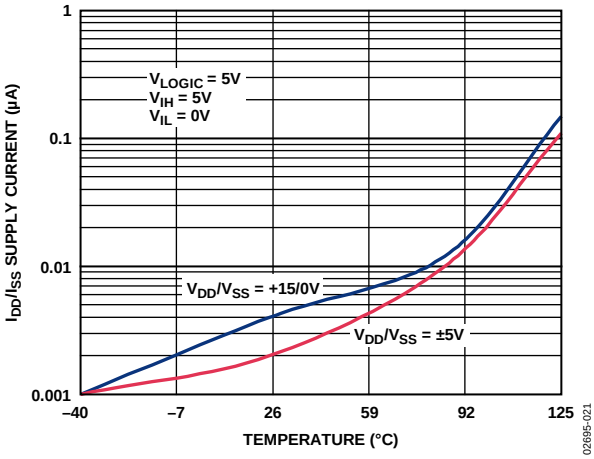


Figure 20. Supply Current vs. Temperature

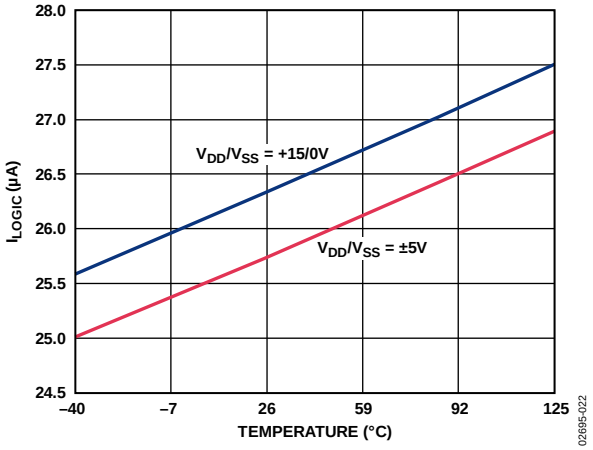


Figure 21. I_{LOGIC} vs. Temperature

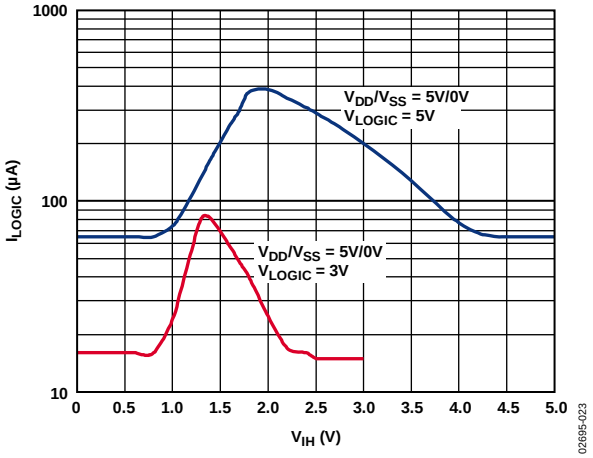


Figure 22. I_{LOGIC} vs. Digital Input Voltage

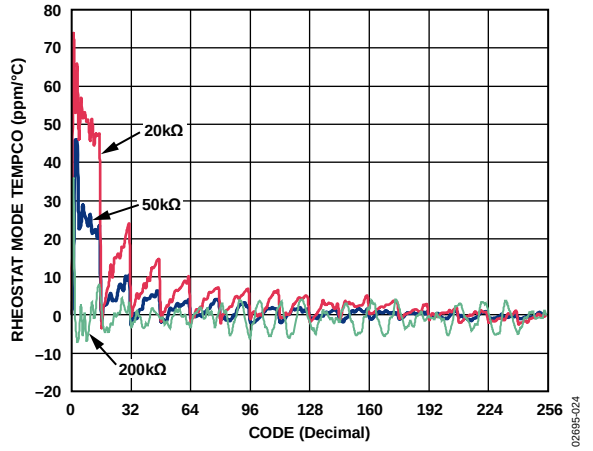


Figure 23. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

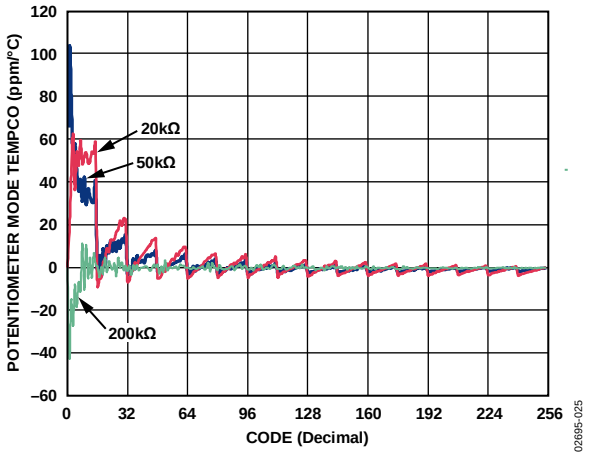


Figure 24. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

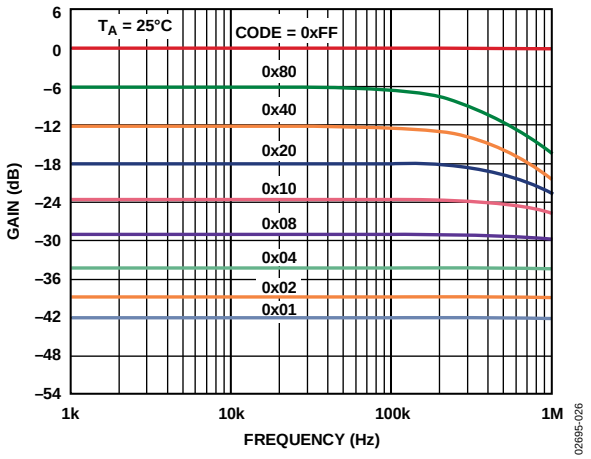


Figure 25. Gain vs. Frequency vs. Code, R_{AB} = 20 kΩ

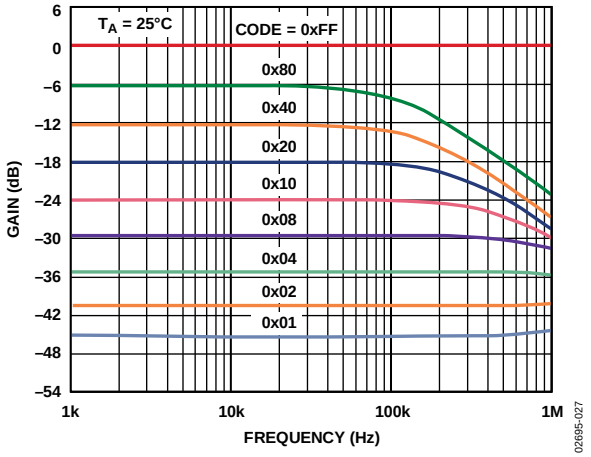


Figure 26. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

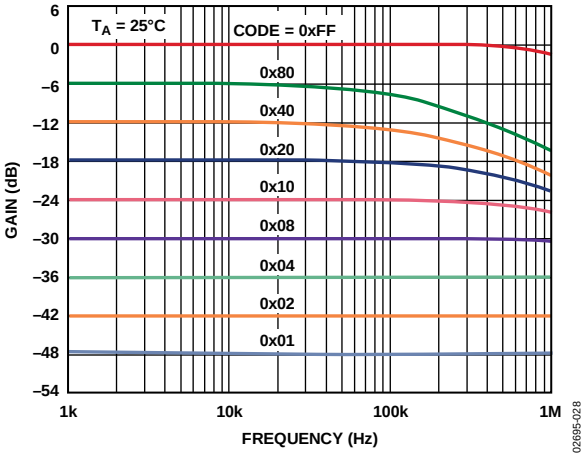


Figure 27. Gain vs. Frequency vs. Code, R_{AB} = 200 kΩ

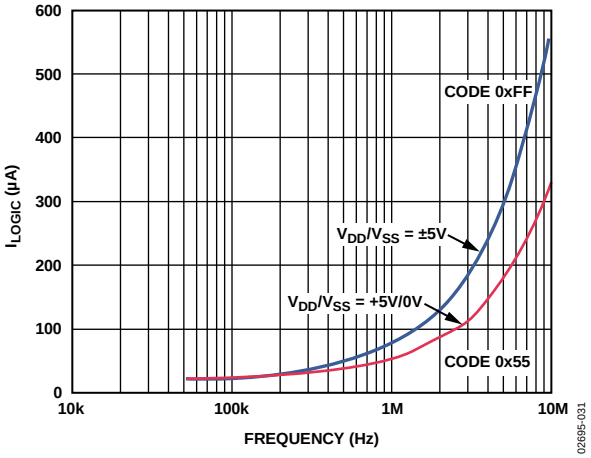


Figure 30. I_{LOGIC} vs. Frequency

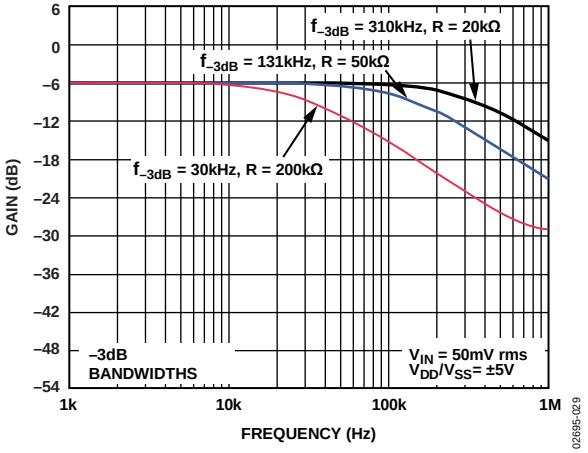


Figure 28. –3 dB Bandwidth

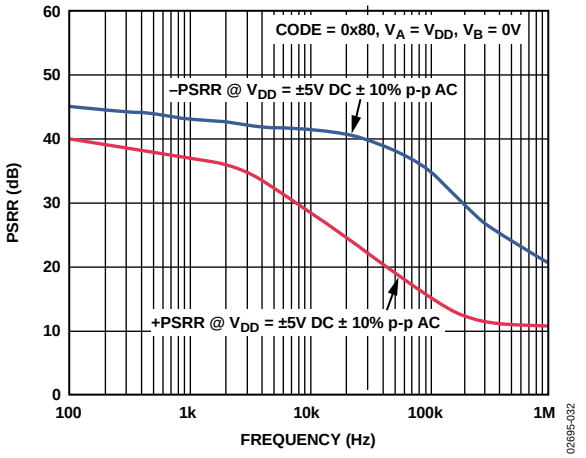


Figure 31. PSRR vs. Frequency

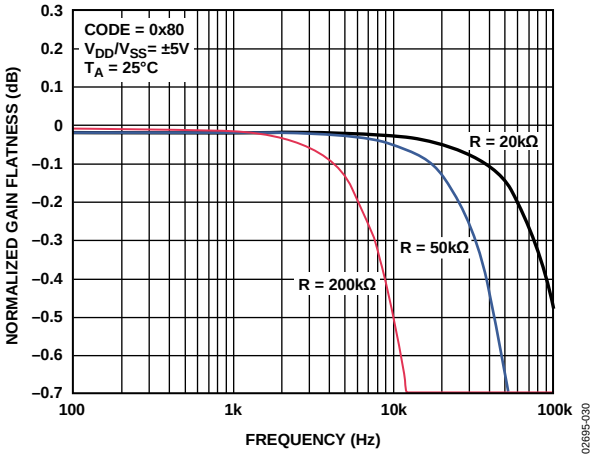


Figure 29. Normalized Gain Flatness vs. Frequency

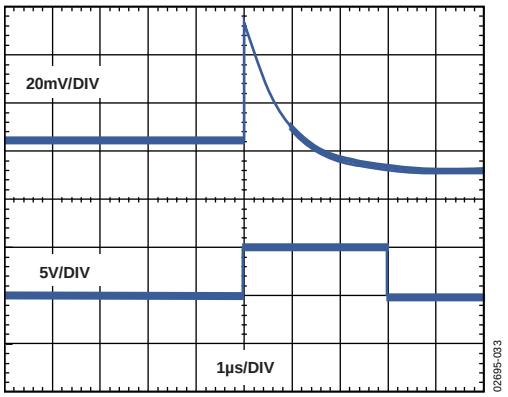


Figure 32. Midscale Glitch Energy, Code 0x80 to 0x7F

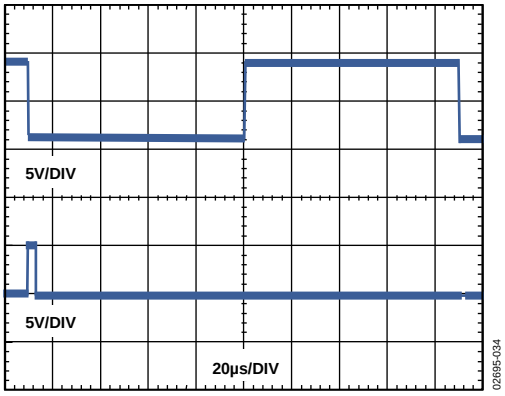


Figure 33. Large Signal Settling Time

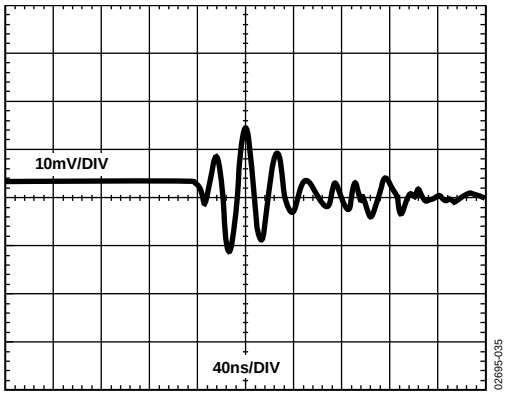


Figure 34. Digital Feedthrough vs. Time

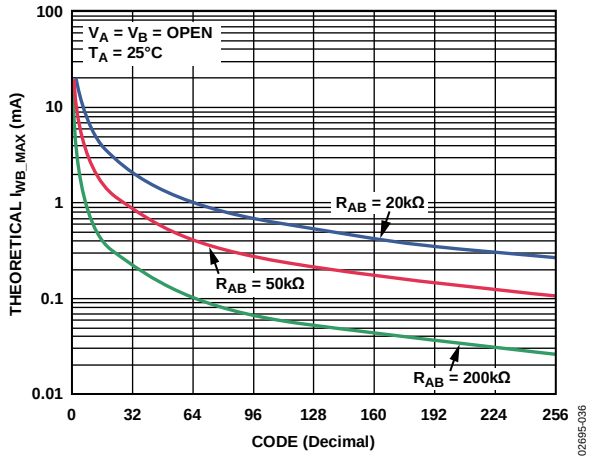


Figure 35. Theoretical Maximum Current vs. Code

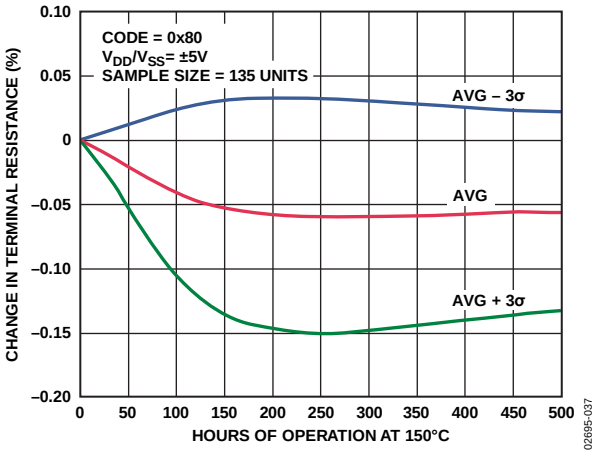


Figure 36. Long-Term Resistance Drift

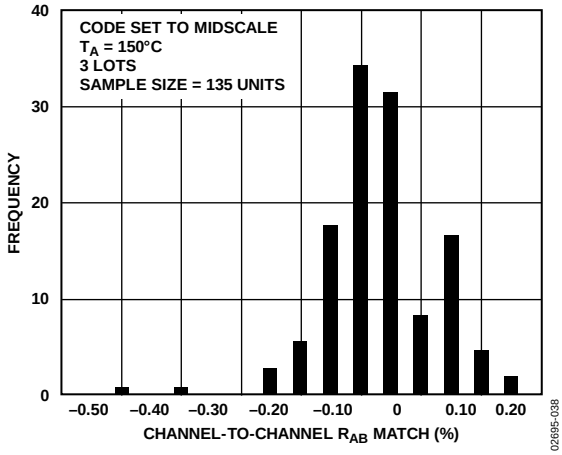


Figure 37. Channel-to-Channel Resistance Matching (AD5262)

TEST CIRCUITS

Figure 38 to Figure 46 define the test conditions used in Table 1.

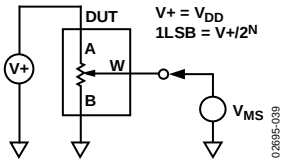


Figure 38. Potentiometer Divider Nonlinearity Error (INL, DNL)

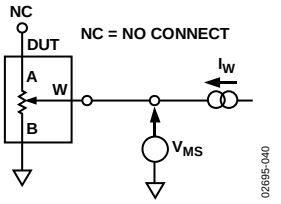


Figure 39. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

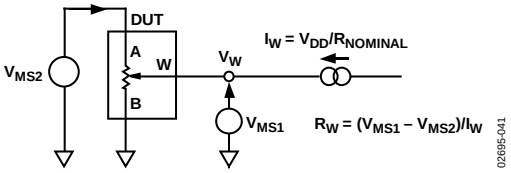


Figure 40. Wiper Resistance

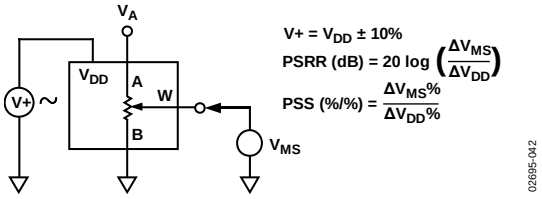


Figure 41. Power Supply Sensitivity (PSS, PSSR)

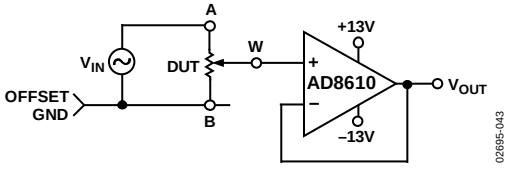


Figure 42. Gain vs. Frequency

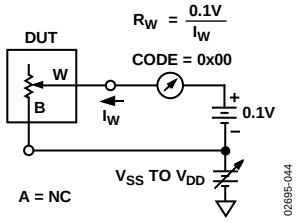


Figure 43. Incremental On Resistance

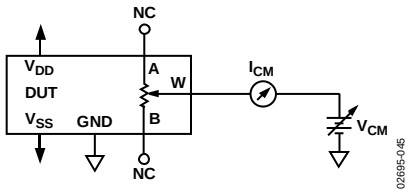


Figure 44. Common-Mode Leakage Current

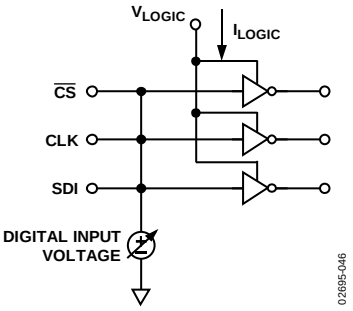


Figure 45. V_{LOGIC} Current vs. Digital Input Voltage

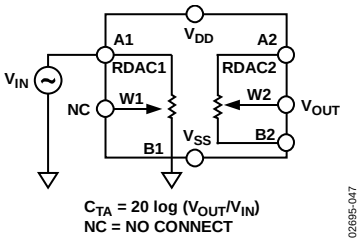


Figure 46. Analog Crosstalk

THEORY OF OPERATION

The AD5260/AD5262 provide a single- or dual-channel, 256-position, digitally controlled variable resistor (VR) device and operate up to 15 V maximum voltage. Changing the programmed VR settings is accomplished by clocking an 8-/9-bit serial data word into the SDI (serial data input) pin. For the AD5262, the format of this data word is one address bit. A0 represents the first bit, B8, followed by eight data bits, B7 to B0, with MSB first. Table 2 and Table 3 provide the serial register data word format. See Table 7 for the AD5262 address assignment to decode the location of the VR latch receiving the serial register data in Bit B7 through Bit B0. VR outputs can be changed one at a time in random sequence. The AD5260/AD5262 preset to a midscale, simplifying fault condition recovery at power-up. Midscale can also be achieved at any time by asserting the $\overline{PR}$ pin. Both parts have an internal power-on preset that places the wiper in a midscale preset condition at power-on. Operation of the power-on preset function depends only on the state of the V_L pin.

The AD5260/AD5262 contain a power shutdown $\overline{SHDN}$ pin that places the RDAC in an almost zero power consumption state where Terminals Ax are open circuited and the Wiper W is connected to B, resulting in only leakage currents being consumed in the VR structure. In the shutdown mode, the VR latch settings are maintained so that, when returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

Table 7. AD5262 Address Decode Table

A0	Latch Loaded
0	RDAC1
1	RDAC2

DIGITAL INTERFACING

The AD5260/AD5262 contain a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). For the AD5260, the 8-bit serial word must be loaded with the MSB first. The format of the word is shown in Table 2. For the AD5262, the 9-bit serial word must be loaded with Address Bit A0 first, then the MSB of the data. The format of the word is shown in Table 3.

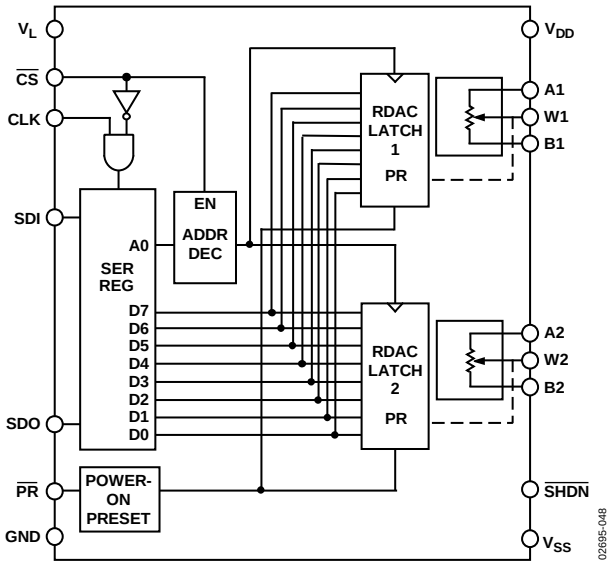


Figure 47. AD5262 Block Diagram

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. Figure 47 shows more detail of the internal digital circuitry. When $\overline{CS}$ is low, the clock loads data into the serial input register on each positive clock edge (see Table 8).

Table 8. Truth Table[1]

CLK	$\overline{CS}$	$\overline{PR}$	$\overline{SHDN}$	Register Activity
Low	Low	High	High	No SR effect, enables SDO pin.
↑	Low	High	High	Shift one bit in from the SDI pin. The eighth previously entered bit is shifted out of the SDO pin.
X	↑	High	High	Load SR data into RDAC latch.
X	High	High	High	No operation.
X	X	Low	High	Sets all RDAC latches to half scale, wiper centered, and SDO latch cleared.
X	High	↑	High	Latches all RDAC latches to 0x80.
X	High	High	Low	Open circuits all Resistor A terminals, connects W to B, and turns off SDO output transistor.

[1] ↑ = positive edge, X = don't care, SR = shift register.

The data setup and data hold times in Table 1 determine the data valid time requirements. The AD5260 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. For the AD5262, the last nine bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. Any extra bits are ignored. At the same time $\overline{CS}$ goes high, it gates the address decoder, enabling one of two positive edge-triggered AD5262 RDAC latches (see Figure 48).

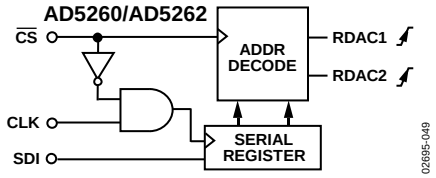


Figure 48. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data word completing one RDAC update. For the AD5262, two separate 9-bit data words must be clocked in to change both VR settings.

During shutdown ($\overline{SHDN}$), the SDO output pin is forced to the off (logic high) state to disable power dissipation in the pull-up resistor. See Figure 49 for the equivalent SDO output circuit schematic.

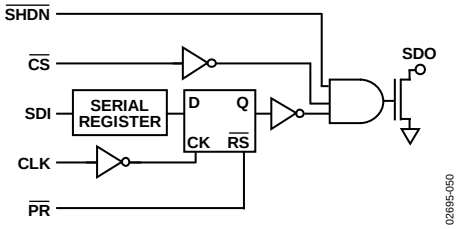


Figure 49. Detail SDO Output Schematic of the AD5260

All digital inputs are protected with a series input resistor and parallel Zener ESD structure as shown in Figure 50. This applies to the $\overline{CS}$, SDI, SDO, $\overline{PR}$, $\overline{SHDN}$, and CLK digital input pins.

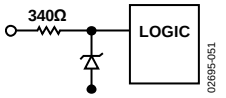


Figure 50. ESD Protection of Digital Pins

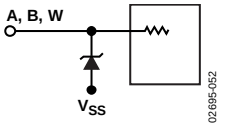


Figure 51. ESD Protection of Resistor Terminals

DAISY-CHAIN OPERATION

The serial data output (SDO) pin contains an open-drain N-channel FET. This output requires a pull-up resistor to transfer data to the SDI pin of the next package. This allows for daisy-chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be larger than the V_{DD} supply voltage. It is recommended to increase the clock period when using a pull-up resistor to the SDI pin of the following device in series because capacitive loading at the daisy-chain node connecting SDO and SDI between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see Figure 52). If two AD5260s are daisy-chained, this requires a total of 16 bits of data. The first eight bits, complying with the format shown in Table 2, go to U2, and the second eight bits with the same format go to U1. The $\overline{CS}$ pin should be kept low until all 16 bits are clocked into their respective serial registers, and the $\overline{CS}$ pin is then pulled high to complete the operation.

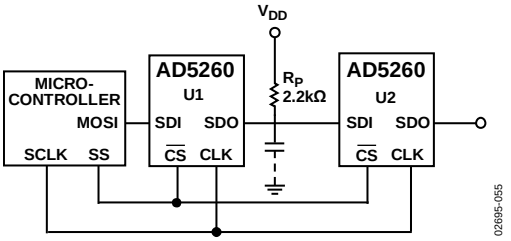


Figure 52. Daisy-Chain Configuration

RDAC STRUCTURE

The RDAC contains a string of equal resistor segments with an array of analog switches that act as the wiper connection. The number of positions is the resolution of the device. The AD5260/AD5262 have 256 connection points, allowing it to provide better than 0.4% settability resolution. Figure 53 shows an equivalent structure of the connections between the three terminals that make up one channel of the RDAC. SW_A and SW_B are always on, while one of the switches SW(0) to SW(2^N – 1) is on one at a time, depending on the resistance position decoded from the data bits. Because the switch is not ideal, there is a 60 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage is, the higher the wiper resistance becomes. Similarly, the higher the temperature is, the higher the wiper resistance becomes. Users should be aware of the contribution of the wiper resistance when accurate prediction of the output resistance is needed.

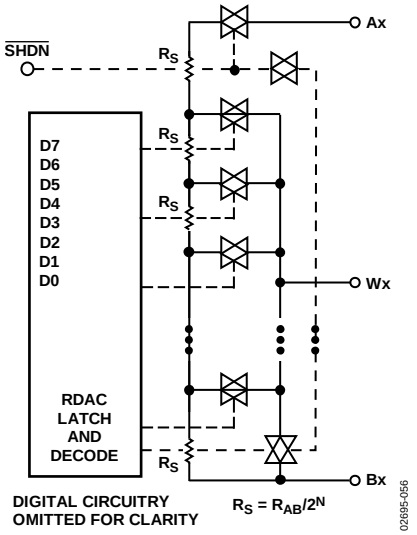


Figure 53. Simplified RDAC Architecture

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistances of the RDAC between Terminal A and Terminal B are available with values of 20 kΩ, 50 kΩ, and 200 kΩ. The final three digits of the part number determine the nominal resistance value, for example, 20 kΩ = 20, 50 kΩ = 50, 200 kΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points

accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 60 Ω wiper contact resistance, such a connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B. The second connection is the first tap point corresponding to 138 Ω (R_{WB} = R_{AB}/256 R_W = 78 Ω + 60 Ω) for Data 0x01. The third connection is the next tap point representing 216 Ω (78 × 2 + 60) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19,982 Ω (R_{AB} – 1 LSB + R_W). The wiper does not directly connect to the B terminal. See Figure 53 for a simplified diagram of the equivalent RDAC circuit.

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where D is the decimal equivalent of the binary code that is loaded in the 8-bit RDAC register and R_{AB} is the nominal end-to-end resistance.

For example, when R_{AB} = 20 kΩ, V_B = 0 V, and the A terminal is open circuit, the following output resistance values of R_{WB} are set for the RDAC latch codes shown in Table 9. The result is the same if Terminal A is tied to W.

Table 9. R_{WB} vs. Code

RDAC (Dec)	R_{WB} (Ω)	Output State
256	19,982	Full scale (R_{AB} – 1 LSB + R_W)
128	10,060	Midscale
1	138	1 LSB
0	60	Zero-scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer the RDAC replaces, the AD5260/AD5262 are completely symmetrical. The resistance between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. Figure 54 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, the B terminal can be left floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For example, when R_{AB} = 20 kΩ, V_A = 0 V, and the B terminal is open circuit, the following output resistance values of R_{WA} are set for the RDAC latch codes shown in Table 10. The result is the same if Terminal B is tied to Terminal W.

Table 10. R_{WA} vs. Code

RDAC (Dec)	R_{WA} (Ω)	Output State
256	60	Full scale
128	10,060	Half scale
1	19,982	1 LSB
0	20,060	Zero scale

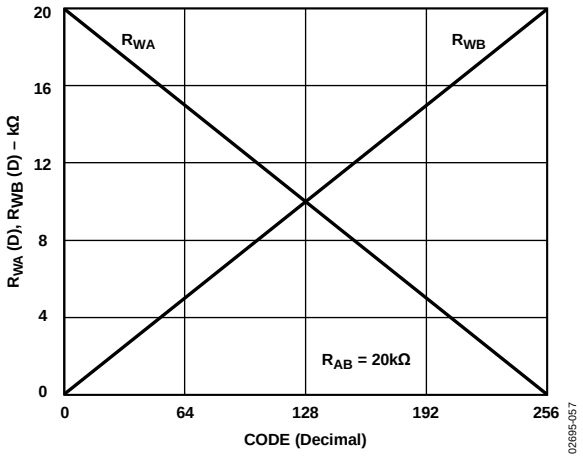


Figure 54. AD5260/AD5262 Equivalent RDAC Circuit

The typical distribution of the nominal resistance R_{AB} from channel to channel matches within ±1%. Device-to-device matching is process lot-dependent with the worst case of ±30% variation. However, because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Ignore the effect of the wiper resistance. For example, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at W-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. Because the AD5260/AD5262 operate from dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} \times V_{AB} + V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values; therefore, the drift reduces to 5 ppm/°C.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ a compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance (see Figure 55). Note that the digital ground should also be joined remotely to the analog ground to minimize the ground bounce.

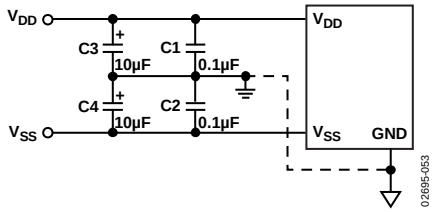


Figure 55. Power Supply Bypassing

TERMINAL VOLTAGE OPERATING RANGE

The AD5260/AD5262 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 56).

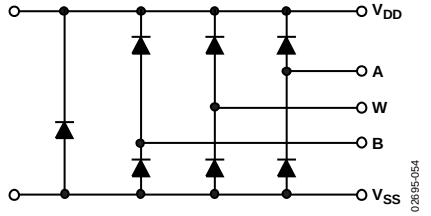


Figure 56. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5260/AD5262 device is primarily used as a digital ground reference, which needs to be tied to the common ground of the PCB. The digital input control signals to the AD5260/AD5262 must be referenced to the device ground pin (GND), and must satisfy the logic level defined in Table 1. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD} regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 56), it is important to power V_{DD}/V_{SS} first before applying any voltage to the A, B, and W terminals. Otherwise, the diode becomes forward biased such that V_{DD}/V_{SS} are powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, V_L, the digital inputs, and $V_A/V_B/V_W$. The order of powering $V_A/V_B/V_W$ and the digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5260 (20 kΩ resistor) measures 310 kHz at half scale. Figure 28 provides the large signal Bode plot characteristics of the three available resistor versions 20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 57. The following section provides a macro model net list for the 20 kΩ RDAC.

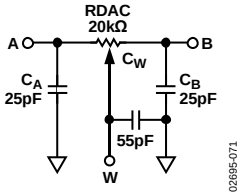


Figure 57. RDAC Circuit Simulation Model for RDAC 20 kΩ

MACRO MODEL NET LIST FOR RDAC

```
PARAM D=256, RDAC=20E3
*
SUBCKT DPOT (A,W,B)
*
CA          A       0       25E-12
RWA         A       W       {(1-D/256)*RDAC+60}
CW          W       0       55E-12
RWB         W       B       {D/256*RDAC+60}
CB          B       0       25E-12
*
.ENDS DPOT
```

APPLICATIONS INFORMATION

BIPOLAR DC OR AC OPERATION FROM DUAL SUPPLIES

The AD5260/AD5262 can be operated from dual supplies enabling control of ground referenced ac signals or bipolar operation. The ac signal, as high as V_{DD}/V_{SS}, can be applied directly across Terminal A and Terminal B with output taken from Terminal W. See Figure 58 for a typical circuit connection.

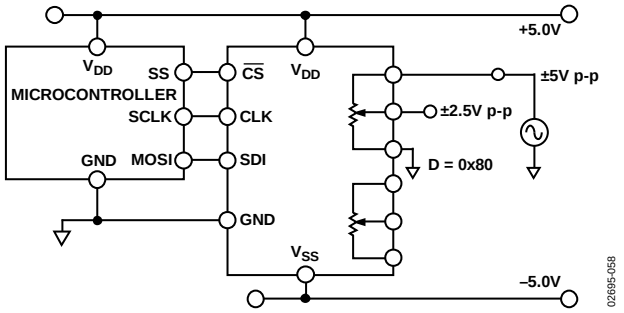


Figure 58. Bipolar Operation from Dual Supplies

GAIN CONTROL COMPENSATION

Digital potentiometers are commonly used in gain control as in the noninverting gain amplifier shown in Figure 59.

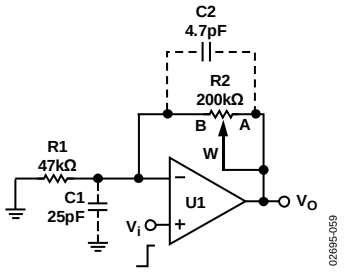


Figure 59. Typical Noninvertng Gain Amplifier

Note that when the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a zero for the $1/\beta_O$ term with +20 dB/dec, whereas a typical op amp gain bandwidth product (GBP) has −20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec and the system has 0 phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach, however, is to include a compensation capacitor, C2, to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, the R1 × C1 = R2 × C2 relationship can be used, and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it avoids the ringing or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of a few picofarads (pF) to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown). Fortunately, their effect at this node is less significant, and the compensation can be avoided in most cases.

PROGRAMMABLE VOLTAGE REFERENCE

For voltage divider mode operation, shown in Figure 60, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, but it also allows a heavier load to be driven.

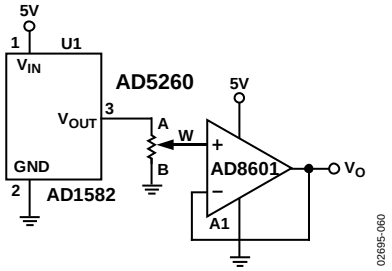


Figure 60. Programmable Voltage Reference

8-BIT BIPOLAR DAC

Figure 61 shows a low cost 8-bit bipolar DAC. It offers the same number of adjustable steps but not the precision of conventional DACs. The linearity and temperature coefficients, especially at low values codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is

$$V_O = \left(\frac{2D}{256} - 1\right) \times V_{REF} \quad (4)$$

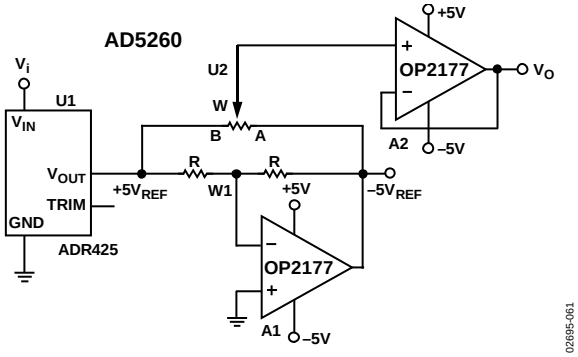


Figure 61. 8-Bit Bipolar DAC

BIPOLAR PROGRAMMABLE GAIN AMPLIFIER

For applications that require bipolar gain, Figure 62 shows one implementation. Digital Potentiometer U1 sets the adjustment range. The wiper voltage at W2 can therefore be programmed between V_i and $-KV_i$ at a given U2 setting. Configuring A2 in the noninverting mode allows linear gain and attenuation. The transfer function is

$$\frac{V_O}{V_i} = \left(1+\frac{R2}{R1}\right)\times\left(\frac{D2}{256}\times(1+K)-K\right) \quad (5)$$

where K is the ratio of R_{WB1}/R_{WA1} set by U1.

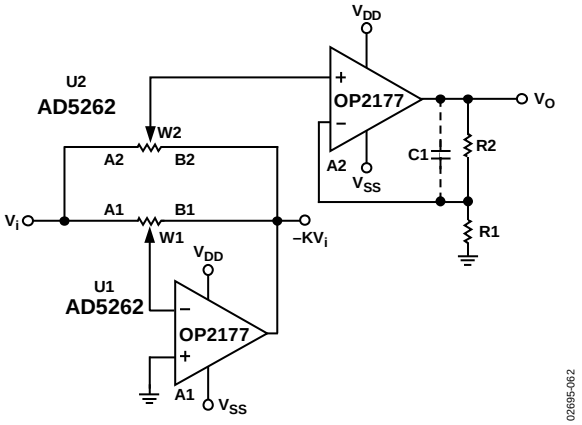


Figure 62. Bipolar Programmable Gain Amplifier

Similar to the previous example, in the simpler and more common case, where K = 1, with a single digital potentiometer, AD5260, U1 is replaced by a matched pair of resistors to apply V_i and $-V_i$ at the ends of the digital potentiometer. The relationship becomes

$$V_O = \left(1+\frac{R2}{R1}\right)\left(\frac{2D2}{256}-1\right)\times V_i \quad (6)$$

If R2 is large, a few picofarad compensation capacitors may be needed to avoid any gain peaking.

Table 11 shows the result of adjusting D, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 256-step resolution.

Table 11. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 × R1
0	−1	−2	−10
64	−0.5	−1	−5
128	0	0	0
192	+0.5	+1	+5
255	+0.968	+1.937	+9.680

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 63).

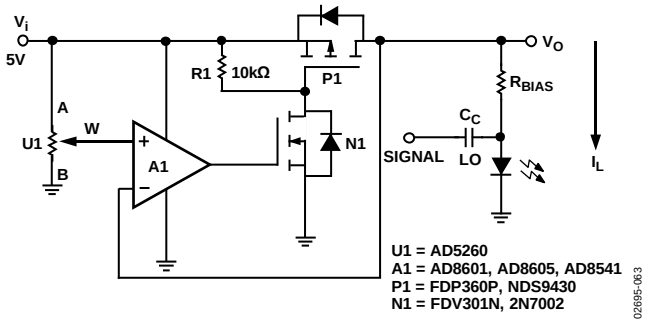


Figure 63. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces V_O to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the P-channel FET, P1. The N-channel FET, N_1, simplifies the op amp driving requirement. A1 must be the rail-to-rail input type. Resistor R1 is needed to prevent P1 from turning off once it is on. The choice of R1 is a balance between the power loss of this resistor and the output turn-off time. N1 can be any general-purpose signal FET. However, P1 is driven in the saturation state, and therefore, its power handling must be adequate to dissipate $(V_i - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA at 5 V supply. Higher current can be achieved with P1 in a larger package. Note that a single N-channel FET can replace P1, N1, and R1 altogether. However, the output swing is limited unless separate power supplies are used. For a precision application, a voltage reference such as the ADR423, ADR292, or AD1584 can be applied at the input of the digital potentiometer.

PROGRAMMABLE 4 mA-TO-20 mA CURRENT SOURCE

A programmable 4 mA-to-20 mA current source can be implemented with the circuit shown in Figure 64. REF191 is a unique low supply headroom and high current handling precision reference that can deliver 20 mA at 2.048 V. The load current is simply the voltage across Terminal B to Terminal W of the digital potentiometer, divided by R_S.

$$I_L = \frac{V_{REF}\times D}{R_S} \quad (7)$$

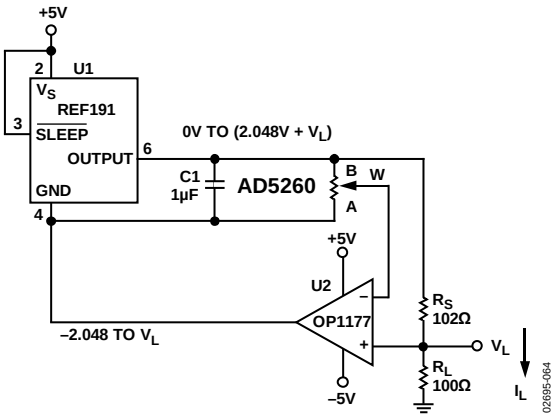


Figure 64. Programmable 4-to-20 mA Current Source

The circuit is simple, but be aware that dual-supply op amps are ideal because the ground potential of REF191 can swing from −2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system is reduced.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 65). If the resistors are matched, the load current is

$$I_L = \frac{(R2A + R2B)/R1}{R2B} \times V_W \quad (8)$$

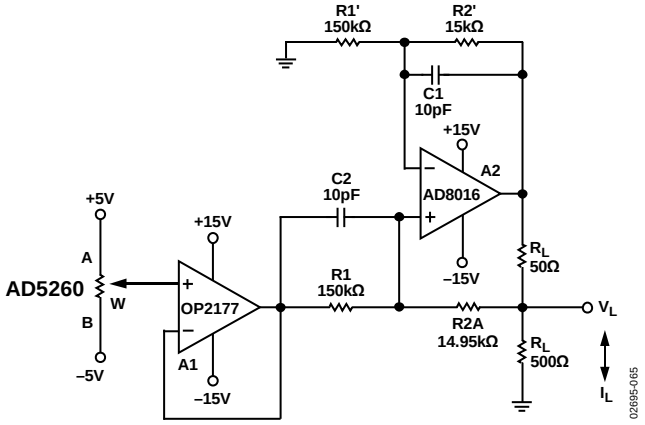


Figure 65. Programmable Bidirectional Current Source

PROGRAMMABLE LOW-PASS FILTER

Digital Potentiometer AD5262 can be used to construct a second-order, Sallen-Key low-pass filter (see Figure 66). The design equations are

$$\frac{V_O}{V_i} = \frac{{\omega_O}^2}{S^2 + \frac{\omega_O}{Q}S + {\omega_O}^2} \quad (9)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (10)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (11)$$

Users can first select any convenient value for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. As a result, users can adjust R1 and R2 to the same settings to achieve the desirable bandwidth.

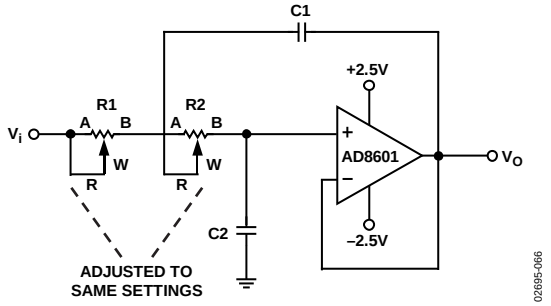


Figure 66. Sallen Key Low-Pass Filter

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator (see Figure 67), the Wien network (R, R', C, C') provides positive feedback, whereas R1 and R2 provide negative feedback. At the resonant frequency, f_o, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R', C = C', and R2 = R2A//(R2B + R_{DIODE}), the oscillation frequency is

$$\omega_O = \frac{1}{RC} \text{ or } f_O = \frac{1}{2\pi RC} \quad (12)$$

where *R* is equal to R_{WA} such that

$$R = \frac{256 - D}{256} R_{AB} \quad (13)$$

At resonance, setting

$$\frac{R2}{R1} = 2 \quad (14)$$

balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure the oscillation can start. However, the alternate turn-on of the diodes, D1 and D2, ensures R2/R1 to be smaller than 2 momentarily and therefore stabilizes the oscillation.

When the frequency is set, the oscillation amplitude can be tuned by R2B because

$$\frac{2}{3} V_O = I_D R2B + V_D \quad (15)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of R2B, an equilibrium is reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to saturate the output.

In both circuits in Figure 66 and Figure 67, the frequency tuning requires that both RDACs be adjusted to the same settings. Because the two channels are adjusted one at a time, an intermedi-

ate state occurs that may not be acceptable for certain applications. As a result, different devices can also be used in daisy-chained mode so that parts can be programmed to the same setting simultaneously.

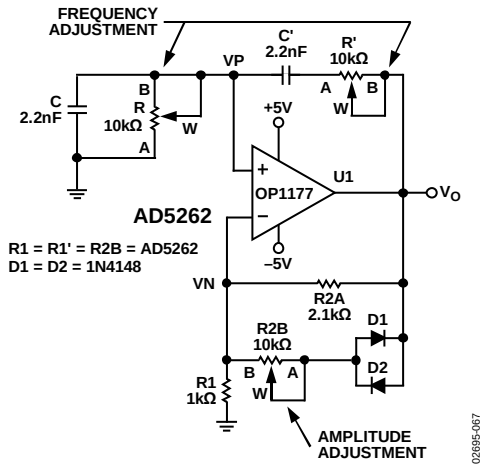


Figure 67. Programmable Oscillator with Amplitude Control

RESISTANCE SCALING

The AD5260/AD5262 offer 20 kΩ, 50 kΩ, and 200 kΩ nominal resistance. For users who need lower resistance and still maintain the numbers of step adjustment, they can place multiple devices in parallel. For example, Figure 68 shows a simple scheme of paralleling both channels of the AD5262. To adjust half of the resistance linearly per step, users need to program both channels coherently with the same settings.

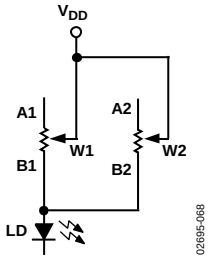


Figure 68. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage divider mode, a much lower resistance can be achieved by paralleling a discrete resistor as shown in Figure 69. The equivalent resistance becomes

$$R_{WB\_eq} = \frac{D}{256}(R1 // R2) + R_W \quad (16)$$

$$R_{WA\_eq} = \left(1 - \frac{D}{256}\right)(R1 // R2) + R_W \quad (17)$$

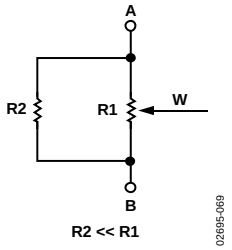


Figure 69. Lowering the Nominal Resistance

Figure 68 and Figure 69 show that the digital potentiometers change steps linearly. However, log taper adjustment is usually preferred in applications like audio control. Figure 70 shows another method of resistance scaling. In this circuit, the smaller R2 is with respect to R_{AB}, the more the pseudo-log taper characteristic behaves.

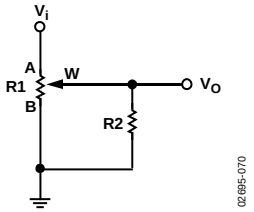
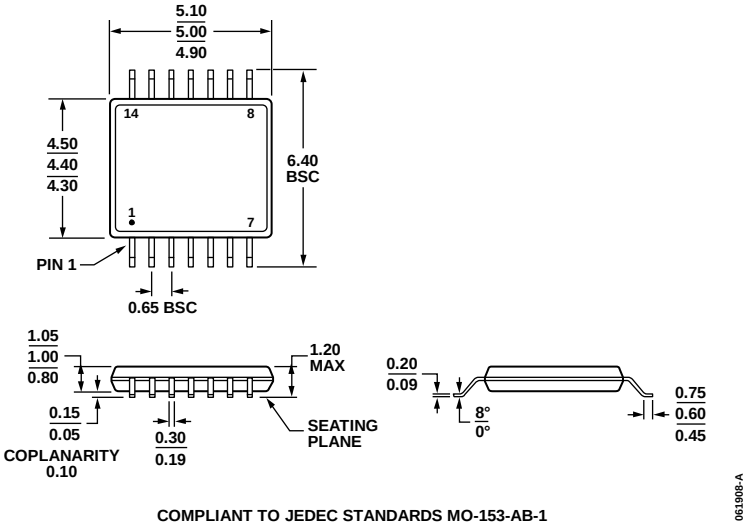


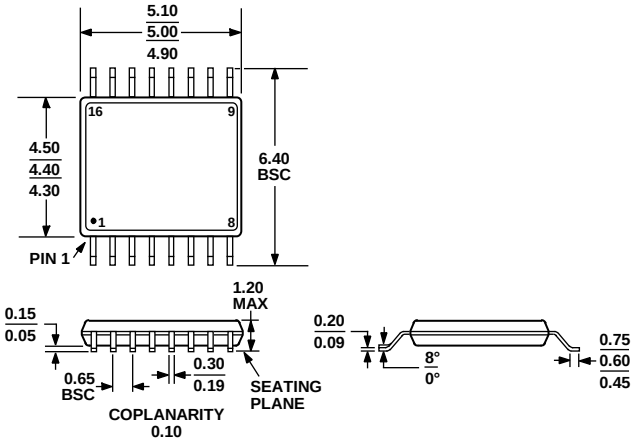
Figure 70. Resistor Scaling with Log Adjustment Characteristics

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 71. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 72. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	RAB (kΩ)	Temperature	Package Description	Package Option	No. of Parts per Container
AD5260BRUZ20	20	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5260BRUZ20-RL7	20	−40°C to +85°C	14-Lead TSSOP	RU-14	1000
AD5260BRUZ50	50	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5260BRUZ50-REEL7	50	−40°C to +85°C	14-Lead TSSOP	RU-14	1000
AD5260BRUZ200	200	−40°C to +85°C	14-Lead TSSOP	RU-14	96
AD5260BRUZ200-RL7	200	−40°C to +85°C	14-Lead TSSOP	RU-14	1000
AD5262BRU20	20	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRU20-REEL7	20	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5262BRU50	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRU50-REEL7	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5262BRU200	200	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRU200-REEL7	200	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5262BRUZ20	20	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRUZ20-RL7	20	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5262BRUZ50	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRUZ50-RL7	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
AD5262BRUZ200	200	−40°C to +85°C	16-Lead TSSOP	RU-16	96
AD5262BRUZ200-RL7	200	−40°C to +85°C	16-Lead TSSOP	RU-16	1000
EVAL-AD5262EBZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

D02695-0-8/10(A)

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