



**THE DATASHEET OF  
AD5258BRMZ10-R7**





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## REVISION HISTORY

### 1/13—Rev. C to Rev. D

Changes to Zero-Scale Error Parameter and Logic Supply Parameter, Table 1 .....	3
Removed Evaluation Board Section and Figure 43, Renumbered Sequentially .....	19

### 5/10—Rev. B to Rev. C

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### 1/10—Rev. A to Rev. B

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### 3/07—Rev. 0 to Rev. A

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### 3/05—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5\text{ V} \pm 10\%$ , or  $3\text{ V} \pm 10\%$ ;  $V_A = V_{DD}$ ;  $V_B = 0\text{ V}$ ;  $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit		
DC CHARACTERISTICS—RHEOSTAT MODE								
Resistor Differential Nonlinearity 1 k $\Omega$	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1.5	$\pm 0.3$	+1.5	LSB		
10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$			-0.25	$\pm 0.1$	+0.25			
Resistor Integral Nonlinearity 1 k $\Omega$	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-5	$\pm 0.5$	+5	LSB		
10 k $\Omega$ /100 k $\Omega$			-0.5	$\pm 0.1$	+0.5			
50 k $\Omega$			-0.25	$\pm 0.1$	+0.25			
Nominal Resistor Tolerance 1 k $\Omega$	$R_{AB}$	$T_A = 25^\circ\text{C}$ , $V_{DD} = 5.5\text{ V}$	0.9		1.5	k $\Omega$		
10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$	$\Delta R_{AB}$		-30		+30	%		
Resistance Temperature Coefficient	$(\Delta R_{AB} \times 10^6)/(R_{AB} \times \Delta T)$	Code = 0x00/0x20		200/15		ppm/ $^\circ\text{C}$		
Total Wiper Resistance	$R_{WB}$	Code = 0x00		75	350	$\Omega$		
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE								
Differential Nonlinearity 1 k $\Omega$	DNL		-1	$\pm 0.3$	+1	LSB		
10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$			-0.25	$\pm 0.1$	+0.25			
Integral Nonlinearity 1 k $\Omega$	INL		-1	$\pm 0.3$	+1	LSB		
10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$			-0.25	$\pm 0.1$	+0.25			
Full-Scale Error 1 k $\Omega$	$V_{WFSE}$	Code = 0x3F	-6	-3	0	LSB		
10 k $\Omega$			-1	-0.3	0			
50 k $\Omega$ /100 k $\Omega$			-1	-0.1	0			
Zero-Scale Error 1 k $\Omega$	$V_{WZSE}$	Code = 0x00 $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	0	3	5	LSB		
							LSB	
				$85^\circ\text{C} < T_A < 125^\circ\text{C}$	0	0.3	1	LSB
				$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	0	0.1	1.5	LSB
10 k $\Omega$		$85^\circ\text{C} < T_A < 125^\circ\text{C}$	0	0.1	0.5	LSB		
50 k $\Omega$ /100 k $\Omega$			0	0.1	0.5	LSB		
Voltage Divider Temperature Coefficient	$(\Delta V_W \times 10^6)/(V_W \times \Delta T)$	Code = 0x00/0x20		120/15		ppm/ $^\circ\text{C}$		
RESISTOR TERMINALS								
Voltage Range	$V_A, V_B, V_W$		GND		$V_{DD}$	V		
Capacitance A, Capacitance B	$C_A, C_B$	$f = 1\text{ MHz}$ , measured to GND, code = 0x20		45		pF		
Capacitance W	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = 0x20		60		pF		
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		10		nA		
DIGITAL INPUTS AND OUTPUTS								
Input Logic High	$V_{IH}$		$0.7 \times V_L$		$V_L + 0.5$	V		
Input Logic Low	$V_{IL}$		-0.5		$+0.3 \times V_L$	V		
Leakage Current	$I_{IL}$					$\mu\text{A}$		
SDA, AD0, AD1		$V_{IN} = 0\text{ V}$ or $5\text{ V}$		0.01	$\pm 1$			
SCL – Logic High		$V_{IN} = 0\text{ V}$	-2.5	-1.4	+1			
SCL – Logic Low		$V_{IN} = 5\text{ V}$		0.01	$\pm 1$			
Input Capacitance	$C_{IL}$			5		pF		

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>POWER SUPPLIES</b>						
Power Supply Range	V <sub>DD</sub>		2.7		5.5	V
Positive Supply Current	I <sub>DD</sub>			0.5	2	μA
Logic Supply	V <sub>LOGIC</sub>		2.7		5.5	V
Logic Supply Current	I <sub>LOGIC</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V −40°C < T <sub>A</sub> < 85°C		3	6	μA
		85°C < T <sub>A</sub> < 125°C			9	μA
Programming Mode Current (EEPROM)	I <sub>LOGIC(PROG)</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V		35		mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V, V <sub>DD</sub> = 5 V	20		40	μW
Power Supply Rejection Ratio	PSRR	V <sub>DD</sub> = +5 V ± 10%, Code = 0x20		±0.01	±0.06	%/%
<b>DYNAMIC CHARACTERISTICS</b>						
Bandwidth −3 dB	BW	Code = 0x20 R <sub>AB</sub> = 1 kΩ		18000		kHz
		R <sub>AB</sub> = 10 kΩ		1000		kHz
		R <sub>AB</sub> = 50 kΩ		190		kHz
		R <sub>AB</sub> = 100 kΩ		100		kHz
Total Harmonic Distortion	THD <sub>W</sub>	R <sub>AB</sub> = 10 kΩ, V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0, f = 1 kHz		0.1		%
V <sub>w</sub> Settling Time	t <sub>s</sub>	R <sub>AB</sub> = 10 kΩ, V <sub>AB</sub> = 5 V, ±1 LSB error band		500		ns
Resistor Noise Voltage Density	e <sub>N,WB</sub>	R <sub>WB</sub> = 5 kΩ, f = 1 kHz		9		nV/√Hz

<sup>1</sup> Typical values represent average readings at 25°C and V<sub>DD</sub> = 5 V.

**TIMING CHARACTERISTICS**

$V_{DD} = V_{LOGIC} = 5 V \pm 10\%$ , or  $3 V \pm 10\%$ ;  $V_A = V_{DD}$ ;  $V_B = 0 V$ ;  $-40^{\circ}C < T_A < +85^{\circ}C$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
<b>I<sup>2</sup>C INTERFACE TIMING CHARACTERISTICS</b>							
SCL Clock Frequency	$f_{SCL}$		0		400	kHz	
$t_{BUF}$ Bus-Free Time Between Stop and Start	$t_1$		1.3			$\mu s$	
$t_{HD,STA}$ Hold Time (Repeated start)	$t_2$	After this period, the first clock pulse is generated.	0.6			$\mu s$	
$t_{LOW}$ Low Period of SCL Clock	$t_3$		1.3			$\mu s$	
$t_{HIGH}$ High Period of SCL Clock	$t_4$		0.6			$\mu s$	
$t_{SU,STA}$ Setup Time for Repeated Start Condition	$t_5$		0.6			$\mu s$	
$t_{HD,DAT}$ Data Hold Time	$t_6$		0		0.9	$\mu s$	
$t_{SU,DAT}$ Data Setup Time	$t_7$		100			ns	
$t_F$ Fall Time of Both SDA and SCL Signals	$t_8$					300	ns
$t_R$ Rise Time of Both SDA and SCL Signals	$t_9$					300	ns
$t_{SU,STO}$ Setup Time for Stop Condition	$t_{10}$		0.6			$\mu s$	
EEPROM Data Storing Time	$t_{EEMEM\_STORE}$				26		ms
EEPROM Data Restoring Time at Power On <sup>1</sup>	$t_{EEMEM\_RESTORE1}$	$V_{DD}$ rise time dependant. Measure without decoupling capacitors at $V_{DD}$ and GND.		300		$\mu s$	
EEPROM Data Restoring Time upon Restore Command <sup>1</sup>	$t_{EEMEM\_RESTORE2}$	$V_{DD} = 5 V$ .		300		$\mu s$	
EEPROM Data Rewritable Time <sup>2</sup>	$t_{EEMEM\_REWRITE}$			540		$\mu s$	
<b>FLASH/EE MEMORY RELIABILITY</b>							
Endurance <sup>3</sup>			100	700		kCycles	
Data Retention <sup>4</sup>				100		Years	

<sup>1</sup> During power-up, the output is momentarily preset to midscale before restoring EEPROM content.

<sup>2</sup> Delay time after power-on preset prior to writing new EEPROM data.

<sup>3</sup> Endurance is qualified to 100,000 cycles per JEDEC Std. 22 Method A117 and is measured at  $-40^{\circ}C$ ,  $+25^{\circ}C$ , and  $+85^{\circ}C$ ; typical endurance at  $+25^{\circ}C$  is 700,000 cycles.

<sup>4</sup> Retention lifetime equivalent at junction temperature ( $T_j$ ) =  $55^{\circ}C$  per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

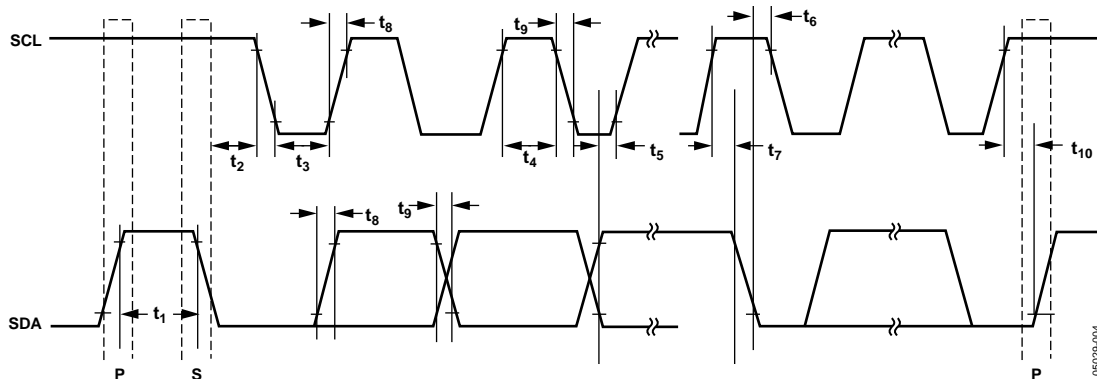


Figure 3. I<sup>2</sup>C Interface Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_A, V_B, V_W$ to GND	GND - 0.3 V, $V_{DD} + 0.3$ V
$I_{MAX}$	
Pulsed <sup>1</sup>	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature ( $T_{JMAX}$ )	150°C
Storage Temperature	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance <sup>2</sup>	200°C/W
$\theta_{JA}$ : MSOP-10	

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation =  $(T_{JMAX} - T_A)/\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

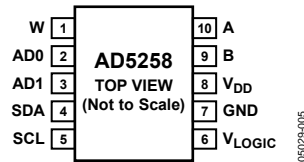


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W	W Terminal, $GND \leq V_W \leq V_{DD}$ .
2	AD0	Programmable Pin 0 for Multiple Package Decoding. State is registered on power-up.
3	AD1	Programmable Pin 1 for Multiple Package Decoding. State is registered on power-up.
4	SDA	Serial Data Input/Output.
5	SCL	Serial Clock Input. Positive edge triggered.
6	V <sub>LOGIC</sub>	Logic Power Supply.
7	GND	Digital Ground.
8	V <sub>DD</sub>	Positive Power Supply.
9	B	B Terminal, $GND \leq V_B \leq V_{DD}$ .
10	A	A Terminal, $GND \leq V_A \leq V_{DD}$ .

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5.5\text{ V}$ ,  $R_{AB} = 10\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

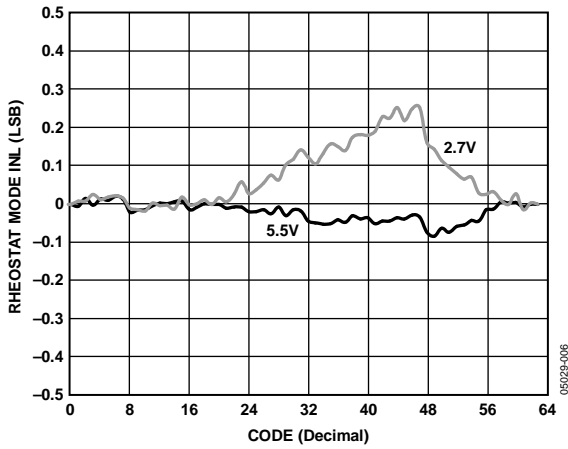


Figure 5. R-INL vs. Code vs. Supply Voltages

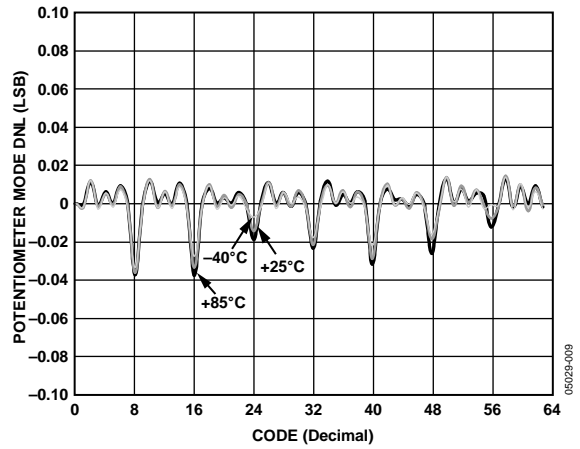


Figure 8. DNL vs. Code vs. Temperature

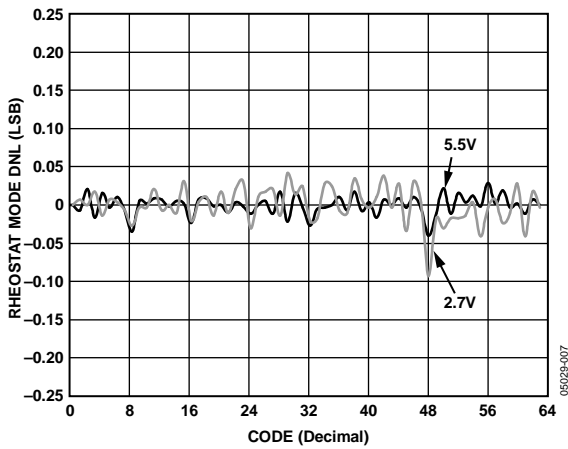


Figure 6. R-DNL vs. Code vs. Supply Voltages

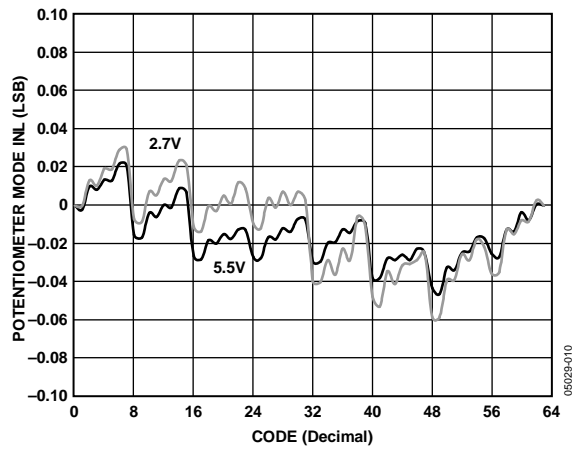


Figure 9. INL vs. Code vs. Supply Voltages

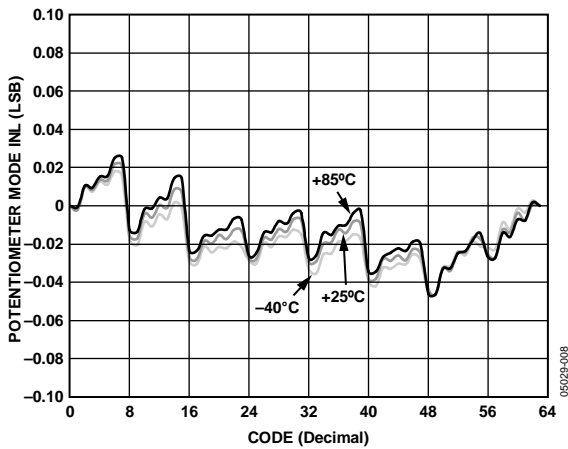


Figure 7. INL vs. Code vs. Temperature

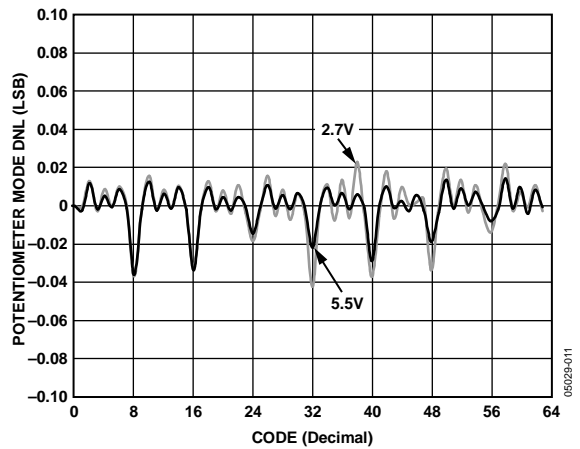


Figure 10. DNL vs. Code vs. Supply Voltages

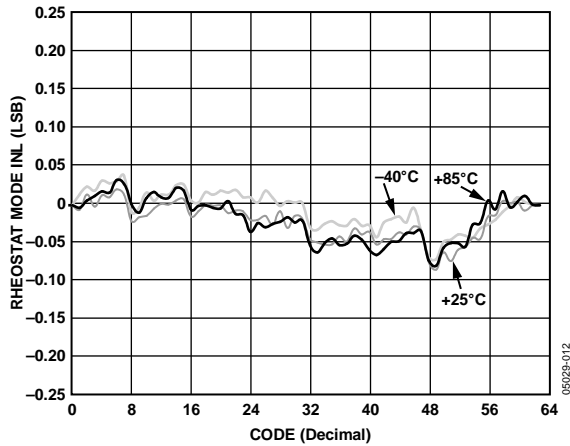


Figure 11. R-INL vs. Code vs. Temperature

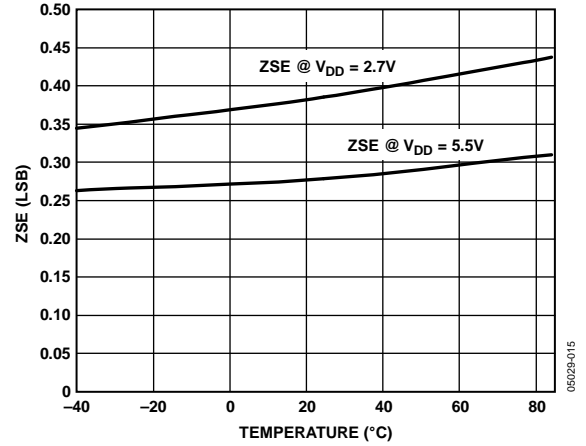


Figure 14. Zero-Scale Error vs. Temperature

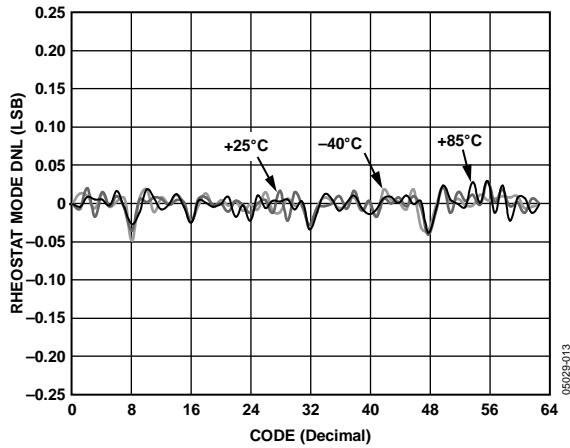


Figure 12. R-DNL vs. Code vs. Temperature

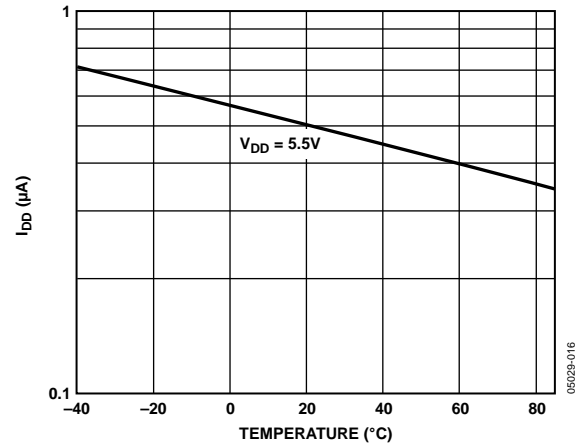


Figure 15. Supply Current vs. Temperature

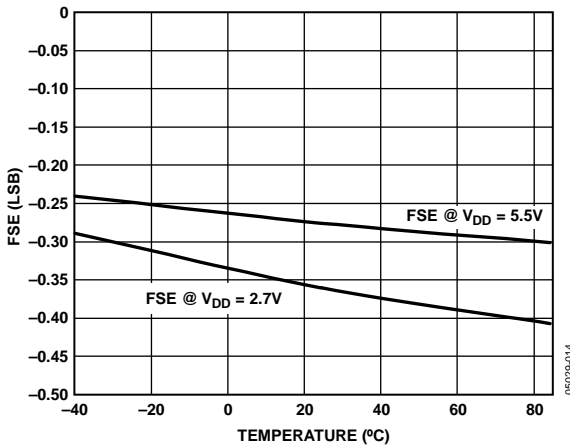


Figure 13. Full-Scale Error vs. Temperature

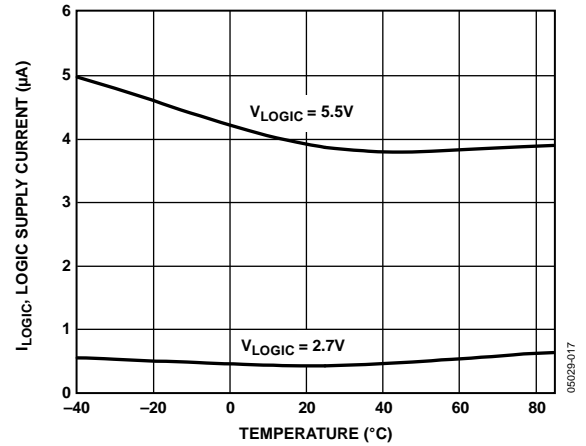


Figure 16. Logic Supply Current vs. Temperature vs.  $V_{LOGIC}$

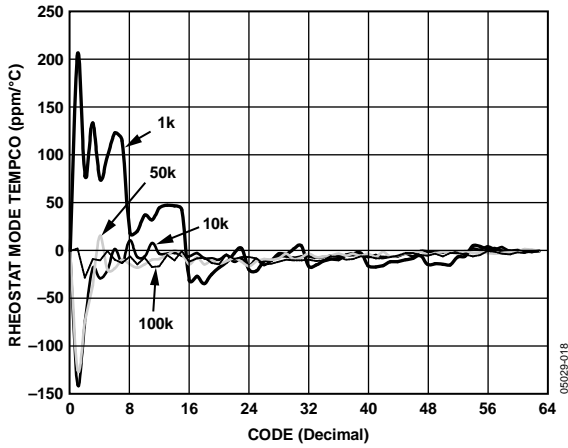


Figure 17. Rheostat Mode Tempco ( $\Delta R_{AB} \times 10^6$ )/( $R_{AB} \times \Delta T$ ) vs. Code

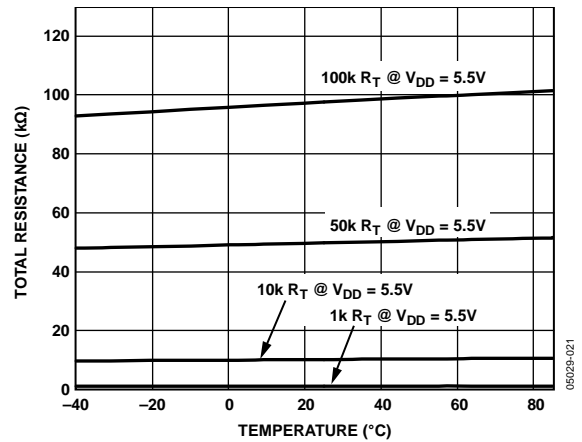


Figure 20. Total Resistance vs. Temperature

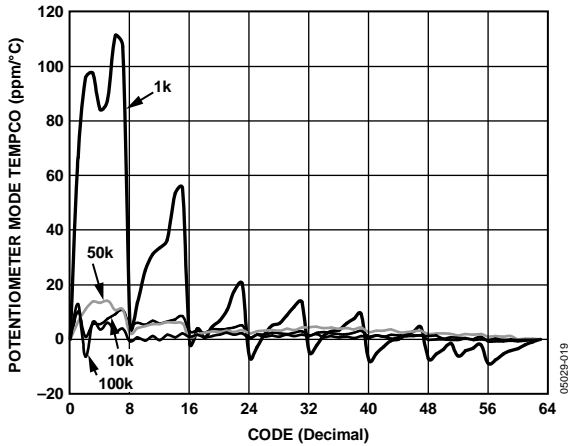


Figure 18. Potentiometer Mode Tempco ( $\Delta V_W \times 10^6$ )/( $V_W \times \Delta T$ ) vs. Code

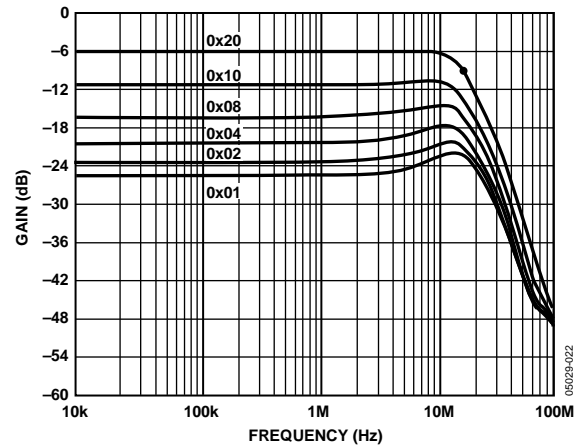


Figure 21. Gain vs. Frequency vs. Code,  $R_{AB} = 1 \text{ k}\Omega$

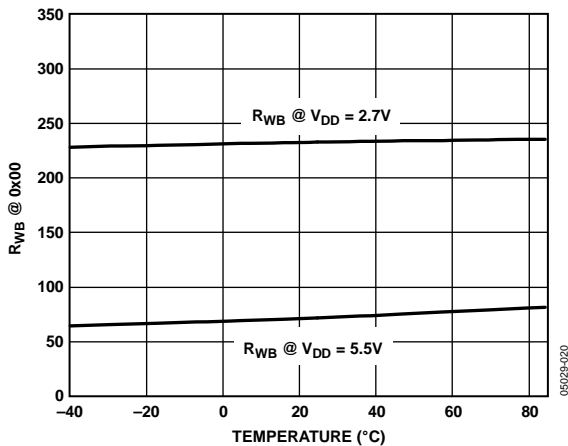


Figure 19.  $R_{WB}$  vs. Temperature

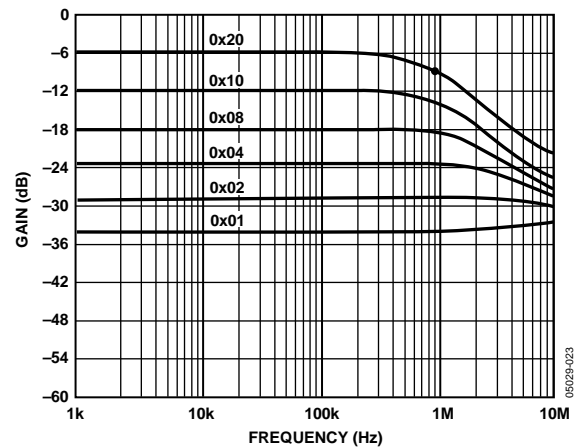


Figure 22. Gain vs. Frequency vs. Code,  $R_{AB} = 10 \text{ k}\Omega$

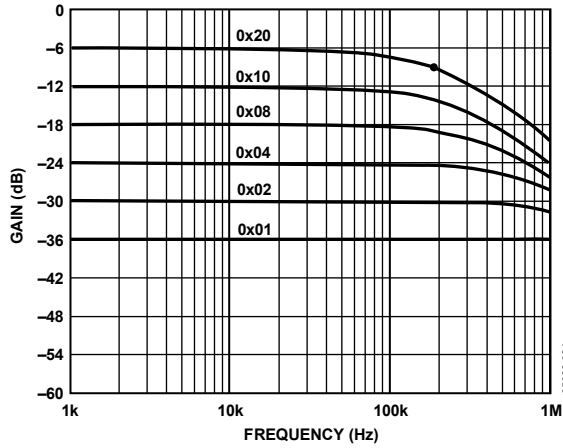


Figure 23. Gain vs. Frequency vs. Code,  $R_{AB} = 50\text{ k}\Omega$

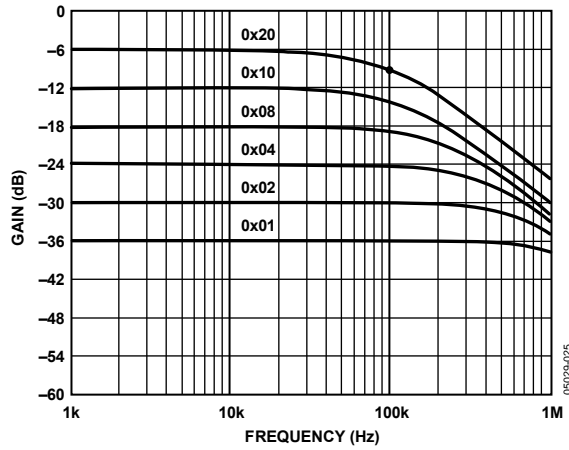


Figure 24. Gain vs. Frequency vs. Code,  $R_{AB} = 100\text{ k}\Omega$

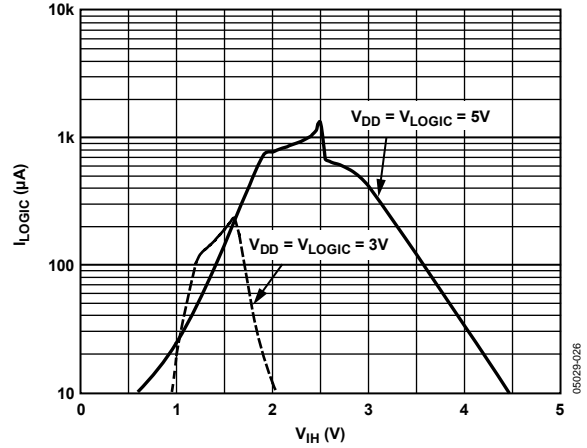


Figure 25. Logic Supply Current vs. Input Voltage

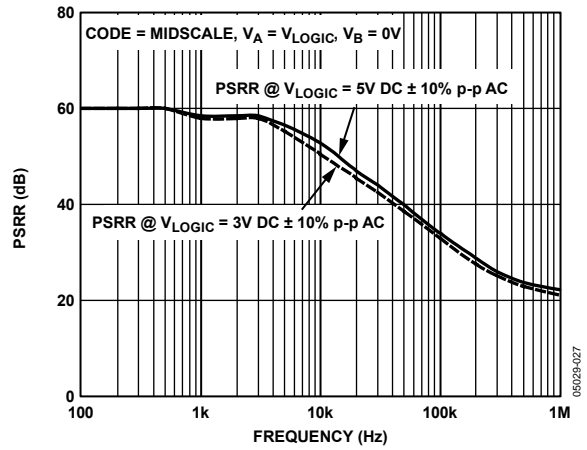


Figure 26. Power Supply Rejection Ratio vs. Frequency

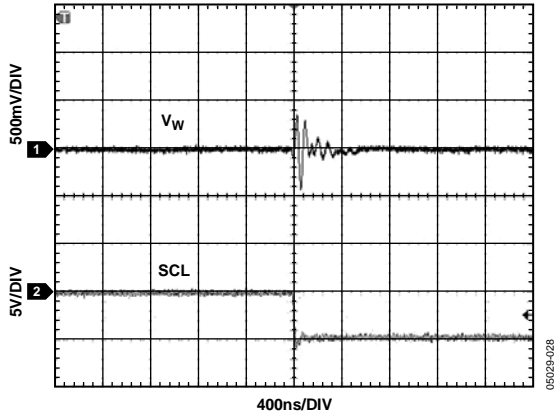


Figure 27. Digital Feedthrough

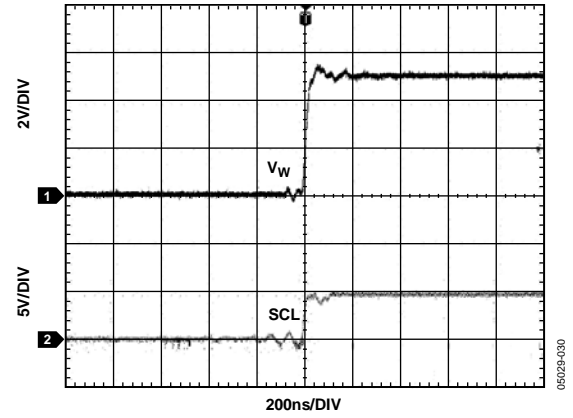


Figure 29. Large-Signal Settling Time

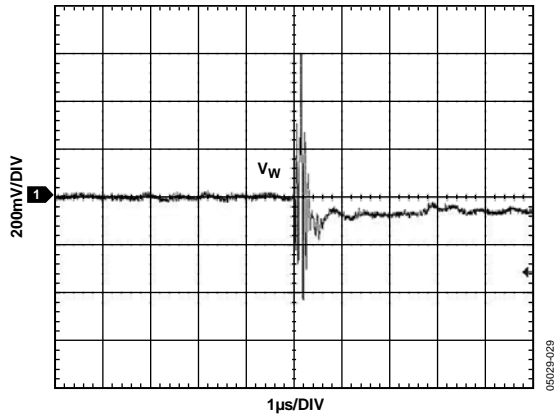


Figure 28. Midscale Glitch, Code 0x7F to Code 0x80

### TEST CIRCUITS

Figure 30 through Figure 35 illustrate the test circuits that define the test conditions used in the product specification tables.

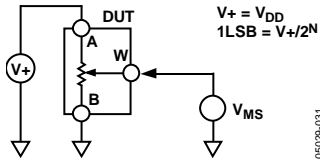


Figure 30. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

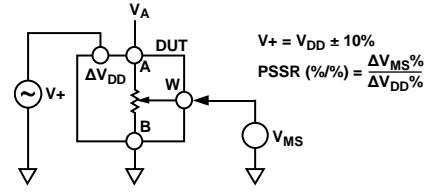


Figure 33. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

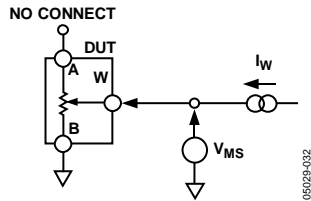


Figure 31. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

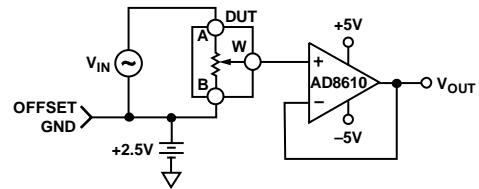


Figure 34. Test Circuit for Gain vs. Frequency

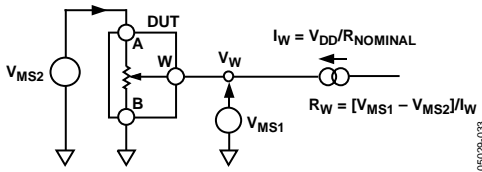


Figure 32. Test Circuit for Wiper Resistance

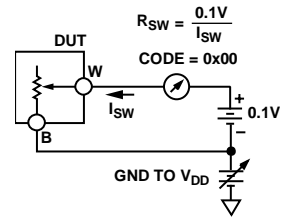


Figure 35. Test Circuit for Common-Mode Leakage Current

## THEORY OF OPERATION

The AD5258 is a 64-position digitally controlled variable resistor (VR) device. The wipers default value prior to programming the EEPROM is midscale.

### PROGRAMMING THE VARIABLE RESISTOR

#### Rheostat Operation

The nominal resistance ( $R_{AB}$ ) of the RDAC between Terminal A and Terminal B is available in 1 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ . The nominal resistance of the VR has 64 contact points accessed by the wiper terminal. The 6-bit data in the RDAC latch is decoded to select one of 64 possible settings.

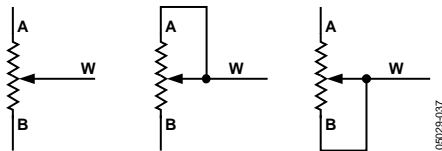


Figure 36. Rheostat Mode Configuration

The general equation determining the digitally programmed output resistance between Wiper W and Terminal B is

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$  is the decimal equivalent of the binary code loaded in the 6-bit RDAC register.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the on resistance of each internal switch.

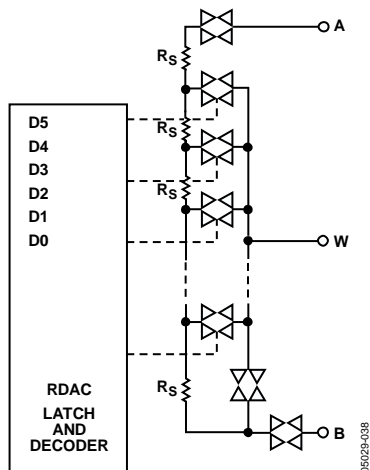


Figure 37. AD5258 Equivalent RDAC Circuit

Note that in the zero-scale condition, there is a relatively low value finite wiper resistance. Care should be taken to limit the current flow between Wiper W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or destruction of the internal switch contact may occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A produces a digitally controlled complementary resistance,  $R_{WA}$ . The resistance value setting for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{64 - D}{64} \times R_{AB} + 2 \times R_W \quad (2)$$

Typical device-to-device matching is process lot dependent and may vary by up to  $\pm 30\%$ . For this reason, resistance tolerance is stored in the EEPROM such that the user will know the actual  $R_{AB}$  within 0.1%.

### PROGRAMMING THE POTENTIOMETER DIVIDER

#### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at Wiper W-to-Terminal B and Wiper W-to-Terminal A proportional to the input voltage at Terminal A-to-Terminal B. Unlike the polarity of  $V_{DD}$ -to-GND, which must be positive, voltage across Terminal A-to-Terminal B, Wiper W-to-Terminal A, and Wiper W-to-Terminal B can be at either polarity.

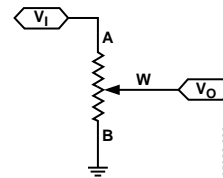


Figure 38. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at Wiper W-to-Terminal B starting at 0 V up to 1 LSB less than 5 V. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{64} V_A + \frac{64 - D}{64} V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance ( $V_W$ ) is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of internal resistors ( $R_{WA}$  and  $R_{WB}$ ) and not the absolute values.

## I<sup>2</sup>C INTERFACE

Note that the wiper's default value prior to programming the EEPROM is midscale.

The master initiates a data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 3). The next byte is the slave address byte, which consists of the slave address (first seven bits) followed by an R/W bit (see Table 6). When the R/W bit is high, the master reads from the slave device. When the R/W bit is low, the master writes to the slave device.

The slave address of the part is determined by two configurable address pins, AD0 and AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I<sup>2</sup>C 7-bit address (see Table 5). The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is termed the slave acknowledge bit).

At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

### WRITING

In the write mode, the last bit (R/W) of the slave address byte is logic low. The second byte is the instruction byte. The first three bits of the instruction byte are the command bits (see Table 6). The user must choose whether to write to the RDAC register or EEPROM register or to activate the software write protect (see Table 7 to Table 10). The final five bits are all zeros (see Table 13 and Table 14). The slave again responds by pulling the SDA line low during the ninth clock pulse.

The final byte is the data byte MSB first. Don't cares can be left either high or low. In the case of the write protect mode, data is not stored; rather, a logic high in the LSB enables write protect. Likewise, a logic low disables write protect. The slave again responds by pulling the SDA line low during the ninth clock pulse.

### STORING/RESTORING

In this mode, only the address and instruction bytes are necessary. The last bit (R/W) of the address byte is logic low. The first three bits of the instruction byte are the command bits (see Table 6). The two choices are transfer data from RDAC-to-EEPROM (store) or from EEPROM-to-RDAC (restore). The final five bits are all zeros (see Table 13 and Table 14). In addition, users should issue an NOP command immediately after restoring the EEMEM setting to RDAC, thereby minimizing supply current dissipation.

### READING

Assuming the register of interest was not just written to, it is necessary to write a dummy address and instruction byte. The instruction byte will vary depending on whether the data that is wanted is the RDAC register, EEPROM register, or tolerance register (see Table 11 to Table 16).

After the dummy address and instruction bytes are sent, a repeat start is necessary. After the repeat start, another address byte is needed, except this time the R/W bit is logic high. Following this address byte is the readback byte containing the information requested in the instruction byte. Read bits appear on the negative edges of the clock. Don't cares may be in either a high or low state.

The tolerance register can be read back individually (see Table 15) or consecutively (see Table 16). Refer to the Read Modes section for detailed information on the interpretation of the tolerance bytes.

After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10<sup>th</sup> clock pulse to establish a stop condition (see Table 8). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10<sup>th</sup> clock pulse and raises SDA high to establish a stop condition (see Table 11).

A repeated write function provides the user with the flexibility of updating the RDAC output multiple times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output is updated on each successive byte until a stop condition is received. If different instructions are needed, the write/read mode must restart with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

## I<sup>2</sup>C BYTE FORMATS

The following generic, write, read, and store/restore control registers for the AD5258 refer to the device addresses listed in Table 5, and following is the mode/condition reference key.

- S = Start Condition
- P = Stop Condition
- SA = Slave Acknowledge
- MA = Master Acknowledge
- NA = No Acknowledge
- $\overline{W}$  = Write
- R = Read
- X = Don't Care
- AD1 and AD0 are two-state address pins.

**Table 5. Device Address Lookup**

AD1 Address Pin	AD0 Address Pin	I <sup>2</sup> C Device Address
0	0	0011000
1	0	0011010
0	1	1001100
1	1	1001110

## GENERIC INTERFACE

**Table 6. Generic Interface Format**

S	7-Bit Device Address (See Table 5)	R/ $\overline{W}$	SA	C2	C1	C0	A4	A3	A2	A1	A0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

**Table 7. RDAC-to-EEPROM Interface Command Descriptions**

C2	C1	C0	Command Description
0	0	0	Operation between I <sup>2</sup> C and RDAC
0	0	1	Operation between I <sup>2</sup> C and EEPROM
0	1	0	Operation between I <sup>2</sup> C and Write Protection Register. See Table 10.
1	0	0	NOP
1	0	1	Restore EEPROM to RDAC <sup>1</sup>
1	1	0	Store RDAC to EEPROM

<sup>1</sup> This command leaves the device in the EEMEM read power state, which consumes power. Issue the NOP command to return the device to its idle state.

## WRITE MODES

**Table 8. Writing to RDAC Register**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	0	0	0	0	0	0	0	SA	X	X	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte										

**Table 9. Writing to EEPROM Register**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	1	0	0	0	0	0	0	SA	X	X	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte										

The wiper's default value prior to programming the EEPROM is midscale.

**Table 10. Activating/Deactivating Software Write Protect**

S	7-Bit Device Address (See Table 5)	0	SA	0	1	0	0	0	0	0	0	0	SA	0	0	0	0	0	0	0	0	WP	SA	P
	Slave Address Byte			Instruction Byte									Data Byte											

To activate the write protection mode, the WP bit in Table 10 must be logic high. To deactivate the write protection, the command must be resent except with the WP in logic zero state.

**READ MODES**

Read modes are referred to as traditional because the first two bytes for all three cases are dummy bytes that function to place the pointer toward the correct register. This is the reason for the repeat start. In theory, this step can be avoided if the user is

interested in reading a register that was previously written to. For example, if the EEPROM was just written to, the user can skip the two dummy bytes and proceed directly to the slave address byte followed by the EEPROM readback data.

**Table 11. Traditional Readback of RDAC Register Value**

<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>0</b>	<b>SA</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SA</b>	<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>1</b>	<b>SA</b>	<b>X</b>	<b>X</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>NA</b>	<b>P</b>
	Slave Address Byte			Instruction Byte												Slave Address Byte		Read-back Data									

↑  
Repeat Start

**Table 12. Traditional Readback of Stored EEPROM Value**

<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>0</b>	<b>SA</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SA</b>	<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>1</b>	<b>SA</b>	<b>X</b>	<b>X</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>NA</b>	<b>P</b>
	Slave Address Byte			Instruction Byte												Slave Address Byte		Read-back Data									

↑  
Repeat Start

**STORE/RESTORE MODES**

**Table 13. Storing RDAC Value to EEPROM**

<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>0</b>	<b>SA</b>	<b>1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SA</b>	<b>P</b>	
	Slave Address Byte			Instruction Byte											

**Table 14. Restoring EEPROM to RDAC<sup>1</sup>**

<b>S</b>	<b>7-Bit Device Address (See Table 5)</b>	<b>0</b>	<b>SA</b>	<b>1</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>SA</b>	<b>P</b>	
	Slave Address Byte			Instruction Byte											

<sup>1</sup> User should issue an NOP command immediately after this command to conserve power.

**TOLERANCE READBACK MODES**

**Table 15. Traditional Readback of Tolerance (Individually)**

S	7-Bit Device Address (See Table 5)							0	SA	0	0	1	1	1	1	0	SA	S	7-Bit Device Address (See Table 5)							1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P									
	Slave Address Byte									Instruction Byte									Slave Address Byte									Sign + Integer Byte																		

↑  
Repeat Start

S	7-Bit Device Address (See Table 5)							0	SA	0	0	1	1	1	1	1	SA	S	7-Bit Device Address (See Table 5)							1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P									
	Slave Address Byte									Instruction Byte									Slave Address Byte									Decimal Byte																		

↑  
Repeat Start

**Table 16. Traditional Readback of Tolerance (Consecutively)**

S	7-Bit Device Address (See Table 5)							0	SA	0	0	1	1	1	1	0	SA	S	7-Bit Device Address (See Table 5)							1	SA	D7	D6	D5	D4	D3	D2	D1	D0	MA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P									
	Slave Address Byte									Instruction Byte									Slave Address Byte									Sign + Integer Byte									Decimal Byte																		

↑  
Repeat Start

**Calculating  $R_{AB}$  Tolerance Stored in Read-Only Memory**

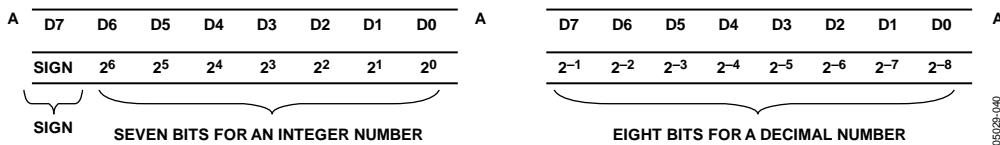


Figure 39. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions (Unit is Percent; Only Data Bytes are Shown)

The AD5258 features a patented  $R_{AB}$  tolerance storage in the nonvolatile memory. Tolerance is stored in the memory during factory production and can be read by users at any time. The knowledge of stored tolerance allows users to accurately calculate  $R_{AB}$ . This feature is valuable for precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

The stored tolerance resides in the read-only memory and is expressed as a percentage. The tolerance is stored in two memory location bytes in sign magnitude binary form (see Figure 39). The two EEPROM address bytes are 11110 (sign + integer) and 11111 (decimal number). The two bytes can be individually accessed with two separate commands (see Table 15). Alternatively, read-back of the first byte followed by the second byte can be done in one command (see Table 16). In the latter case, the memory pointer automatically increments from the first to the second EEPROM location (increments from 11110 to 11111) if read consecutively.

In the first memory location, the MSB is designated for the sign (0 = + and 1 = -) and the seven LSBs are designated for the integer portion of the tolerance. In the second memory location, all eight data bits are designated for the decimal portion of tolerance. Note that the decimal portion has a limited accuracy of only 0.1%. For example, if the rated  $R_{AB} = 10\text{ k}\Omega$  and the data readback from Address 11110 shows 0001 1100 and from Address 11111 shows 0000 1111, the tolerance can be calculated as

$$\begin{aligned}
 \text{MSB: } 0 &= + \\
 \text{Next 7 MSB: } 001\ 1100 &= 28 \\
 \text{8 LSB: } 0000\ 1111 &= 15 \times 2^{-8} = 0.06 \\
 \text{Tolerance} &= 28.06\% \\
 \text{Rounded Tolerance} &= 28.1\% \text{ and therefore} \\
 R_{AB\_ACTUAL} &= 12.810\text{ k}\Omega
 \end{aligned}$$

## ESD PROTECTION OF DIGITAL PINS AND RESISTOR TERMINALS

The AD5258  $V_{DD}$ ,  $V_{LOGIC}$ , and GND power supplies define the boundary conditions for proper 3-terminal and digital input operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed  $V_{DD}$  or GND are clamped by the internal forward-biased ESD protection diodes (see Figure 40). Digital Input SCL and Digital Input SDA are clamped by ESD protection diodes with respect to  $V_{LOGIC}$  and GND as shown in Figure 41.

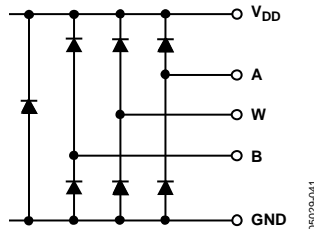


Figure 40. Maximum Terminal Voltages Set by  $V_{DD}$  and GND

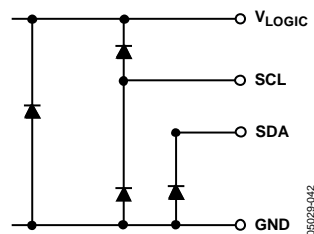


Figure 41. Maximum Terminal Voltages Set by  $V_{LOGIC}$  and GND

## POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 40), it is important to power GND/ $V_{DD}$ / $V_{LOGIC}$  before applying any voltage to Terminal A, Terminal B, and Terminal W; otherwise, the diode is forward-biased such that  $V_{DD}$  and  $V_{LOGIC}$  are powered unintentionally and may affect the user's circuit. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ ,  $V_{LOGIC}$ , digital inputs, and then  $V_A$ ,  $V_B$ ,  $V_W$ . The relative order

of powering  $V_A$ ,  $V_B$ ,  $V_W$  and the digital inputs is not important as long as they are powered after GND,  $V_{DD}$ , and  $V_{LOGIC}$ .

## LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ . In addition, low ESR 1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 42). As well, the digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

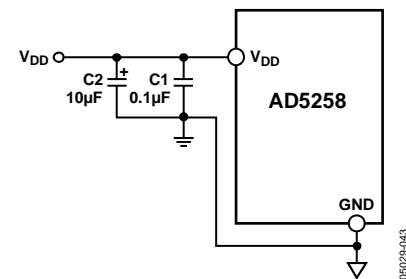


Figure 42. Power Supply Bypassing

## MULTIPLE DEVICES ON ONE BUS

The AD5258 has two configurable address pins, AD0 and AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I<sup>2</sup>C-compatible 7-bit address (see Table 5). This allows up to four devices on the bus to be written to or read from independently.

## DISPLAY APPLICATIONS

### CIRCUITRY

A special feature of the AD5258 is its unique separation of the  $V_{\text{LOGIC}}$  and  $V_{\text{DD}}$  supply pins. The reason for doing this is to provide greater flexibility in applications that do not always provide the needed supply voltages.

In particular, LCD panels often require a  $V_{\text{COM}}$  voltage in the range of 3 V to 5 V. The circuit in Figure 43 is the rare exception in which a 5 V supply is available to power the digital potentiometer.

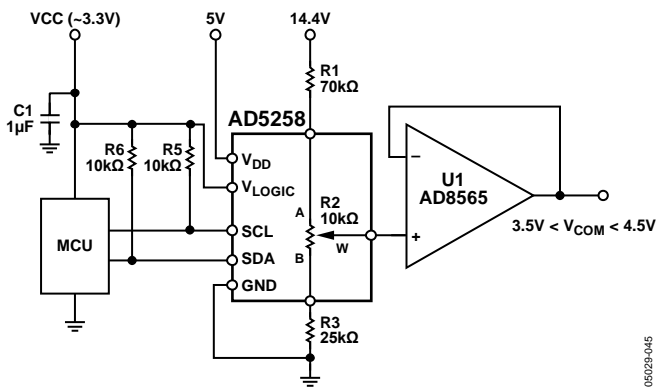


Figure 43.  $V_{\text{COM}}$  Adjustment Application

More commonly, only analog 14.4 V and digital logic 3.3 V supplies are available (see Figure 44). By placing discrete resistors above and below the digital potentiometer,  $V_{\text{DD}}$  can be tapped off the resistor string itself. Based on the chosen resistor values, the voltage at  $V_{\text{DD}}$  in this case equals 4.8 V, allowing the wiper to be safely operated up to 4.8 V. The current draw of  $V_{\text{DD}}$  will not

affect that node's bias because it is only on the order of microamps.  $V_{\text{LOGIC}}$  is tied to the microcontroller's (MCU) 3.3 V digital supply because  $V_{\text{LOGIC}}$  will draw the 35 mA that is needed when writing to the EEPROM. It would be impractical to try to source 35 mA through the 70 k $\Omega$  resistor; therefore,  $V_{\text{LOGIC}}$  is not connected to the same node as  $V_{\text{DD}}$ .

For this reason,  $V_{\text{LOGIC}}$  and  $V_{\text{DD}}$  are provided as two separate supply pins that can either be tied together or treated independently;  $V_{\text{LOGIC}}$  supplies the logic/EEPROM with power, and  $V_{\text{DD}}$  biases up the A, B, and W terminals for added flexibility.

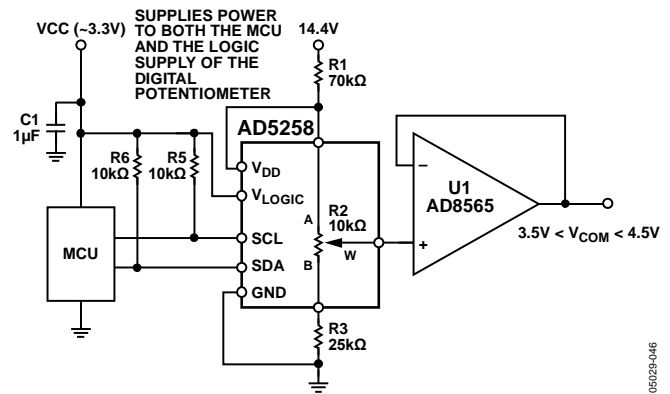
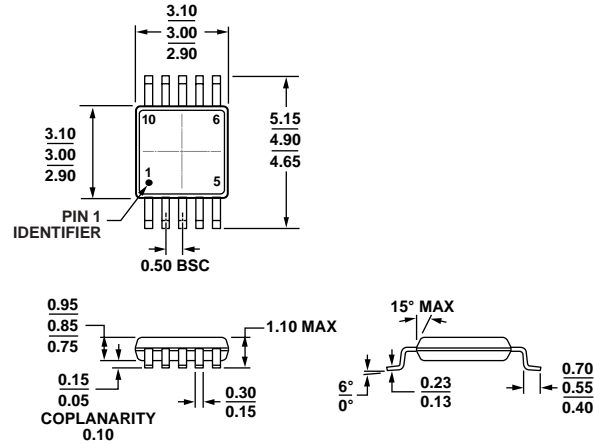


Figure 44. Circuitry When a Separate Supply Is Not Available for  $V_{\text{DD}}$

For a more detailed look at this application, refer to the article, "Simple  $V_{\text{COM}}$  Adjustment uses any Logic-Supply Voltage" in the September 30, 2004, issue of *EDN* magazine.

### OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA  
 Figure 45. 10-Lead Mini Small Outline Package [MSOP]  
 (RM-10)  
 Dimensions shown in millimeters

081709-A

### ORDERING GUIDE

Model <sup>1</sup>	R <sub>AB</sub> (kΩ)	Temperature Range	Package Description <sup>2</sup>	Package Option	Branding
AD5258BRMZ1	1	-40°C to +85°C	10-Lead MSOP	RM-10	D4K
AD5258BRMZ1-R7	1	-40°C to +85°C	10-Lead MSOP	RM-10	D4K
AD5258BRMZ10	10	-40°C to +85°C	10-Lead MSOP	RM-10	D4L
AD5258BRMZ10-R7	10	-40°C to +85°C	10-Lead MSOP	RM-10	D4L
AD5258BRMZ50	50	-40°C to +85°C	10-Lead MSOP	RM-10	D4M
AD5258BRMZ50-R7	50	-40°C to +85°C	10-Lead MSOP	RM-10	D4M
AD5258BRMZ100	100	-40°C to +85°C	10-Lead MSOP	RM-10	D4N
AD5258BRMZ100-R7	100	-40°C to +85°C	10-Lead MSOP	RM-10	D4N
EVAL-AD5258DBZ			Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> The evaluation board is shipped with the 10 kΩ R<sub>AB</sub> resistor option; however, the board is compatible with all available resistor value options.

**NOTES**

**NOTES**

**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

## Looking for pricing, stock, or lifecycle information?

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 [View AD5258BRMZ10-R7 on WIN SOURCE](#)

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