



**THE DATASHEET OF
74HC2G00DP,125**



74HC2G00; 74HCT2G00

Dual 2-input NAND gate

Rev. 6 — 20 November 2018

Product data sheet

1. General description

The 74HC2G00; 74HCT2G00 is a dual 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC2G00: CMOS level
 - For 74HCT2G00: TTL level
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - HBM JESD22-A114E exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT2G00DP				
74HC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT2G00DC				

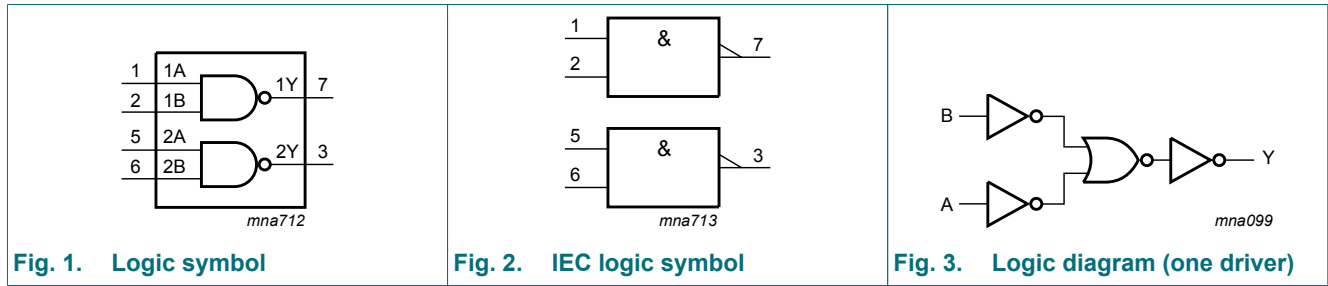
4. Marking

Table 2. Marking code

Type number	Marking code[1]
74HC2G00DP	H00
74HCT2G00DP	T00
74HC2G00DC	H00
74HCT2G00DC	T00

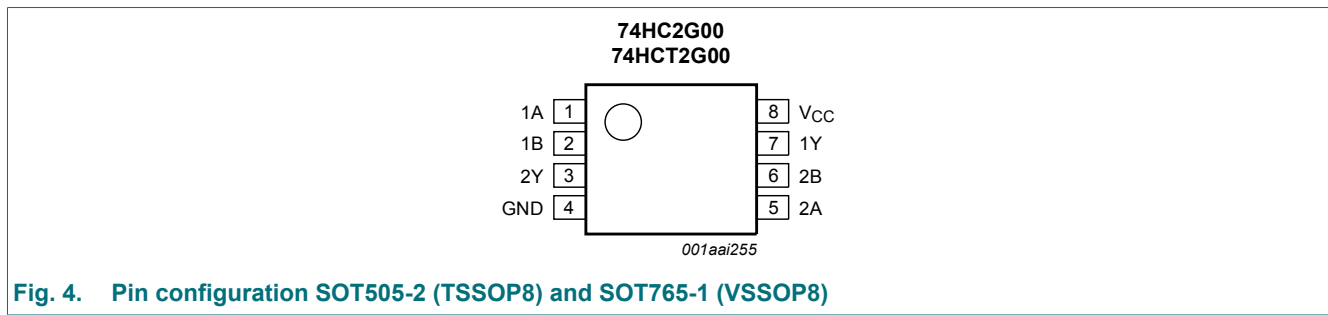
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ [1]	-	25	mA
I_{CC}	supply current	[1]	-	50	mA
I_{GND}	ground current	[1]	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_D	dynamic power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G00			74HCT2G00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC2G00								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
		I _{CC}	supply current	per input pin; V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-
C _I	input capacitance		-	1.5	-	-	-	pF
74HCT2G00								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	375	-	410	μA
C _I	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); all typical values are measured at $T_{amb} = 25\text{ °C}$; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC2G00								
t_{pd}	propagation delay	nA and nB to nY; see Fig. 5 [1]						
		$V_{CC} = 2.0\text{ V}$	-	25	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	9	19	-	22	ns
		$V_{CC} = 6.0\text{ V}$	-	7	16	-	20	ns
t_t	transition time	see Fig. 5 [2]						
		$V_{CC} = 2.0\text{ V}$	-	18	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	6	19	-	25	ns
		$V_{CC} = 6.0\text{ V}$	-	5	16	-	20	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [3]	-	10	-	-	-	pF
74HCT2G00								
t_{pd}	propagation delay	nA and nB to nY; see Fig. 5 [1]						
		$V_{CC} = 4.5\text{ V}$	-	12	24	-	29	ns
t_t	transition time	$V_{CC} = 4.5\text{ V}$; see Fig. 5 [2]	-	6	19	-	22	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [3]	-	10	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{TLH} and t_{THL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

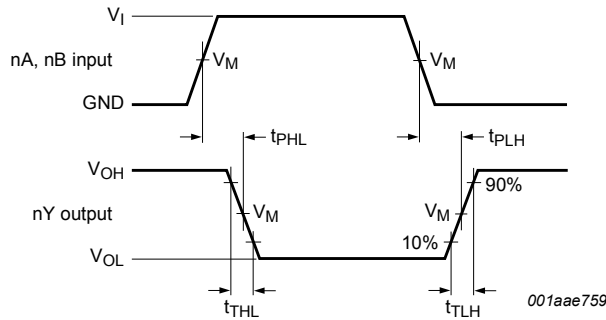
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



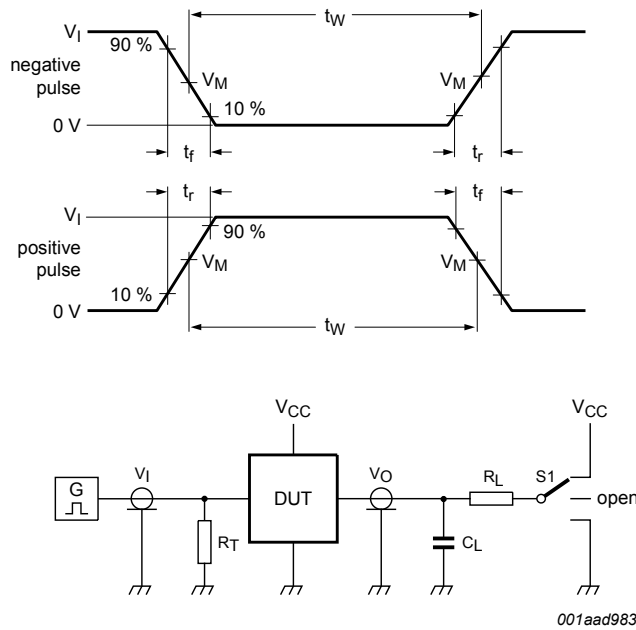
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC2G00	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT2G00	1.3 V	1.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance; S1 = Test selection switch.

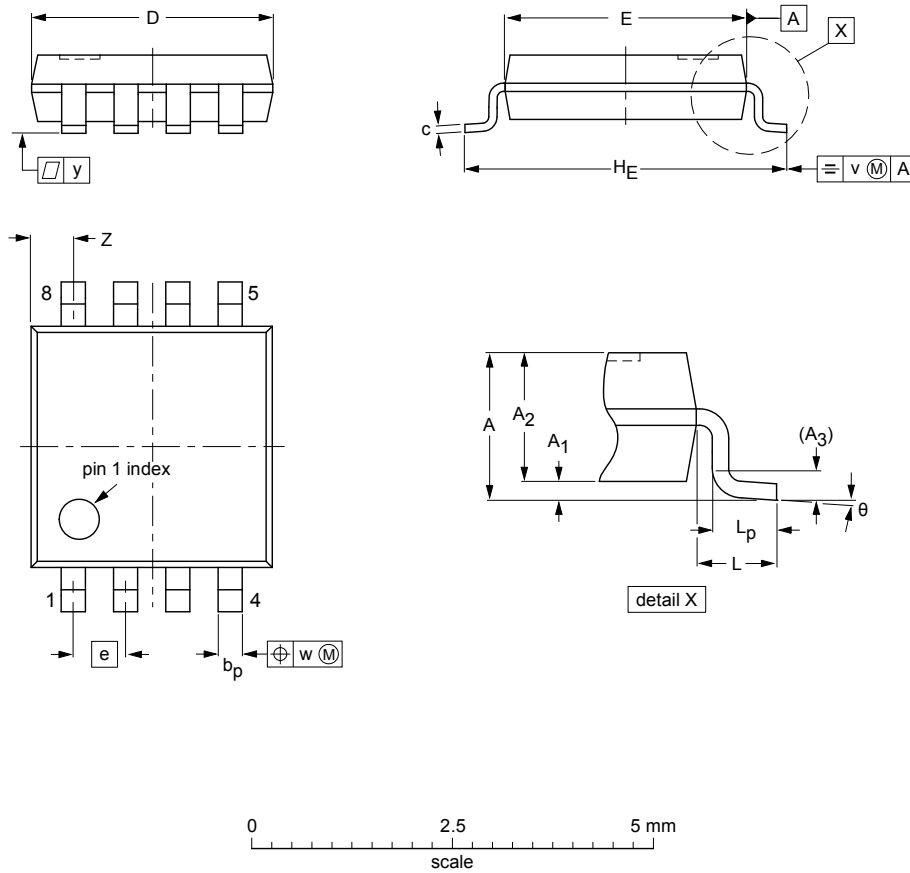
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC2G00	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open
74HCT2G00	3 V	≤ 6 ns	50 pF	1 k Ω	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

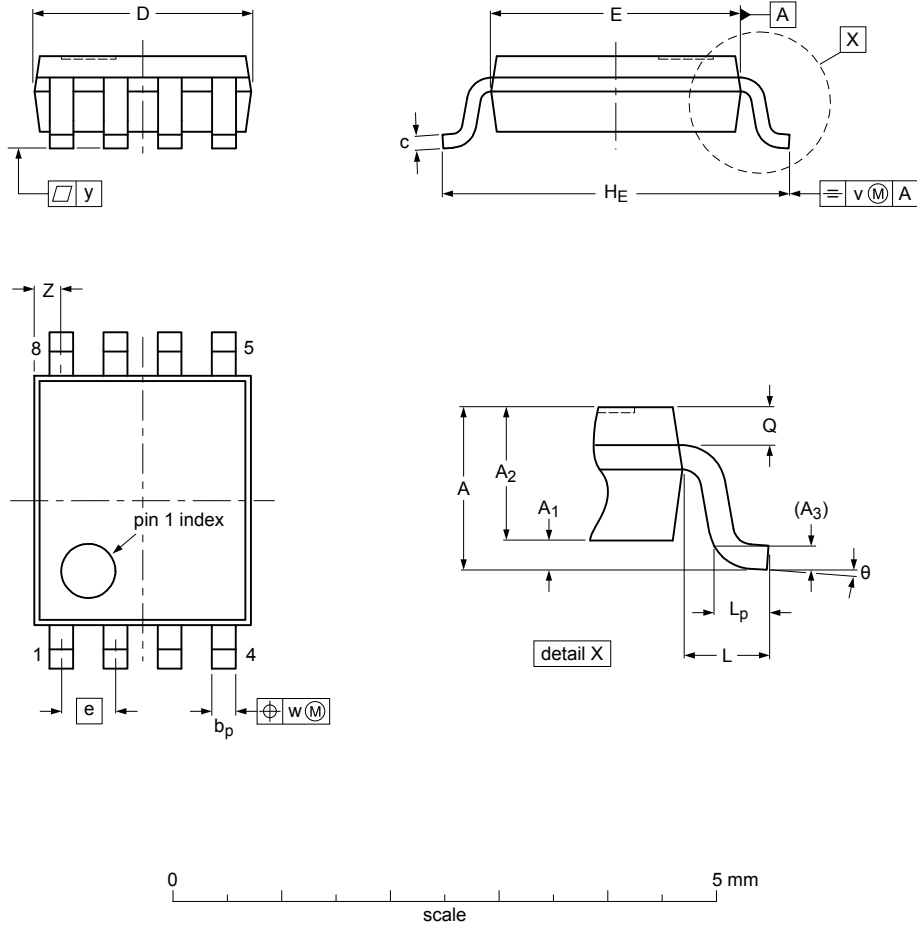
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
max	0.15	0.85			0.27	0.23	2.1	2.4		3.2	0.40	0.21					0.4	8°
mm	nom	1		0.12				0.5		3.0	0.4	0.15		0.2	0.08	0.1	0.1	0°
	min		0.00	0.60	0.17	0.08	1.9	2.2										

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT765-1		MO-187			07-06-02-16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G00 v.6	20181120	Product data sheet	-	74HC_HCT2G00 v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC2G00GD and 74HCT2G00GD (SOT996-2/XSON8) removed. 			
74HC_HCT2G00 v.5	20130926	Product data sheet	-	74HC_HCT2G00 v.4
Modifications:	<ul style="list-style-type: none"> For type numbers 74HC2G00GD and 74HCT2G00GD XSON8U has changed to XSON8. 			
74HC_HCT2G00 v.4	20080703	Product data sheet	-	74HC_HCT2G00 v.3
74HC_HCT2G00 v.3	20060405	Product data sheet	-	74HC_HCT2G00 v.2
74HC_HCT2G00 v.2	20030212	Product specification	-	74HC_HCT2G00 v.1
74HC_HCT2G00 v.1	20020710	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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