THE DATASHEET OF

LP3470M5-2.83/NOPB

LP3470 Voltage Supervisor With Programmable Delay and 1% Reset Threshold

1 Features

- 5-Pin SOT-23 Package
- Open-Drain $\overline{\text{Reset}}$ Output
- Programmable Reset Time-Out Period Using an External Capacitor
- Immune to Short V_{CC} Transients
- ±1% Reset Threshold Accuracy Over Temperature
- Low Quiescent Current (16 µA typical)
- $\overline{\text{Reset}}$ Valid Down to V_{CC} = 0.5 V

2 Applications

- Critical µP and µC Power Monitoring
- Intelligent Instruments
- Computers
- Portable and Battery-Powered Equipment

3 Description

The LP3470 device is a micropower voltage supervisory circuit designed to monitor voltages within 1% of reset threshold over temperature. It provides maximum adjustability for power-on-reset (POR) and supervisory functions.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage falls below a reset threshold. The reset time-out period is adjustable using an external capacitor. Reset remains asserted for an interval (programmed by an external capacitor) after V_{CC} has risen above the threshold voltage.

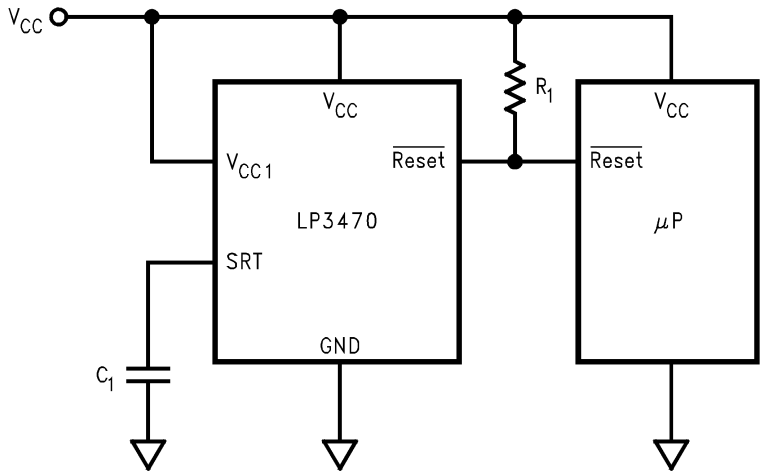
For information on available reset threshold voltage options, see *Mechanical, Packaging, and Orderable Information*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3470	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the Package Option Addendum at the end of the data sheet.

Basic Operating Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G — **Page**

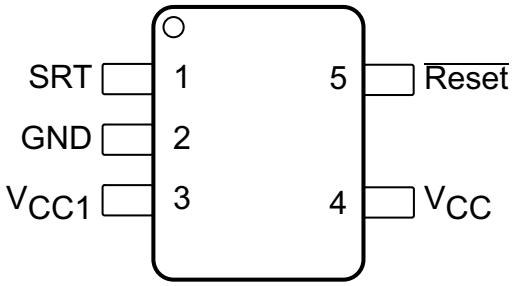
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved *Operating temperature* parameters from *Absolute Maximum Ratings* to *Recommended Operating Conditions* ... 4

Changes from Revision E (September 2009) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SRT	O	Set reset time-out. Connect a capacitor between this pin and ground to select the reset time-out period (t_{RP}). t_{RP} = 2000 × C_1 (C_1 in µF and t_{RP} in ms). If no capacitor is connected, leave this pin floating.
2	GND	—	Ground pin.
3	V_{CC1}	I	Always connect to pin V_{CC} (Pin 4).
4	V_{CC}	I	Supply voltage, and reset threshold monitor input.
5	$\overline{\text{Reset}}$	O	Open-drain, active-low reset output. Connect to an external pullup resistor. $\overline{\text{Reset}}$ changes from high to low whenever the monitored voltage (V_{CC}) drops below the reset threshold voltage (V_{RTH}). Once V_{CC} exceeds V_{RTH}, $\overline{\text{Reset}}$ remains low for the reset time-out period (t_{RP}) and then goes high.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{CC} voltage	–0.3	6	V
$\overline{\text{Reset}}$ voltage	–0.3	6	V
Output current ($\overline{\text{Reset}}$)		10	mA
Power dissipation (T_A = 25°C)(3)		300	mW
Lead temperature (soldering, 5 sec)		260	°C
Junction temperature, T_{JMAX}		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/ \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Operating voltage		0.5		5.5	V
T_A	Operating temperature	LP3470	–20		85	°C
		LP3470I	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)		LP3470 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits and typical numbers are for T_J = 25°C, and V_{CC} = 2.4 V to 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{CC}	Operating voltage	T_J = –20°C to 85°C		0.5		5.5	V
I_{CC}	V_{CC} supply current	V_{CC} = 4.5 V	T_J = 25°C		16		µA
			T_J = –20°C to 85°C			30	
V_{RTH}	Reset threshold voltage	LP3470		0.99 × V_{RTH}	V_{RTH}	1.01 × V_{RTH}	V
		LP3470I	T_J = 25°C	0.99 × V_{RTH}	V_{RTH}	1.01 × V_{RTH}	
			T_J = –40°C to 85°C	0.985 × V_{RTH}		1.015 × V_{RTH}	
V_{HYST}	Hysteresis voltage(3)	T_J = 25°C			35		mV
		T_J = –20°C to 85°C		15		65	
t_{PD}	V_{CC} to reset delay	V_{CC} falling at 1 mV/µs	T_J = 25°C		100		µs
			T_J = –20°C to 85°C			300	
t_{RP}	Reset time-out period(4)	C_1 = 1 nF	T_J = 25°C		2		ms
			T_J = –20°C to 85°C	1		3.5	
V_{OL}	Reset output voltage low	V_{CC} = 0.5 V, I_{OL} = 30 µA, T_J = –20°C to 85°C				0.1	V
		V_{CC} = 1 V, I_{OL} = 100 µA, T_J = –20°C to 85°C				0.1	
		V_{CC} = V_{RTH} − 100 mV, I_{OL} = 4 mA, T_J = –20°C to 85°C				0.4	
R_1	External pullup resistor			0.68	20	68	kΩ
I_{LEAK}	Reset output leakage current	T_J = 25°C			0.15	1	µA
		T_J = –20°C to 85°C				6	

(1) Minimum and maximum limits in standard typeface are 100% production tested at 25°C. Minimum and maximum limits in full operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) V_{HYST} affects the relation between V_{CC} and $\overline{\text{Reset}}$ as shown in the timing diagram.
(4) t_{RP} is programmable by varying the value of the external capacitor (C_1) connected to pin SRT. The equation is: t_{RP} = 2000 × C_1 (C_1 in µF and t_{RP} in ms).

6.6 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

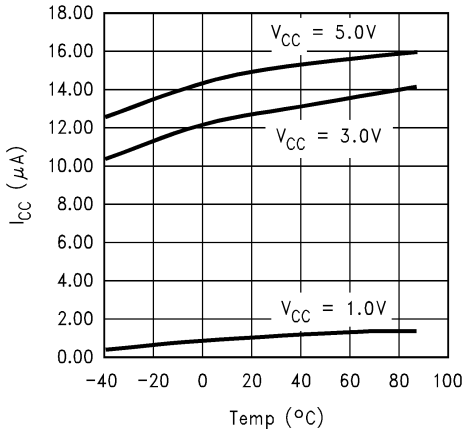


Figure 1. I_{CC} vs Temperature

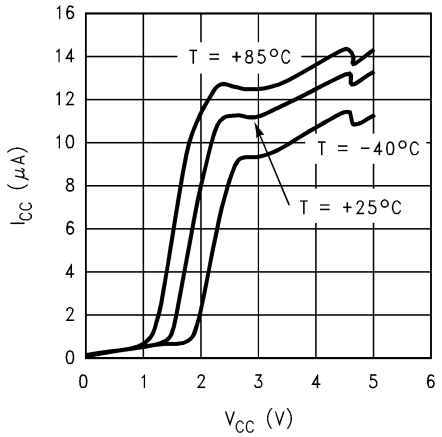


Figure 2. I_{CC} vs V_{CC}

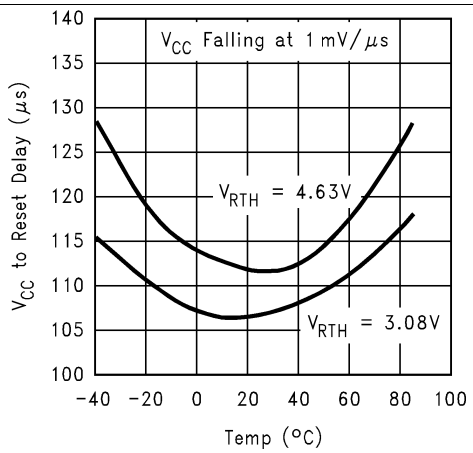


Figure 3. V_{CC} to Reset Delay vs Temperature

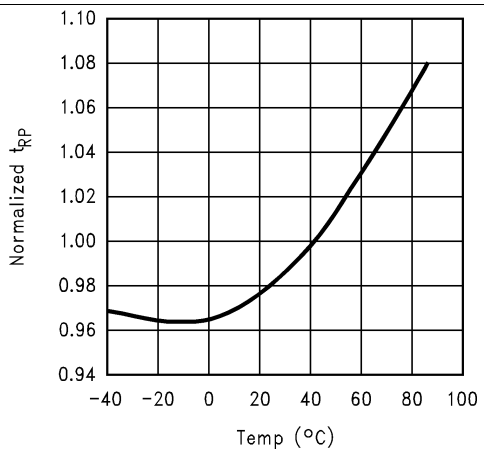


Figure 4. Normalized t_{RP} vs Temperature

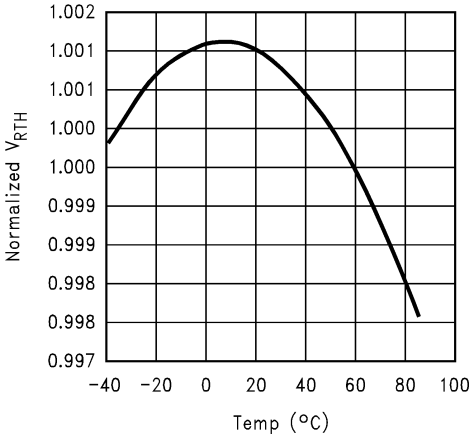


Figure 5. Normalized V_{RTH} vs Temperature

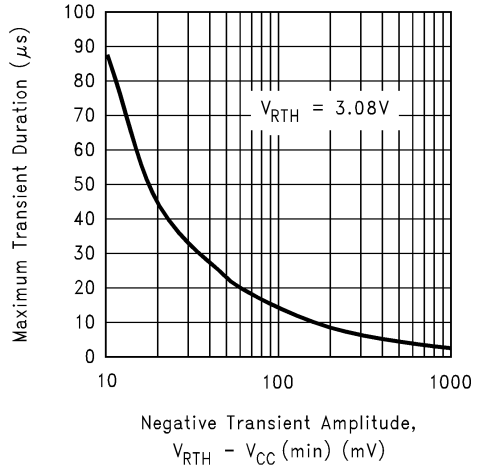


Figure 6. Transient Rejection

Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

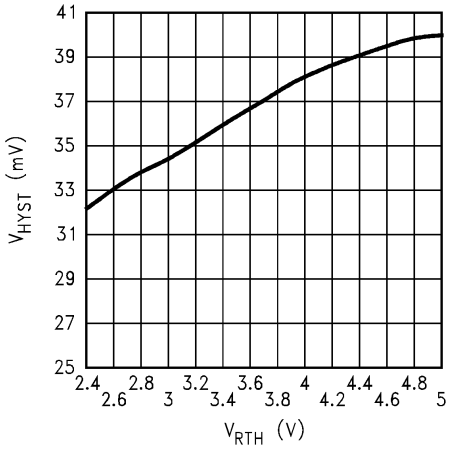


Figure 7. V_{HYST} vs V_{RTH}

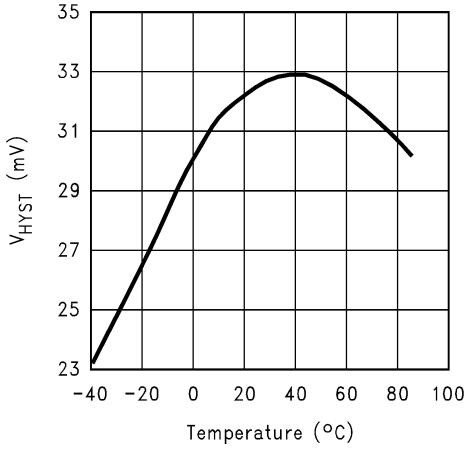


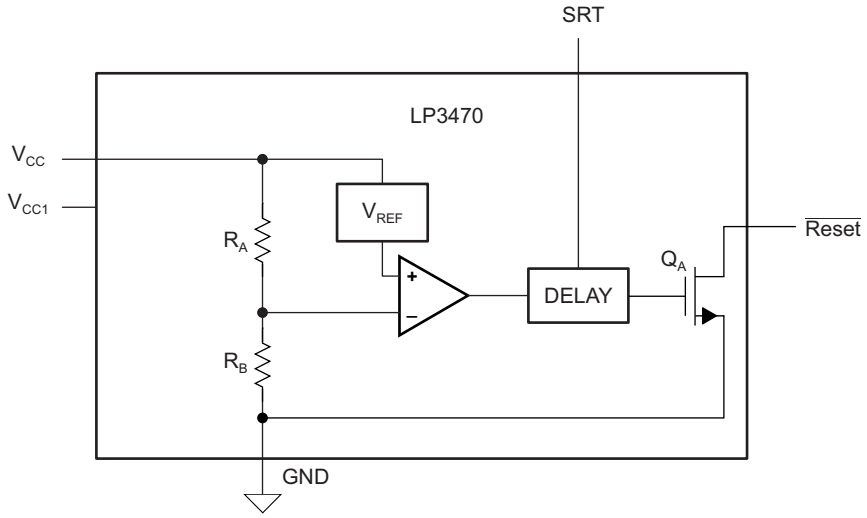
Figure 8. V_{HYST} vs Temperature

7 Detailed Description

7.1 Overview

The LP3470 micropower voltage supervisory circuit provides a simple solution to monitor the power supplies in microprocessor and digital systems and provides a reset controlled by the factory-programmed reset threshold on the V_{CC} supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for an interval programmed by an external capacitor after V_{CC} has risen above the threshold voltage. The reset threshold options are 2.63 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 $\overline{\text{Reset}}$ Time-Out Period

The reset time-out period (t_{RP}) is programmable using an external capacitor (C_1) connected to pin SRT of LP3470. A ceramic chip capacitor rated at or above 10 V is sufficient. The reset time-out period (t_{RP}) can be calculated using Equation 1.

$$t_{RP}\ (ms) = 2000 \times C_1\ (\mu F) \quad (1)$$

For example a C_1 of 100 nF will achieve a t_{RP} of 200 ms. If no delay due to t_{RP} is needed in a certain application, the pin SRT must be left floating.

7.3.2 $\overline{\text{Reset}}$ Output

In applications like microprocessor (µP) systems, errors might occur in system operation during power up, power down, or brownout conditions. It is imperative to monitor the power supply voltage to prevent these errors from occurring.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage is below a threshold (V_{RTH}) voltage. $\overline{\text{Reset}}$ is ensured to be a logic low for V_{CC} > 0.5 V. Once V_{CC} exceeds the reset threshold, the reset is kept asserted for a time period (t_{RP}) programmed by an external capacitor (C_1); after this interval $\overline{\text{Reset}}$ goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold minus a small hysteresis), $\overline{\text{Reset}}$ goes low. When V_{CC} returns above the reset threshold, $\overline{\text{Reset}}$ remains low for a time period t_{RP} before going to logic high. Figure 9 shows this behavior.

Feature Description (continued)

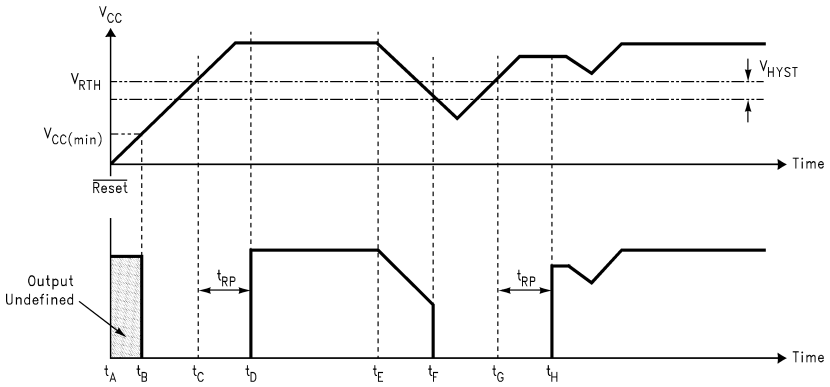


Figure 9. $\overline{\text{Reset}}$ Output Timing Diagram

7.3.3 Pullup Resistor Selection

The $\overline{\text{Reset}}$ output structure of the LP3470 is a simple open-drain N-channel MOSFET switch. A pullup resistor (R_1) must be connected to V_{CC}.

R_1 must be large enough to limit the current through the output MOSFET (Q_1) below 10 mA. A resistor value of more than 680 Ω ensures this. R_1 must also be small enough to ensure a logic high while supplying all the leakage current through the $\overline{\text{Reset}}$ pin. A resistor value of less than 68 kΩ satisfies this condition. A typical pullup resistor value of 20 kΩ is sufficient in most applications.

7.3.4 Negative-Going V_{CC} Transients

The LP3470 is relatively immune to short duration negative-going V_{CC} transients (glitches). The *Typical Characteristics* show the maximum transient duration versus negative transient amplitude (see Figure 6), for which reset pulses are not generated. This graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the transient amplitude increases (in other words, goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1-µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

7.4 Device Functional Modes

7.4.1 $\overline{\text{Reset}}$ Output Low

When the V_{CC} supply voltage is below a threshold (V_{RTH}) voltage minus a hysteresis (V_{HYST}) voltage, the $\overline{\text{Reset}}$ pin will output logic low. $\overline{\text{Reset}}$ is ensured to be a logic low for V_{CC} > 0.5 V.

7.4.2 $\overline{\text{Reset}}$ Output High

When the V_{CC} supply voltage exceeds the reset threshold, the $\overline{\text{Reset}}$ is kept asserted for a time period (t_{RP}) programmed by an external capacitor (C_1); after this interval Reset goes to logic high.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3470 is a micropower CMOS voltage supervisor that is ideal for use in battery-powered microprocessor and other digital systems. It is small in size and provides maximum adjustability for power-on-reset (POR) and supervisory functions, making it a good solution in a variety of applications. The LP3470 is available in six standard reset threshold voltage options, and the reset time-out period is adjustable using an external capacitor providing maximum flexibility in any application. This device can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum V_{in} supply is satisfied.

8.2 Typical Application

The LP3470 can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in Figure 10.

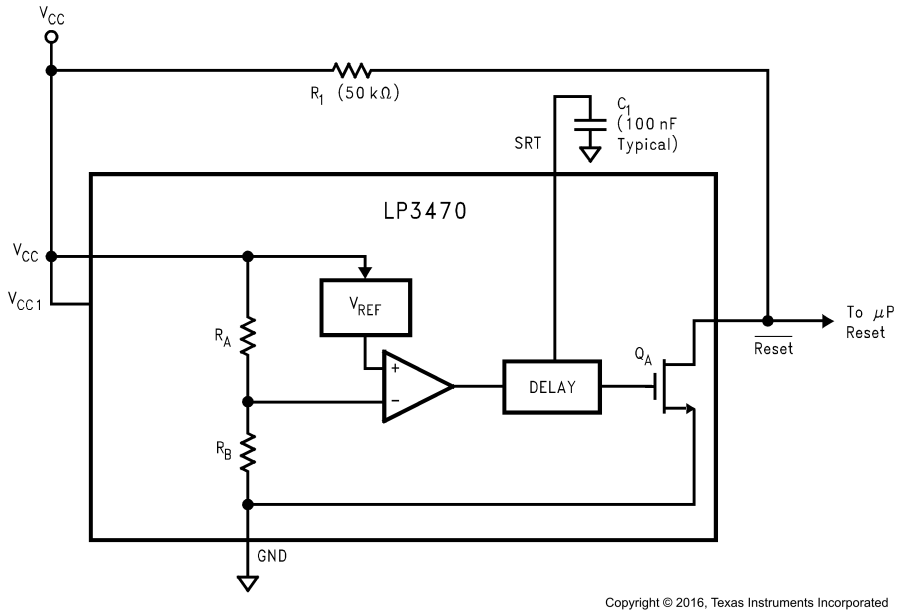


Figure 10. Power-On Reset Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage	0.5 to 5.5 V
Reset threshold voltage	2.63 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V
External pullup resistor	0.68 to 68 kΩ
External reset time-out period capacitor	C_1 = 1 nF
Reset time-out period	2 ms

8.2.2 Detailed Design Procedure

The minimum application circuit requires the LP3470 Power-On Reset Circuit IC and a pullup resistor connecting the reset pin to V_{CC}. The reset delay can be programmed with an additional capacitor connected from the SRT pin to GND. See *Reset Time-Out Period* and *Pullup Resistor Selection* for information on choosing specific values for components.

8.2.3 Application Curves

Two capacitor values for C_D (0.1 µF and 1 µF) are used as examples to show the programmability of the output time delay as shown in Figure 11 and Figure 12.

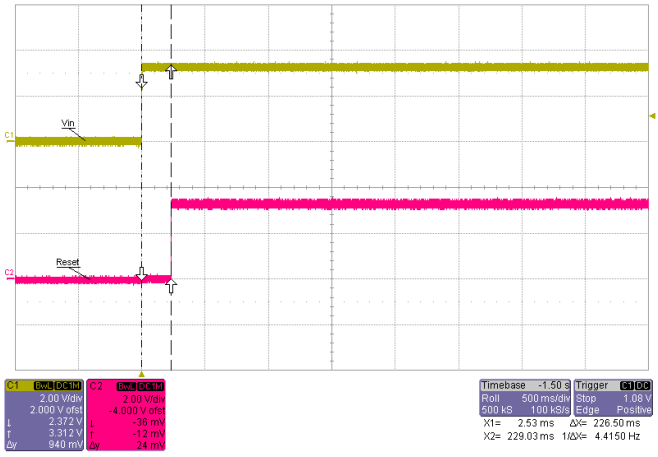


Figure 11. 0.1-µF Capacitor Programmed Delay

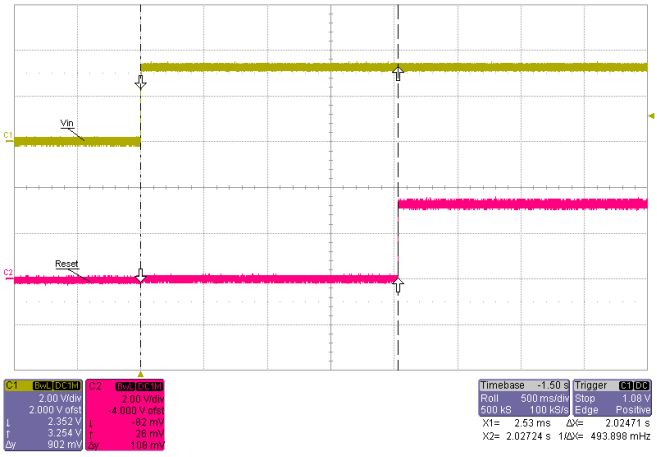


Figure 12. 1-µF Capacitor Programmed Delay

9 Power Supply Recommendations

The input of the LP3470 is designed to handle up to the supply voltage absolute maximum rating of 6 V. If the input supply is susceptible to any large transients above the maximum rating, then take extra precautions. An input capacitor is optional but not required to help avoid false reset output triggers due to noise.

10 Layout

10.1 Layout Guidelines

- Place components as close as possible to the IC
- Keep traces short between the IC and the C_1 capacitor to ensure the timing delay is as accurate as possible.

10.2 Layout Example

Figure 13 shows a layout example.

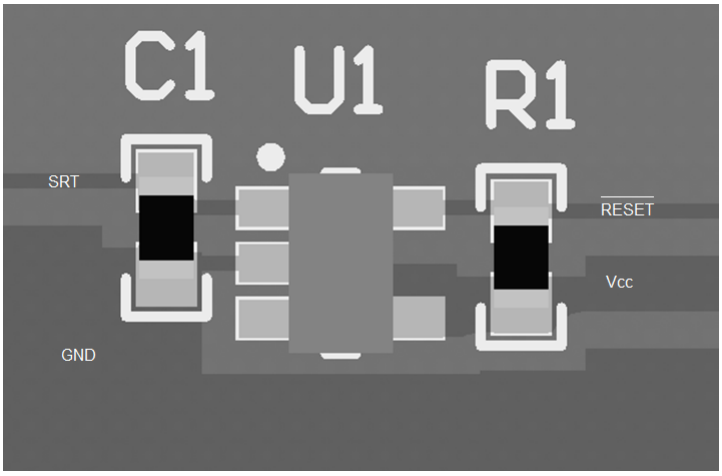


Figure 13. LP3470 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3470IM5-2.63/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D25C	
LP3470IM5-2.75/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D38C	
LP3470IM5-2.83/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D39C	
LP3470IM5-2.93	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D26C	
LP3470IM5-2.93/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D26C	
LP3470IM5-3.08	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D28C	
LP3470IM5-3.08/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D28C	
LP3470IM5-3.65/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D37C	
LP3470IM5-4.00	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D29C	
LP3470IM5-4.00/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D29C	
LP3470IM5-4.38	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D30C	
LP3470IM5-4.38/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D30C	
LP3470IM5-4.63	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D31C	
LP3470IM5-4.63/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D31C	
LP3470IM5-4.8/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D15C	
LP3470IM5X-2.63/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D25C	
LP3470IM5X-2.83/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D39C	
LP3470IM5X-2.93/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D26C	
LP3470IM5X-3.08	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	D28C	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3470IM5X-3.08/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D28C	
LP3470IM5X-4.00	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	D29C	
LP3470IM5X-4.00/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D29C	
LP3470IM5X-4.38/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D30C	
LP3470IM5X-4.63/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D31C	
LP3470M5-2.63/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D25B	
LP3470M5-2.93/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D26B	
LP3470M5-3.08	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-20 to 85	D28B	
LP3470M5-3.08/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D28B	
LP3470M5-4.00/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D29B	
LP3470M5-4.38/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D30B	
LP3470M5-4.63	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-20 to 85	D31B	
LP3470M5-4.63/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D31B	
LP3470M5X-2.93/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D26B	
LP3470M5X-3.08/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D28B	
LP3470M5X-4.00/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D29B	
LP3470M5X-4.63/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	D31B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

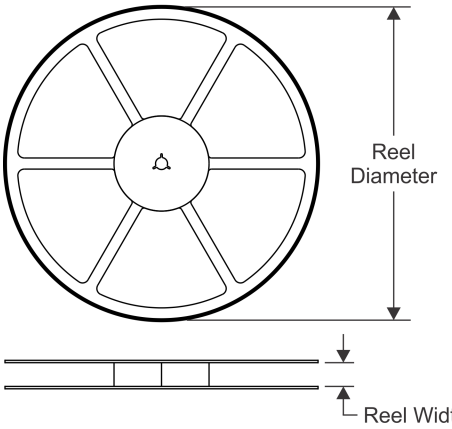
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

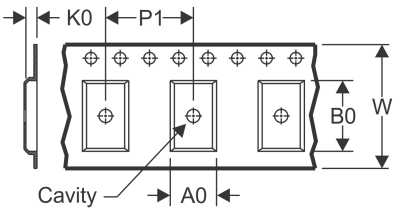
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

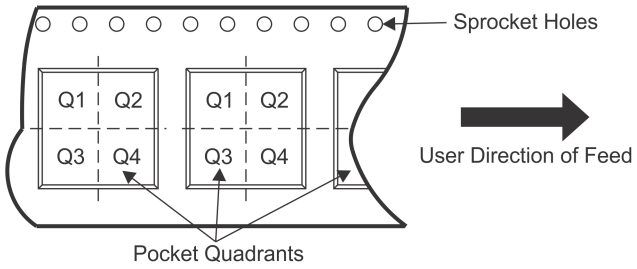


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

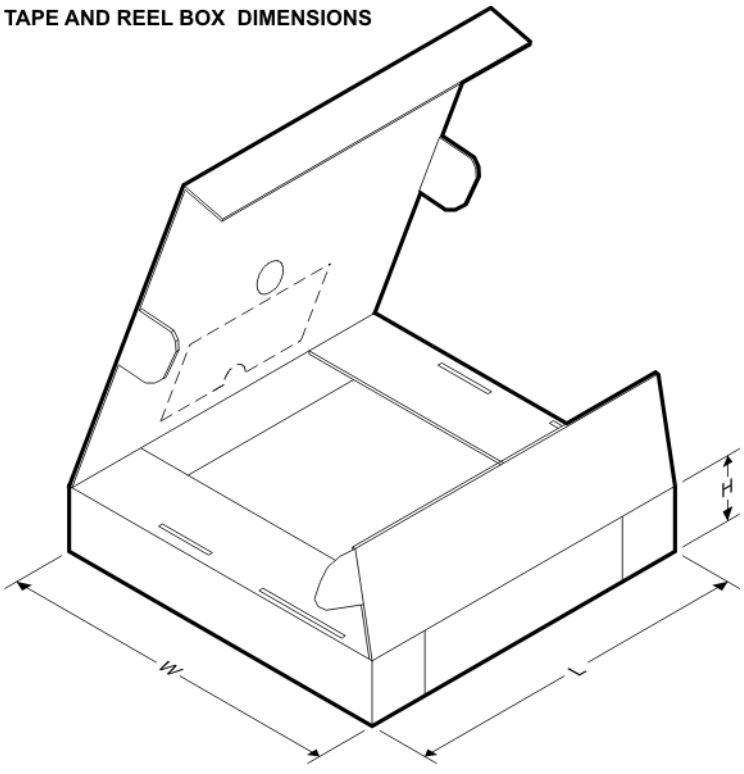


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470IM5-2.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.75/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.83/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.93	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.93/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.08	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.65/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.00	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.00/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.38	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.38/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.63	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.83/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.93/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470IM5X-3.08	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.00	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.00/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.38/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-2.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-2.93/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-3.08	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.00/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.38/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.63	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-2.93/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-4.00/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-4.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

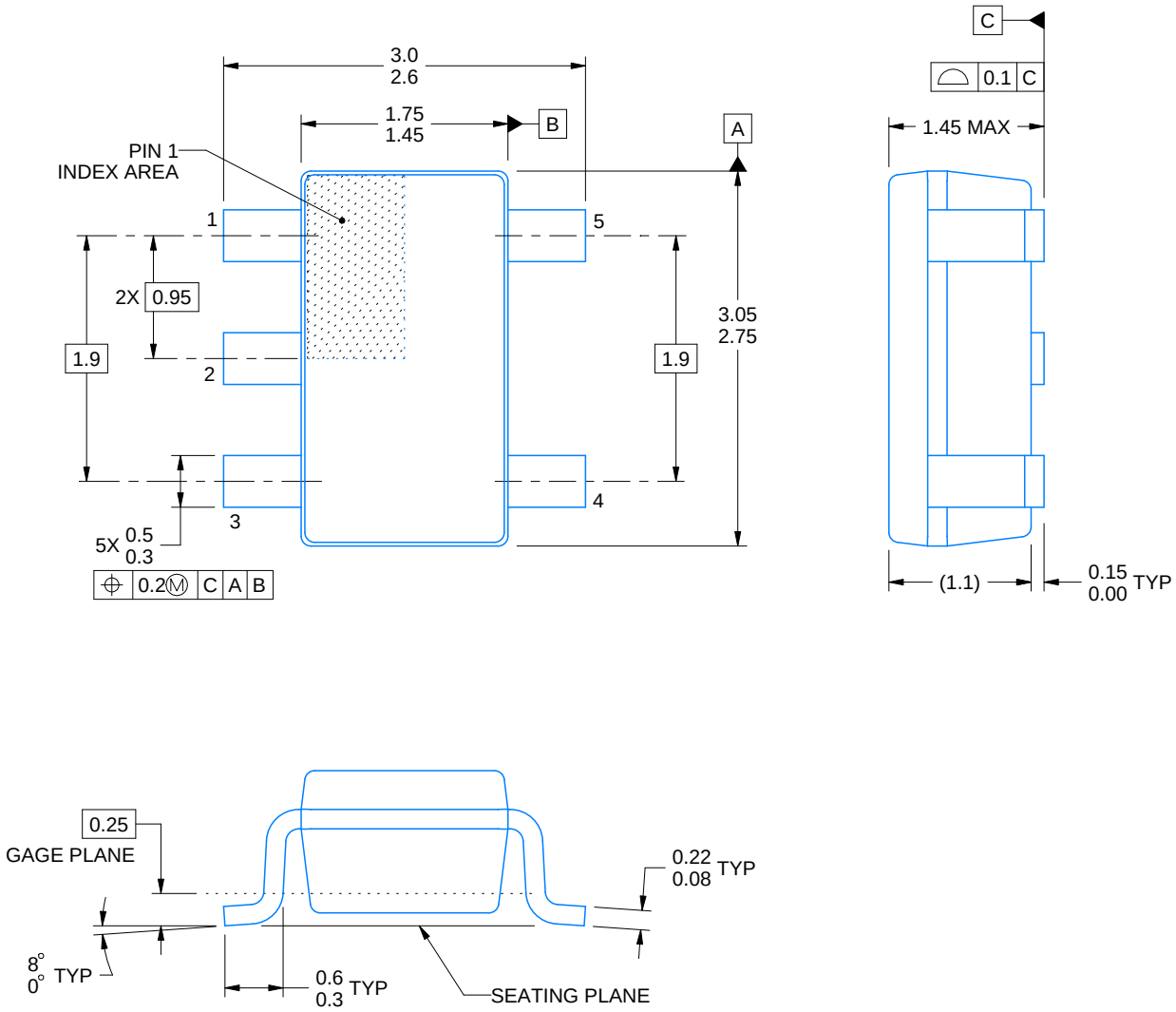
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3470IM5-2.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.75/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.83/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.93	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.93/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.08	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.65/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.00	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.00/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.38	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.38/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.63	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5X-2.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-2.83/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-2.93/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-3.08	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-3.08/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.00	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.00/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.38/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5-2.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-2.93/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-3.08	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.00/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.38/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.63	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5X-2.93/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-3.08/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-4.00/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-4.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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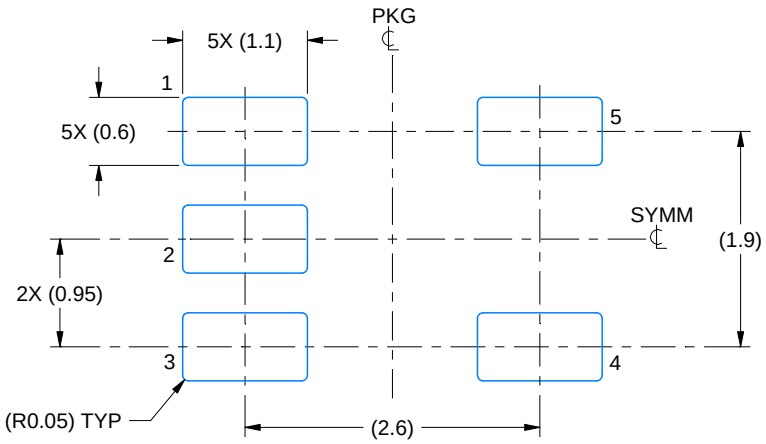
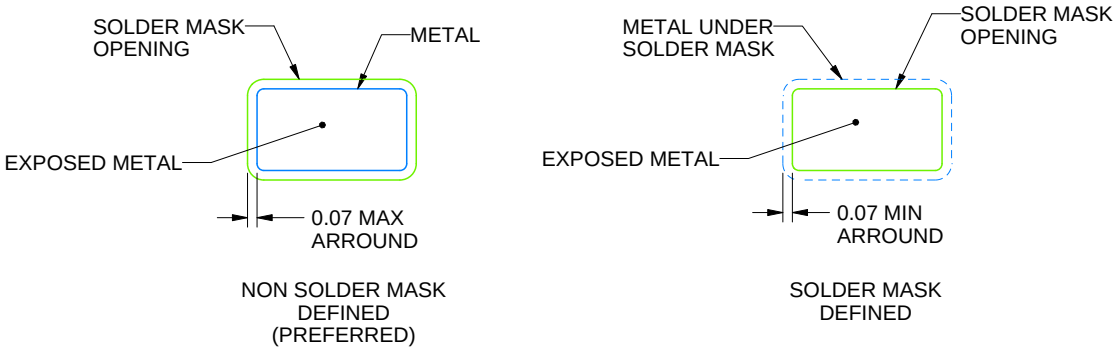
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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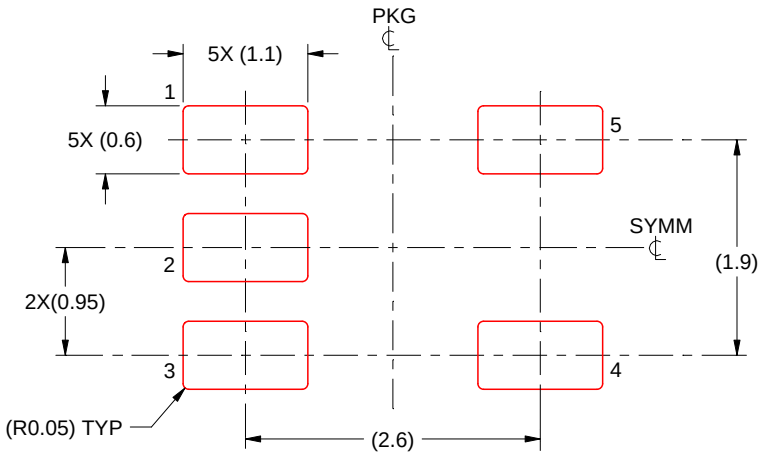
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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