PCA8575

Remote 16-bit I/O expander for I²C-bus with interrupt

Rev. 02 — 21 March 2007 Product data sheet

1. General description

The PCA8575 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional I²C-bus (serial clock (SCL), serial data (SDA)).

The device consists of a 16-bit quasi-bidirectional port and an I²C-bus interface. The PCA8575 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs.

The PCA8575 also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. The internal Power-On Reset (POR) initializes the I/Os as inputs.

2. Features

- 400 kHz I²C-bus interface
- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 16-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 400 mA
- Active LOW open-drain interrupt output
- 8 programmable slave addresses using 3 address pins
- Readable device ID (manufacturer, device type, and revision)
- Low standby current (10 μA max.)
- –40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO24, SSOP24 (QSOP24), TSSOP24, HVQFN24, DHVQFN24

3. Applications

- LED signs and displays
- Servers
- Industrial control
- Medical equipment
- PLCs
- Cellular telephones

- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA8575D	PCA8575D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA8575DB	PCA8575DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
PCA8575DK	PCA8575	SSOP24[1]	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
PCA8575PW	PCA8575PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA8575BQ	8575	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1
PCA8575BS	8575	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

[1] Also known as QSOP24.

5. Block diagram

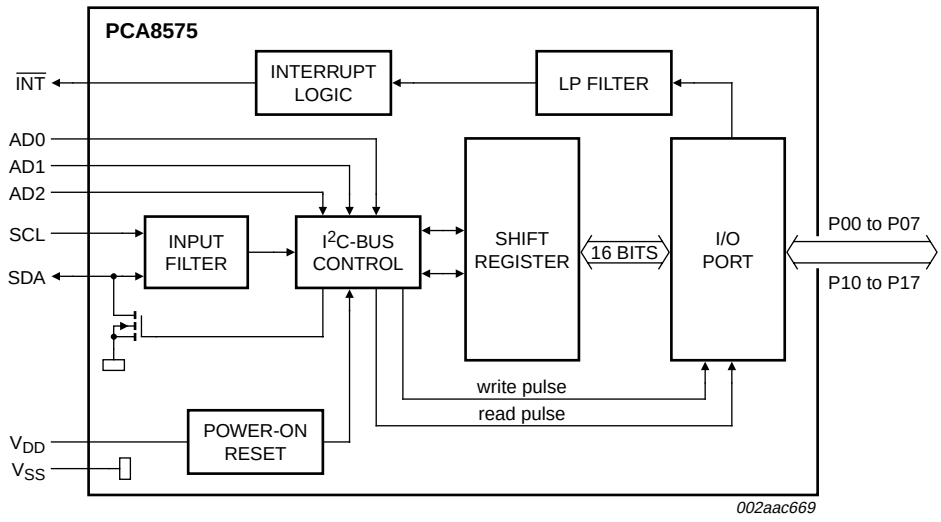


Fig 1. Block diagram of PCA8575

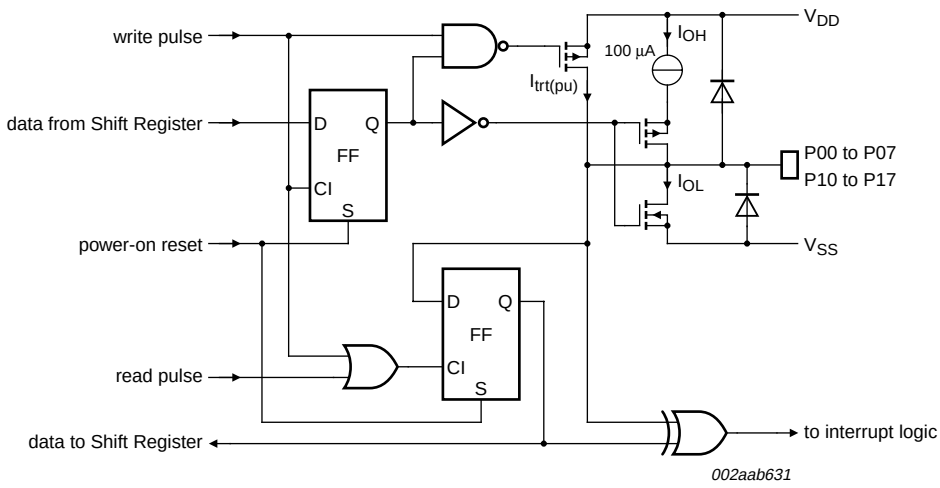


Fig 2. Simplified schematic diagram of P00 to P17

6. Pinning information

6.1 Pinning

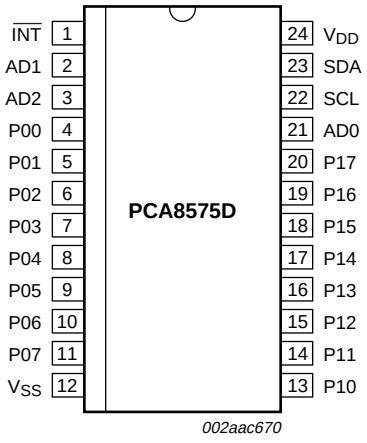


Fig 3. Pin configuration for SO24

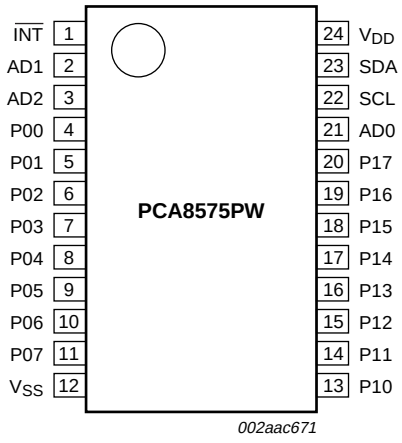


Fig 4. Pin configuration for TSSOP24

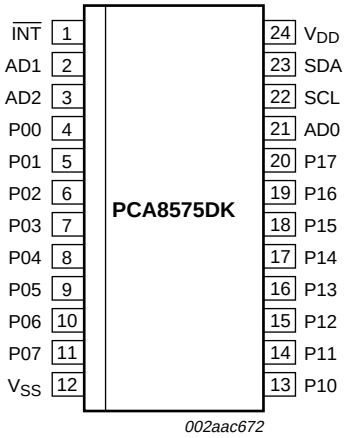


Fig 5. Pin configuration for SSOP24 (QSOP24)

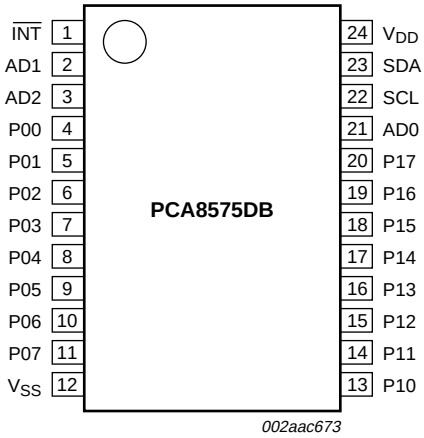
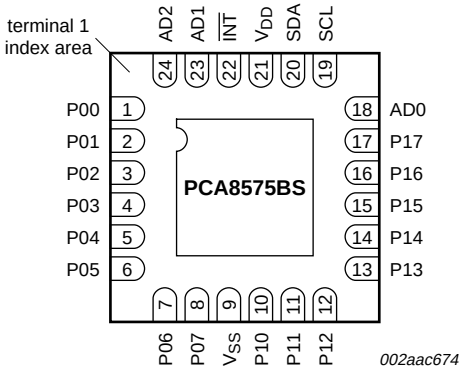
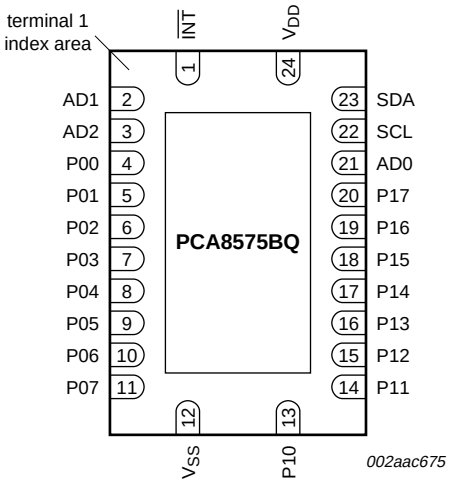


Fig 6. Pin configuration for SSOP24



Transparent top view

Fig 7. Pin configuration for HVQFN24



Transparent top view

Fig 8. Pin configuration for DHVQFN24

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SO24, SSOP24, TSSOP24, DHVQFN24	HVQFN24	
$\overline{INT}$	1	22	interrupt output (active LOW)
AD1	2	23	address input 1
AD2	3	24	address input 2
P00	4	1	quasi-bidirectional I/O 00
P01	5	2	quasi-bidirectional I/O 01
P02	6	3	quasi-bidirectional I/O 02
P03	7	4	quasi-bidirectional I/O 03
P04	8	5	quasi-bidirectional I/O 04
P05	9	6	quasi-bidirectional I/O 05
P06	10	7	quasi-bidirectional I/O 06
P07	11	8	quasi-bidirectional I/O 07
V_{SS}	12[1]	9[1]	supply ground
P10	13	10	quasi-bidirectional I/O 10
P11	14	11	quasi-bidirectional I/O 11
P12	15	12	quasi-bidirectional I/O 12
P13	16	13	quasi-bidirectional I/O 13
P14	17	14	quasi-bidirectional I/O 14
P15	18	15	quasi-bidirectional I/O 15
P16	19	16	quasi-bidirectional I/O 16
P17	20	17	quasi-bidirectional I/O 17
AD0	21	18	address input 0
SCL	22	19	serial clock line input
SDA	23	20	serial data line input/output
V_{DD}	24	21	supply voltage

[1] HVQFN and DHVQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA8575”.

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA8575 is shown in Figure 9. Slave address pins AD2, AD1, and AD0 choose 1 of 8 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table 3 “PCA8575 address map”.

Remark: The General Call address (0000 0000b) and the Device ID address (1111 100Xb) are reserved and cannot be used as device address. Failure to follow this requirement will cause the PCA8575 not to acknowledge.

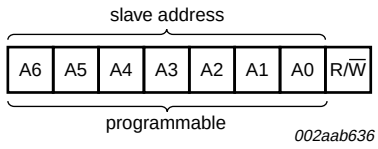


Fig 9. PCA8575 address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When AD2, AD1 and AD0 are held to V_{DD} or V_{SS}, the same address as the PCF8575 is applied.

7.1.1 Address map

Table 3. PCA8575 address map

A6	A5	A4	A3	A2	A1	A0	Address (hex)
0	1	0	0	0	0	0	20h
0	1	0	0	0	0	1	21h
0	1	0	0	0	1	0	22h
0	1	0	0	0	1	1	23h
0	1	0	0	1	0	0	24h
0	1	0	0	1	0	1	25h
0	1	0	0	1	1	0	26h
0	1	0	0	1	1	1	27h

8. I/O programming

8.1 Quasi-bidirectional I/O architecture

The PCA8575's 16 ports (see Figure 2) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode (see Figure 12). Output data is transmitted to the ports in the Write mode (see Figure 11).

Every data transmission from the PCA8575 must consist of an even number of bytes, the first byte will be referred to as P07 to P00, and the second byte as P17 to P10. The third will be referred to as P07 to P00, and so on.

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to V_{DD} is active. An additional strong pull-up to V_{DD} ($I_{trt(pu)}$) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the Write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS}.

8.2 Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the Write mode is entered. The PCA8575 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCA8575, the second data byte P17 to P10 is sent by the master. Once again, the PCA8575 acknowledges the receipt of the data. Each 8-bit data is presented on the port lines after it has been acknowledged by the PCA8575.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10). See Figure 10.

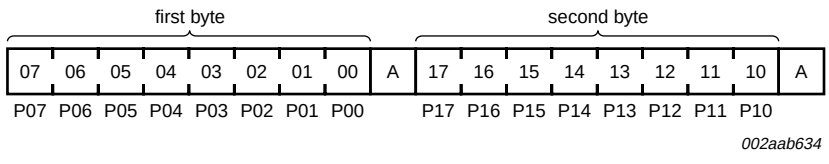


Fig 10. Correlation between bits and ports

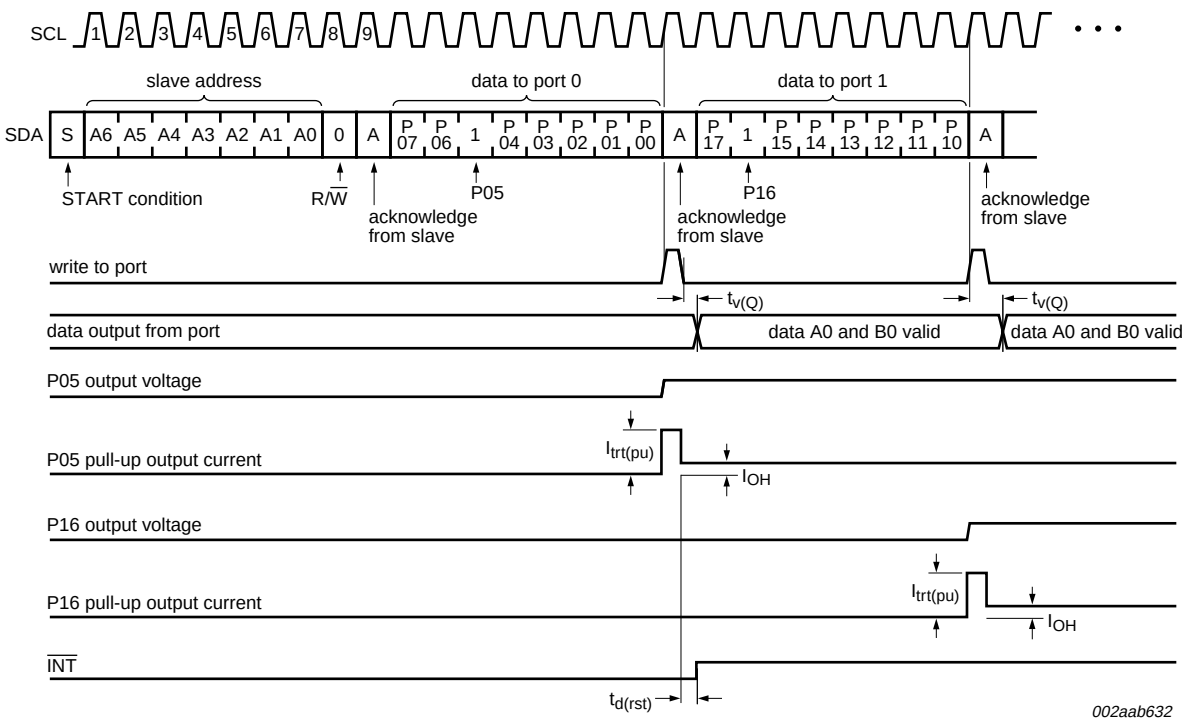
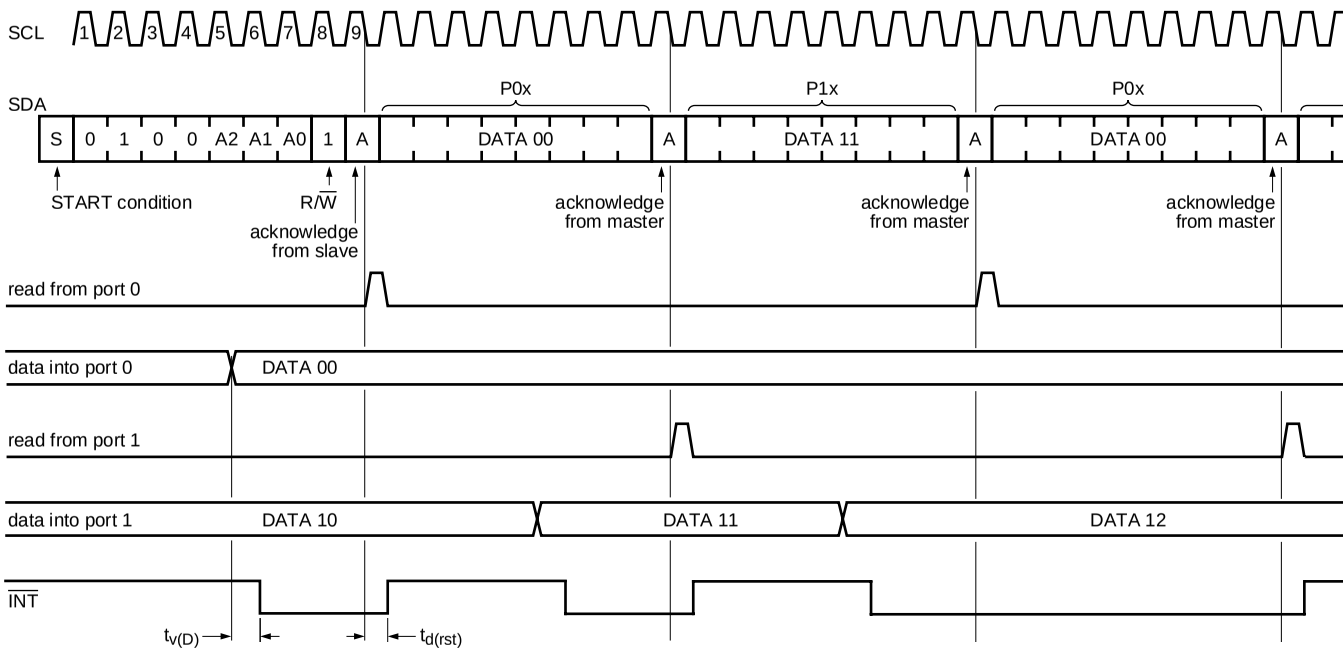


Fig 11. Write mode (output)

8.3 Reading from a port (Input mode)

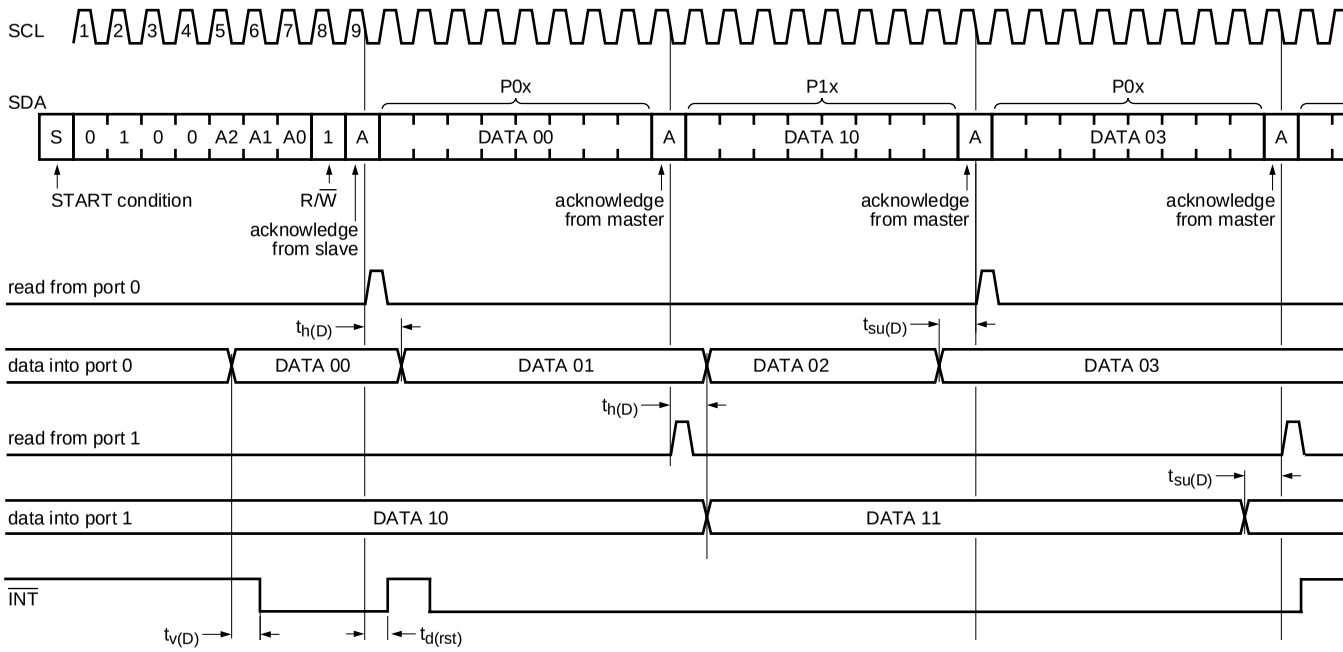
All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.



Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is

Fig 12. Read input port register, scenario 1



Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is

Fig 13. Read input port register, scenario 2

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA8575 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA8575 registers and I²C-bus/SMBus state machine will initialize to their default states. Thereafter V_{DD} must be lowered below 0.2 V to reset the device.

8.5 Interrupt output ($\overline{INT}$)

The PCA8575 provides an open-drain interrupt ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figure 12, Figure 13, and Figure 14). This gives these chips a kind of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time $t_{v(D)}$ the signal $\overline{INT}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the Write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the Read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{INT}$.

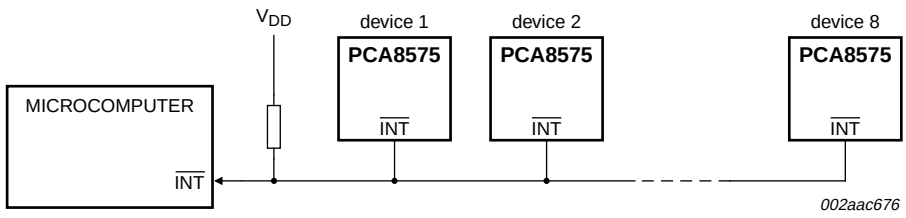


Fig 14. Application of multiple PCA8575s with interrupt

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).

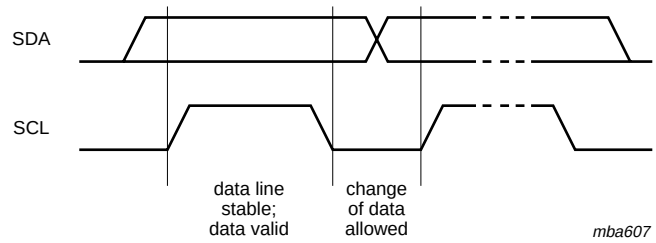


Fig 15. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16.)

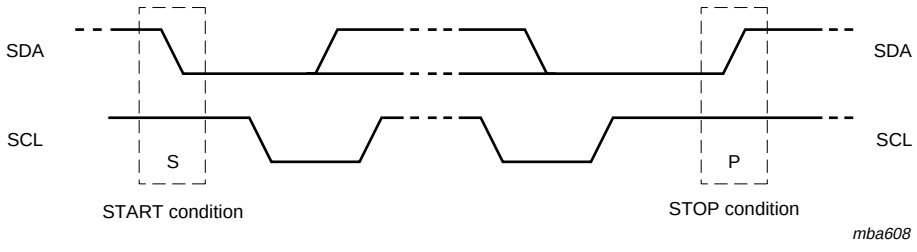


Fig 16. Definition of START and STOP conditions

9.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 17).

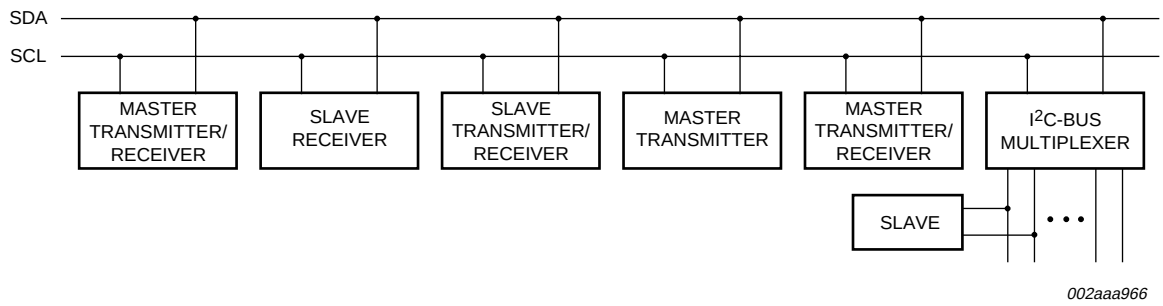


Fig 17. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

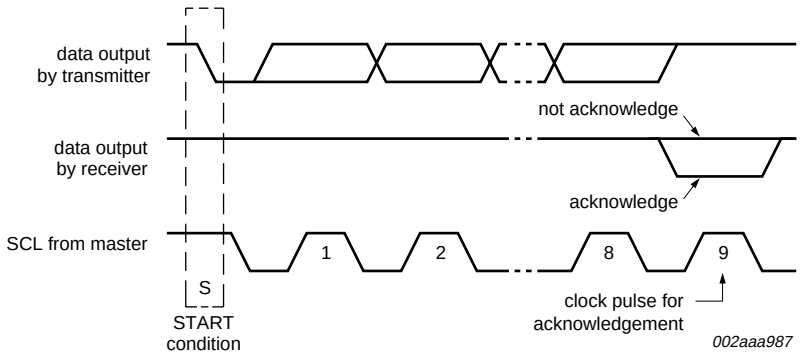


Fig 18. Acknowledgement on the I²C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 19, P00 and P01 are inputs, and P02 to P07 are outputs. When used in this configuration, during a write, the input (P00 and P01) must be written as HIGH so the external devices fully control the input ports. The desired HIGH or LOW logic levels may be written to the I/Os used as outputs (P02 to P07). During a read, the logic levels of the external devices driving the input ports (P00 and P01) and the previous written logic level to the output ports (P02 to P07) will be read.

The GPIO also has an interrupt line ($\overline{INT}$) that can be connected to the interrupt logic of the microprocessor. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there is incoming data or a change of data on its ports without having to communicate via the I²C-bus.

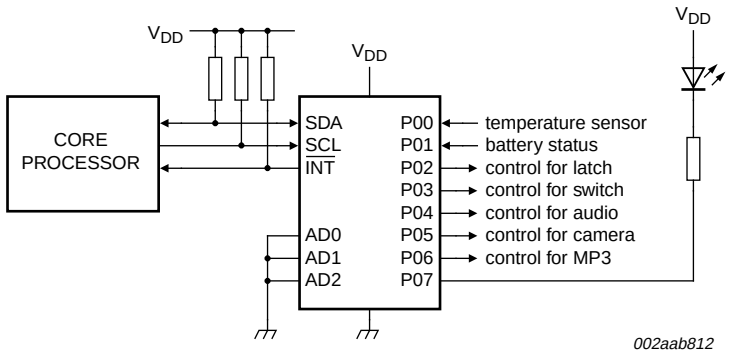


Fig 19. Bidirectional I/O expander application

10.2 High current-drive load applications

The GPIO has a maximum sinking current of 25 mA per bit. In applications requiring additional drive, two port pins in the same octal may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins (one octal) can be connected together to drive 200 mA.

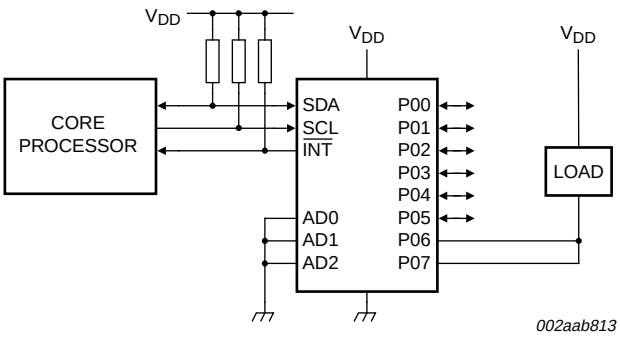


Fig 20. High current-drive load application

10.3 Differences between the PCA8575 and the PCF8575

The PCA8575 is a drop in replacement for the PCF8575 and can used without electrical or software modifications, but there is a difference in interrupt output release timing during the read operation.

Write operations are identical. At the completion of each 8-bit write sequence the data is stored in its associated 8-bit write register at ACK or NACK. The first byte goes to P0n while the second goes to P1n. Subsequent writes without a STOP wrap around to P0n then P1n again. Any write will update both read registers and clear interrupts.

Read operations are identical. Both devices update the byte register with the pin data as each 8-bit read is initiated, the very first read after an address cycle corresponds to ports P0n while the second (even byte) corresponds to P1n and subsequent reads without a STOP wrap around to P0n then P1n again.

During read operations, the PCA8575 interrupt output will be cleared in a byte-wise fashion as each byte is read. Reading the first byte will clear any interrupts associated with the P0n pins. This first byte read operation will have no effect on interrupts associated with changes of state on the P1n pins. Interrupts associated with the P1n pins will be cleared when the second byte is read. Reading the second byte has no effect on interrupts associated with the changes of state on the P0x pins. The PCF8575 interrupt output will clear after reading both bytes of data regardless of whether data was changed in the first byte or the second byte or both bytes.

11. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6	V
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±600	mA
V_I	input voltage		V_{SS} – 0.5	5.5	V
I_I	input current		-	±20	mA
I_O	output current		-	±50[1]	mA
P_{tot}	total power dissipation		-	600	mW
P/out	power dissipation per output		-	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] Total package (maximum) output current is 600 mA.

12. Static characteristics

Table 5. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	Operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 400 kHz	-	100	200	µA
I_{stb}	standby current	Standby mode; no load; $V_I = V_{DD}$ or V_{SS}	-	2.5	10	µA
V_{POR}	power-on reset voltage	[1]	-	1.8	2.0	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	20	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	5	10	pF
I/Os; P00 to P07 and P10 to P17						
I_{OL}	LOW-level output current[2]	V_{OL} = 0.5 V; V_{DD} = 2.3 V	12	28	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	17	35	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	25	42	-	mA
$I_{OL(tot)}$	total LOW-level output current[2]	V_{OL} = 0.5 V; V_{DD} = 4.5 V	-	-	400	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$	−30	−102	−300	µA
$I_{trt(pu)}$	transient boosted pull-up current	$V_{OH} = V_{SS}$; see Figure 11	−0.5	−1.0	-	mA
$C_{io(off)}$	off-state input/output capacitance	[3]	-	9	10	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	6	-	-	mA
C_o	output capacitance		-	3	5	pF
Inputs AD0, AD1, AD2						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.5	5	pF

[1] The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and set all I/Os to logic 1 (with current source to V_{DD}).

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 400 mA due to internal busing limits.

[3] The value is not tested, but verified on sampling basis.

13. Dynamic characteristics

Table 6. Dynamic characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Fast mode I²C-bus			Unit
			Min	Typ	Max	
f_{SCL}	SCL clock frequency		0	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.1	-	0.9	µs
$t_{VD;DAT}$	data valid time	[2]	50	-	-	ns
$t_{SU;DAT}$	data set-up time		100	-	-	ns
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	$20 + 0.1C_b$ [5]	-	300	ns
t_r	rise time of both SDA and SCL signals		$20 + 0.1C_b$ [5]	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	-	50	ns
Port timing; $C_L \leq 100$ pF (see Figure 11 and Figure 12)						
$t_{v(Q)}$	data output valid time		-	-	4	µs
$t_{su(D)}$	data input set-up time		0	-	-	µs
$t_{h(D)}$	data input hold time		4	-	-	µs
Interrupt timing; $C_L \leq 100$ pF (see Figure 11 and Figure 12)						
$t_{v(D)}$	data input valid time		-	-	4	µs
$t_{d(rst)}$	reset delay time		-	-	4	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

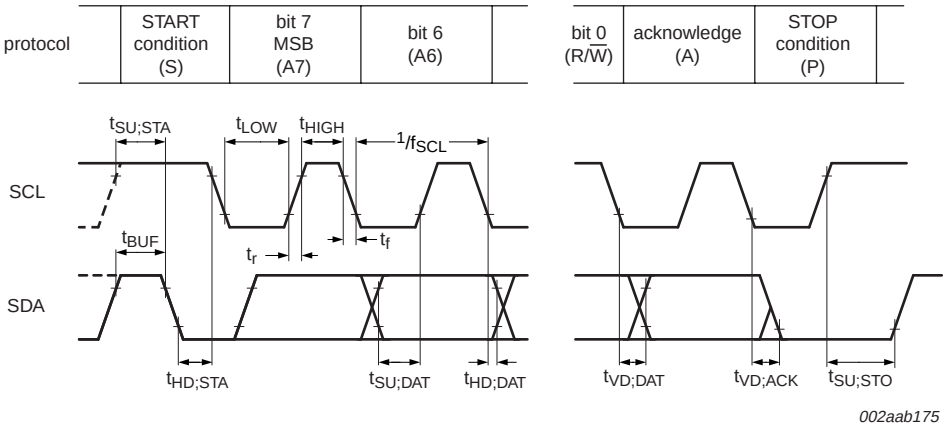
[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

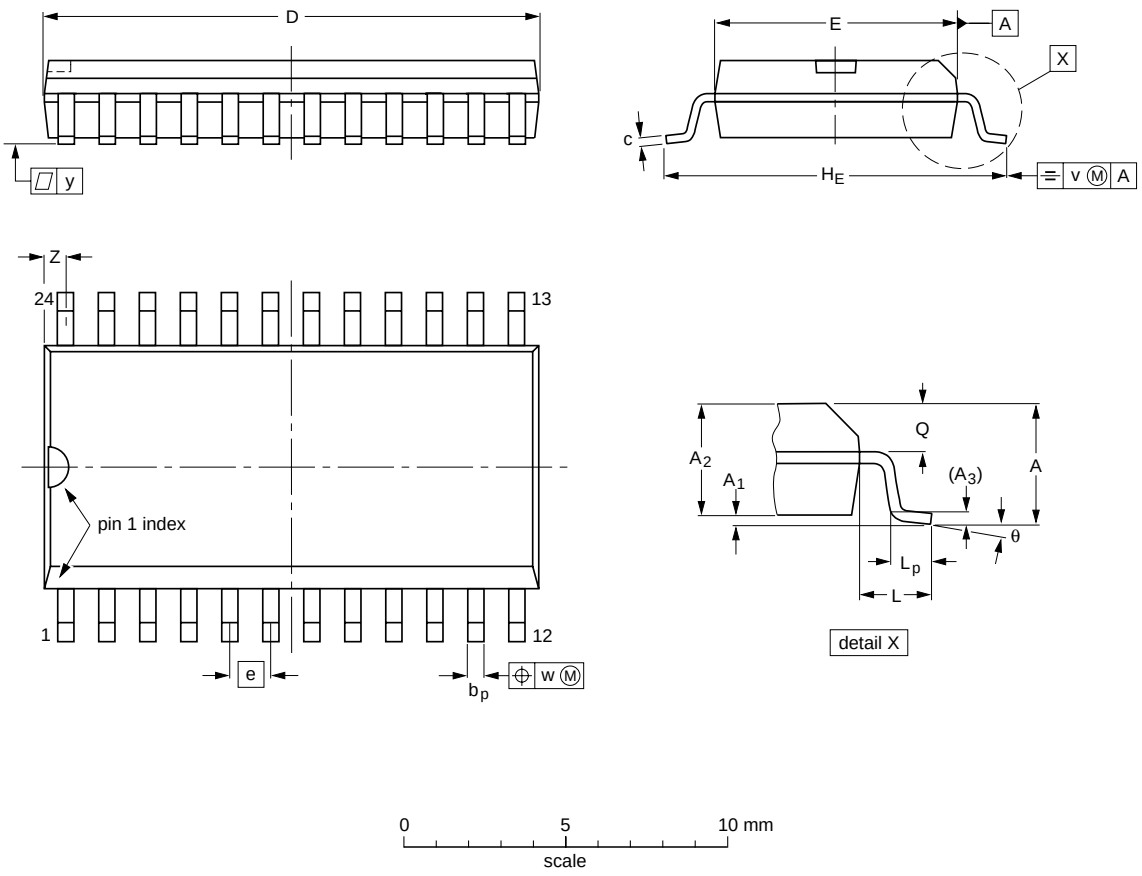


Rise and fall times refer to V_{IL} and V_{IH}.

Fig 21. I²C-bus timing diagram

14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

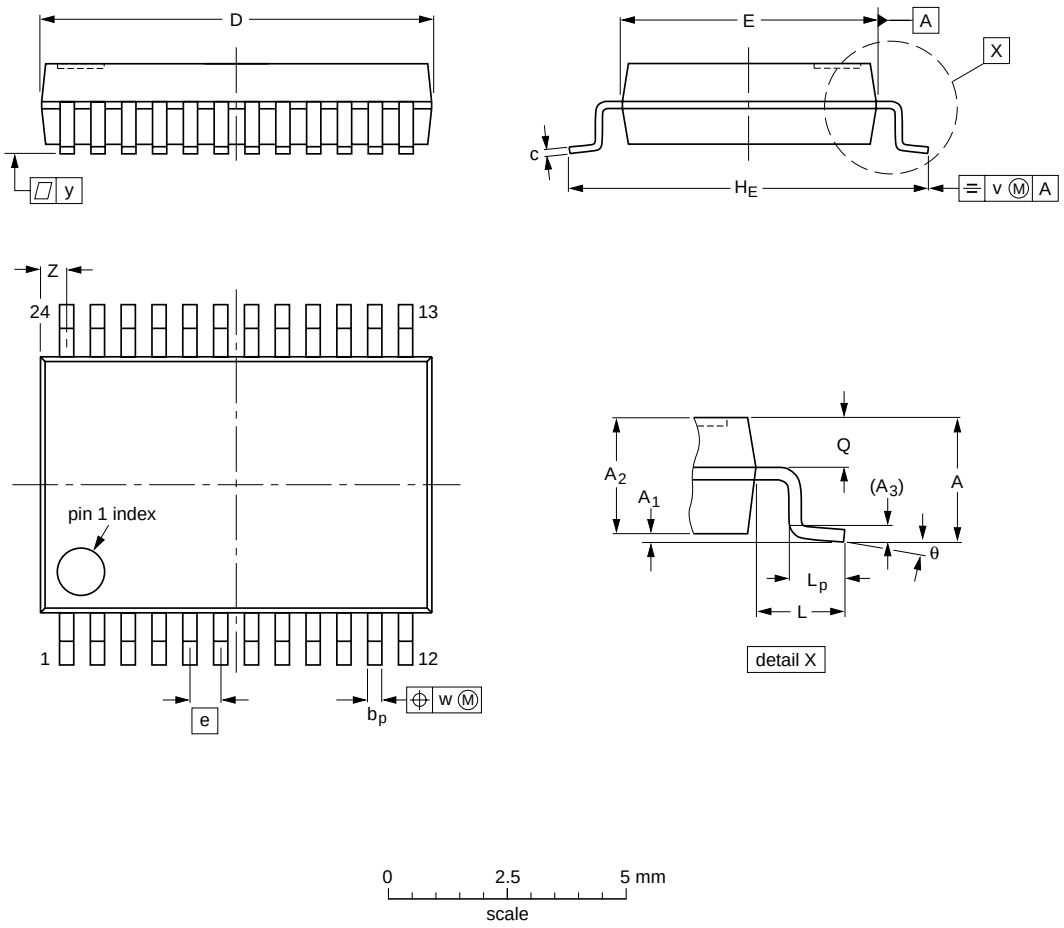
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

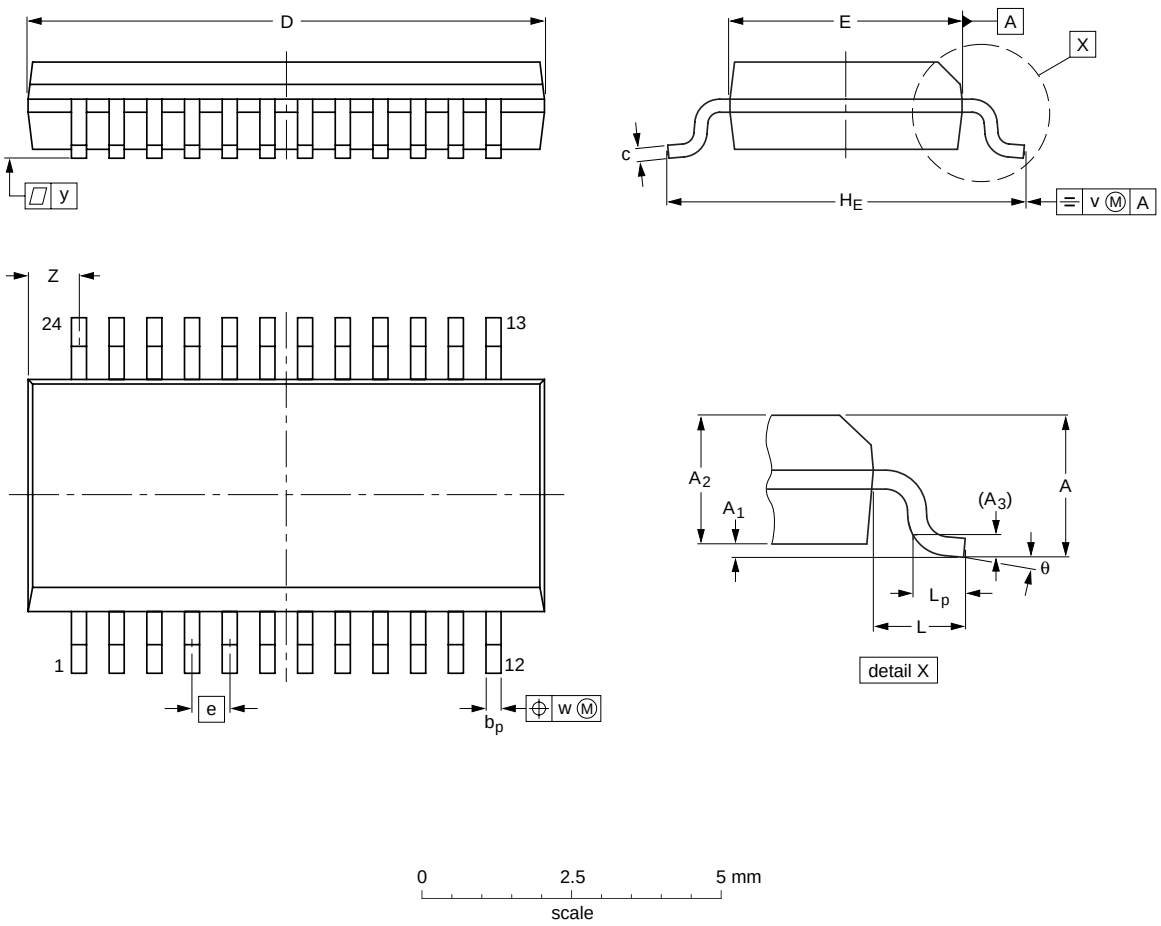
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT340-1 (SSOP24)

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT556-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.05 0.66	8^o 0^o
inches	0.068	0.0098 0.0040	0.061 0.055	0.01	0.012 0.008	0.0098 0.0075	0.344 0.337	0.157 0.150	0.025	0.244 0.228	0.041	0.035 0.016	0.01	0.007	0.004	0.040 0.026	8^o 0^o

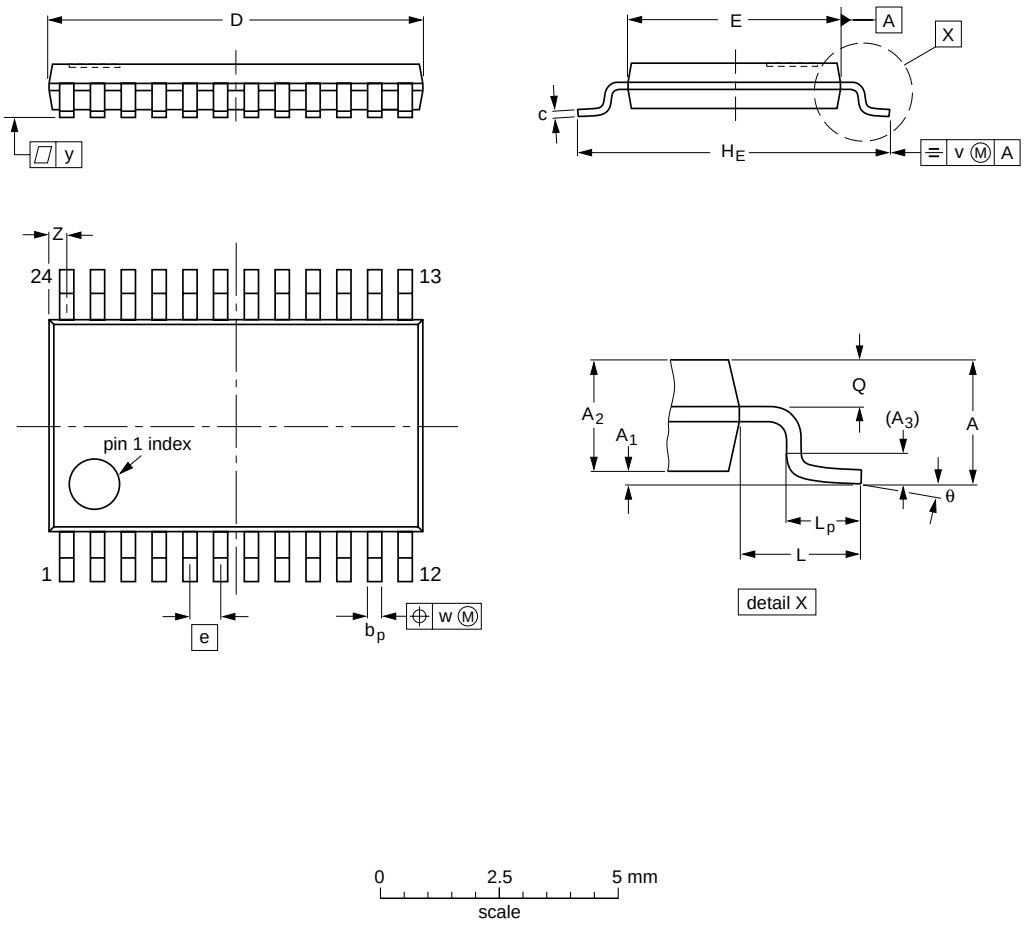
Note

1. Plastic or metal protrusions of 0.2 mm (0.008 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT556-1		MO-137				~~99-12-27~~ 03-02-18

Fig 24. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

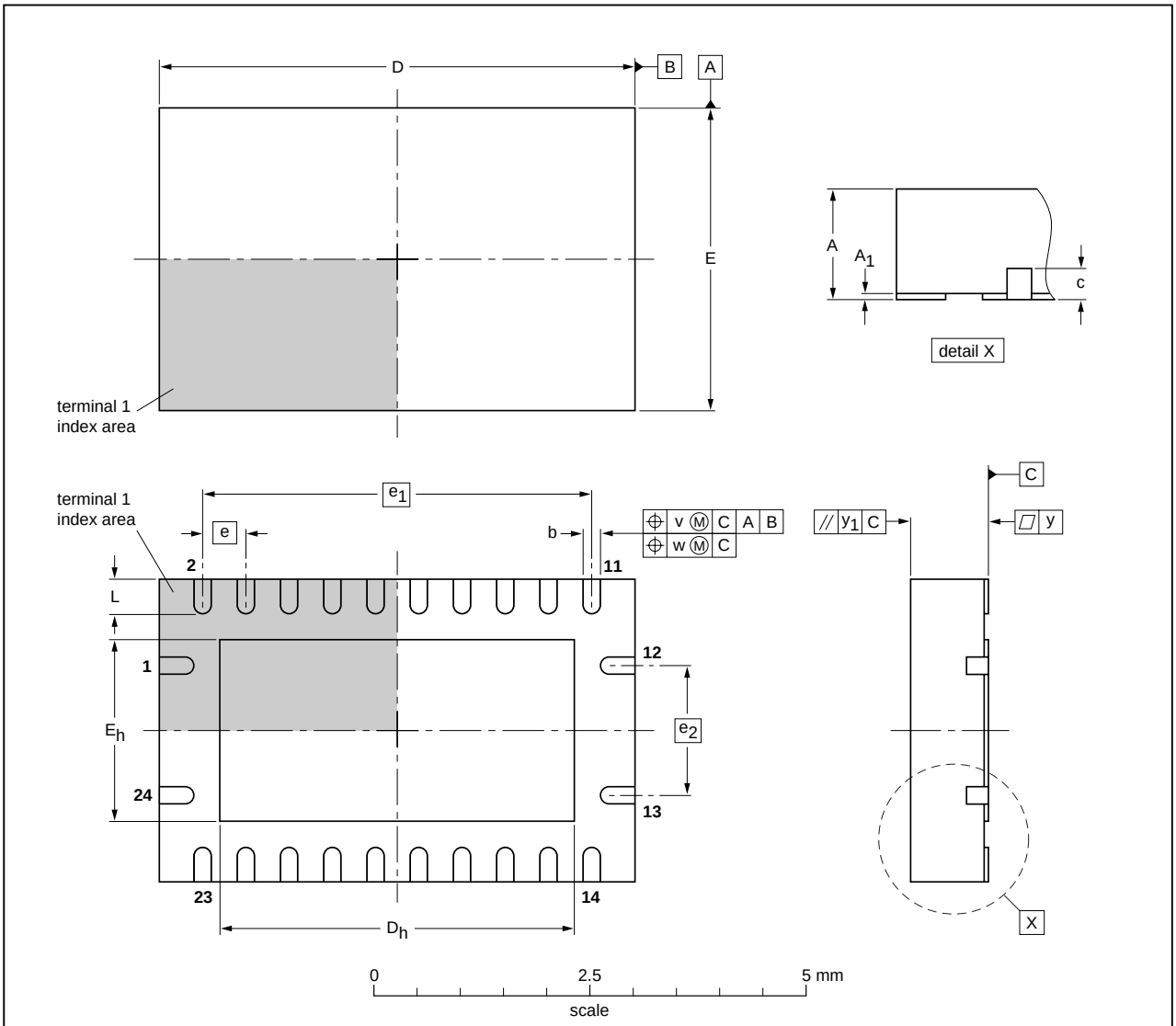
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 25. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

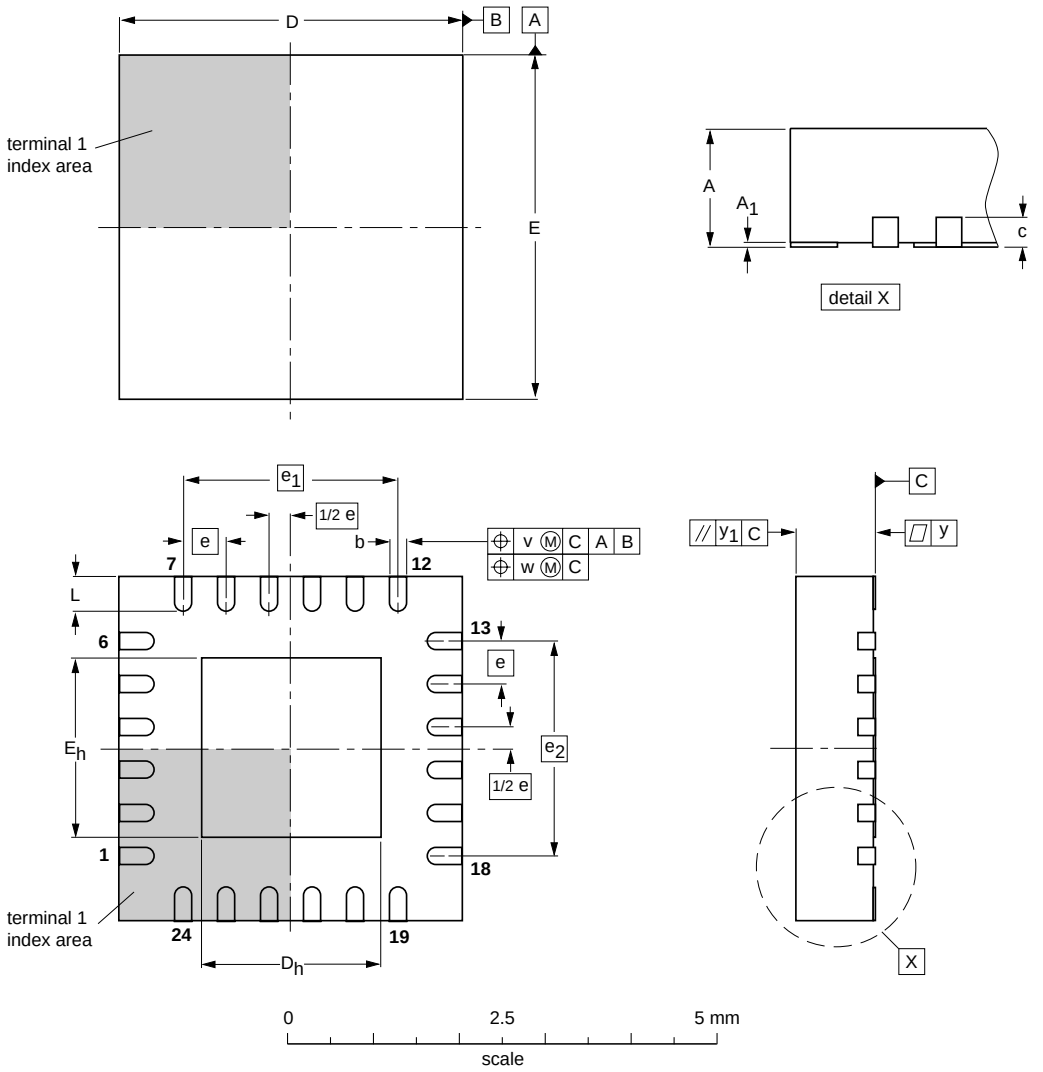
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 26. Package outline SOT815-1 (DHVQFN24)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 27. Package outline SOT616-1 (HVQFN24)

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

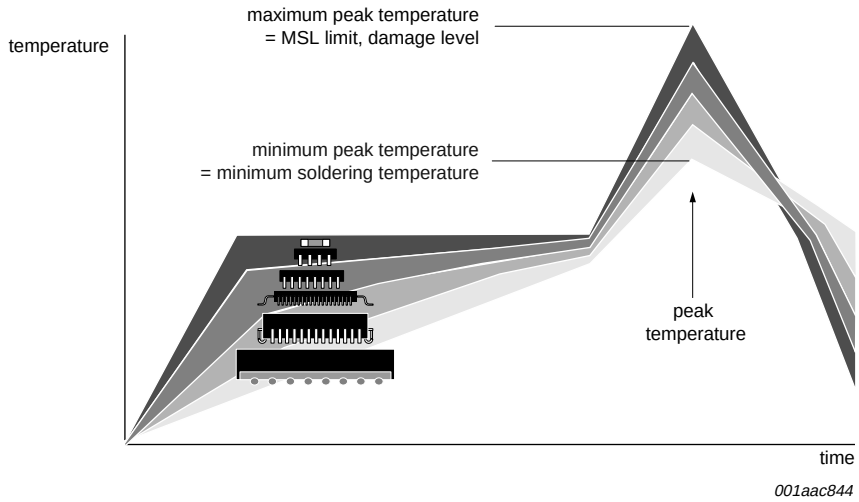
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.



MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
ID	Identification
LED	Light Emitting Diode
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PLC	Programmable Logic Controller
RAID	Redundant Array of Independent Disks
SMBus	System Management Bus

18. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8575_2	20070321	Product data sheet	-	PCA8575_1
Modifications:	• Table 5 “Static characteristics”, sub-section “I/Os; P00 to P07 and P10 to P17”: – I_{OL} (Typ) for V_{DD} = 2.3 V changed from <tbd> to 28 mA – I_{OL} (Typ) for V_{DD} = 3.0 V changed from <tbd> to 35 mA – I_{OL} (Typ) for V_{DD} = 4.5 V changed from <tbd> to 42 mA – I_{OH} (Typ) changed from <tbd> to −102 µA – Symbol C_i, input capacitance changed to $C_{io(off)}$, off-state input/output capacitance; changed Typ value from <tbd> to 9 pF – removed Symbol C_o row			
PCA8575_1	20061130	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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