



**THE DATASHEET OF
74LV74D,118**



74LV74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 4 — 9 December 2015

Product data sheet

1. General description

The 74LV74 is a dual positive edge triggered, D-type flip-flop. It has individual data (nD) inputs, clock (nCP) inputs, set (nSD) and (nRD) inputs, and complementary nQ and nQ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LV74D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LV74DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LV74PW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram

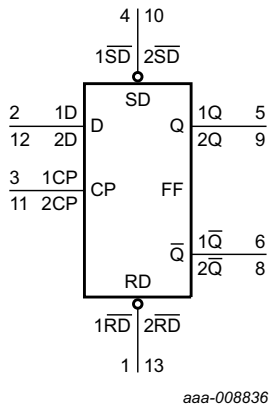


Fig 1. Logic symbol

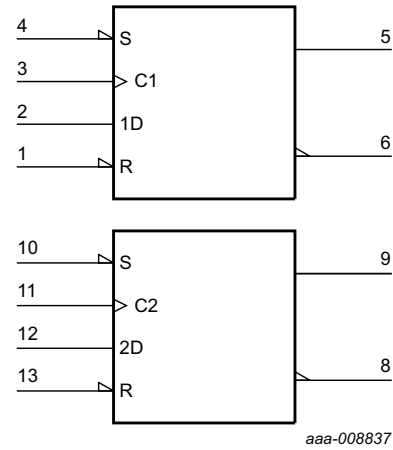


Fig 2. IEC logic symbol

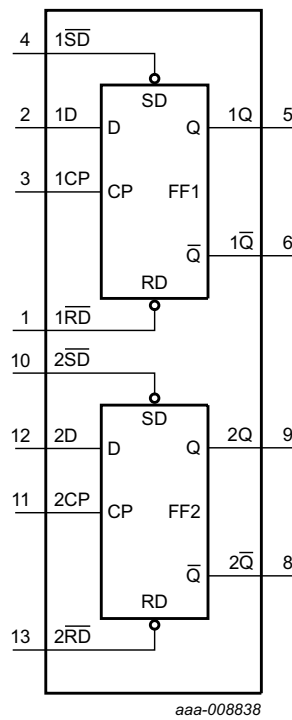


Fig 3. Functional diagram

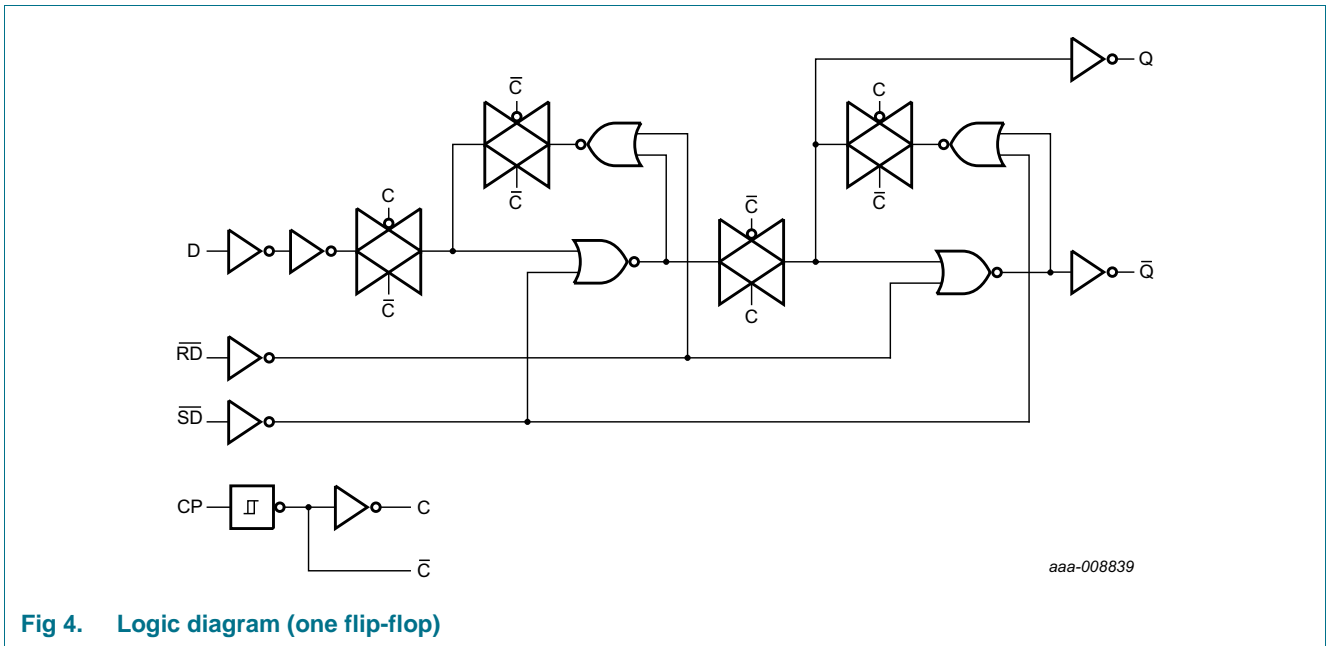


Fig 4. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning

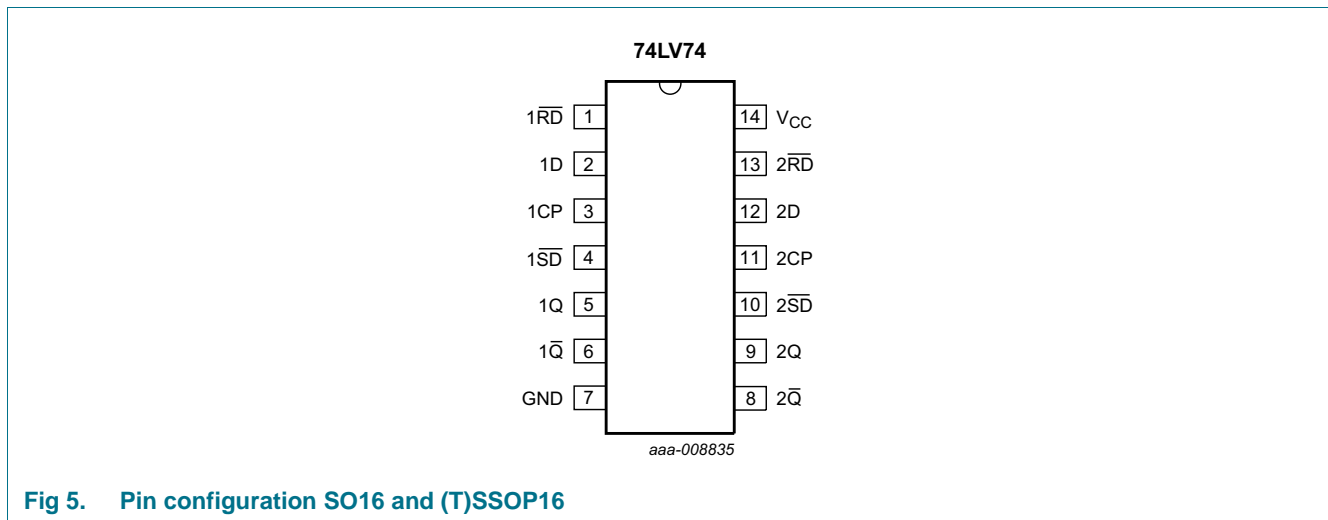


Fig 5. Pin configuration SO16 and (T)SSOP16

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------|-----|--|
| $\overline{1RD}$ | 1 | asynchronous reset-direct input (active-LOW) |
| 1D | 2 | data inputs |
| 1CP | 3 | clock input (LOW-to-HIGH), edge-triggered) |
| $\overline{1SD}$ | 4 | asynchronous set-direct input (active-LOW) |
| 1Q | 5 | true flip-flop outputs |
| $\overline{1Q}$ | 6 | complement flip-flop outputs |
| GND | 7 | ground (0 V) |
| $\overline{2Q}$ | 8 | complement flip-flop outputs |
| 2Q | 9 | true flip-flop outputs |
| $\overline{2SD}$ | 10 | asynchronous set-direct input (active-LOW) |
| 2CP | 11 | clock input (LOW-to-HIGH), edge-triggered) |
| 2D | 12 | data inputs |
| $\overline{2RD}$ | 13 | asynchronous reset-direct input (active-LOW) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | | Output | | | |
|-------|-----|-----|----|--------|-----|------------------|--------------------|
| nSD | nRD | nCP | nD | nQ | nQ̄ | Q _{n+1} | nQ̄ _{n+1} |
| L | H | X | X | H | L | - | - |
| H | L | X | X | L | H | - | - |
| L | L | X | X | H | H | - | - |
| H | H | ↑ | L | - | - | L | H |
| H | H | ↑ | H | - | - | H | L |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | 20 | mA |
| V _I | input voltage | | -0.5 | +7 | V |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 | - | ±50 | mA |
| I _O | output current | -0.5 V < V _O < V _{CC} + 0.5 V | - | ±25 | mA |
| I _{CC} | supply current | | - | ±50 | mA |
| I _{GND} | ground current | | - | ±50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | | | |
| | | SO16 package | - | 500 | mW |
| | | (T)SSOP16 package | - | 400 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| V_{CC} | supply voltage ^[1] | | 1.0 | 3.3 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.0\text{ V to }2.0\text{ V}$ | 0 | - | 500 | ns/V |
| | | $V_{CC} = 2.0\text{ V to }2.7\text{ V}$ | 0 | - | 200 | ns/V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0 | - | 100 | ns/V |
| | | $V_{CC} = 3.6\text{ V to }5.5\text{ V}$ | 0 | - | 50 | ns/V |

[1] LV is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---------------------------|--|---------------------|--------------------|---------------------|---------------------|---------------------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.2\text{ V}$ | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $0.7 \times V_{CC}$ | - | - | $0.7 \times V_{CC}$ | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.2\text{ V}$ | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | $0.3 \times V_{CC}$ | - | $0.3 \times V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} ; $I_O = -100\ \mu\text{A}$ | | | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 1.2 | - | - | - | |
| | | $V_{CC} = 2.0\text{ V}$ | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $V_{CC} = 2.7\text{ V}$ | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $V_{CC} = 3.0\text{ V}$ | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $V_{CC} = 4.5\text{ V}$ | 4.3 | 4.5 | - | 4.3 | - | V |
| | | standard outputs: $V_I = V_{IH}$ or V_{IL} | | | | | | |
| | | $V_{CC} = 3.0\text{ V}$; $I_O = -6\text{ mA}$ | 2.40 | 2.82 | - | 2.20 | - | V |
| $V_{CC} = 4.5\text{ V}$; $I_O = -12\text{ mA}$ | 3.60 | 4.20 | - | 3.50 | - | V | | |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit | |
|---|---------------------------|--|------------------|--------------------|------|-------------------|------|------|--|
| | | | Min | Typ ^[1] | Max | Min | Max | | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; I _O = 100 μA | | | | | | | |
| | | V _{CC} = 1.2 V | - | 0 | - | - | - | | |
| | | V _{CC} = 2.0 V | - | 0 | 0.2 | | 0.2 | V | |
| | | V _{CC} = 2.7 V | - | 0 | 0.2 | | 0.2 | V | |
| | | V _{CC} = 3.0 V | - | 0 | 0.2 | | 0.2 | V | |
| | | V _{CC} = 4.5 V | - | 0 | 0.2 | | 0.2 | V | |
| | | standard outputs: V _I = V _{IH} or V _{IL} | | | | | | | |
| | | V _{CC} = 3.0 V; I _O = 6 mA | - | 0.25 | 0.40 | - | 0.50 | V | |
| V _{CC} = 4.5 V; I _O = 12 mA | - | 0.35 | 0.55 | - | 0.65 | V | | | |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1 | - | ±1 | μA | |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 20 | - | 80 | μA | |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA | |
| C _I | input capacitance | | - | 3.5 | - | | | pF | |

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see [Figure 8](#)

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|-------------------|--|------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | nCP to nQ, n \bar{Q} ; see Figure 6 ^[2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 70 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 24 | 44 | - | 56 | ns |
| | | V _{CC} = 2.7 V | - | 18 | 28 | - | 41 | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | - | 13 | 26 | - | 33 | ns |
| | | V _{CC} = 3.3 V; C _L = 15 pF | - | 11 | - | - | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V ^[4] | - | 9.5 | 17 | - | 23 | ns |
| | | n $\bar{S}D$ to nQ, n \bar{Q} ; see Figure 7 | | | | | | |
| | | V _{CC} = 1.2 V | - | 90 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 31 | 46 | - | 58 | ns |
| | | V _{CC} = 2.7 V | - | 23 | 34 | - | 43 | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | - | 17 | 27 | - | 34 | ns |
| | | V _{CC} = 3.3 V; C _L = 15 pF | - | 14 | - | - | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V ^[4] | - | 12 | 19 | - | 24 | ns |
| | | n $\bar{R}D$ to nQ, n \bar{Q} ; see Figure 7 | | | | | | |
| | | V _{CC} = 1.2 V | - | 90 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 31 | 46 | - | 58 | ns |
| | | V _{CC} = 2.7 V | - | 23 | 34 | - | 43 | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | - | 17 | 27 | - | 34 | ns |
| | | V _{CC} = 3.3 V; C _L = 15 pF | - | 14 | - | - | - | ns |
| V _{CC} = 4.5 V to 5.5 V ^[4] | - | 12 | 19 | - | 24 | ns | | |
| t _w | pulse width | nCP input HIGH to LOW; see Figure 6 | | | | | | |
| | | V _{CC} = 2.0 V | 34 | 10 | - | 41 | - | ns |
| | | V _{CC} = 2.7 V | 25 | 8 | - | 30 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | 20 | 7 | - | 24 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V ^[4] | 15 | 6 | - | 18 | - | ns |
| | | n $\bar{S}D$ or n $\bar{R}D$ pulse width LOW; see Figure 7 | | | | | | |
| | | V _{CC} = 2.0 V | 34 | 10 | - | 41 | - | ns |
| | | V _{CC} = 2.7 V | 25 | 8 | - | 30 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | 20 | 7 | - | 24 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V ^[4] | 15 | 6 | - | 18 | - | ns |

Table 7. Dynamic characteristics ...continued
 GND (ground = 0 V): for test circuit, see [Figure 8](#)

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|------------------|---|--|------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{rec} | recovery time | nRD; see Figure 7 | | | | | | |
| | | V _{CC} = 1.2 V | - | 5 | - | - | - | ns |
| | | V _{CC} = 2.0 V | 14 | 2 | - | 15 | - | ns |
| | | V _{CC} = 2.7 V | 10 | 1 | - | 11 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | 8 | 1 | - | 9 | - | ns |
| | V _{CC} = 4.5 V to 5.5 V ^[4] | 6 | 1 | - | 7 | - | ns | |
| t _{su} | set-up time | nD to nCP; see Figure 6 | | | | | | |
| | | V _{CC} = 1.2 V | - | 10 | - | - | - | ns |
| | | V _{CC} = 2.0 V | 22 | 4 | - | 26 | - | ns |
| | | V _{CC} = 2.7 V | 12 | 3 | - | 15 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | 8 | 2 | - | 10 | - | ns |
| | V _{CC} = 4.5 V to 5.5 V ^[4] | 6 | 1 | - | 8 | - | ns | |
| t _h | hold time | nD to nCP; see Figure 6 | | | | | | |
| | | V _{CC} = 1.2 V | - | -10 | - | - | - | ns |
| | | V _{CC} = 2.0 V | 3 | -2 | - | 3 | - | ns |
| | | V _{CC} = 2.7 V | 3 | -2 | - | 3 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 3 | -2 | - | 3 | - | ns |
| | V _{CC} = 4.5 V to 5.5 V | 3 | -2 | - | 3 | - | ns | |
| f _{max} | maximum frequency | nCP; see Figure 6 | | | | | | |
| | | V _{CC} = 2.0 V | 14 | 40 | - | 12 | - | MHz |
| | | V _{CC} = 2.7 V | 50 | 90 | - | 40 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | 60 | 100 | - | 48 | - | MHz |
| | V _{CC} = 4.5 V to 5.5 V ^[4] | 70 | 110 | - | 56 | - | MHz | |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ^[5] | - | 24 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] Typical value measured at V_{CC} = 3.3 V.

[4] Typical values are measured at V_{CC} = 5.0 V.

[5] C_{PD} is used to determine the dynamic power dissipation P_D = C_{PD} × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) (P_D in μW), where:

f_i = input frequency in MHz;

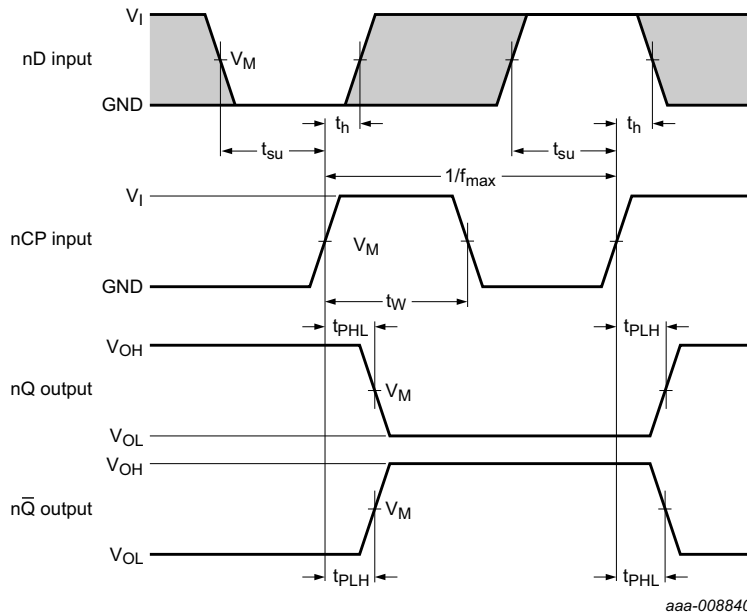
f_o = output frequency in MHz;

Σ (C_L × V_{CC}² × f_o) = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

11. Waveforms

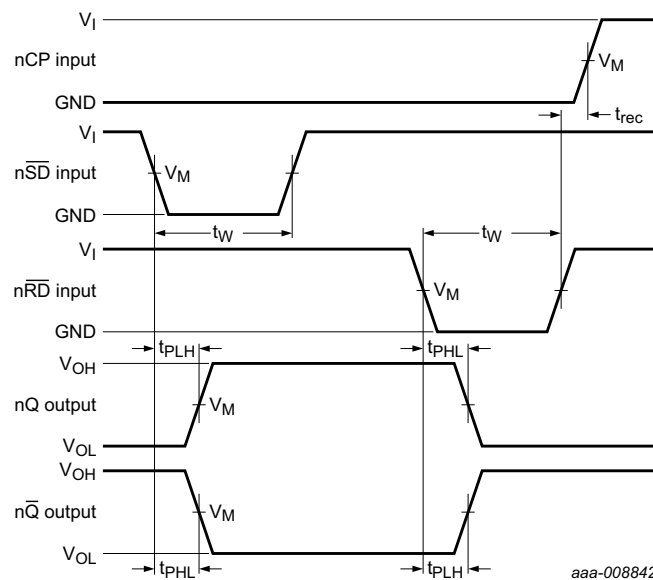


aaa-008840

Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 6. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width and maximum frequency



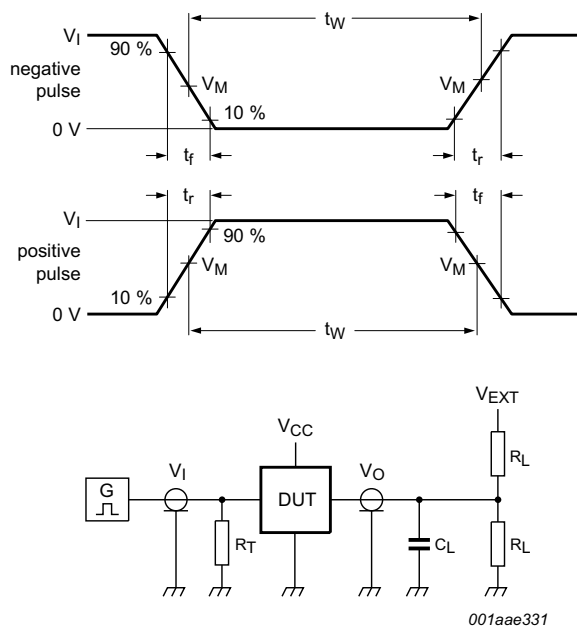
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Measurement points are given in [Table 8](#).

Fig 7. The set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD to nCP recovery time

Table 8. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{CC} | V_M | V_M |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} |
|----------------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} |
| < 2.7 V | V_{CC} | 2.5 ns | 50 pF | 1 k Ω | open |
| 2.7 V to 3.6 V | 2.7 V | 2.5 ns | 50 pF, 15 pF | 1 k Ω | open |
| ≥ 4.5 V | V_{CC} | 2.5 ns | 50 pF | 1 k Ω | open |

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

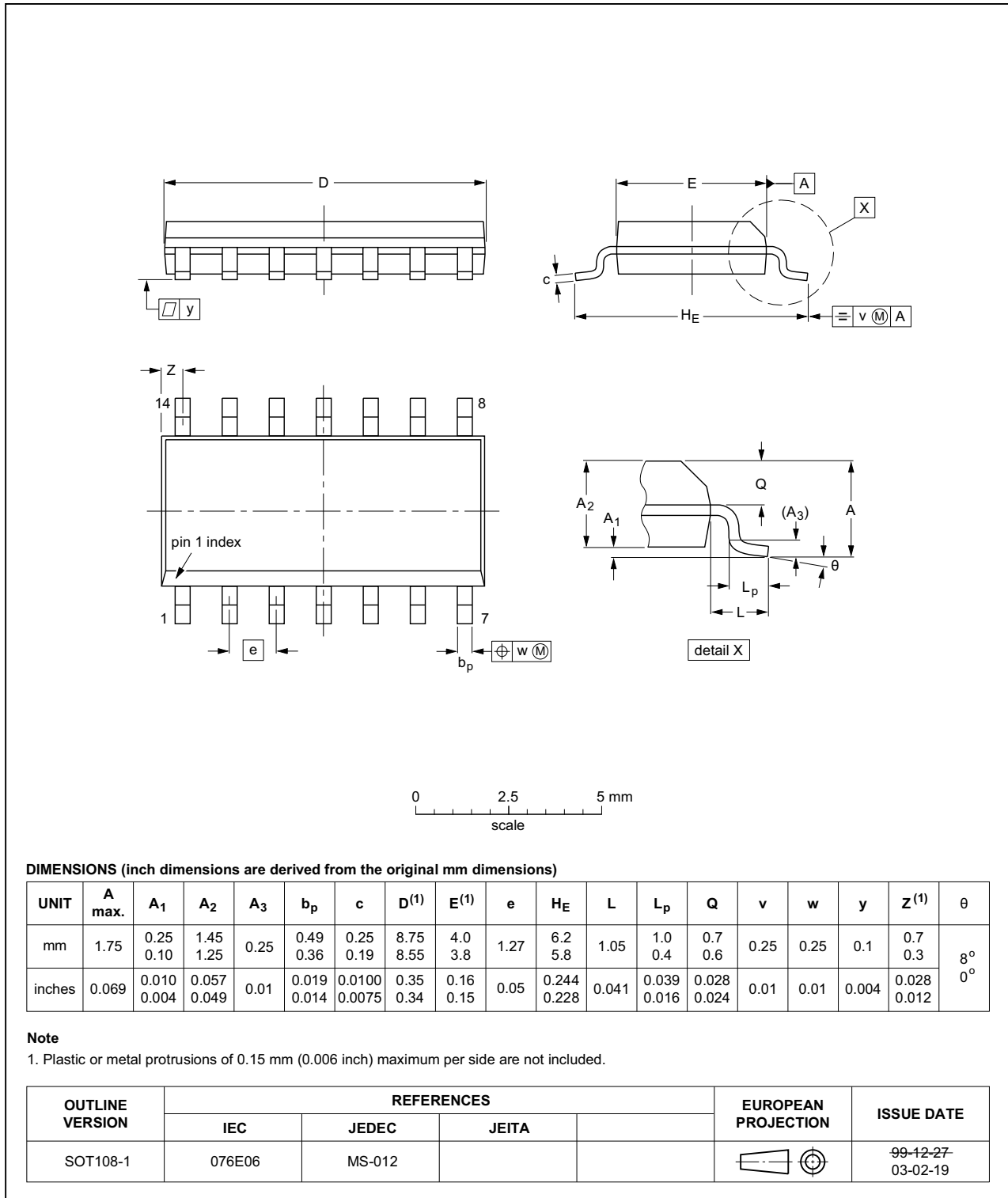


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

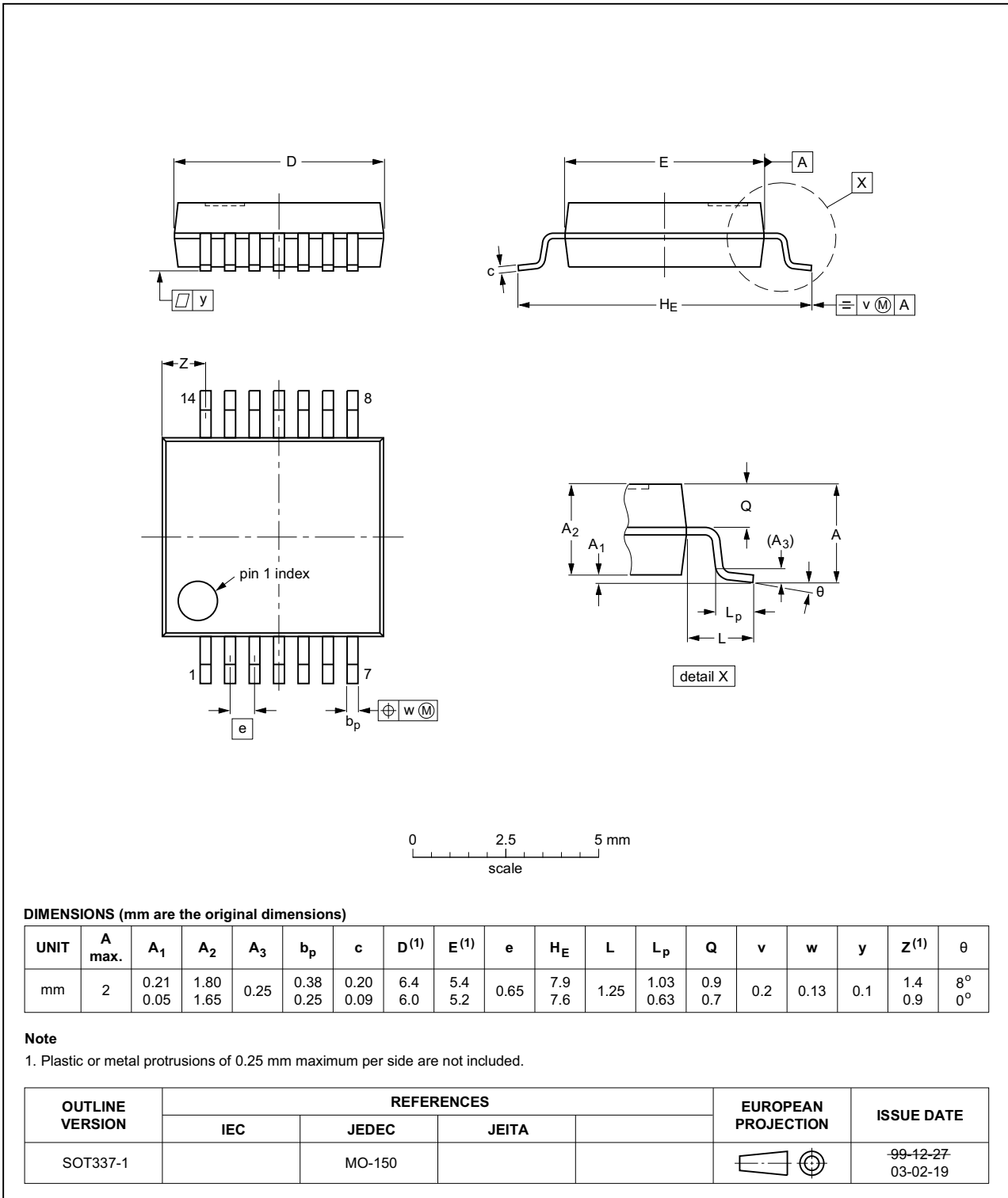


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

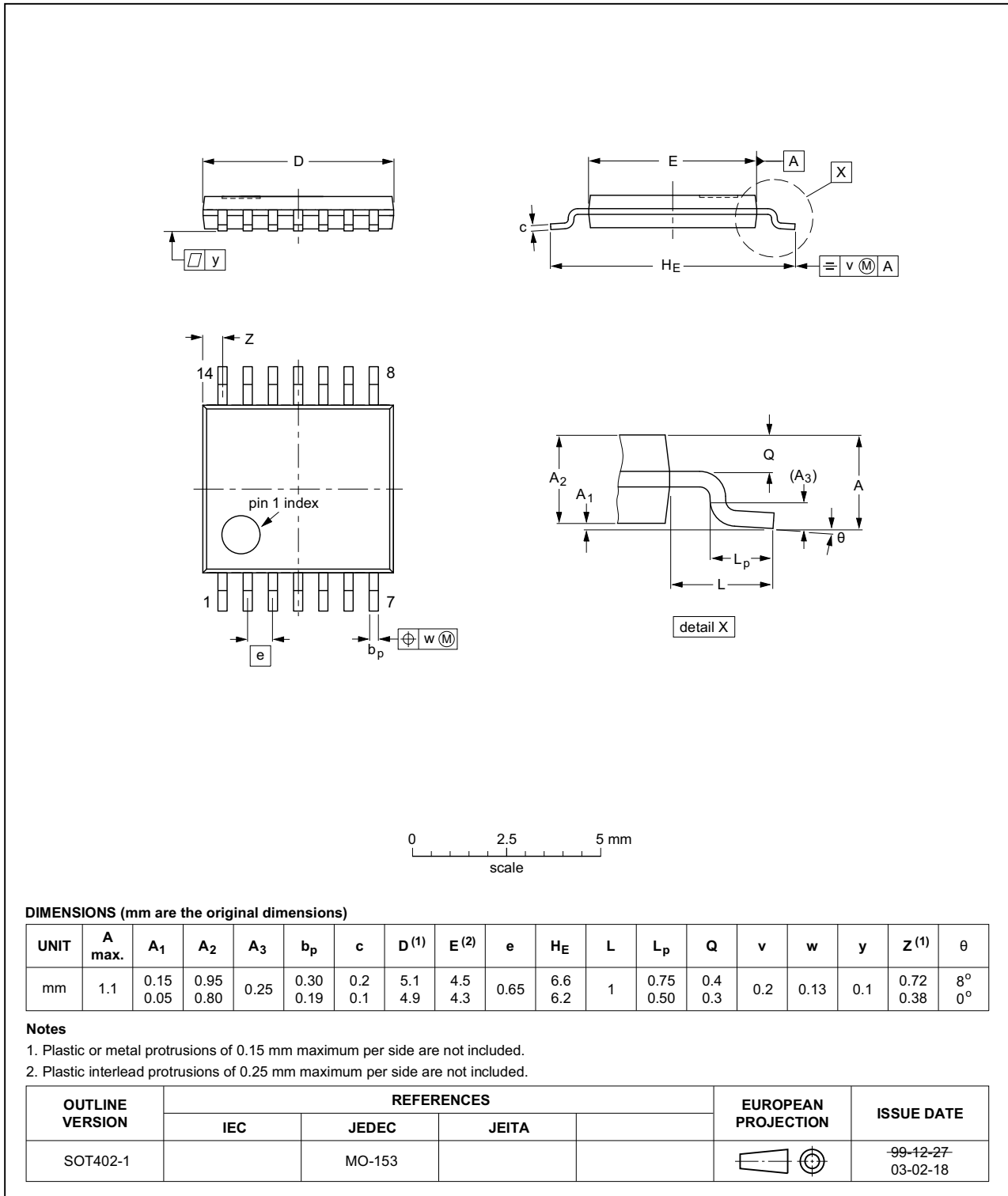


Fig 11. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|----------------|
| 74LV74 v.4 | 20151209 | Product data sheet | - | 74LV74 v.3 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LV74N (SOT27-1) removed. | | | |
| 74LV74 v.3 | 20130909 | Product data sheet | - | 74LV74_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Family data added, see Section 9 "Static characteristics" | | | |
| 74LV74_CNV v.2 | April 1998 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

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Dual D-type flip-flop with set and reset; positive-edge trigger

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