



**THE DATASHEET OF
SP3222EBEY-L/TR**



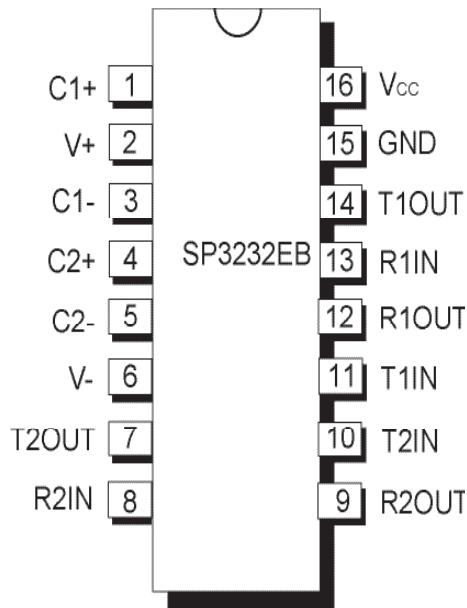


SP3222EB/SP3232EB

True +3.0V to +5.5V RS-232 Transceivers

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- 250kbps Transmission Rate Under Load
- 1 μ A Low Power Shutdown with Receivers active (**SP3222EB**)
- Interoperable with RS-232 down to a +2.7V power source
- Enhanced ESD Specifications:
 - \pm 15kV Human Body Model
 - \pm 15kV IEC61000-4-2 Air Discharge
 - \pm 8kV IEC61000-4-2 Contact Discharge



DESCRIPTION

The SP3222EB/SP3232EB series is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook or laptop computers. The SP3222EB/SP3232EB series has a high-efficiency, charge-pump power supply that requires only 0.1 μ F capacitors in 3.3V operation. This charge pump allows the SP3222EB/SP3232EB series to deliver true RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The SP3222EB/SP3232EB are 2-driver/2-receiver devices. The ESD tolerance of the SP3222EB/SP3232EB devices is over \pm 15kV for both Human Body Model and IEC61000-4-2 Air discharge test methods. The SP3222EB device has a low-power shutdown mode where the devices' driver outputs and charge pumps are disabled. During shutdown, the supply current falls to less than 1 μ A.

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Shutdown	TTL 3-State	# of Pins
SP3222EB	+3.0V to +5.5V	2	2	4 Capacitors	Yes	Yes	18, 20
SP3232EB	+3.0V to +5.5V	2	2	4 Capacitors	No	No	16

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}	-0.3V to +6.0V
V+ (NOTE 1).....	-0.3V to +7.0V
V- (NOTE 1).....	+0.3V to -7.0V
V+ + V- (NOTE 1).....	+13V
I_{CC} (DC V_{CC} or GND current).....	± 100 mA

Input Voltages

TxIN, \overline{EN}	-0.3V to +6.0V
RxIN.....	+25V

Output Voltages

TxOUT.....	± 13.2 V
RxOUT,	-0.3V to (V_{CC} +0.3V)

Short-Circuit Duration

TxOUT.....	Continuous
Storage Temperature.....	-65°C to +150°C

Power Dissipation per package

20-pin SSOP (derate 9.25mW/°C above +70°C).....	750mW
18-pin SOIC (derate 15.7mW/°C above +70°C).....	1260mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).....	890mW
16-pin SSOP (derate 9.69mW/°C above +70°C).....	775mW
16-pin Wide SOIC (derate 11.2mW/°C above +70°C).....	900mW
16-pin TSSOP (derate 10.5mW/°C above +70°C).....	850mW
16-pin nSOIC (derate 13.57mW/°C above +70°C).....	1086mW

Maximum Junction Temperature	+125°C
Thermal Resistance (16-pin TSSOP) θ_{JA}	100.4°C/W
Thermal Resistance (16-pin TSSOP) θ_{JC}	19.0°C/W
Thermal Resistance (16-pin QFN) θ_{JA}	44.0°C/W
Thermal Resistance (16-pin QFN) θ_{JC}	7.3°C/W

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

NOTE 2: Driver Input hysteresis is typically 250mV.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0$ V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX} , C1 - C4 = 0.1 μ F.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ\text{C}$, TxIN = GND or V_{CC}
Shutdown Supply Current		1.0	10	μ A	$\overline{SHDN} = \text{GND}$, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ\text{C}$, TxIN = V_{CC} or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW	GND		0.8	V	TxIN, \overline{EN} , \overline{SHDN} , Note 2
Input Logic Threshold HIGH	2.0		V_{CC}	V	$V_{CC} = 3.3$ V, Note 2
Input Logic Threshold HIGH	2.4		V_{CC}	V	$V_{CC} = 5.0$ V, Note 2
Input Leakage Current		± 0.01	± 1.0	μ A	TxIN, \overline{EN} , \overline{SHDN} , $T_{AMB} = +25^\circ\text{C}$, $V_{IN} = 0$ V to V_{CC}
Output Leakage Current		± 0.05	± 10	μ A	Receivers disabled, $V_{OUT} = 0$ V to V_{CC}
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA
DRIVER OUTPUTS					
Output Voltage Swing	± 5.0	± 5.4		V	All driver outputs loaded with 3k Ω to GND, $T_{AMB} = +25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0V$ to $+5.5V$ with $T_{AMB} = T_{MIN}$ to T_{MAX} , $C1 - C4 = 0.1\mu F$. Typical values apply at $V_{CC} = +3.3V$ or $+5.0V$ and $T_{AMB} = 25^{\circ}C$.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	$V_{CC} = V+ = V- = 0V, V_{OUT} = \pm 2V$
Output Short-Circuit Current		± 35	± 60	mA	$V_{OUT} = 0V$
Output Leakage Current			± 25	μA	$V_{CC} = 0V$ or $3.0V$ to $5.5V, V_{OUT} = \pm 12V$, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k Ω	
TIMING CHARACTERISTICS					
Maximum Data Rate	250			kbps	$R_L = 3k\Omega, C_L = 1000pF$, one driver active
Receiver Propagation Delay, t_{PHL}		0.15		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Propagation Delay, t_{PLH}		0.15		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100		ns	$ t_{PHL} - t_{PLH} , T_{AMB} = 25^{\circ}C$
Receiver Skew		50		ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate			30	V/ μs	$V_{CC} = 3.3V, R_L = 3k\Omega, C_L = 1000pF, T_{AMB} = 25^{\circ}C$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 1000kbps data rate, all drivers loaded with 3k Ω , 0.1 μF charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.

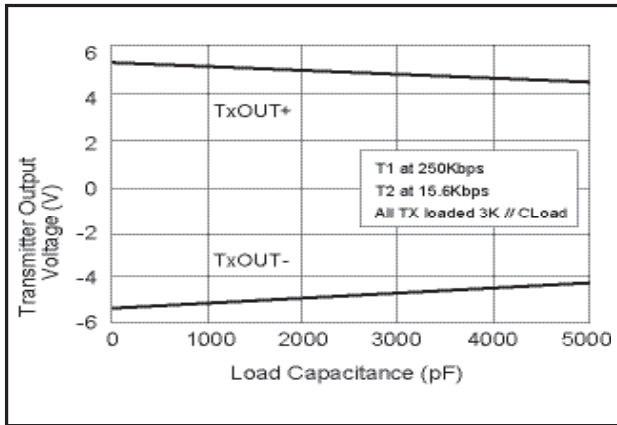


Figure 1. Transmitter Output Voltage vs Load Capacitance

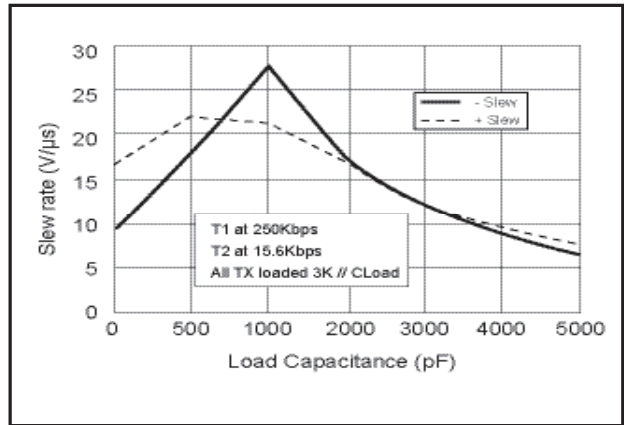


Figure 2. Slew Rate vs Load Capacitance

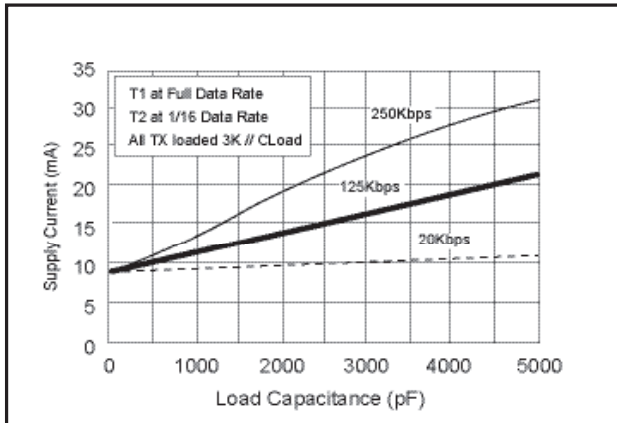


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

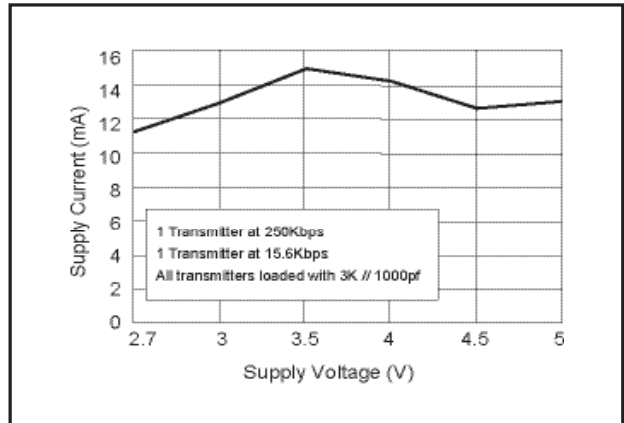


Figure 4. Supply Current VS. Supply Voltage

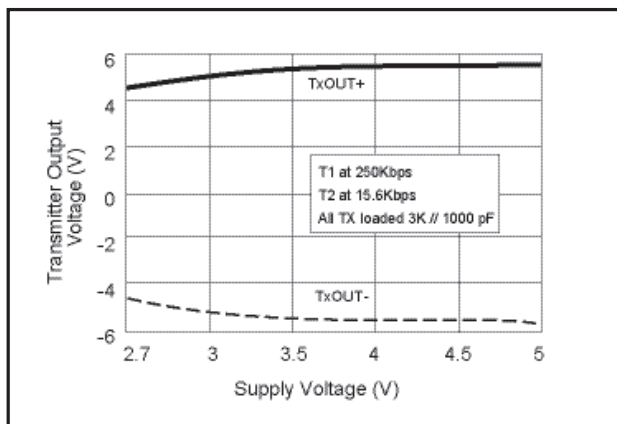


Figure 5. Transmitter Output Voltage vs Supply Voltage

NAME	FUNCTION	PIN NUMBER			
		SP3222EB		SP3232EB	
		SOIC	SSOP TSSOP	SSOP TSSOP NSOIC WSOIC	QFN
$\overline{\text{EN}}$	Receiver Enable. Apply Logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state)	1	1	-	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor	2	2	1	15
V+	+5.5V output generated by the charge pump	3	3	2	16
C1-	Negative terminal of the voltage doubler charge-pump capacitor	4	4	3	1
C2+	Positive terminal of the inverting charge-pump capacitor	5	5	4	2
C2-	Negative terminal of the inverting charge-pump capacitor	6	6	5	3
V-	-5.5V output generated by the charge pump	7	7	6	4
T ₁ OUT	RS-232 driver output.	15	17	14	12
T ₂ OUT	RS-232 driver output.	8	8	7	5
R ₁ IN	RS-232 receiver input	14	16	13	11
R ₂ IN	RS-232 receiver input	9	9	8	6
R ₁ OUT	TTL/CMOS receiver output	13	15	12	10
R ₂ OUT	TTL/CMOS receiver output	10	10	9	7
T ₁ IN	TTL/CMOS driver input	12	13	11	9
T ₂ IN	TTL/CMOS driver input	11	12	10	8
GND	Ground.	16	18	15	13
V _{CC}	+3.0V to +5.5V supply voltage	17	19	16	14
$\overline{\text{SHDN}}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply	18	20	-	-
N.C.	No Connect	-	11, 14	-	-

Table 1. Device Pin Description

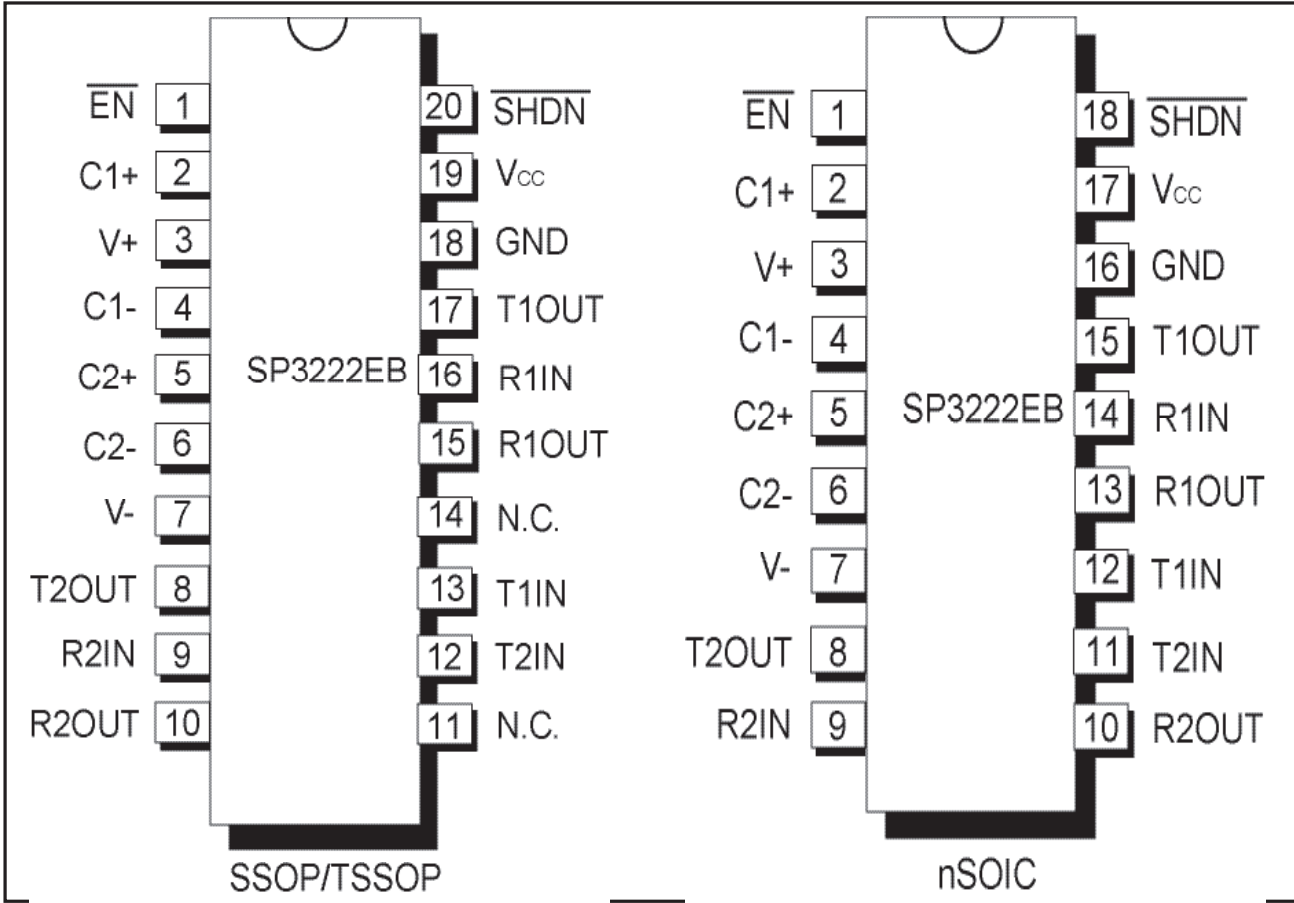


Figure 6. Pinout Configurations for the SP3222EB

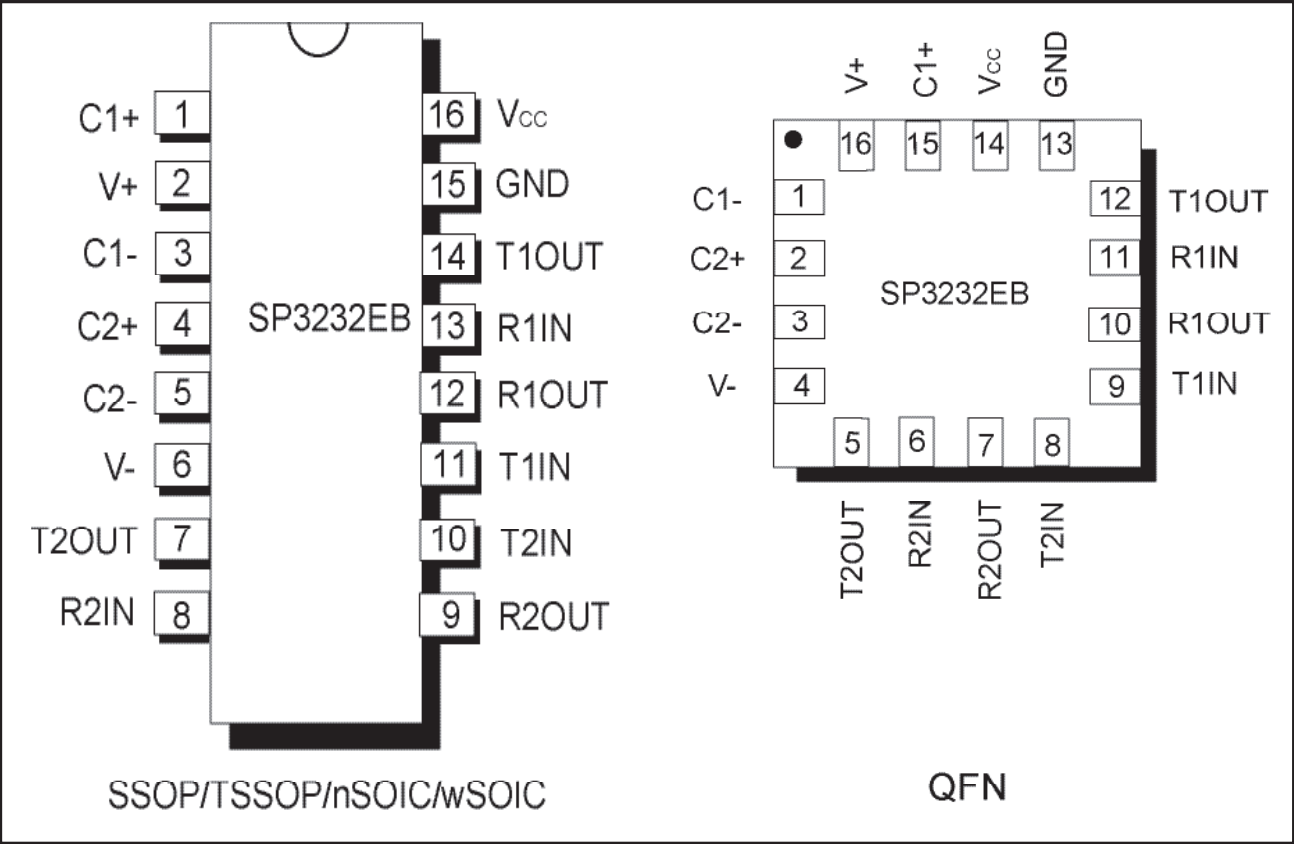


Figure 7. Pinout Configuration for the SP3232EB

TYPICAL OPERATING CIRCUITS

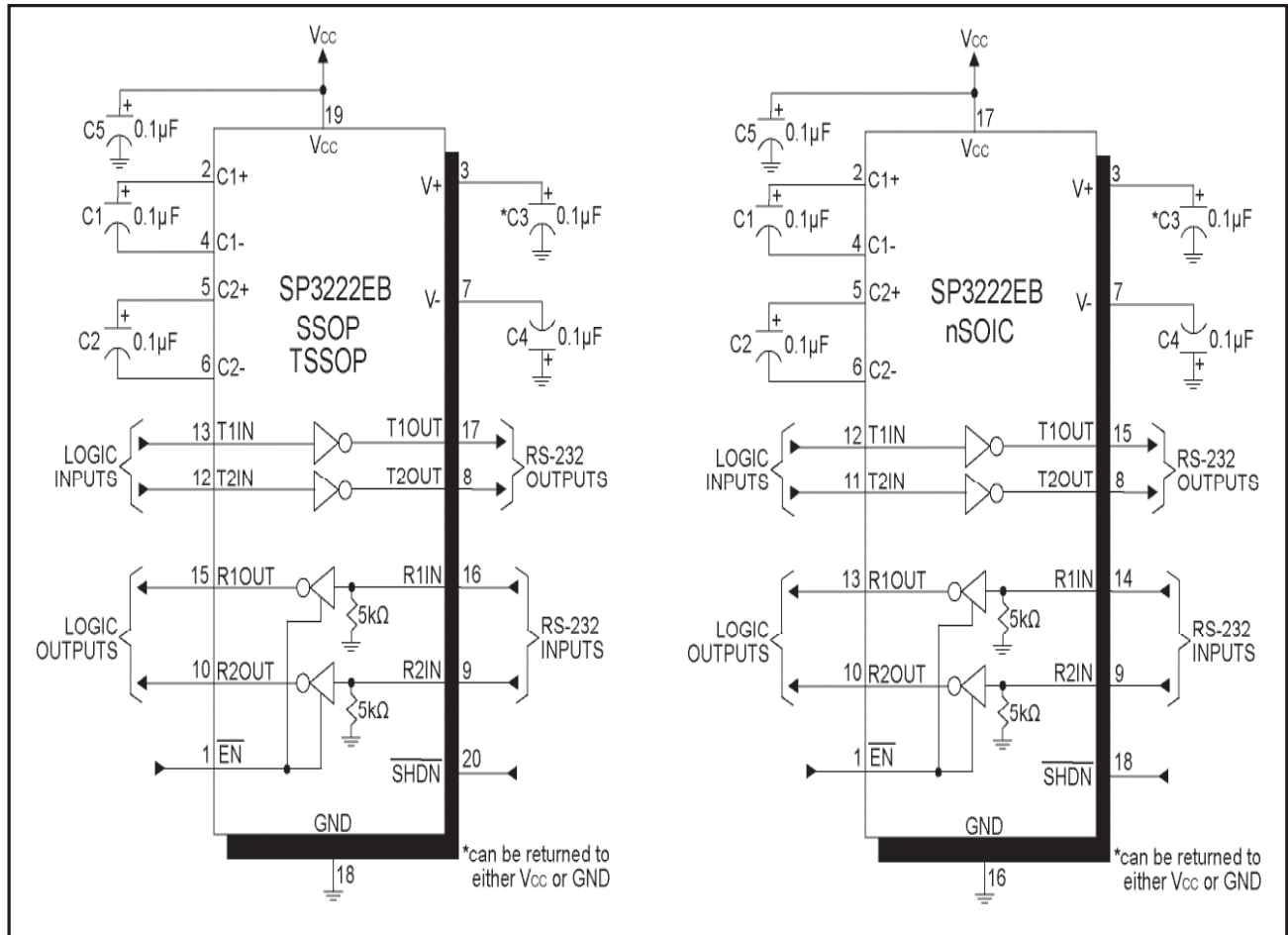


Figure 8. SP3222EB Typical Operating Circuits

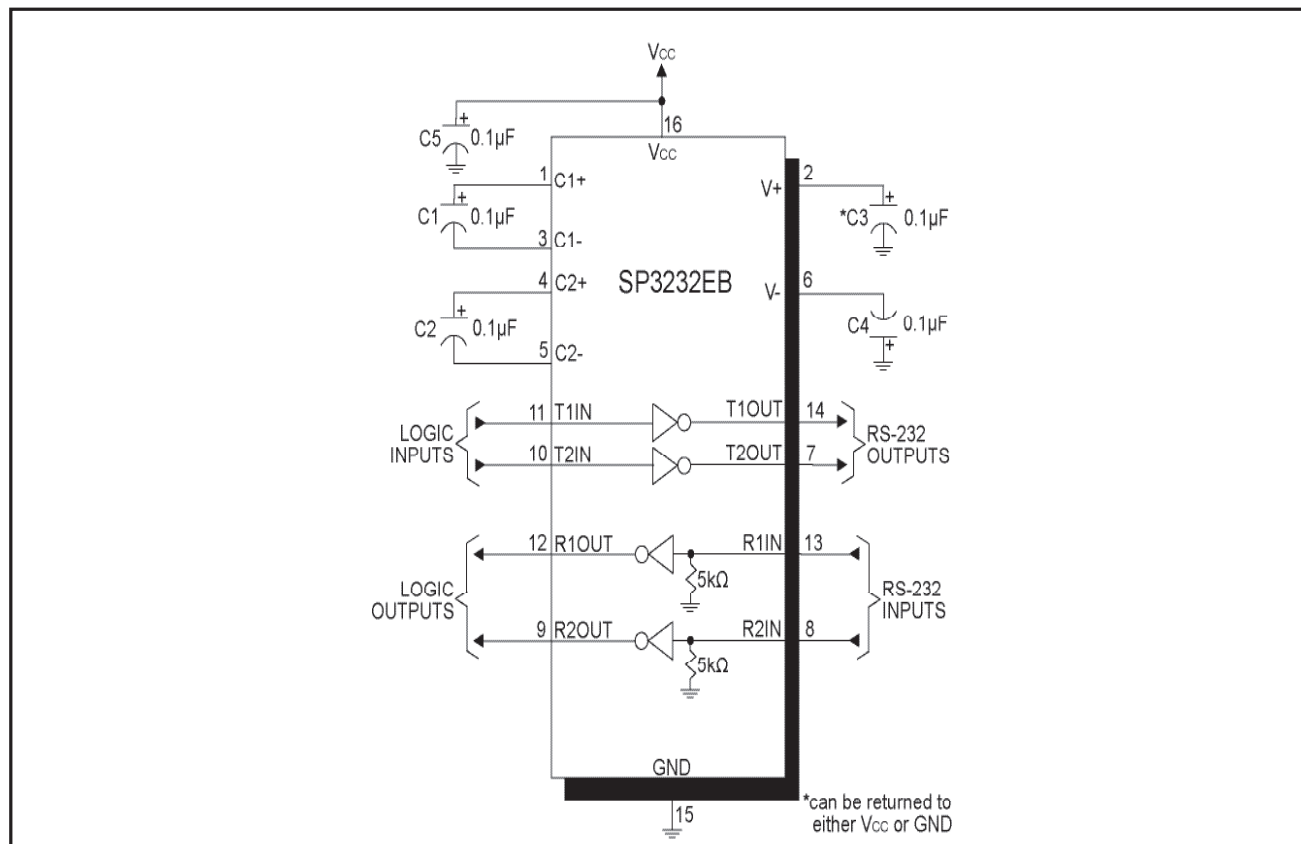


Figure 9. SP3232EB Typical Operating Circuit

The **SP3222EB/SP3232EB** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3222EB/SP3232EB** devices feature Exar's proprietary on-board charge pump circuitry that generates $\pm 5.5V$ for RS-232 voltage levels from a single $+3.0V$ to $+5.5V$ power supply. This series is ideal for $+3.3V$ -only systems, mixed $+3.3V$ to $+5.5V$ systems, or $+5.0V$ -only systems that require true RS-232 performance. The **SP3222EB/SP3232EB** devices can operate at a data rate of 250kbps when fully loaded.

The **SP3222EB** and **SP3232EB** are 2-driver/2-receiver devices ideal for portable or hand-held applications. The **SP3222EB** features a $1\mu A$ shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only $1\mu A$ supply current.

THEORY OF OPERATION

The **SP3222EB/SP3232EB** series is made up of three basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm 5.0V$ EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.4V$ with no load and $\pm 5V$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of $\pm 3.7V$ with supply voltages as low as $2.7V$.

The drivers can guarantee a data rate of 250kbps fully loaded with $3k\Omega$ in parallel with $1000pF$, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver is internally limited to a maximum of $30V/\mu s$ in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meet the monotonicity requirements of the standard.

Figure 10 shows a loopback test circuit used to test the RS-232 Drivers. Figure 11 shows the test results of the loopback circuit with all drivers active at 120kbps with RS-232 loads in parallel with a $1000pF$ capacitor. Figure 12 shows the test results where one driver was active at 250kbps and all drivers loaded with an RS-232 receiver in parallel with $1000pF$ capacitors. A solid RS-232 data transmission rate of 250kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3222EB** driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the **SP3222EB** device permits the outputs to be driven up to $\pm 12V$. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than $1\mu A$, where $\overline{SHDN} = \text{LOW}$. When the **SP3222EB** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with $V+$ pulled down to V_{CC} and $V-$ pulled to GND. The time required to exit shutdown is typically $100\mu s$. Connect \overline{SHDN} to V_{CC} if the shutdown mode is not used.

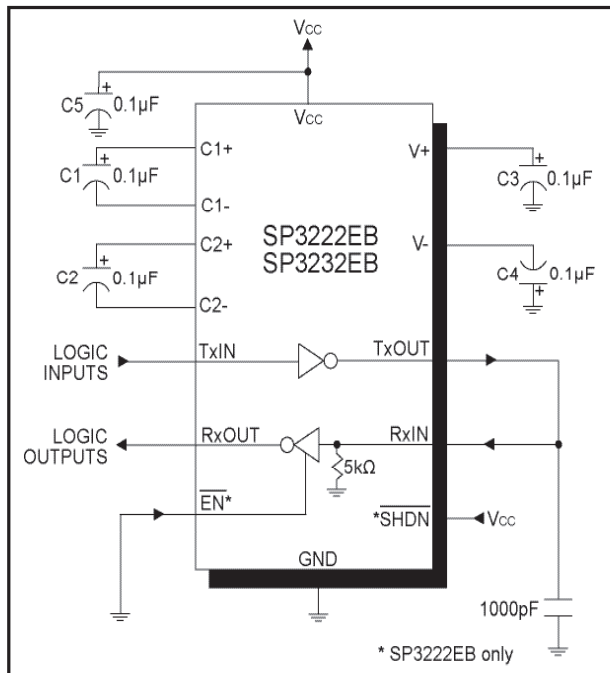


Figure 10. SP3222EB/SP3232EB Driver Loopback Test Circuit

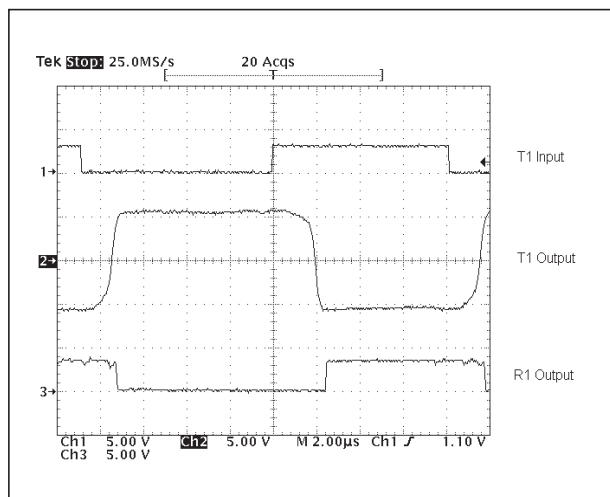


Figure 11. Loopback Test results at 120kbps

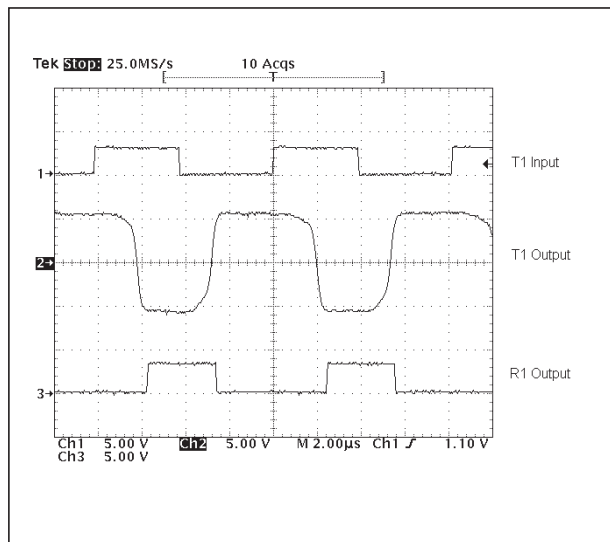


Figure 12. Loopback Test results at 250kbps

Receivers

The Receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The **SP3222EB** receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control $\overline{\text{EN}}$ = HIGH. In the shutdown mode, the receivers can be active or inactive. $\overline{\text{EN}}$ has no effect on TxOUT. The truth table logic of the **SP3222EB** driver and receiver outputs can be found in Table 2.

$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. SP3222EB Truth Table Logic for Shutdown and Enable Control

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5k Ω pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is an Exar-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of $\pm 5.5\text{V}$ regardless of the input voltage (V_{cc}) over the +3.0V to +5.5V range.

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1 μ F bypass capacitor at C5 (refer to figures 8 and 9)

In applications that are sensitive to power-supply noise, decouple Vcc to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^- . Since C_2^+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now 2 times V_{CC} .

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3 . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at V_{CC} , the voltage potential across C_2 is 2 times V_{CC} .

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4 , the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} , in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

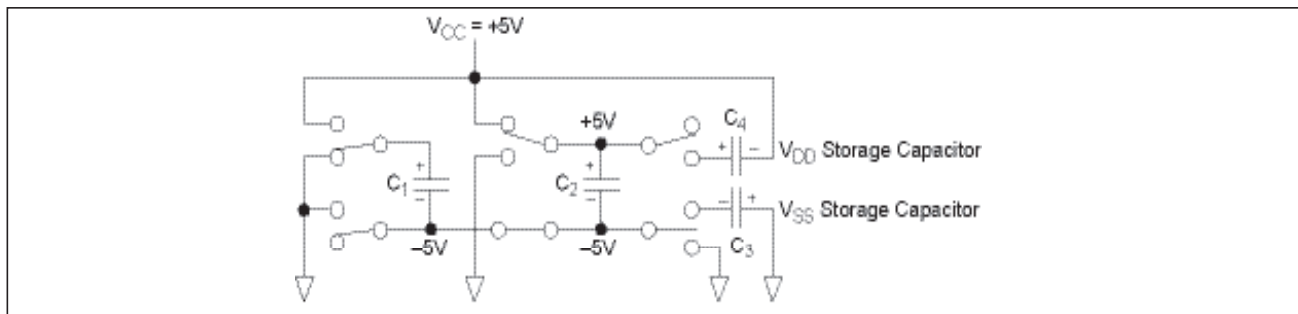


Figure 13. Charge Pump — Phase 1

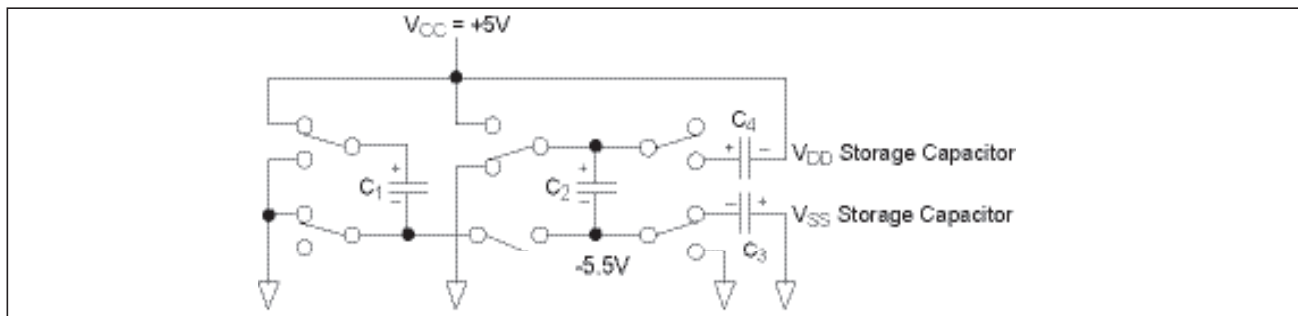


Figure 14. Charge Pump — Phase 2

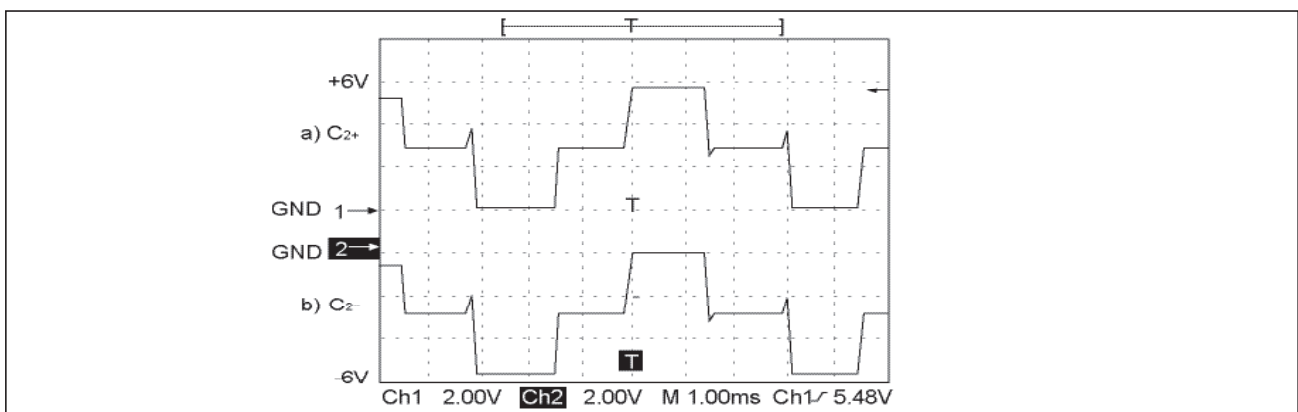


Figure 15. Charge Pump Waveforms

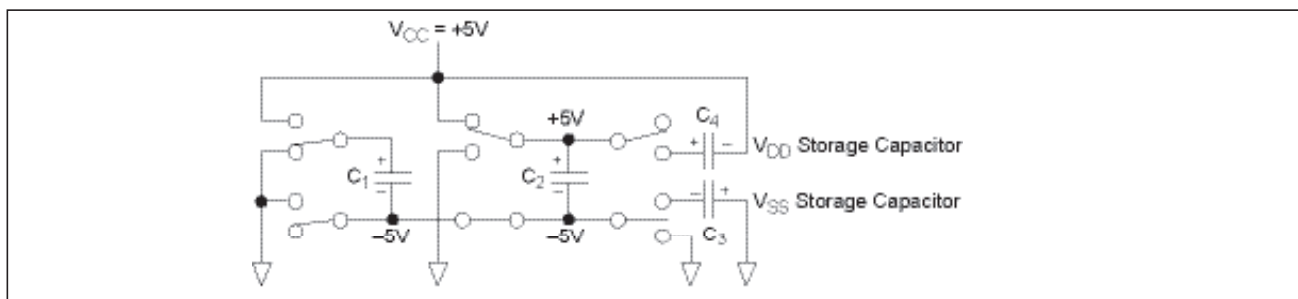


Figure 16. Charge Pump — Phase 3

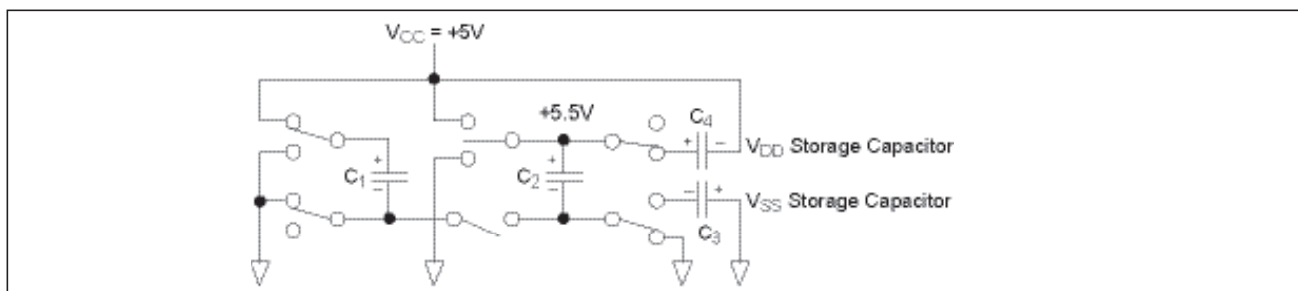


Figure 17. Charge Pump — Phase 4

ESD TOLERANCE

The **SP3222EB/SP3232EB** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC61000-4-2 Air-Discharge
- c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 18. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that

the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 19. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the

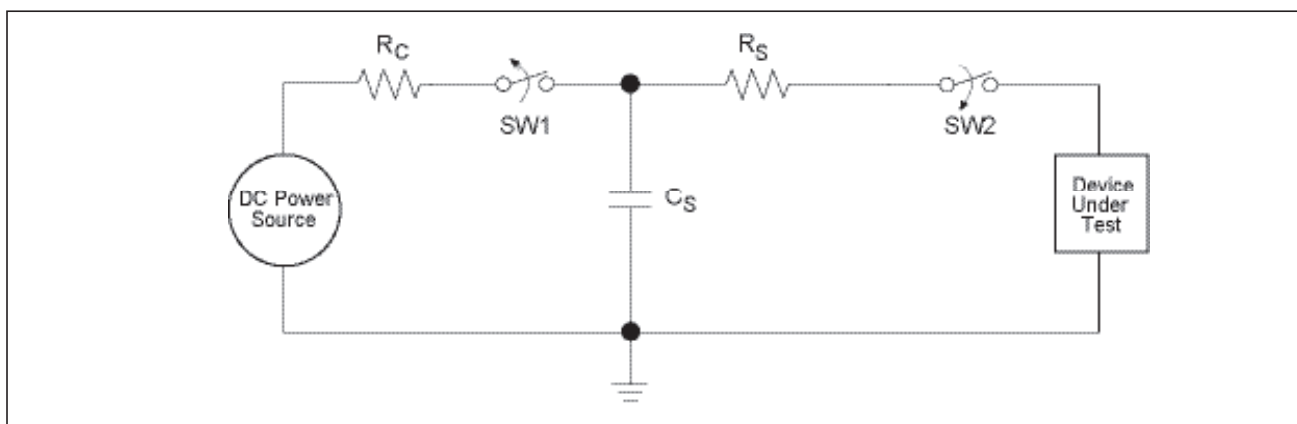


Figure 18. ESD Test Circuit for Human Body Model

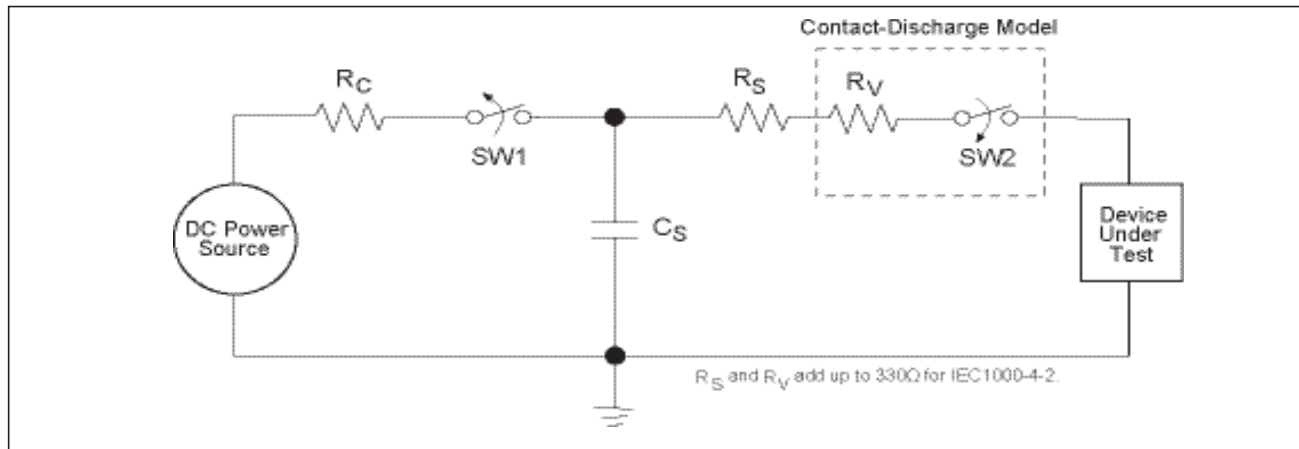


Figure 19. ESD Test Circuit for IEC61000-4-2

equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 18 and 19 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5k Ω and 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330 Ω and 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

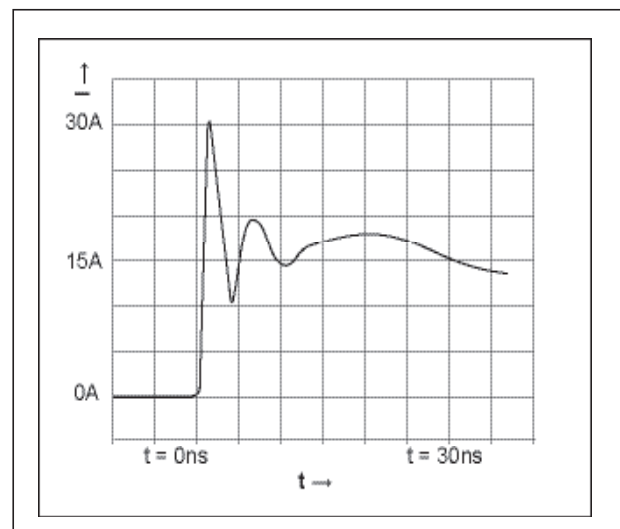
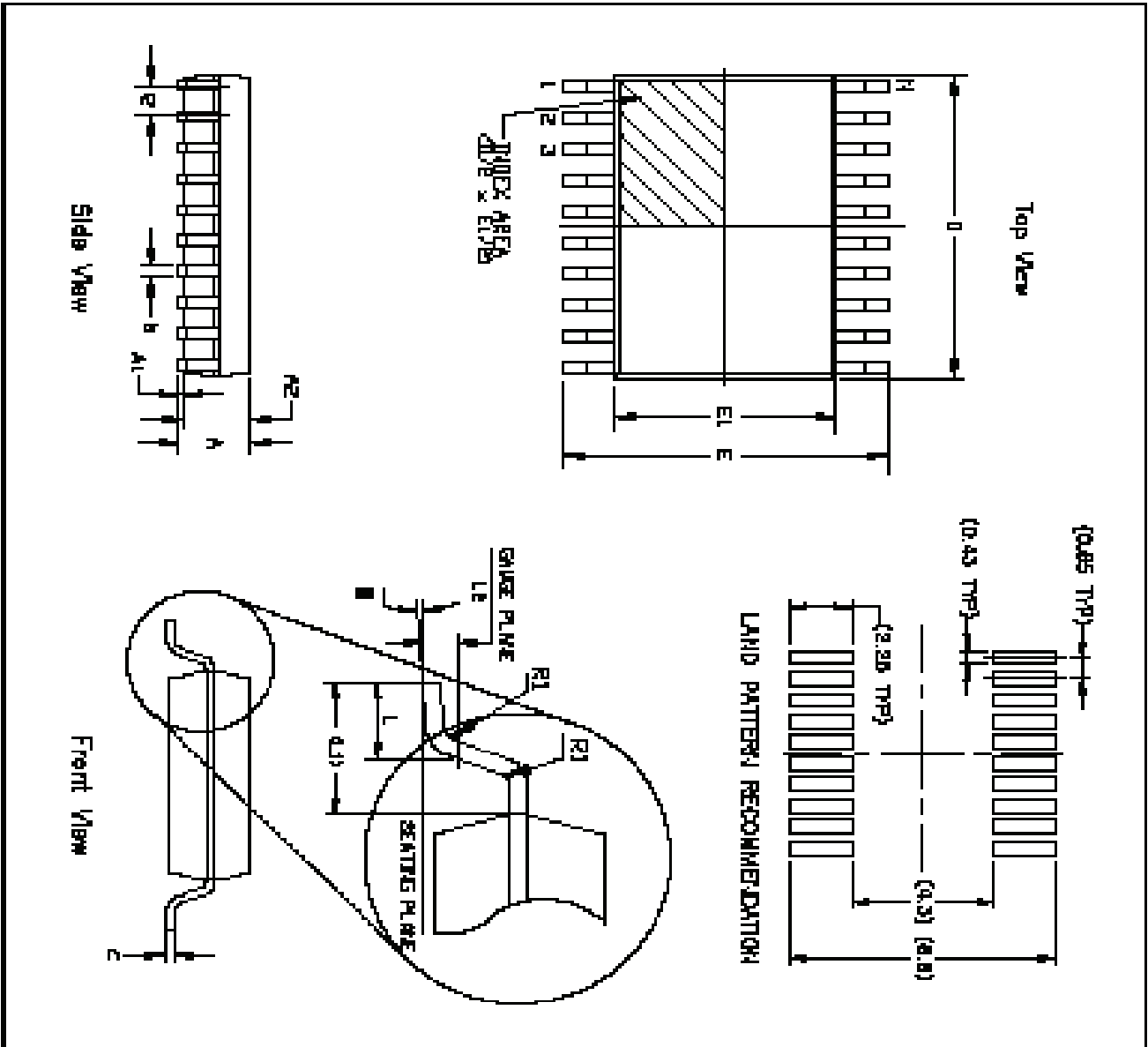


Figure 20. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15\text{kV}$	$\pm 15\text{kV}$	$\pm 8\text{kV}$	4
Receiver Inputs	$\pm 15\text{kV}$	$\pm 15\text{kV}$	$\pm 8\text{kV}$	4

Table 3. Transceiver ESD Tolerance Levels



REV	DESCRIPTION	DATE	APPRO
A	INITIAL RELEASE	04/26/04	A
B	REVISED LAND PATTERN RECOMMENDATION	07/24/04	A
D	REVISED DRAWING LEAD AND SEATING PLANE	11/07/07	A

20 PIN SSOP 450°C W/ 150 VARIATION P/2		DIMENSIONS IN MM		DIMENSIONS IN INCH	
DIMENSIONS		(CONFORM LIMIT)		(CONFORM LIMIT)	
A	—	0.20	—	0.008	—
A1	0.05	—	0.002	—	—
A2	1.19	1.49	0.047	0.059	0.073
b	0.22	—	0.009	—	0.010
D	0.00	—	0.004	—	0.010
E	7.40	0.59	0.020	0.007	0.023
E1	3.00	0.40	0.016	0.009	0.020
φ	0.03 MAX	—	0.004 MAX	—	—
L	0.55	0.25	0.010	0.010	0.007
L1	1.29 REF	—	0.048 REF	—	—
L2	0.25 BSC	—	0.010 BSC	—	—
R1	0.00	—	0.004	—	—
■	φ	φ	φ	φ	φ
D	0.40	7.20	7.20	0.016	0.283
H	—	20	—	20	—

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20 PIN SSOP PACKAGE OUTLINE

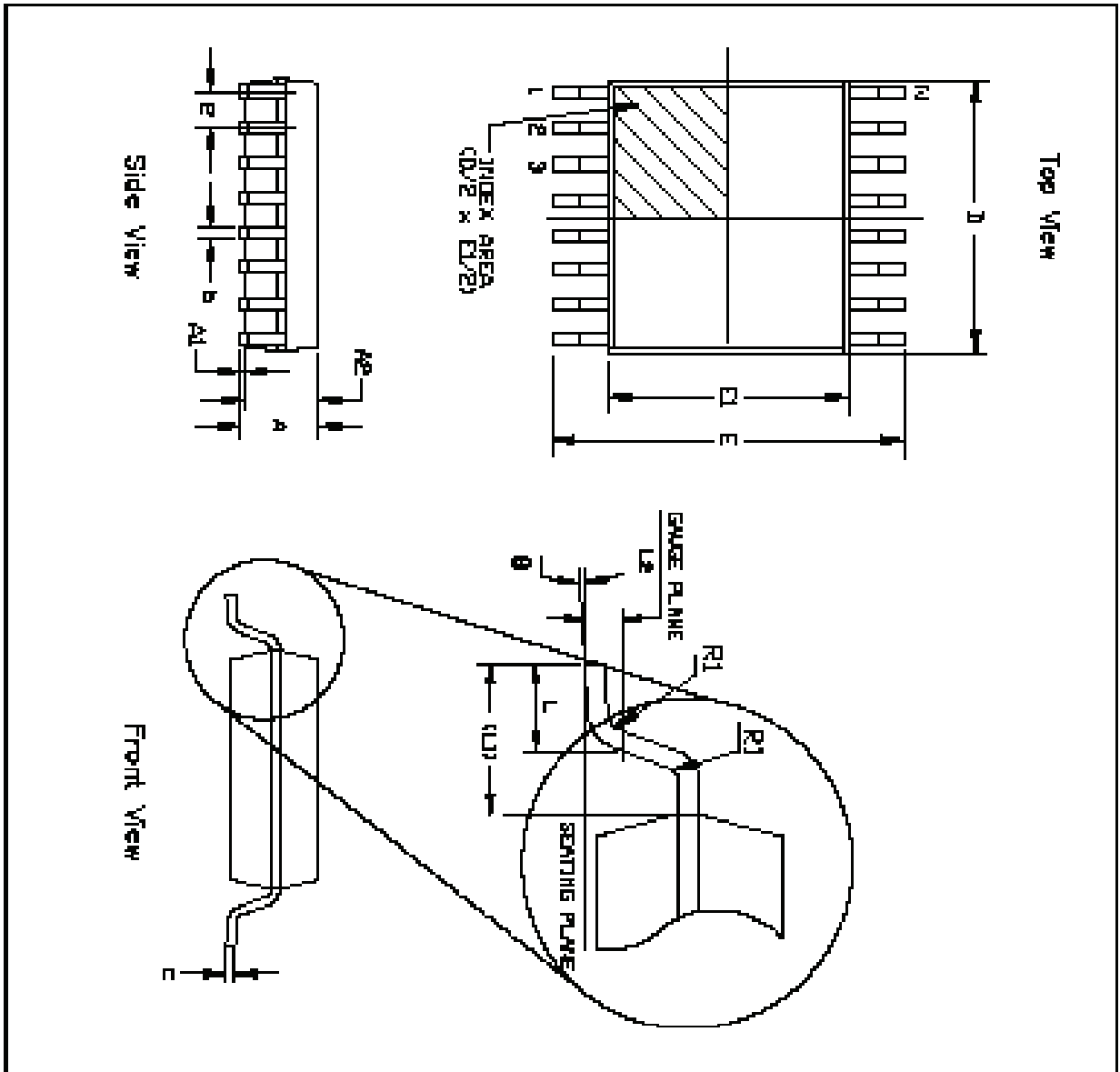
Drawing No.: 20-PIN SSOP

11/07/07

REVISED

DATE

1 OF 1

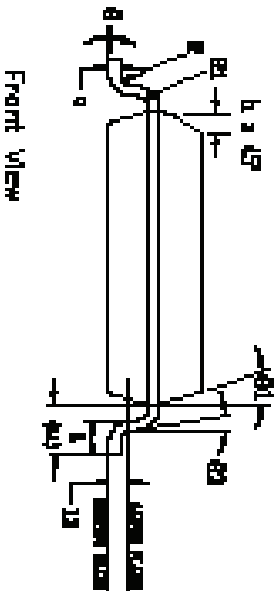
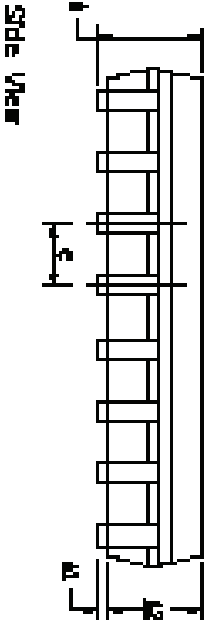
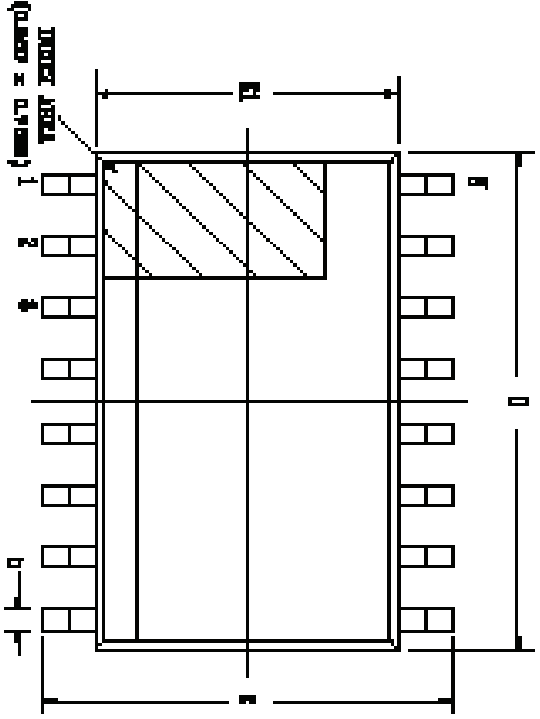


PINNOUT			
REF	DESCRIPTION	REF	NOTE
A	DRIVING SIGNAL	MAX/MIN	1
B	DRIVING SIGNAL	MAX/MIN	1

16 Pin SSOP JEDEC NID-150 Variation AC							
SYMBOLS	DIMENSIONS IN MM (CONFORM UNITS)		DIMENSIONS IN INCH (REFERENCE UNITS)		MIN	TYP	MAX
	MIN	MAX	MIN	MAX			
A	—	2.00	—	—	0.078		
A1	0.65	—	0.026	—	—		
A2	1.50	1.75	0.060	0.069	0.075		
b	0.25	—	0.009	—	0.015		
c	0.48	—	0.019	—	0.019		
E	7.40	7.60	0.291	0.307	0.293		
E1	0.60	0.30	0.017	0.012	0.230		
f	0.65	0.65	0.026	0.026			
L	0.00	0.75	0.000	0.030	0.037		
L1	1.20	REF	0.048	REF			
L2	0.20	0.95	0.010	0.038			
R1	0.08	—	0.004	—	—		
Ø	0°	4°	0°	4°	0°		
Ø	0.90	4.20	0.035	0.165	0.280		
U	16	16	16	16			

		EXAR CORPORATION	
Packaging Approval:		Drawing No: 16-PIN SSOP	
Date: 11/20/07		Revision: B Sheet: 1 of 1	
		EXAR CORPORATION	
16 PIN SSOP PACKAGE DIMENSIONS		16-PIN SSOP	

PINNING SCHEMATIC			
REF	DESCRIPTION	SIZE	APPROX
A	INSULATED PIN HEAD	1.40mm	±
B	INSULATED PIN HEAD DIAMETER	0.475mm	±
D	INSULATED PIN HEAD PIN SPACING PITCH	1.27mm	±

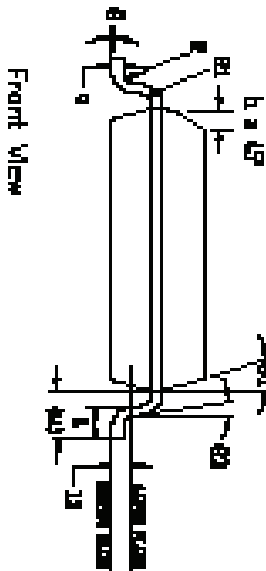
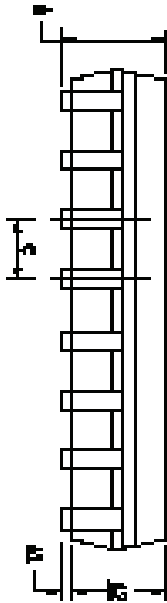
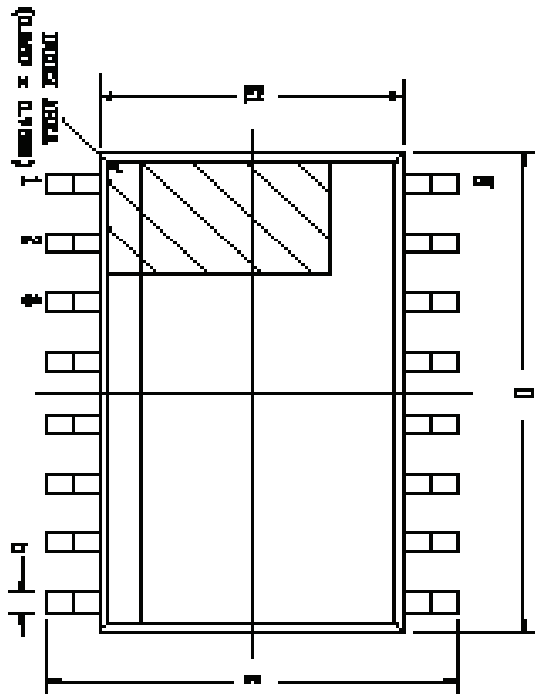


16 PIN SOICW INDEX MS-Q13 Variation A4			
SYMBOL	DESCRIPTION IN INCH (Symbol Unit)	DESCRIPTION IN MM (Reference Unit)	MAX
A	2.08	2.08	0.104
A1	0.10	0.008	0.019
A2	2.05	0.081	0.106
B	0.31	0.012	0.026
C	0.28	0.008	0.013
E	10.30 REF	0.409 REF	
G1	2.50 REF	0.280 REF	
H	1.27 REF	0.050 REF	
I	0.40	0.016	0.040
L	0.40	0.016	0.040
U1	1.40 REF	0.055 REF	
U2	0.40 REF	0.016 REF	
R	0.65	0.025	—
M	0.65	0.025	—
Q	0.7	0.028	—
RL	0.7	0.028	—
DR	0.7	0.028	—
D	10.30 REF	0.409 REF	
H	1.27	0.050	

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16 PIN SOICW PACKAGE OUTLINE

Part No.	Rev	11/20/07	Revision	5	Sheet	1 of 1
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18 Pin WSOIC JDEC HS-013 Variation A/B		Dimensional Callouts		Dimensions in Inch	
Symbol	Parameter	Min	Max	Min	Max
A	Lead Length	0.100	0.125	0.004	0.005
B	Lead Width	0.100	0.125	0.004	0.005
C	Lead Thickness	0.005	0.010	0.002	0.004
D	Lead Spacing	0.100	0.125	0.004	0.005
E	Lead Angle	0.000	0.000	0.000	0.000
F	Lead Position	0.000	0.000	0.000	0.000
G	Lead Tolerance	0.000	0.000	0.000	0.000
H	Lead Finish	0.000	0.000	0.000	0.000
I	Lead Material	0.000	0.000	0.000	0.000
J	Lead Color	0.000	0.000	0.000	0.000
K	Lead Surface	0.000	0.000	0.000	0.000
L	Lead Treatment	0.000	0.000	0.000	0.000
M	Lead Plating	0.000	0.000	0.000	0.000
N	Lead Thickness	0.000	0.000	0.000	0.000
O	Lead Width	0.000	0.000	0.000	0.000
P	Lead Spacing	0.000	0.000	0.000	0.000
Q	Lead Angle	0.000	0.000	0.000	0.000
R	Lead Position	0.000	0.000	0.000	0.000
S	Lead Tolerance	0.000	0.000	0.000	0.000
T	Lead Finish	0.000	0.000	0.000	0.000
U	Lead Material	0.000	0.000	0.000	0.000
V	Lead Color	0.000	0.000	0.000	0.000
W	Lead Surface	0.000	0.000	0.000	0.000
X	Lead Treatment	0.000	0.000	0.000	0.000
Y	Lead Plating	0.000	0.000	0.000	0.000
Z	Lead Thickness	0.000	0.000	0.000	0.000

REVISION HISTORY			
REV	DESCRIPTION	DATE	APP'D
1	INITIAL RELEASE	04/24/04	A
2	CHANGE DIMENSIONAL CALLOUTS	11/27/07	A

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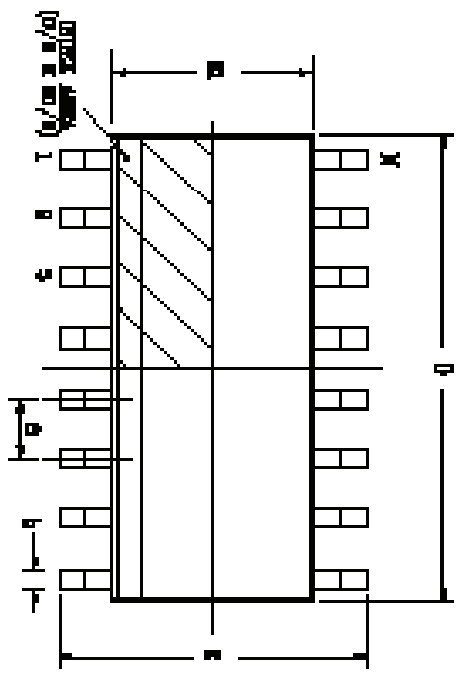
18 PIN SOIC PACKAGE OUTLINE

Drawing No: 18-PIN SOIC
Revision: B Sheet 1 of 1

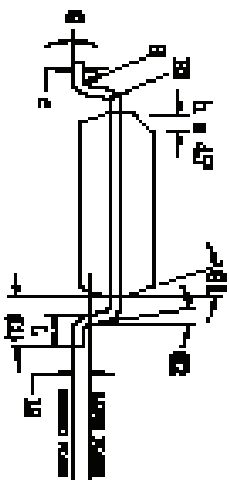
Packaging Approval: 11/27/07

PACKING METHOD				
REV	DESCRIPTION	DATE	APP'D	BY
A	PACKAGE DIMENSIONS	04/10/03		A
B	PACKAGE DIMENSIONS	05/11/03		A
D	PACKAGE DIMENSIONS WITH NEW DIMENSIONAL TOLERANCES	11/20/07		A

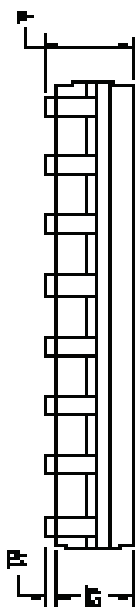
16 PIN SOIC JEDEC MS-012 VARIATION A2			
SYMBOL	DESCRIPTION IN MM (DIMENSIONAL LIMIT)	DESCRIPTION IN INCH (DIMENSIONAL LIMIT)	UNIT
A	1.90	1.75	0.003
A1	0.10	0.004	0.010
A2	1.35	1.05	0.004
b	0.31	0.012	0.003
c	0.17	0.007	0.010
e	0.20 BSC	0.008 BSC	
E1	1.20 BSC	0.124 BSC	
F	1.57 BSC	0.000 BSC	
H	0.25	0.010	0.000
L	0.40	1.27	0.014
L1	1.04 REF	0.041 REF	
L2	0.25 BSC	0.010 BSC	
n	0.07	0.003	—
n1	0.07	0.003	—
1	0	0	—
n1	0	0	—
n2	0	0	—
D	1.80 BSC	0.070 BSC	18
H	18	18	



Top View

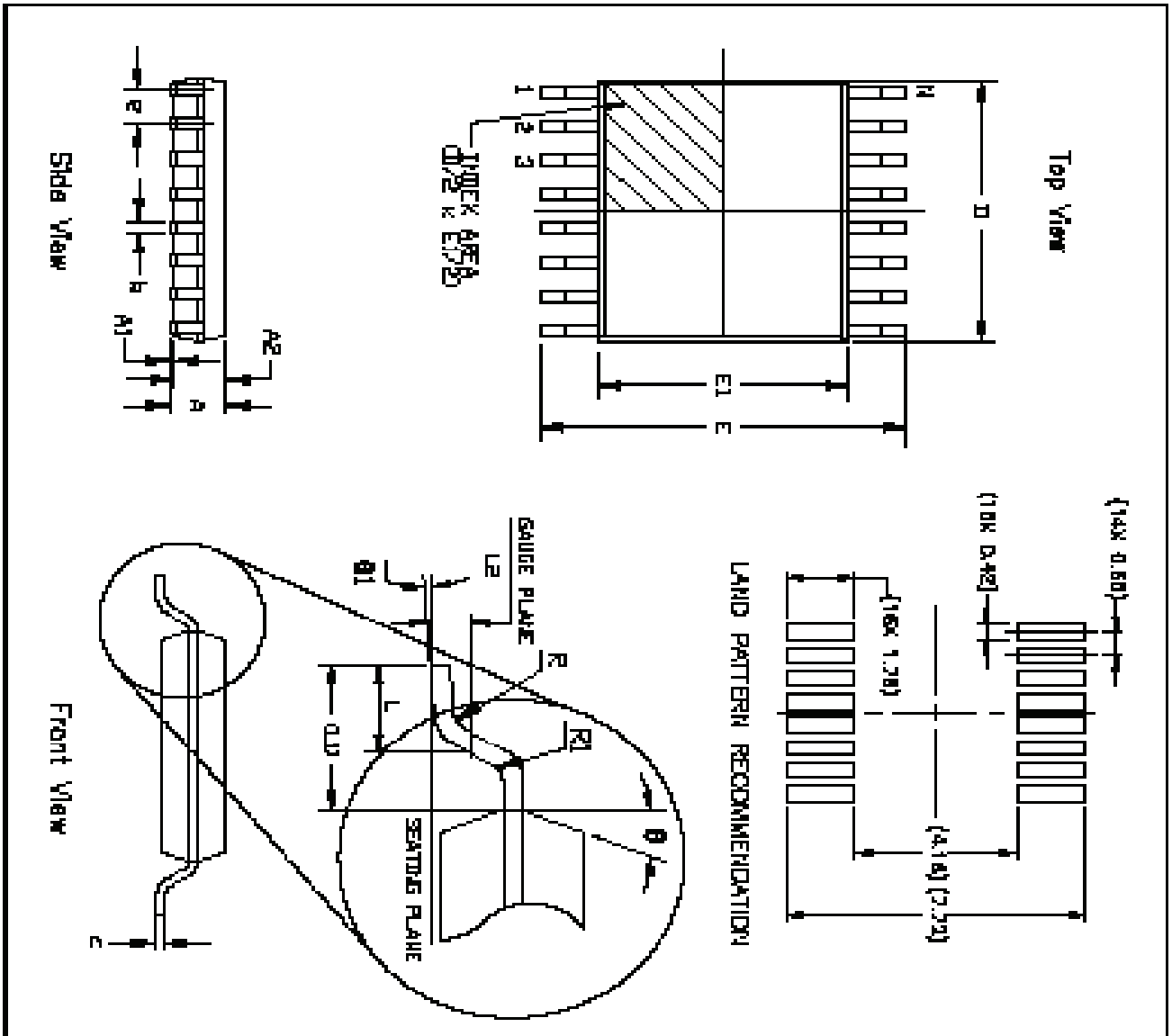


Front View




Side View

		EXAR CORPORATION	
Packaging Approval:		Drawing No: 16-PIN SOIC	
DATE: 11/20/07	BY: [Signature]	DATE: 11/20/07	BY: [Signature]



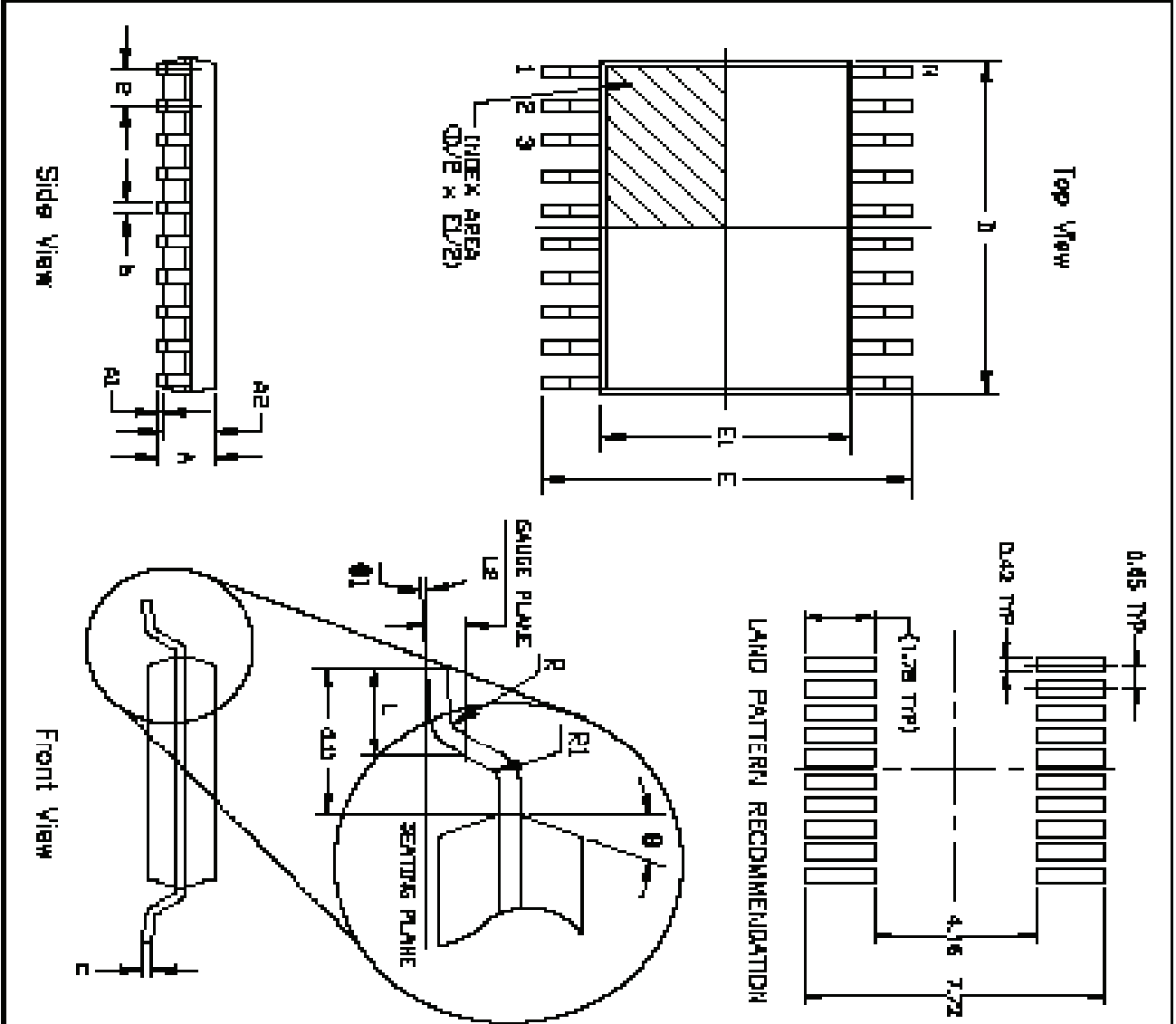
PINNING SYSTEM			
EX	DESCRIPTION	NOT	APPRO
1	MINIMUM RECOMMENDED	14.1/14.9	1
2	MAX LEAD LENGTH RECOMMENDATION	0.25/0.28	1
3	OPTIMAL LEAD LENGTH AND FOOTPRINT RANGE	11.0/13.7	1

16 PIN TSSOP JONES NO. 153 VARIATION A/B						
SYMBOL	DESCRIPTION IN MM (TYPICAL LIMIT)	DESCRIPTION IN INCH (TYPICAL LIMIT)	MIN	MAX	MIN	MAX
A	—	1.20	—	—	0.0437	—
A1	0.04	0.10	0.002	—	0.0008	—
A2	0.05	1.05	0.001	0.004	0.004	0.044
h	0.10	—	0.002	—	0.012	—
e	0.07	—	0.001	—	0.0003	—
E	0.40 BSC	—	0.012 BSC	—	—	—
E1	0.20	0.40	0.001	0.173	0.177	—
h	0.45 BSC	—	0.008 BSC	—	—	—
L	0.45	0.90	0.018	0.024	0.030	—
L1	1.00 REF	—	0.039 REF	—	—	—
L2	0.20 BSC	—	0.010 BSC	—	—	—
R	0.08	—	0.006	—	—	—
R1	0.08	—	0.006	—	—	—
Ø	12° REF	—	12° REF	—	—	—
Ø1	0	—	0	—	0	—
D	1.89	0.010	0.185	0.187	0.200	—
P	—	—	—	—	—	—



EXAR CORPORATION

Package/Type Approval	16 PIN TSSOP PACKAGE DANLINE
Drawing No.	16-PIN TSSOP
Rev.	11/70/07 Rev.0011 © EXAR 1 OF 1



PINNING SCHEMATIC			
1	INDEX MARKER	19	NC
2	AND LAND PATTERN RECOMMENDATION	20	NC
3	INDEX MARKER	1	NC

20 PIN TSSOP JEDEC MO-153 VARIATION #2			
DIMENSIONS IN MM		DIMENSIONS IN INCH	
SYMBOLS (MILITARY UNIT)			
MIN	FORM	MAX	UNIT
A	—	1.25	—
A1	0.60	0.15	0.052
A2	0.60	1.00	0.039
B	0.16	0.30	0.007
C	0.68	—	0.026
E	0.40 BSC	—	0.016 BSC
EL	4.30	4.50	0.169
L	0.45	0.75	0.018
L1	1.00 REF	—	0.039 REF
L2	0.25 BSC	—	0.010 BSC
R	0.08	—	0.003
R1	0.08	—	0.003
Ø	12° REF	—	12° REF
Ø1	0	0	0
D	6.40	6.60	0.252
H	20	20	20

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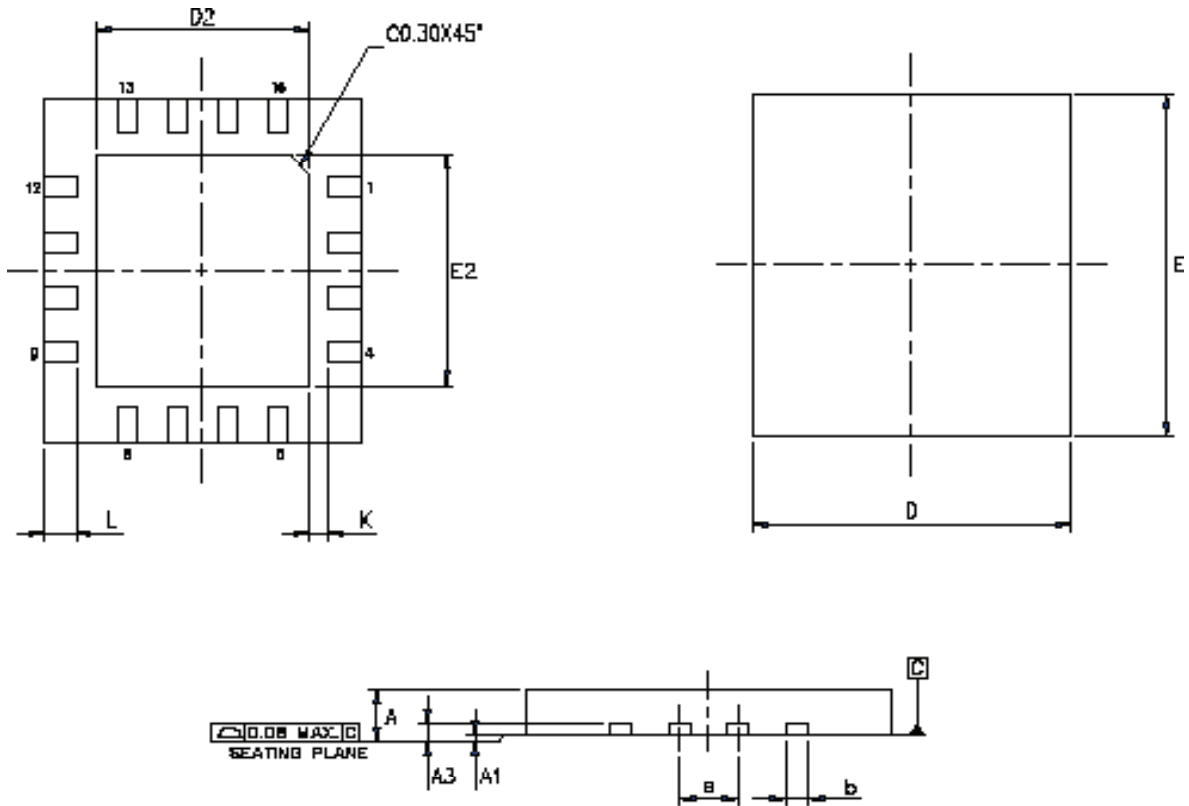
20 PIN TSSOP PACKAGE OUTLINE

Drawing No: 20-PIN TSSOP

Revision: 5

Sheet: 1 of 1

Package Approval: 11/20/07



PACKAGE TYPE	
JEDEC CODE	MO-22D
PKG CODE	WQFN(YS16)
SYMBOLS	MIN. NOM. MAX.
A	0.80 0.85 0.90
A1	0.00 0.02 0.05
A3	0.203 REF.
b	0.25 0.30 0.35
D	4.85 5.00 5.05
E	4.85 5.00 5.05
e	0.80 BSC
L	0.45 0.50 0.55
K	0.20 - -

PAD SIZE	E2			D2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Th	PPF	
142X142 ML	3.28	3.38	3.43	3.28	3.38	3.43	V	X	N/A

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

ORDERING INFORMATION

Part Number	Temp. Range	Package
SP3222EBCA-L	0°C to +70°C	20 Pin SSOP
SP3222EBCA-L/TR	0°C to +70°C	20 Pin SSOP
SP3222EBCT-L	0°C to +70°C	18 Pin WSOIC
SP3222EBCT-L/TR	0°C to +70°C	18 Pin WSOIC
SP3222EBCY-L	0°C to +70°C	20 Pin TSSOP
SP3222EBCY-L/TR	0°C to +70°C	20 Pin TSSOP
SP3222EBEA-L	-40°C to +85°C	20 Pin SSOP
SP3222EBEA-L/TR	-40°C to +85°C	20 Pin SSOP
SP3222EBET-L	-40°C to +85°C	18 Pin WSOIC
SP3222EBET-L/TR	-40°C to +85°C	18 Pin WSOIC
SP3222EBEY-L	-40°C to +85°C	20 Pin TSSOP
SP3222EBEY-L/TR	-40°C to +85°C	20 Pin TSSOP

Part Number	Temp. Range	Package
SP3232EBCA-L	0°C to +70°C	16 Pin SSOP
SP3232EBCA-L/TR	0°C to +70°C	16 Pin SSOP
SP3232EBCN-L	0°C to +70°C	16 Pin NSOIC
SP3232EBCN-L/TR	0°C to +70°C	16 Pin NSOIC
SP3232EBCT-L	0°C to +70°C	16 Pin WSOIC
SP3232EBCT-L/TR	0°C to +70°C	16 Pin WSOIC
SP3232EBCY-L	0°C to +70°C	16 Pin TSSOP
SP3232EBCY-L/TR	0°C to +70°C	16 Pin TSSOP
SP3232EBEA-L	-40°C to +85°C	16 Pin SSOP
SP3232EBEA-L/TR	-40°C to +85°C	16 Pin SSOP
SP3232EBEN-L	-40°C to +85°C	16 Pin NSOIC
SP3232EBEN-L/TR	-40°C to +85°C	16 Pin NSOIC
SP3232EBET-L	-40°C to +85°C	16 Pin WSOIC
SP3232EBET-L/TR	-40°C to +85°C	16 Pin WSOIC
SP3232EBEY-L	-40°C to +85°C	16 Pin TSSOP
SP3232EBEY-L/TR	-40°C to +85°C	16 Pin TSSOP
SP3232EBER-L	-40°C to +85°C	16 Pin QFN
SP3232EBER-L/TR	-40°C to +85°C	16 Pin QFN

Note: "/TR" is for tape and Reel option. "-L" is for lead free packaging

REVISION HISTORY

DATE	REVISION	DESCRIPTION
11/02/05	--	Legacy Sipex Datasheet
09/09/09	1.0.0	Convert to Exar Format, Update ordering information and change revision to 1.0.0.
06/07/11	1.0.1	Remove obsolete devices per PDN 110510-01 and change ESD rating to IEC-61000-4-2.
03/14/13	1.0.2	Correct type error to RX input voltage range and TX transition region slew rate condition.
8/14/14	1.0.3	Add Max Junction temperature and package thermal information.
5/28/15	1.0.4	Update Absolute Max Rating for RxIN input voltage to +/-25V, update logo.
10/27/15	1.0.5	Add SP3232EBER (QFN_16) preliminary package option.
2/23/16	1.0.6	Remove preliminary status of QFN_16 package option.

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Datasheet February 2016

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