THE DATASHEET OF

CBTU4411EE,518

CBTU4411

11-bit DDR2 SDRAM MUX/bus switch with 12 Ω ON resistance

Rev. 4 — 18 June 2012 Product data sheet

1. General description

This 11-bit bus switch is designed for 1.7 V to 1.9 V V_{DD} operation and SSTL_18 select input levels.

Each Host port pin (HPn) is multiplexed to one of four DIMM port pins (xDPn). The selection of the DIMM port to be connected to the Host port is controlled by a decoder driven by three hardware select pins S0, S1 and $\overline{EN}$. Driving pin $\overline{EN}$ HIGH disconnects all DIMM ports from their respective host ports. When $\overline{EN}$ is driven LOW, pins S0 and S1 select one of four DIMM ports to be connected to their respective host port. When disconnected, any DIMM port is terminated to the externally supplied voltage V_{bias} by means of an on-chip pull-down resistor of typically 400 Ω. The ON-state connects the Host port to the DIMM port through a 12 Ω nominal series resistance. The design is intended to have only one DIMM port active at any time.

The CBTU4411 can also be configured to support a differential strobe signal on channel 10 (TRUE) and channel 9 (complementary Strobe). When its LVCMOS configuration input strobe enable (STREN) is HIGH, channel 10 is pulled up to $^3/_4$ of V_{DD} internally by a resistive divider when the DIMM port is idle. When the CBTU4411 is disabled ($\overline{EN}$ = HIGH in Strobe mode), the pull-down on channel 10 is disabled for current savings, pulling channel 10 to V_{DD}. When strobe enable (STREN) is LOW, channel 10 behaves the same as all other channels.

The select inputs (S0, S1) are pseudo-differential type SSTL_18. A reference voltage should be provided to input pin VREF at nominally $0.5V_{DD}$. This topology provides accurate control of switching times by reducing dependency on select signal slew rates. S0 and S1 are provided with selectable input termination to $0.5V_{DD}$ (active when LVCMOS input TERM is HIGH). When the CBTU4411 is disabled ($\overline{EN}$ = HIGH), both S0 and S1 inputs are pulled LOW.

The part incorporates a very low crosstalk design. It has a very low skew between outputs (< 30 ps) and low skew (< 30 ps) for rising and falling edges. The part has optimal performance in DDR2 data bus applications.

Each switch has been optimized for connection to 1- or 2-rank DIMMs.

The low internal RC time constant of the switch allows data transfer to be made with minimal propagation delay.

The CBTU4411 is characterized for operation from 0 °C to +85 °C.

2. Features and benefits

- Enable ($\overline{EN}$) and select signals (S0, S1) are SSTL_18 compatible
- Optimized for use in Double Data Rate 2 (DDR2) SDRAM applications
- Suitable to be used with 400 Mbit/s to 800 Mbit/s, 200 MHz to 400 MHz DDR2 data bus
- Switch ON-resistance is designed to eliminate the need for series resistor to DDR2 SDRAM
- 12 Ω ON-resistance
- Controlled enable/disable times support fast bus turnaround
- Pseudo-differential select inputs support accurate and low-skew control of switching times
- Selectable built-in termination resistors on the Sn inputs
- Internal 400 Ω pull-down resistors on xDPn port
- VBIAS input for optimal DIMM-port pull-down when disabled
- Configurable to support differential strobe with pull-up to $^3/_4$ of V_{DD} on channel 10 when idle
- Low differential skew
- Matched rise/fall slew rate
- Low crosstalk data-data/data-DQM
- Simplified 1 : 4 switch position control by 2-bit encoded input
- Single input pin puts all bus switches in OFF (high-impedance) position
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 1500 V HBM per JESD22-A114 and 750 V CDM per JESD22-C101

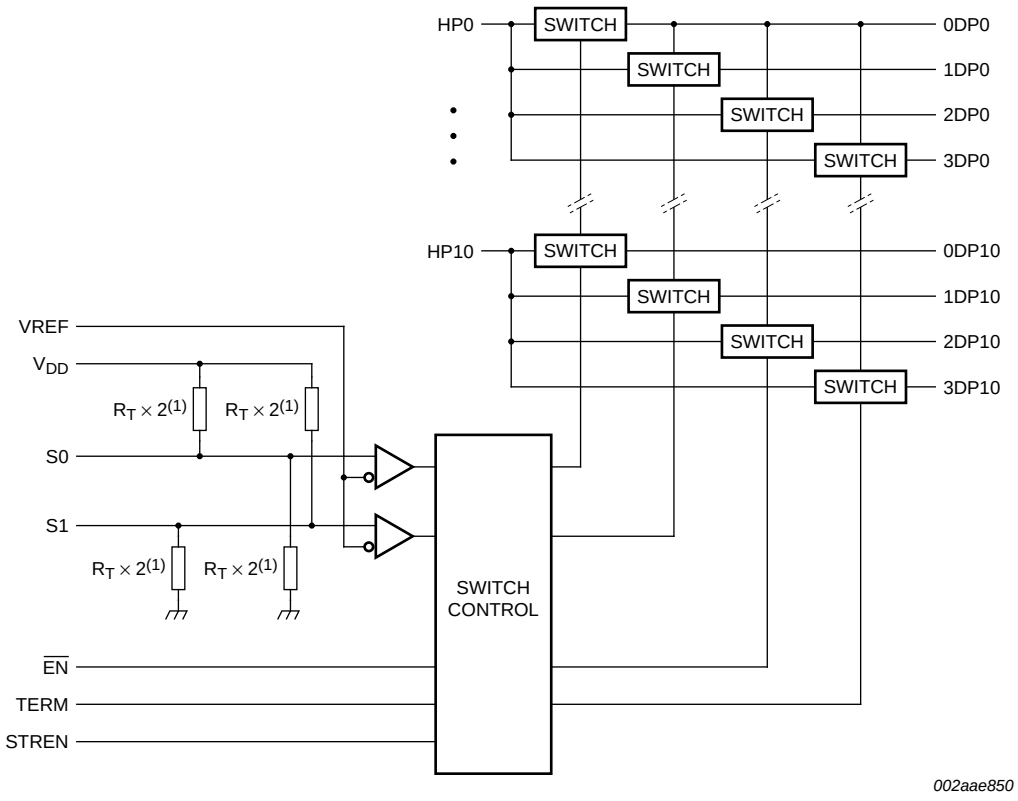
3. Ordering information

Table 1. Ordering information

T_{amb} = 0 °C to +85 °C.

Type number	Package		
	Name	Description	Version
CBTU4411EE	LFBGA72	plastic low profile fine-pitch ball grid array package; 72 balls; body 7 × 7 × 1.05 mm	SOT856-1

4. Functional diagram



(1) Selectable.

Fig 1. Functional diagram (positive logic)

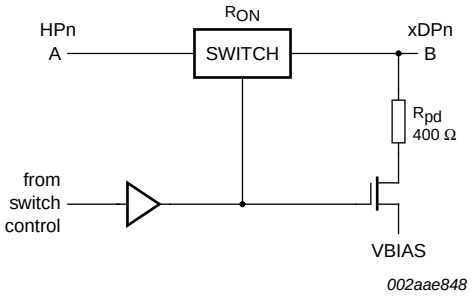


Fig 2. Simplified schematic, channel 0 to channel 9

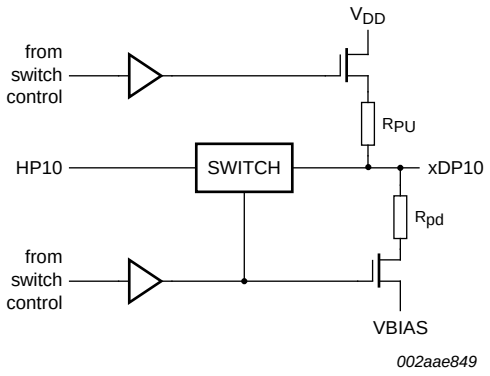
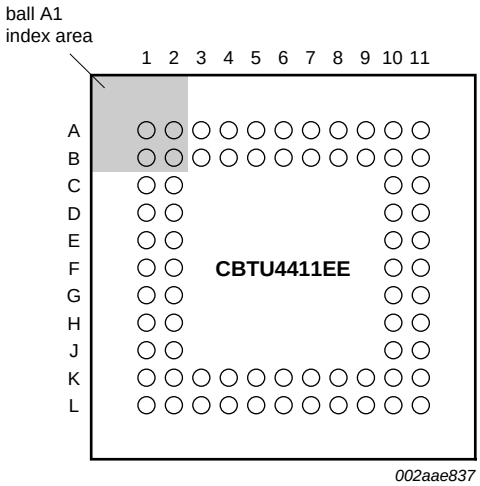


Fig 3. Simplified schematic, channel 10

5. Pinning information

5.1 Pinning



Transparent top view

Fig 4. Pin configuration

	1	2	3	4	5	6	7	8	9	10	11
A	S1	STREN	V_{DD}	0DP0	1DP0	2DP0	1DP1	2DP1	3DP1	0DP2	1DP2
B	TERM	S0	V_{DD}	GND	HP0	3DP0	0DP1	HP1	GND	HP2	2DP2
C	VREF	$\overline{EN}$								0DP3	3DP2
D	VBIAS	GND								HP3	1DP3
E	2DP10	3DP10								2DP3	3DP3
F	1DP10	HP10								GND	0DP4
G	0DP10	GND								HP4	1DP4
H	3DP9	2DP9								2DP4	3DP4
J	1DP9	HP9								1DP5	0DP5
K	0DP9	GND	HP8	0DP8	HP7	0DP7	GND	HP6	0DP6	HP5	2DP5
L	3DP8	2DP8	1DP8	3DP7	2DP7	1DP7	3DP6	2DP6	1DP6	V_{DD}	3DP5

002aae838

Blank cell indicates no ball at that location.

Fig 5. Ball mapping (transparent top view)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
HP0 to HP10	B5, B8, B10, D10, G10, K10, K8, K5, K3, J2, F2	Host ports
$\overline{EN}$	C2	LVCMOS level enable input (active LOW). When connected HIGH, all DIMM ports will be disconnected (show a high-impedance path) from the Host ports.
STREN	A2	Strobe enable. LVCMOS level strobe enable input (active HIGH). When tied LOW, channel 10 (HP10 and its DP ports) functions identically to all other channels. When tied HIGH, channel 10 is designated as the Strobe channel (see Section 6.1 “Function selection”, Figure 2 and Figure 3).
S0	B2	Select inputs; type SSTL_18. See Section 6.1 “Function selection”.
S1	A1	
VREF	C1	Reference voltage for the pseudo-differential SSTL_18 select inputs (S0, S1).
VBIAS	D1	Voltage bias for the DIMM port pull-down resistor (R_{pd}).
TERM	B1	LVCMOS level input pin activates termination resistance on Sn inputs when HIGH; high-impedance when LOW.
0DP0, 1DP0, 2DP0, 3DP0	A4, A5, A6, B6	DIMM port 0
0DP1, 1DP1, 2DP1, 3DP1	B7, A7, A8, A9	DIMM port 1
0DP2, 1DP2, 2DP2, 3DP2	A10, A11, B11, C11	DIMM port 2
0DP3, 1DP3, 2DP3, 3DP3	C10, D11, E10, E11	DIMM port 3
0DP4, 1DP4, 2DP4, 3DP4	F11, G11, H10, H11	DIMM port 4
0DP5, 1DP5, 2DP5, 3DP5	J11, J10, K11, L11	DIMM port 5
0DP6, 1DP6, 2DP6, 3DP6	K9, L9, L8, L7	DIMM port 6
0DP7, 1DP7, 2DP7, 3DP7	K6, L6, L5, L4	DIMM port 7
0DP8, 1DP8, 2DP8, 3DP8	K4, L3, L2, L1	DIMM port 8
0DP9, 1DP9, 2DP9, 3DP9	K1, J1, H2, H1	DIMM port 9
0DP10, 1DP10, 2DP10, 3DP10	G1, F1, E1, E2	DIMM port 10
GND	B4, B9, D2, F10, G2, K2, K7	Ground
V_{DD}	A3, B3, L10	Positive supply voltage

6. Functional description

Refer to Figure 1 “Functional diagram (positive logic)”.

6.1 Function selection

Table 3. Function selection, channel 0 to channel 9

H = HIGH voltage level; L = LOW voltage level; high-Z = high-impedance; X = Don’t care.

Inputs			Function							
			0DPn		1DPn		2DPn		3DPn	
$\overline{EN}$	S1	S0	HPn	VBIAS	HPn	VBIAS	HPn	VBIAS	HPn	VBIAS
L	L	L	R_{ON}	high-Z	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}
L	L	H	high-Z	R_{pd}	R_{ON}	high-Z	high-Z	R_{pd}	high-Z	R_{pd}
L	H	L	high-Z	R_{pd}	high-Z	R_{pd}	R_{ON}	high-Z	high-Z	R_{pd}
L	H	H	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}	R_{ON}	high-Z
H	X	X	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}

Table 4. Function selection, channel 10

H = HIGH voltage level; L = LOW voltage level; high-Z = high-impedance; X = Don't care.

Inputs				Function								
				0DP10			1DP10			2DP10		
$\overline{EN}$	S1	S0	STREN	HP10	VBIAS	V_{DD}	HP10	VBIAS	V_{DD}	HP10	VBIAS	V_{DD}
L	L	L	L	R_{ON}	high-Z	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
L	L	L	H	R_{ON}	high-Z	high-Z	high-Z	R_{pd}	R_{PU}	high-Z	R_{pd}	R_{PU}
L	L	H	L	high-Z	R_{pd}	high-Z	R_{ON}	high-Z	high-Z	high-Z	R_{pd}	high-Z
L	L	H	H	high-Z	R_{pd}	R_{PU}	R_{ON}	high-Z	high-Z	high-Z	R_{pd}	R_{PU}
L	H	L	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	R_{ON}	high-Z	high-Z
L	H	L	H	high-Z	R_{pd}	R_{PU}	high-Z	R_{pd}	R_{PU}	R_{ON}	high-Z	high-Z
L	H	H	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
L	H	H	H	high-Z	R_{pd}	R_{PU}	high-Z	R_{pd}	R_{PU}	high-Z	R_{pd}	R_{PU}
H	X	X	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
H	X	X	H	high-Z	high-Z	R_{PU}	high-Z	high-Z	R_{PU}	high-Z	high-Z	R_{PU}

Table 5. S0, S1 input termination

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

$\overline{EN}$	TERM	Sn input termination
L	L	Termination resistors on S0, S1 inputs disconnected (high-impedance).
L	H	Termination resistors on S0, S1 inputs active.
H	X	Pull-down to GND via $R_T \times 2$. Also disables the S0, S1 input receivers for power savings.

7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
The package thermal impedance is calculated in accordance with JESD 51.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
I_{IK}	input clamping current	$V_{I/O} < 0$ V		-	–50	mA
V_I	input voltage	S0, S1 pins only	[1]	-	$V_{DD} + 0.3$	V
		except S0, S1 pins	[1]	–0.5	+2.5	V
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamping current ratings are observed.

8. Recommended operating conditions

Table 7. Operating conditions

All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	1.9	V
V_{ref}	reference voltage			$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{bias}	bias voltage	pull-down resistor input	[1]	0	$0.30 \times V_{DD}$	$0.33 \times V_{DD}$	V
V_T	termination voltage			$V_{ref} - 0.04$	V_{ref}	$V_{ref} + 0.04$	V
V_i	input voltage			0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	S0, S1 inputs		$V_{ref} + 0.250$	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	S0, S1 inputs		-	-	$V_{ref} - 0.250$	V
$V_{IH(DC)}$	DC HIGH-level input voltage	S0, S1 inputs		$V_{ref} + 0.125$	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	S0, S1 inputs		-	-	$V_{ref} - 0.125$	V
V_{IH}	HIGH-level input voltage	$\overline{EN}$, STREN, TERM pins		$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$, STREN, TERM pins		-	-	$0.35 \times V_{DD}$	V
T_{amb}	ambient temperature	operating in free air		0	-	+85	°C

[1] $V_{bias} > 0.5 \times V_{DD}$ is reserved for test purposes only.

9. Static characteristics

Table 8. Static characteristics

T_{amb} = 0 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{DD} = 1.7 V; I_I = –18 mA		-	-	–1.2	V
V_T	termination voltage	on S0, S1 inputs when Sn = open circuit and TERM = HIGH		$0.5V_{DD}$ – 0.04	$0.5V_{DD}$	$0.5V_{DD}$ + 0.04	V
V_{pu}	pull-up voltage	channel 10 DIMM port; $\overline{EN}$ = LOW; V_{bias} = 0.54 V; V_{DD} = 1.8 V; STREN = HIGH; unselected DIMM port		$0.5V_{DD}$ + 0.25	$0.75V_{DD}$	$0.75V_{DD}$ + 0.25	V
I_{LI}	input leakage current	V_{DD} = 1.8 V; V_I = V_{DD} or GND; Sn = V_{DD}; V_{bias} = V_{DD}; TERM = LOW					
		S0, S1		-	-	±100	µA
		host port		-	-	±100	µA
		DIMM port		-	-	±100	µA
I_{DD}	supply current	V_{DD} = 1.8 V; I_O = 0 A; V_I = V_{DD} or GND					
		$\overline{EN}$ = LOW		-	6	9	mA
		$\overline{EN}$ = HIGH		-	5	100	µA
C_{in}	input capacitance	S0, S1 pins; V_I = 1.8 V or 0 V		-	3	-	pF
C_{sw}	switch capacitance	switch ON; V_I = 0.9 V		-	4	6	pF
R_{ON}	ON resistance	V_{DD} = 1.8 V; V_{HPn} = V_{ref}; V_{xDPn} = V_{ref} ± 250 mV	[2]	10	12	17	Ω
		V_{DD} = 1.8 V; V_{HPn} = V_{ref}; V_{xDPn} = V_{ref} ± 500 mV	[2]	10	12	17	Ω
R_{pd}	pull-down resistance	$\overline{EN}$ = HIGH; V_{bias} = 0.54 V; V_{DD} = 1.8 V		280	400	520	Ω
		channel 10; STREN = LOW		280	400	520	Ω
		channel 10; STREN = HIGH		780	1120	1460	Ω
R_{PU}	pull-up resistance	$\overline{EN}$ = HIGH; V_{bias} = 0.54 V; V_{DD} = 1.8 V; channel 10; STREN = HIGH		430	622	810	Ω
R_T	termination resistance	Sn input; Thevenin equivalent (see Figure 1); input voltage sweep 0 < V_I (Sn) < V_{DD}; TERM = HIGH		55	80	105	Ω

[1] All typical values are at V_{DD} = 1.8 V, T_{amb} = 25 °C.

[2] Measured by the current between the host and the DIMM terminals at the indicated voltages on each side of the switch.

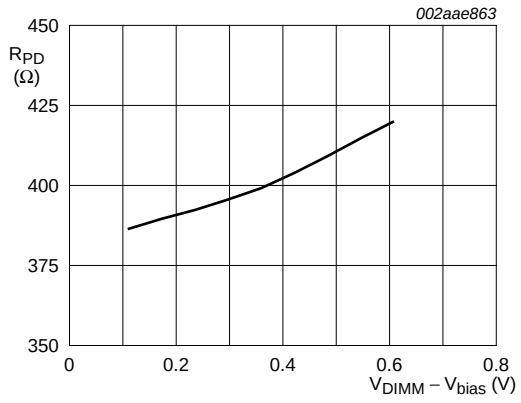


Fig 6. Pull-down resistance versus voltage

10. Dynamic characteristics

Table 9. Dynamic characteristics

V_{DD} = 1.8 V ± 0.1 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	from HPn or xDPn to xDPn or HPn; Figure 9, Figure 13	[1]	-	50	100	ps
t_{PZH}	driver enable delay to HIGH level	from Sn to HPn or xDPn		0.75	-	1.75	ns
t_{PZL}	driver enable delay to LOW level	from Sn to HPn or xDPn		0.75	-	1.75	ns
t_{PHZ}	driver disable delay from HIGH level	from Sn to HPn or xDPn		0.75	-	1.75	ns
t_{PLZ}	driver disable delay from LOW level	from Sn to HPn or xDPn		0.75	-	1.75	ns
$t_{sk(o)}$	output skew time	from any output to any output; Figure 12	[2]	-	25	30	ps
$t_{sk(edge)}$	edge skew time	Figure 11	[2][3]	-	25	30	ps

[1] This parameter is not production tested.

[2] Skew is not production tested.

[3] Difference of rising edge propagation delay to falling edge propagation delay.

11. HPn to xDPn AC waveforms and test circuit

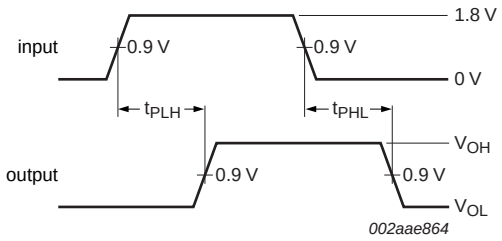
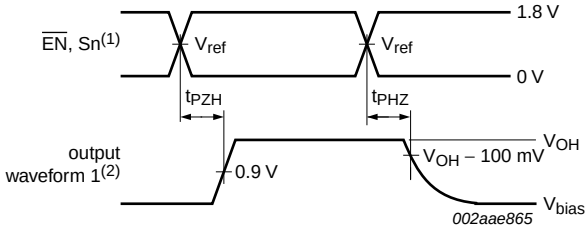


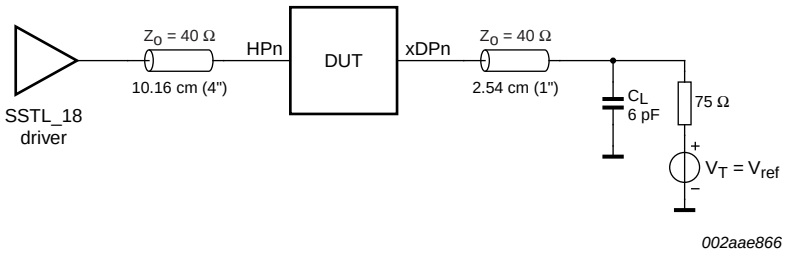
Fig 7. Input to output propagation delays



(1) See Section 6.1 “Function selection”.

(2) Waveform 1 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 8. 3-state output enable and disable times

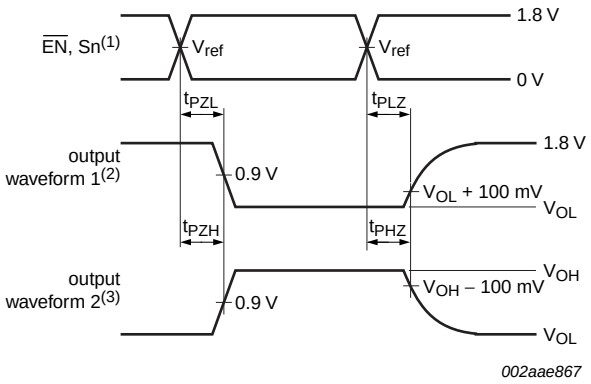


All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_o = 50 Ω; slew rate = 2.5 V/ns.

The outputs are measured one at a time with one transition per measurement.

Fig 9. Test circuit (HPn to xDPn)

12. xDPn to HPn AC waveforms and test circuit



(1) See Section 6.1 “Function selection”.

(2) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

(3) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 10. 3-state output enable and disable times

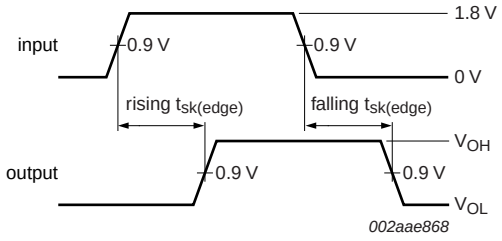


Fig 11. Rising and falling edge skew

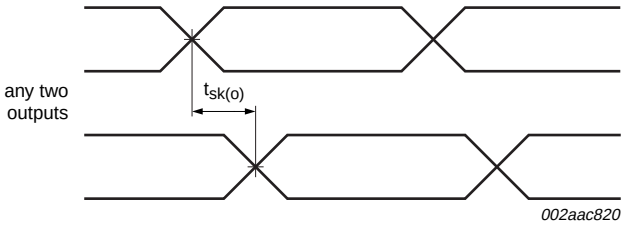
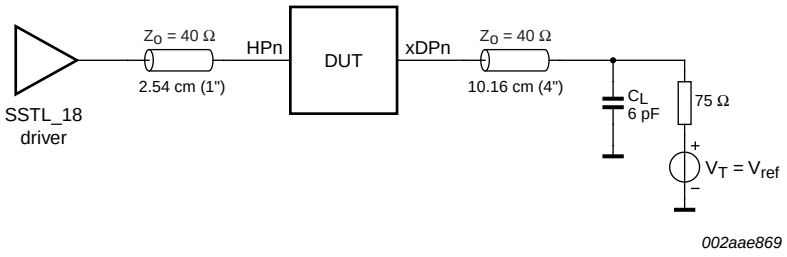


Fig 12. Skew between any two outputs



All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; slew rate = 2.5 V/ns.

The outputs are measured one at a time with one transition per measurement.

Fig 13. Test circuit (xDPn to HPn)

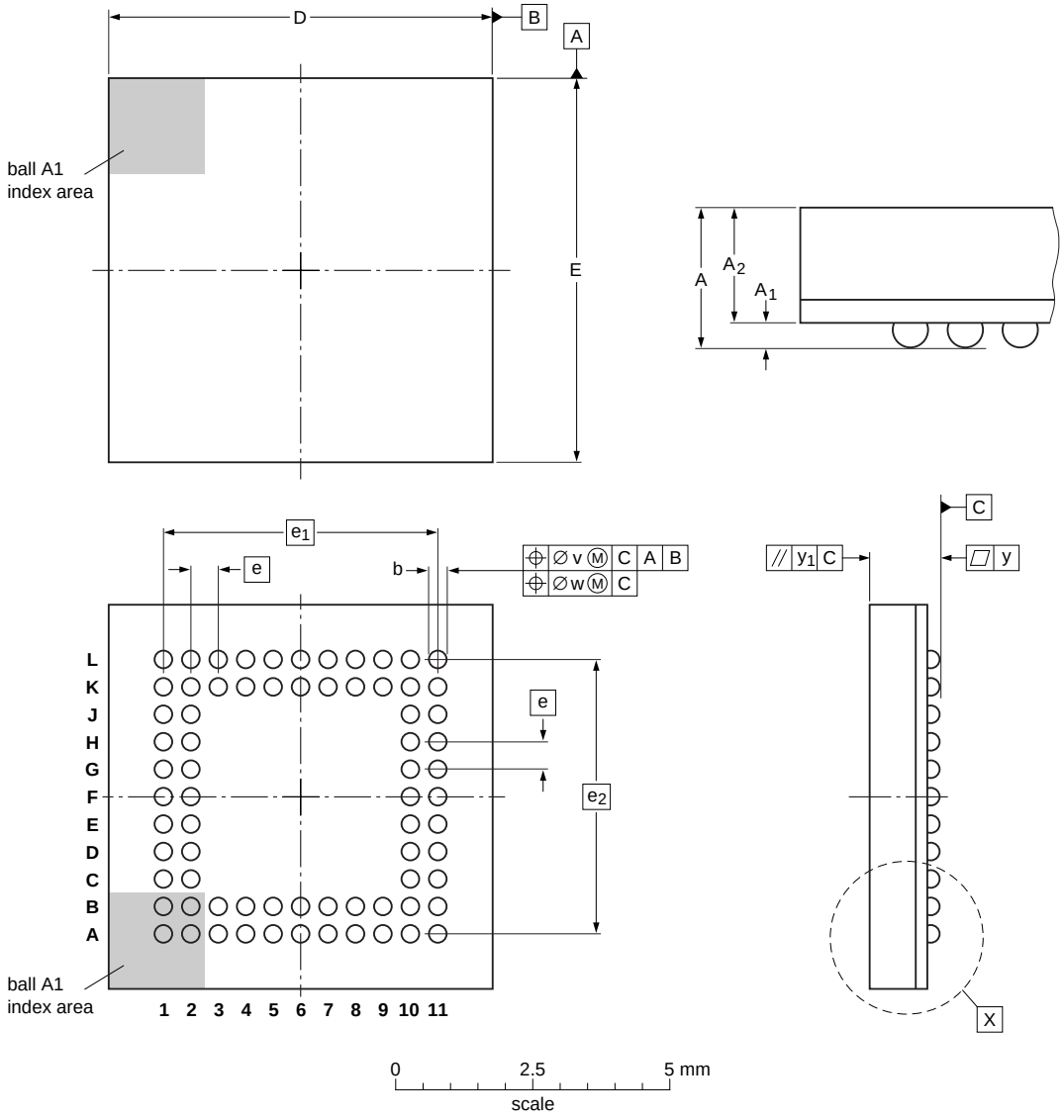
13. Test information

Table 10. I_{DD} test mode

Condition	Description
$V_{bias} = V_{DD}$	All DIMM ports are disconnected (high-impedance) from their host ports, and disconnected (high-impedance) from VBIAS and R_{PU}. Used for production testing only.
$V_{bias} < 0.5V_{DD}$	Normal operation. See Section 6.1 “Function selection”.

14. Package outline

LFBGA72: plastic low profile fine-pitch ball grid array package; 72 balls; body 7 x 7 x 1.05 mm **SOT856-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.3 0.2	1.20 0.95	0.35 0.25	7.2 6.8	7.2 6.8	0.5	5	5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT856-1						~~04-04-27~~ 04-05-12

Fig 14. Package outline SOT856-1 (LFBGA72)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

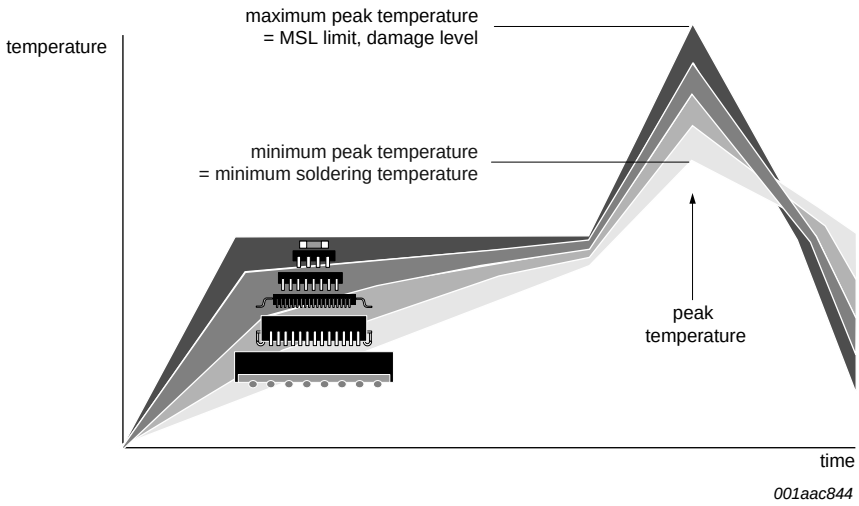
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.



MSL: Moisture Sensitivity Level

Fig 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DDR2	Double Data Rate 2
DIMM	Dual In-Line Memory Module
DQM	Data Queue Mask
ESD	ElectroStatic Discharge
HBM	Human Body Model
LVCMOS	Low Voltage Complementary Metal-Oxide Semiconductor
MUX	Multiplexer
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network
SDRAM	Synchronous Dynamic Random Access Memory
SSTL_18	Stub Series Terminated Logic for 1.8 V

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTU4411 v.4	20120618	Product data sheet	-	CBTU4411 v.3
Modifications:	• Section 2 “Features and benefits”, 18th bullet item: removed phrase “200 V MM per JESD22-A115” • Table 8 “Static characteristics”: – Symbol/Parameter “C_{on}, switch on capacitance” changed to “C_{sw}, switch capacitance” (and placed “switch ON” under Conditions) – R_{ON} Min value for Condition “$V_{xDPn} = V_{ref} \pm 250$ mV” changed from “7 Ω” to “10 Ω” – R_{ON} Min value for Condition “$V_{xDPn} = V_{ref} \pm 500$ mV” changed from “7 Ω” to “10 Ω” – deleted ΔR_{ON} row • Table 13 “Abbreviations”: removed “MM” from list of acronyms			
CBTU4411 v.3	20091012	Product data sheet	-	CBTU4411 v.2
CBTU4411 v.2	20060922	Product data sheet	-	CBTU4411 v.1
CBTU4411 v.1 (9397 750 12977)	20050107	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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