THE DATASHEET OF

ESD218B102ELE6327XTMA1

Protection Device

TVS (Transient Voltage Suppressor)

ESD218-B1 Series

Bi-directional, 24 V, 3 pF, 0201, 0402, RoHS and Halogen Free compliant

ESD218-B1-02ELS
ESD218-B1-02EL

Data Sheet

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Final

Power Management & Multimarket

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1 Product Overview

1.1 Features

- ESD / transient protection according to:
  - **IEC61000-4-2 (ESD): ±20 kV (air), ±18 kV (contact)**
  - **IEC61000-4-4 (EFT): ±2 kV / 40 A (5/50 ns)**
  - **IEC61000-4-5 (Surge): ±1.5 A (8/20 µs)**
- Bi-directional, working voltage up to V_{RWM} **= ±24 V**
- Low capacitance: C_L **= 3 pF (typical)**
- Low clamping voltage: V_{CL} **= 51 V (typical) at** I_{TLP} **= 16 A**
- Very low reverse current. I_R **= < 1nA (typical)**
- Pb-free (RoHS compliant) and halogen free package

1.2 Application Examples

- ESD protection of USB-battery charger interface
- LCD Backlight protection
- NFC antenna protection
- Protection of high speed bus rated up to ±24 V

1.3 Product Description

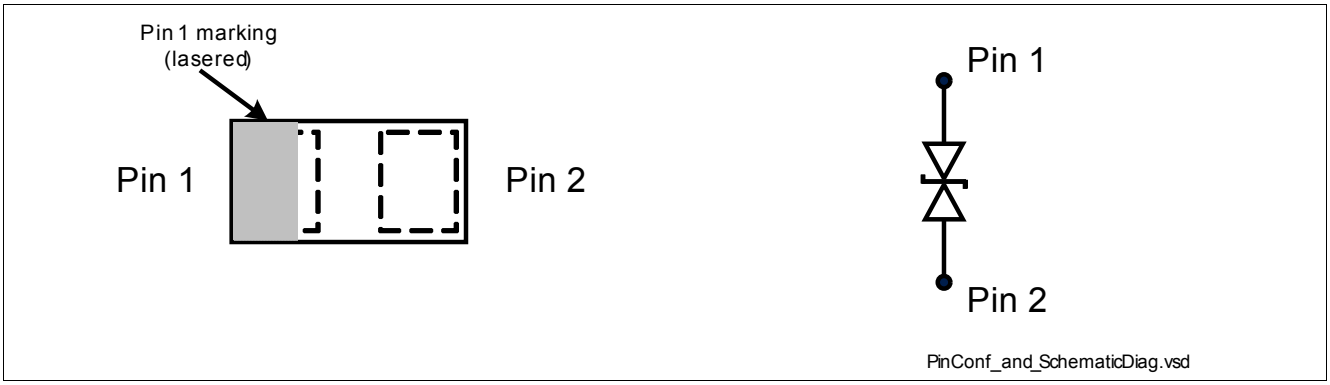

Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD218-B1-02ELS	TSSLP-2-4	1 line, bi-directional	4
ESD218-B1-02EL	TSLP-2-20	1 line, bi-directional	AA

2 Maximum Ratings

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values	Unit
ESD air discharge[2)] ESD contact discharge[2)]	V_{ESD}	±20 ±18	kV
Peak pulse power[3)]	P_{PK}	67	W
Peak pulse current[3)]	I_{PP}	±1.5	A
Operating temperature range	T_{OP}	-55 to 150	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical
2) V_{ESD} according to IEC61000-4-2
3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics

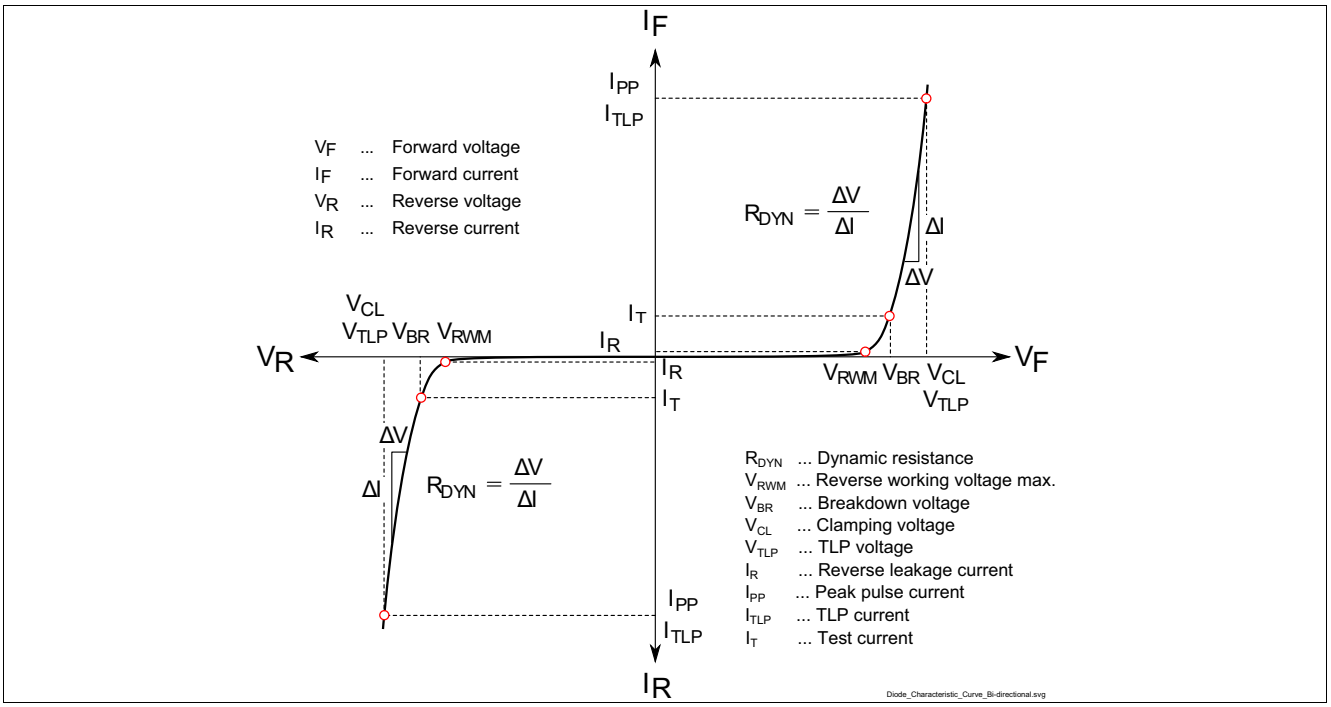

Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-24	–	24	V	
Breakdown voltage	V_{BR}	24.3	25.5	30	V	I_T = 1 mA
Reverse leakage current	I_R	–	<1	50	nA	V_R = 24 V

1) Device is electrically symmetrical

Table 3-2 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	– –	3 3	3.5 3.5	pF	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz
Series inductance	L_S	– –	0.2 0.4	– –	nH	ESD218-B1-02ELS ESD218-B1-02EL

Table 3-3 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	–	51	55.5	V	I_{TLP} = 16 A, t_p = 100 ns
		–	66	70.5		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage[3)]		–	37	41.5		I_{PP} = 1 A, t_p = 8/20 µs
			40	44.5		I_{PP} = 1.5 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	–	0.9	–	Ω	t_p = 100 ns

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps.

3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

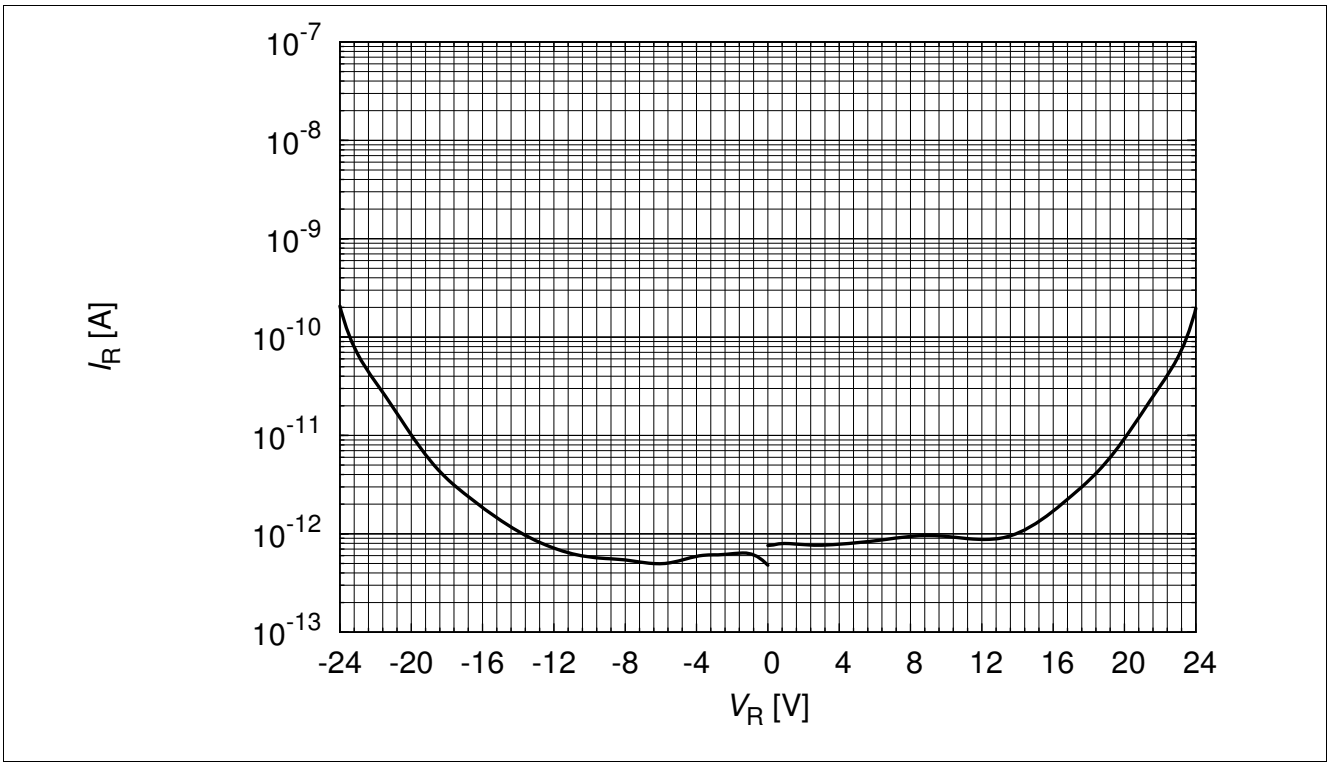

Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

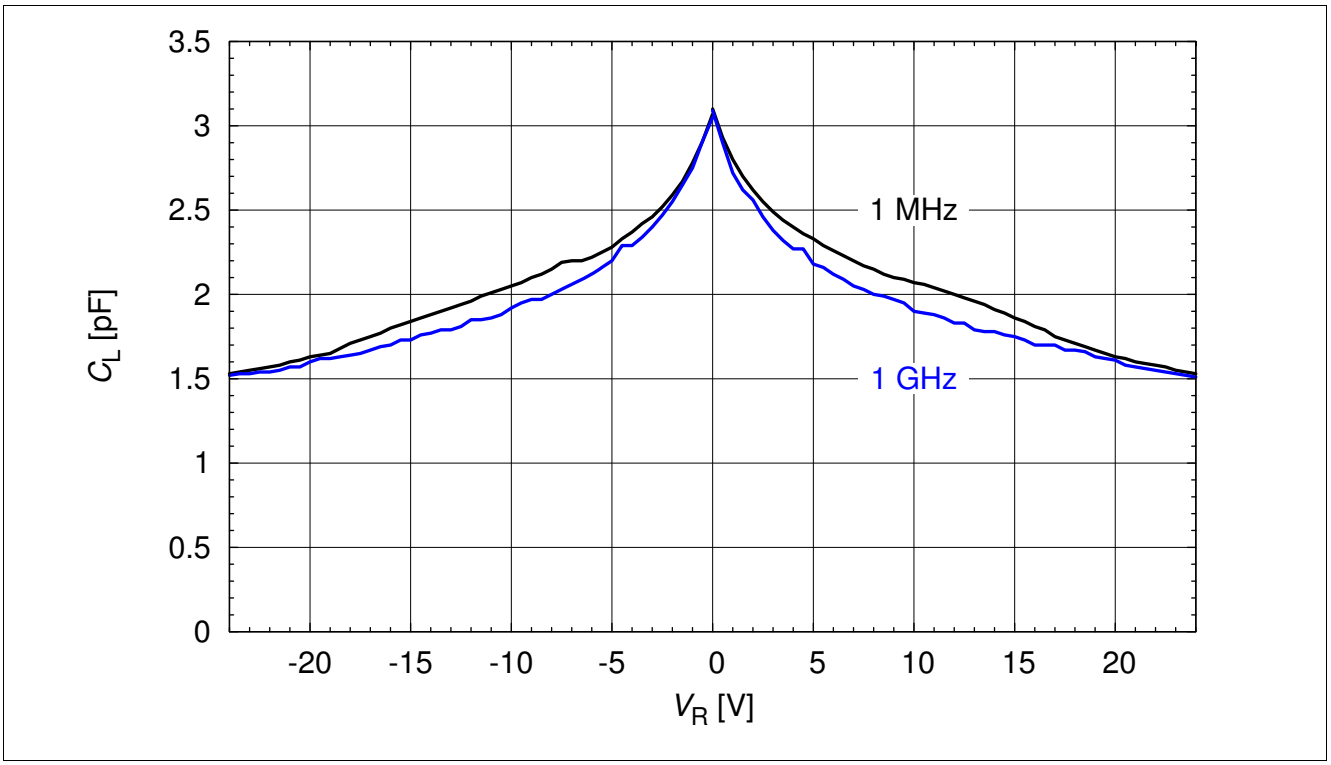

Figure 4-2 Line capacitance: $C_L = f(V_R)$

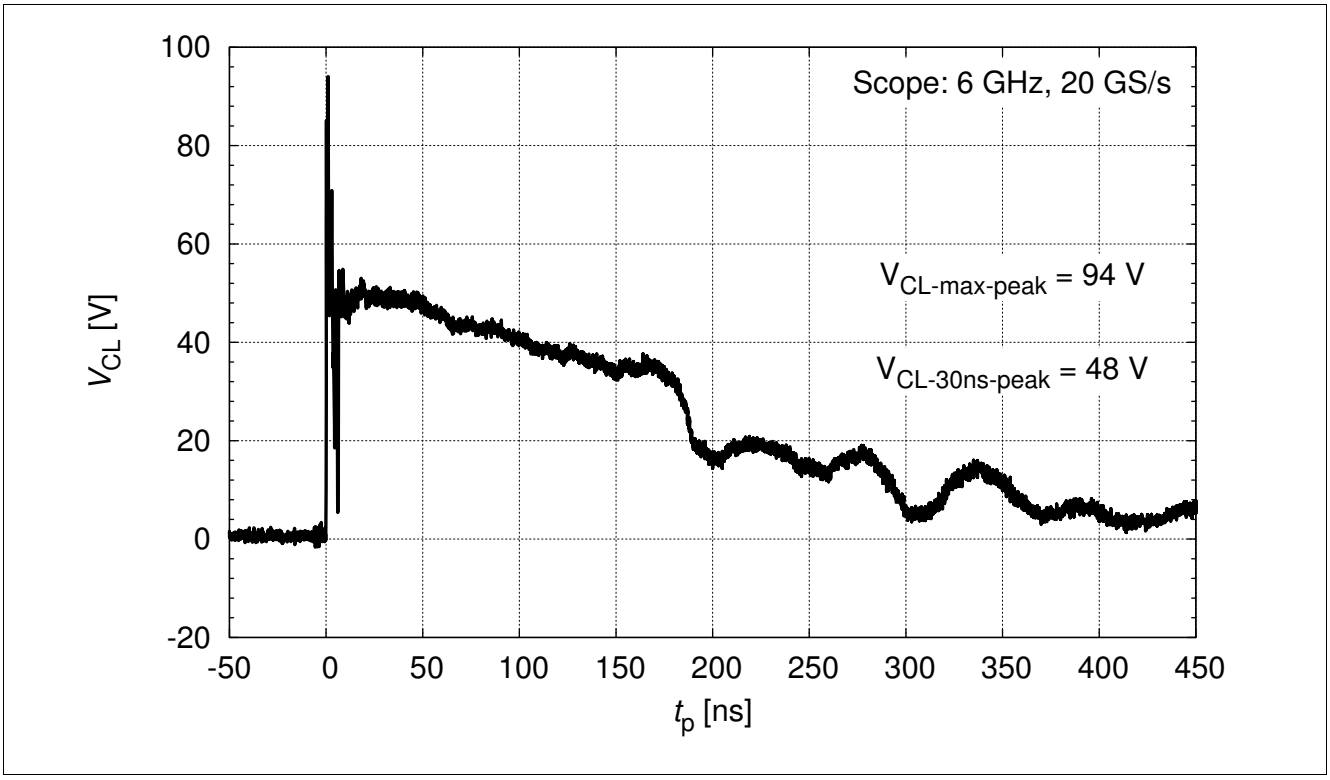

Figure 4-3 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

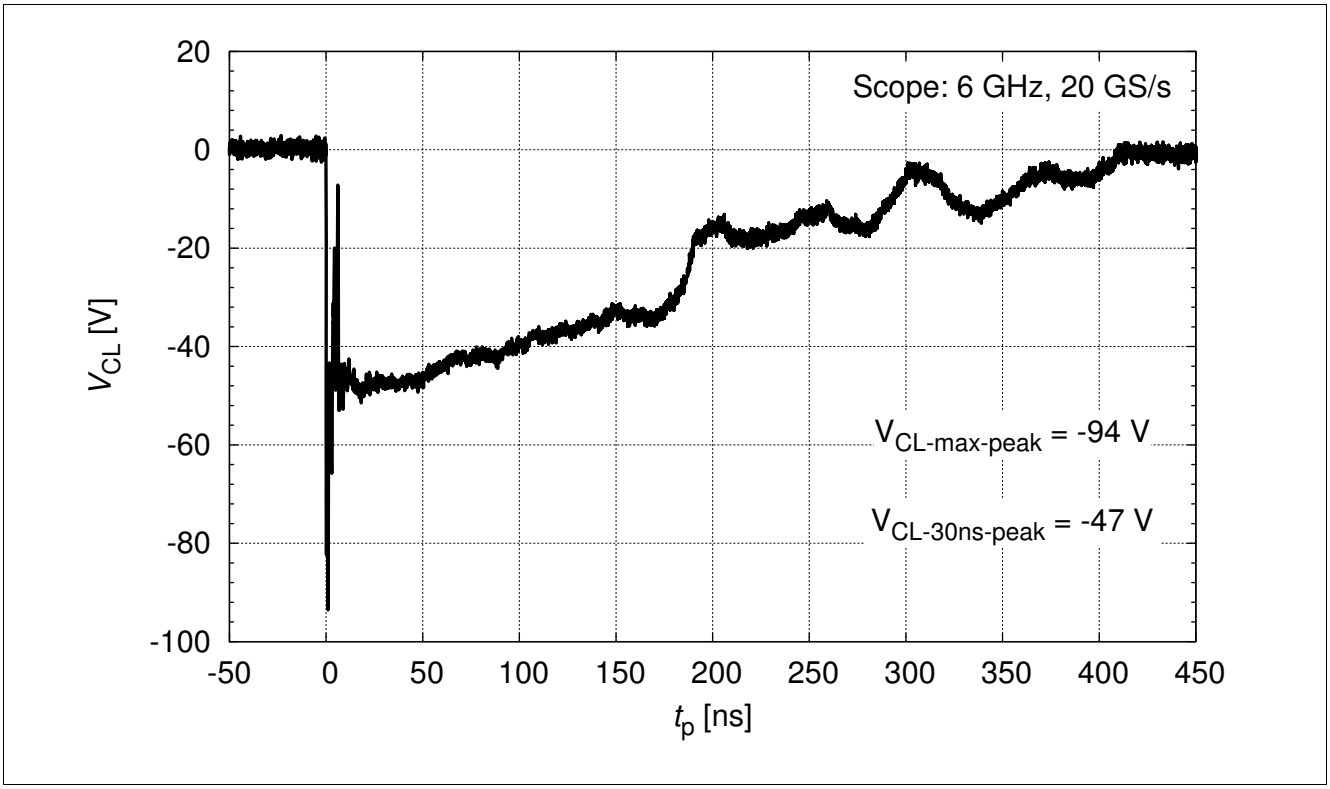

Figure 4-4 Clamping voltage (ESD) $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

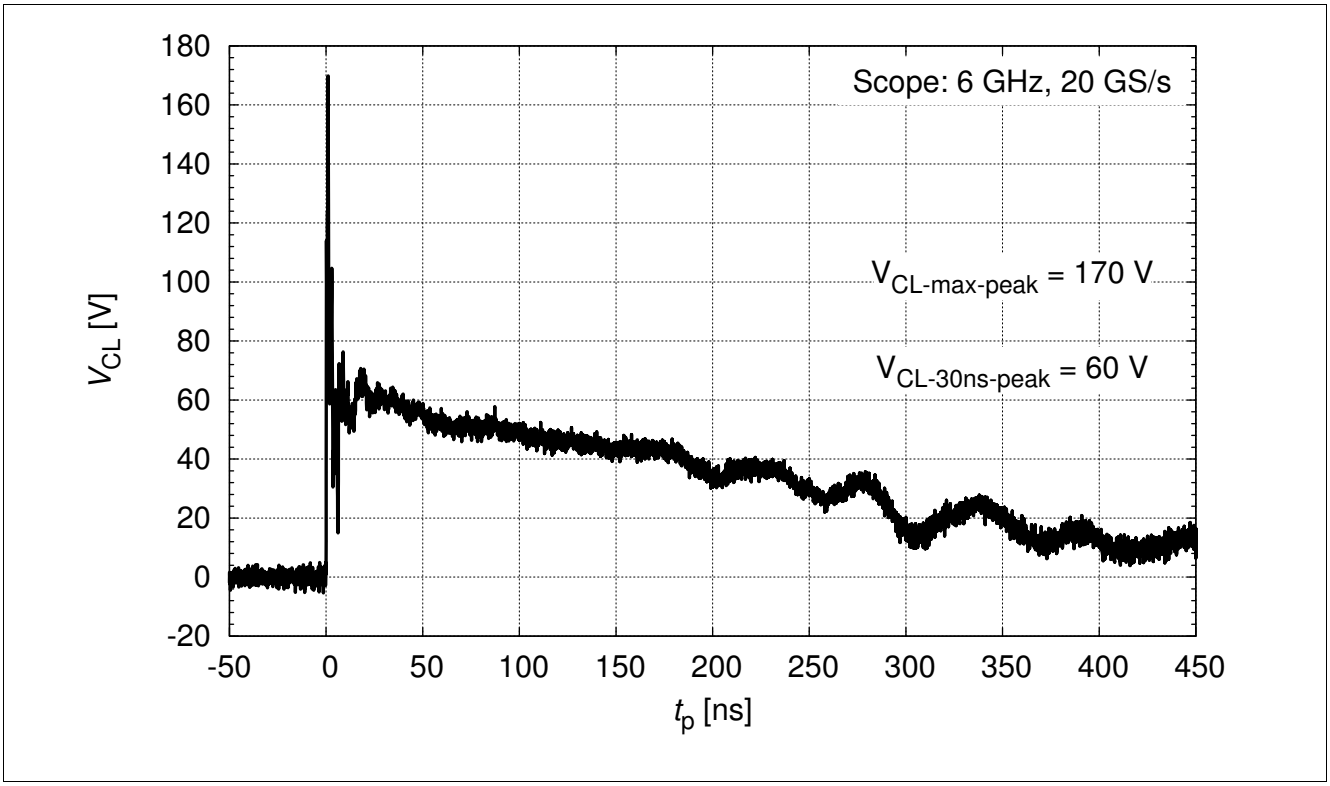

Figure 4-5 Clamping voltage (ESD) $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

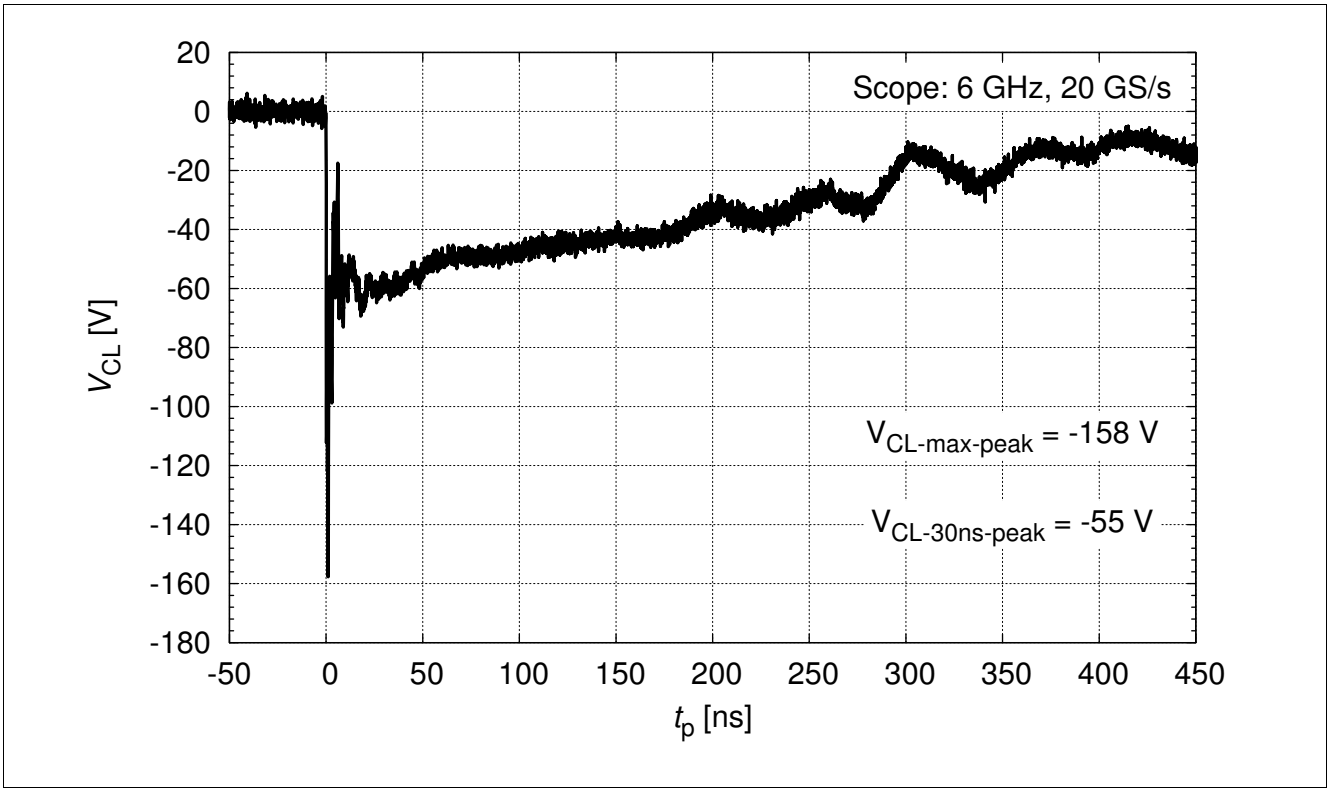

Figure 4-6 Clamping voltage (ESD) $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

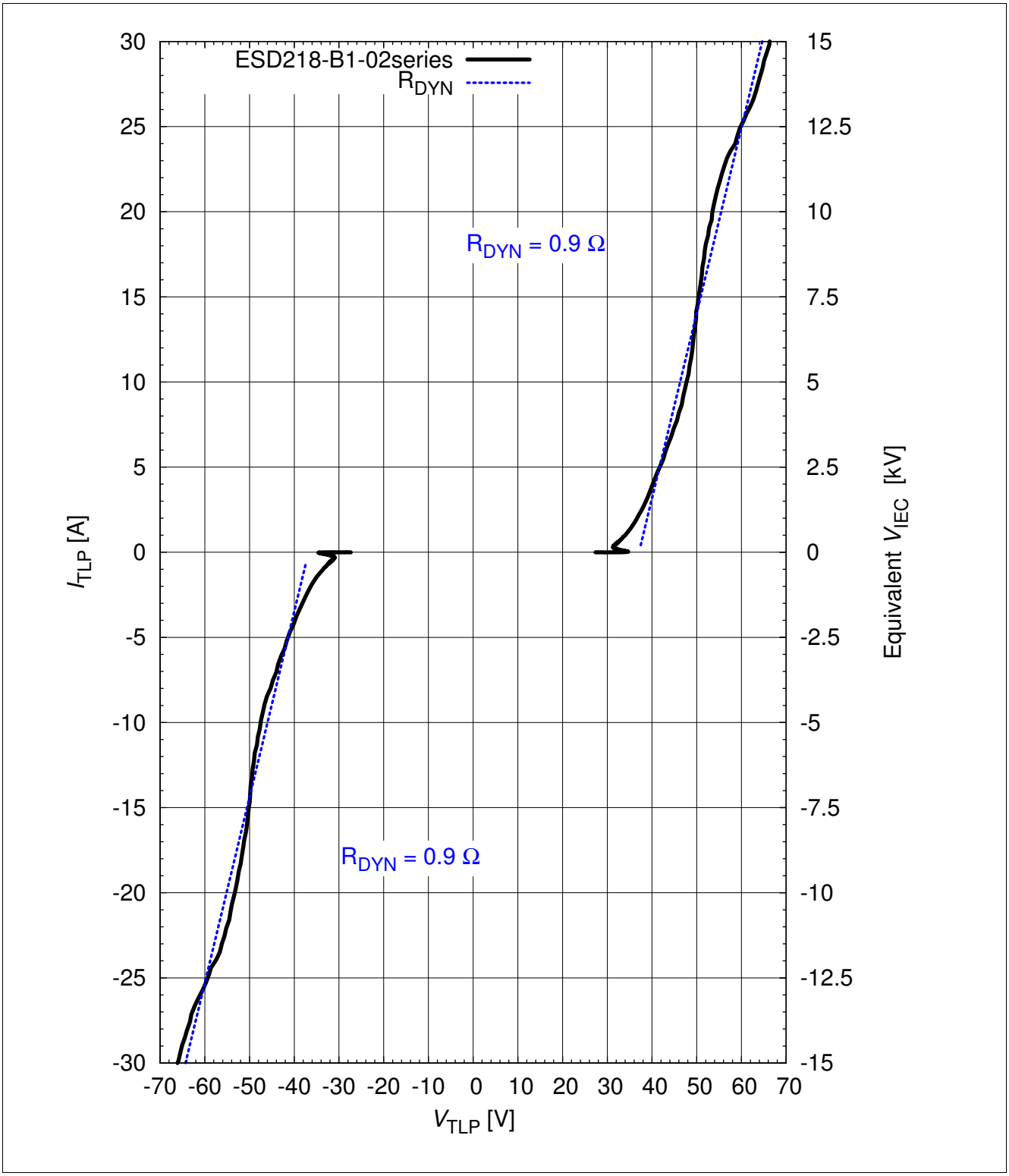

Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$[1], pin 2 to pin 1

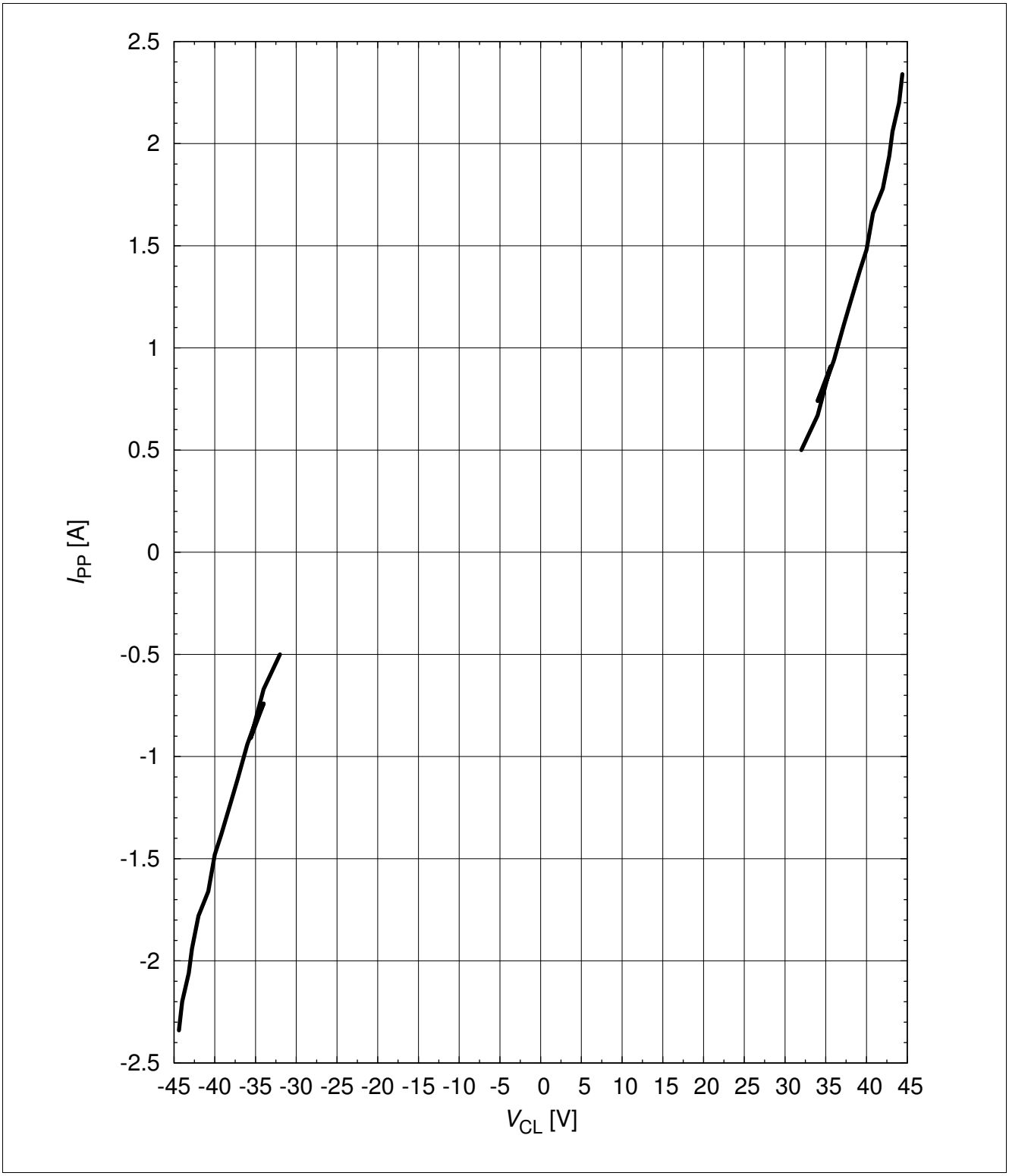

Figure 4-8 Clamping voltage(Surge): $I_{PP} = f(V_{CL})$[1]

5 Package Information

5.1 TSSLP-2-4

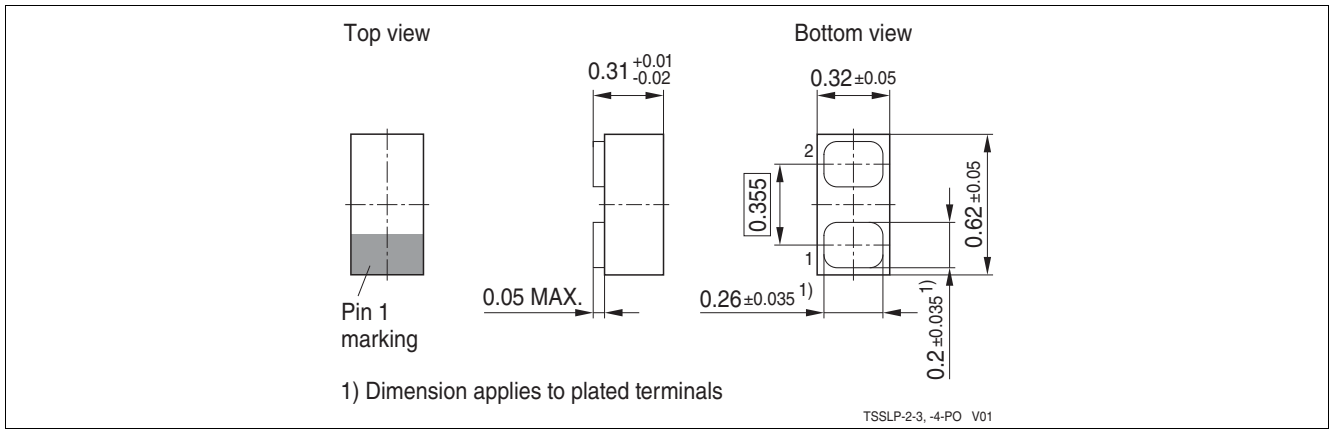

Figure 5-1 TSSLP-2-4 Package outline

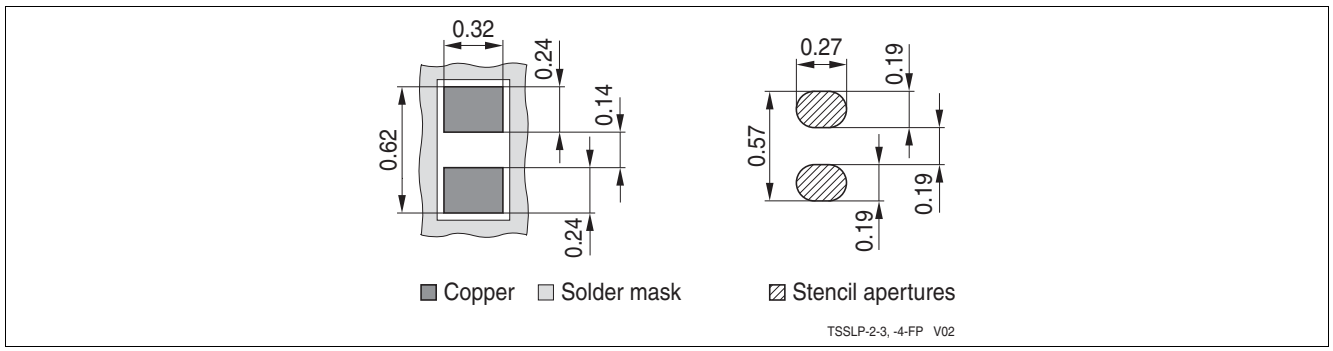

Figure 5-2 TSSLP-2-4 Footprint

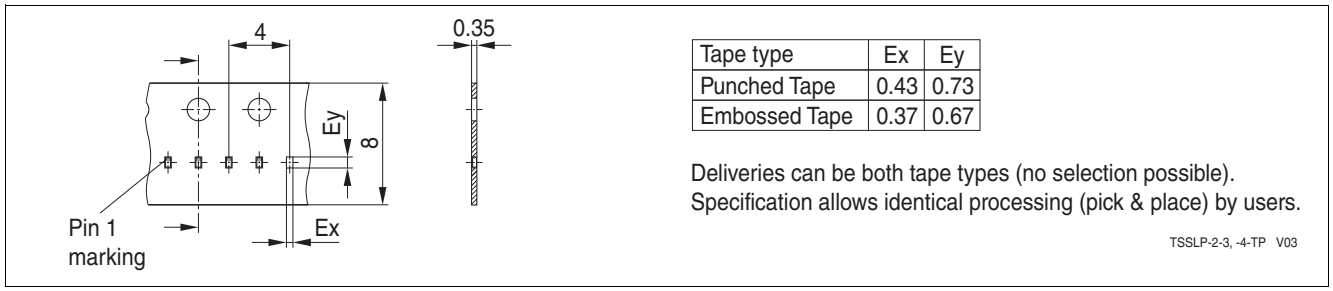

Figure 5-3 TSSLP-2-4 Packing

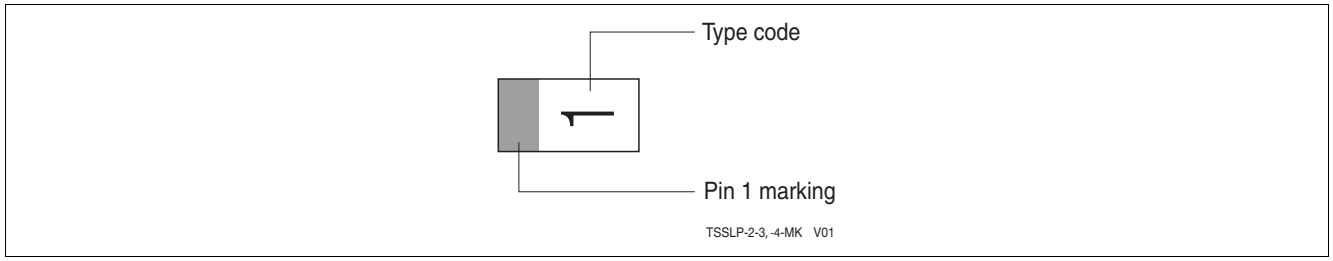

Figure 5-4 TSSLP-2-4 Marking example, Type code see: Table 1-1 “Part Information” on Page 3

5.2 TSLP-2-20

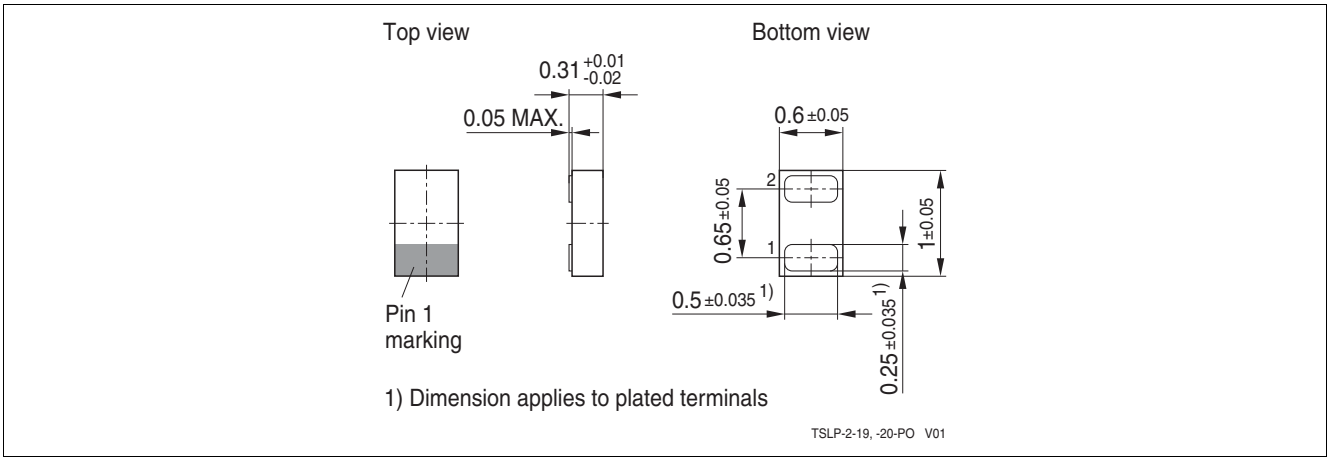

Figure 5-5 TSLP-2-20 Package outline

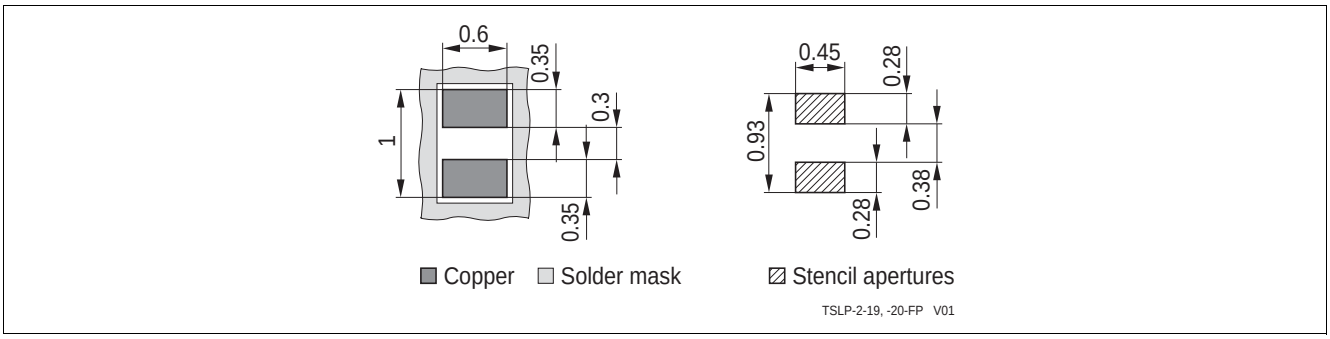

Figure 5-6 TSLP-2-20 Footprint

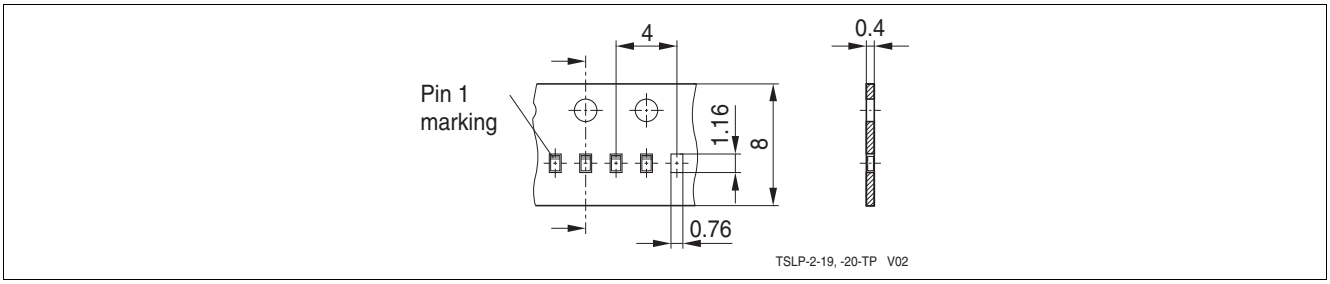

Figure 5-7 TSLP-2-20 Packing

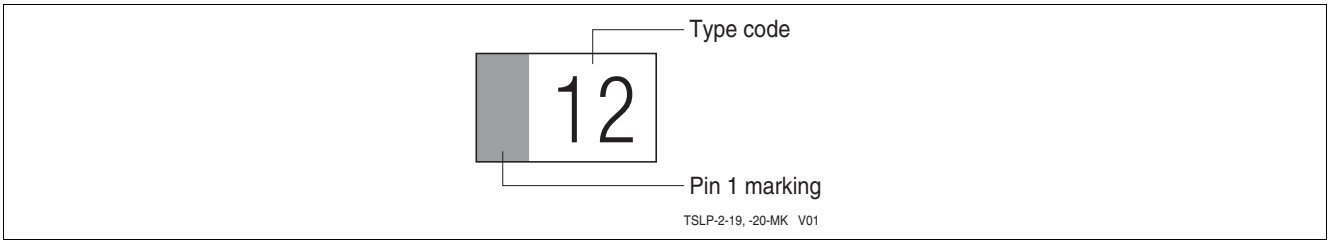

Figure 5-8 TSLP-2-20 Marking example, Type code see: Table 1-1 “Part Information” on Page 3

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

Revision History: Rev. 1.0, 2014-04-08	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2015-01-13	
11	Correction of Footprint drawing

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