



# THE DATASHEET OF SZP6SMB36CAT3G



# P6SMB11CAT3G Series, SZP6SMB11CAT3G Series

## 600 Watt Peak Power Zener Transient Voltage Suppressors

### Bidirectional\*

The SMB series is designed to protect voltage sensitive components from high voltage, high energy transients. They have excellent clamping capability, high surge capability, low zener impedance and fast response time. The SMB series is supplied in ON Semiconductor's exclusive, cost-effective, highly reliable SURMETIC® package and is ideally suited for use in communication systems, automotive, numerical controls, process controls, medical equipment, business machines, power supplies and many other industrial/consumer applications.

#### Features

- Working Peak Reverse Voltage Range – 9.4 to 77.8 V
- Standard Zener Breakdown Voltage Range – 11 to 91 V
- Peak Power – 600 W @ 1 ms
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- Maximum Clamp Voltage @ Peak Pulse Current
- Low Leakage < 5  $\mu$ A Above 10 V
- UL 497B for Isolated Loop Circuit Protection
- Response Time is Typically < 1 ns
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices\*

#### Mechanical Characteristics:

**CASE:** Void-Free, Transfer-Molded, Thermosetting Plastic

**FINISH:** All External Surfaces are Corrosion Resistant and Leads are Readily Solderable

**MAXIMUM CASE TEMPERATURE FOR SOLDERING PURPOSES:** 260°C for 10 Seconds

**LEADS:** Modified L-Bend Providing More Contact Area to Bond Pads

**POLARITY:** Polarity Band Will Not be Indicated

**MOUNTING POSITION:** Any

\*Please see P6SMB6.8AT3 to P6SMB200AT3 for Unidirectional devices.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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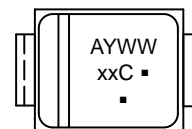
**PLASTIC SURFACE MOUNT  
ZENER OVERVOLTAGE  
TRANSIENT SUPPRESSORS  
9.4–78 VOLTS  
600 WATT PEAK POWER**



**SMB  
CASE 403A  
PLASTIC**



#### MARKING DIAGRAM



xxC = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
P6SMBxxCAT3G	SMB (Pb-Free)	2,500 / Tape & Reel
SZP6SMBxxCAT3G	SMB (Pb-Free)	2,500 / Tape & Reel

The "T3" suffix refers to a 13 inch reel.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1) @ $T_L = 25^\circ\text{C}$ , Pulse Width = 1 ms	$P_{PK}$	600	W
DC Power Dissipation @ $T_L = 75^\circ\text{C}$ Measured Zero Lead Length (Note 2) Derate Above $75^\circ\text{C}$	$P_D$	3.0	W
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	40	$\text{mW}/^\circ\text{C}$
		25	$^\circ\text{C}/\text{W}$
DC Power Dissipation (Note 3) @ $T_A = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	0.55	W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	4.4	$\text{mW}/^\circ\text{C}$
		226	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

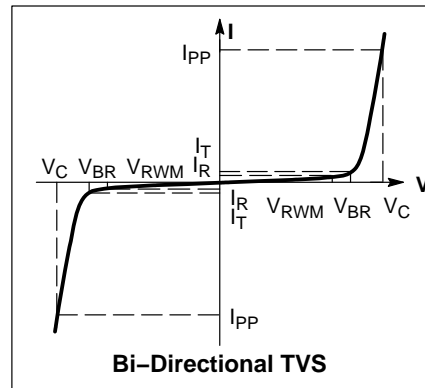
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 10 X 1000  $\mu\text{s}$ , non-repetitive
- 1" square copper pad, FR-4 board
- FR-4 board, using ON Semiconductor minimum recommended footprint, as shown in 403A case outline dimensions spec.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$\Theta V_{BR}$	Maximum Temperature Coefficient of $V_{BR}$



## ELECTRICAL CHARACTERISTICS (Devices listed in bold, italic are ON Semiconductor Preferred devices.)

Device*	Device Marking	$V_{RWM}$ (Note 4) Volts	$I_R$ @ $V_{RWM}$ $\mu\text{A}$	Breakdown Voltage				$V_C$ @ $I_{PP}$ (Note 6)		$\Theta V_{BR}$ %/°C	$C_{typ}$ (Note 7) pF
				$V_{BR}$ Volts (Note 5)			@ $I_T$	$V_C$	$I_{PP}$		
				Min	Nom	Max	mA	Volts	Amps		
P6SMB11CAT3G	11C	9.4	5	10.5	11.05	11.6	1	15.6	38	0.075	865
P6SMB12CAT3G	12C	10.2	5	11.4	12	12.6	1	16.7	36	0.078	800
P6SMB15CAT3G	15C	12.8	5	14.3	15.05	15.8	1	21.2	28	0.084	645
P6SMB16CAT3G	16C	13.6	5	15.2	16	16.8	1	22.5	27	0.086	610
P6SMB18CAT3G	18C	15.3	5	17.1	18	18.9	1	25.2	24	0.088	545
P6SMB20CAT3G	20C	17.1	5	19	20	21	1	27.7	22	0.09	490
P6SMB22CAT3G	22C	18.8	5	20.9	22	23.1	1	30.6	20	0.09	450
P6SMB24CAT3G	24C	20.5	5	22.8	24	25.2	1	33.2	18	0.094	415
P6SMB27CAT3G	27C	23.1	5	25.7	27.05	28.4	1	37.5	16	0.096	370
P6SMB30CAT3G	30C	25.6	5	28.5	30	31.5	1	41.4	14.4	0.097	335
P6SMB33CAT3G	33C	28.2	5	31.4	33.05	34.7	1	45.7	13.2	0.098	305
P6SMB36CAT3G	36C	30.8	5	34.2	36	37.8	1	49.9	12	0.099	280
P6SMB39CAT3G	39C	33.3	5	37.1	39.05	41	1	53.9	11.2	0.1	260
P6SMB43CAT3G	43C	36.8	5	40.9	43.05	45.2	1	59.3	10.1	0.101	240
P6SMB47CAT3G	47C	40.2	5	44.7	47.05	49.4	1	64.8	9.3	0.101	220
P6SMB51CAT3G	51C	43.6	5	48.5	51.05	53.6	1	70.1	8.6	0.102	205
P6SMB56CAT3G	56C	47.8	5	53.2	56	58.8	1	77	7.8	0.103	185
P6SMB62CAT3G	62C	53	5	58.9	62	65.1	1	85	7.1	0.104	170
P6SMB68CAT3G	68C	58.1	5	64.6	68	71.4	1	92	6.5	0.104	155
P6SMB82CAT3G	82C	70.1	5	77.9	82	86.1	1	113	5.3	0.105	130

- A transient suppressor is normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal to or greater than the DC or continuous peak operating voltage level.
  - $V_{BR}$  measured at pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .
  - Surge current waveform per Figure 2 and derate per Figure 3 of the General Data – 600 Watt at the beginning of this group.
  - Bias Voltage = 0 V, F = 1 MHz,  $T_J = 25^\circ\text{C}$
- \*Include SZ-prefix devices where applicable.

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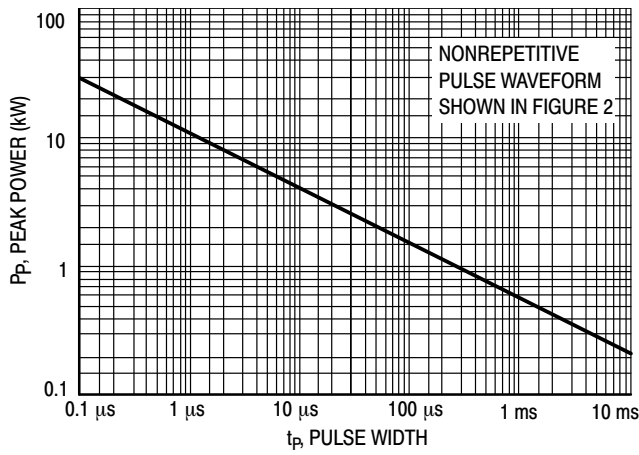


Figure 1. Pulse Rating Curve

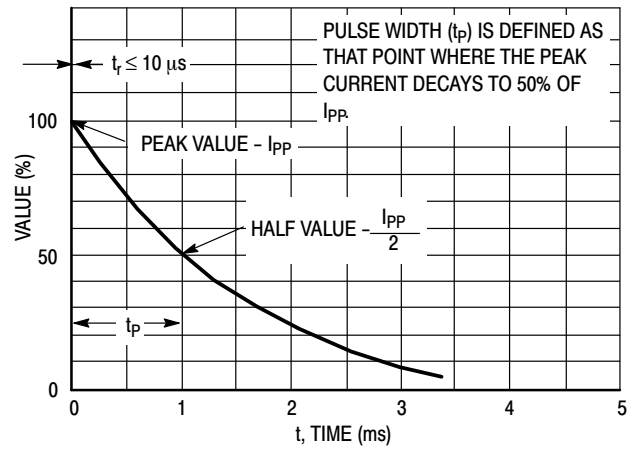


Figure 2. Pulse Waveform

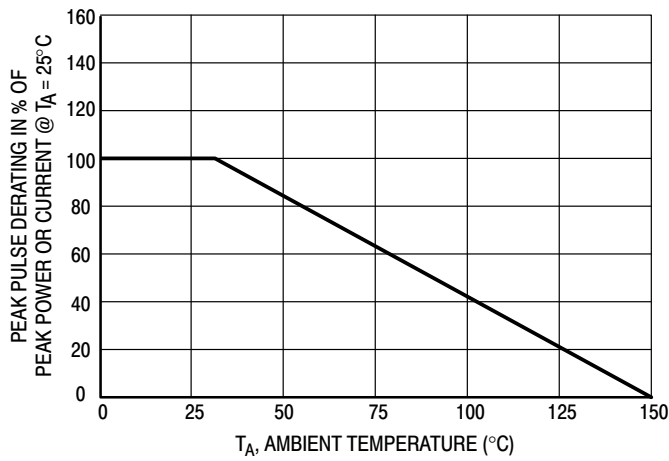


Figure 3. Pulse Derating Curve

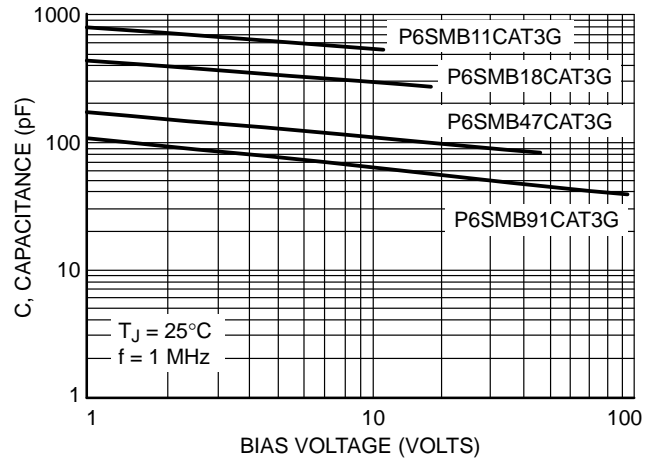
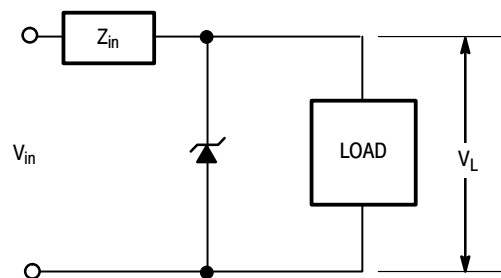


Figure 4. Typical Junction Capacitance vs. Bias Voltage

## TYPICAL PROTECTION CIRCUIT



APPLICATION NOTES

**Response Time**

In most applications, the transient suppressor device is placed in parallel with the equipment or component to be protected. In this situation, there is a time delay associated with the capacitance of the device and an overshoot condition associated with the inductance of the device and the inductance of the connection method. The capacitive effect is of minor importance in the parallel protection scheme because it only produces a time delay in the transition from the operating voltage to the clamp voltage as shown in Figure 4.

The inductive effects in the device are due to actual turn-on time (time required for the device to go from zero current to full current) and lead inductance. This inductive effect produces an overshoot in the voltage across the equipment or component being protected as shown in Figure 5. Minimizing this overshoot is very important in the application, since the main purpose for adding a transient suppressor is to clamp voltage spikes. The SMB series have a very good response time, typically < 1 ns and negligible inductance. However, external inductive effects could produce unacceptable overshoot. Proper circuit layout, minimum lead lengths and placing the

suppressor device as close as possible to the equipment or components to be protected will minimize this overshoot.

Some input impedance represented by  $Z_{in}$  is essential to prevent overstress of the protection device. This impedance should be as high as possible, without restricting the circuit operation.

**Duty Cycle Derating**

The data of Figure 1 applies for non-repetitive conditions and at a lead temperature of 25°C. If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 6. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

At first glance the derating curves of Figure 6 appear to be in error as the 10 ms pulse has a higher derating factor than the 10 μs pulse. However, when the derating factor for a given pulse of Figure 6 is multiplied by the peak power value of Figure 1 for the same pulse, the results follow the expected trend.

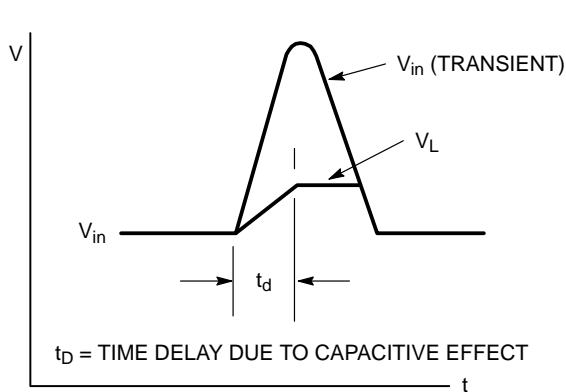


Figure 5.

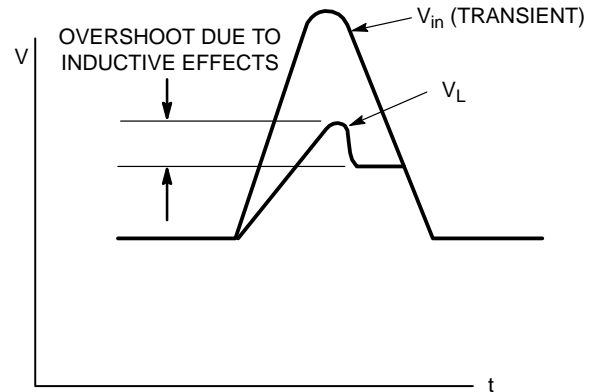


Figure 6.

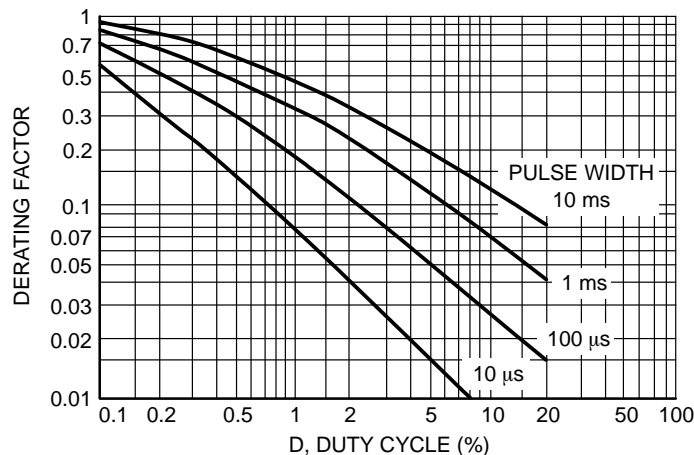


Figure 7. Typical Derating Factor for Duty Cycle

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### UL RECOGNITION

The entire series has *Underwriters Laboratory Recognition* for the classification of protectors (QVGQ2) under the UL standard for safety 497B and File #E210057. Many competitors only have one or two devices recognized or have recognition in a non-protective category. Some competitors have no recognition at all. With the UL497B recognition, our parts successfully passed several tests

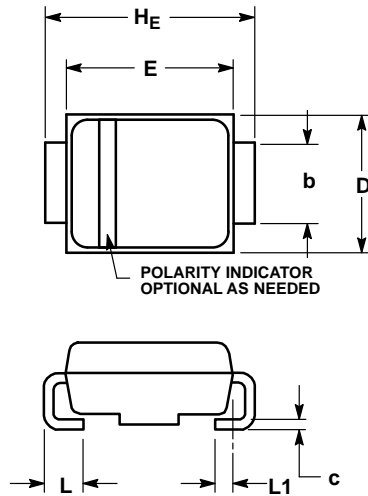
including Strike Voltage Breakdown test, Endurance Conditioning, Temperature test, Dielectric Voltage-Withstand test, Discharge test and several more.

Whereas, some competitors have only passed a flammability test for the package material, we have been recognized for much more to be included in their Protector category.

# P6SMB11CAT3G Series, SZP6SMB11CAT3G Series

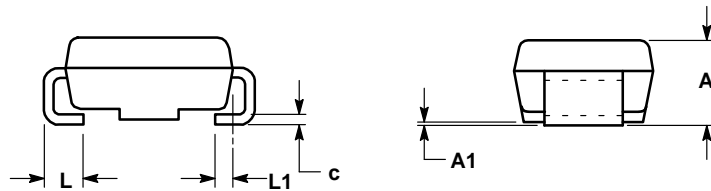
## PACKAGE DIMENSIONS

### SMB CASE 403A-03 ISSUE J

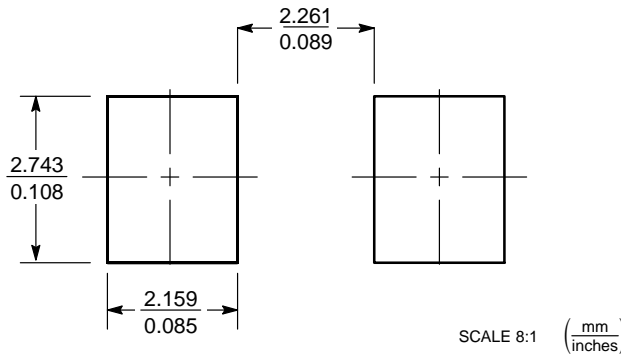


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION b SHALL BE MEASURED WITHIN DIMENSION L1.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.95	2.30	2.47	0.077	0.091	0.097
A1	0.05	0.10	0.20	0.002	0.004	0.008
b	1.96	2.03	2.20	0.077	0.080	0.087
c	0.15	0.23	0.31	0.006	0.009	0.012
D	3.30	3.56	3.95	0.130	0.140	0.156
E	4.06	4.32	4.60	0.160	0.170	0.181
HE	5.21	5.44	5.60	0.205	0.214	0.220
L	0.76	1.02	1.60	0.030	0.040	0.063
L1	0.51 REF			0.020 REF		



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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