



THE DATASHEET OF TPI8011NRL



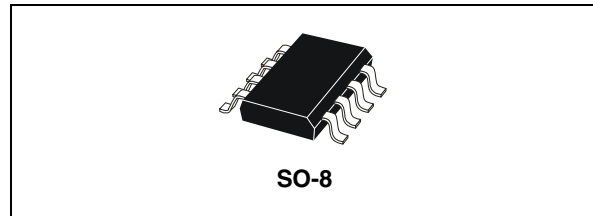
Tripolar protection for ISDN interfaces

Features

- Bidirectional triple crowbar protection
- Peak pulse current:
 $I_{PP} = 30 \text{ A}$, 10/1000 μs
- Breakdown voltage:
 - TPI80N: 80 V
 - TPI120N: 120 V
- Available in SO-8 package
- Low dynamic breakover voltage:
 - TPI8011N: 120 V
 - TPI12011N: 170 V

Benefits

- Low capacitance from lines to ground, allowing high speed transmission without signal attenuation
- Good capacitance balance between lines to ensure longitudinal balance
- Fixed breakdown voltage in both common and differential modes
- The same surge current capability in both common and differential modes
- A particular attention has been given to the internal wire bonding. The “4-point” configuration ensures a reliable protection, eliminating overvoltages introduced by the parasitic inductances of the wiring (Ld/dt), especially for very fast transient overvoltages



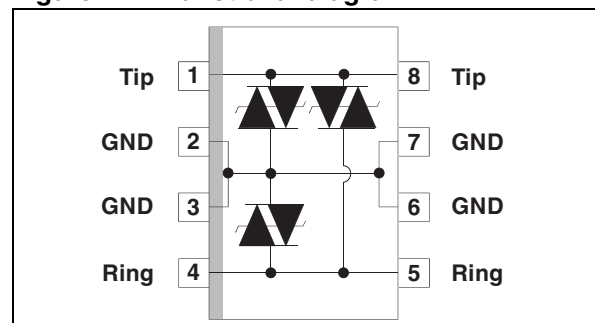
Complies with following standards

- CCITT K17-K20
 - 10/700 μs , 1.5 kV
 - 5/310 μs , 38 A
- VDE 0433
 - 10/700 μs , 2 kV
 - 5/310 μs , 50 A
- VDE 0878
 - 1.2/50 μs , 1.5 kV
 - 1/20 μs , 40 A
- IEC 61000-4-2 level 4
 - 0.5/700 μs , 1.5 kV
 - 0.2/310 μs , 38 A

Description

Dedicated devices for **ISDN** interface and high speed data telecom line protection. Equivalent to a triple Trisil™ with low capacitance.

Figure 1. Functional diagram



TM: Trisil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
I_{PP}	Peak pulse current (see note ⁽¹⁾)	10/1000 μs	30
		5/310 μs	40
		2/10 μs	90
I_{TSM}	Non repetitive surge peak on-state current ($F = 50\text{ Hz}$)	$t_p = 10\text{ ms}$	8
		$t = 1\text{ s}$	3.5
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Maximum junction temperature	150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s.	260	$^{\circ}\text{C}$

1. See [Figure 3](#).

Table 2. Thermal resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient	170	$^{\circ}\text{C/W}$

Table 3. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter							
V_{RM}	Stand-off voltage							
V_{BR}	Breakdown voltage							
V_{BO}	Breakover voltage							
I_{RM}	Leakage current							
I_{PP}	Peak pulse current							
I_{BO}	Breakover current							
I_H	Holding current							
V_F	Forward voltage drop							
C	Capacitance							
Order code	$I_{RM} @ V_{RM}$							
	max.		min.		max. note ⁽¹⁾	typ. note ⁽²⁾	max. note ⁽¹⁾	min. note ⁽³⁾
	μA	V	V	mA	V	V	mA	mA
TPI8011N	10	70	80	1	110	120	800	150
TPI12011N	10	105	120	1	160	170	800	150

1. See the reference test circuit 1 ([Figure 5](#).)
2. Surge test according to CCITT 1.5 kV, 10/700 μs between Tip or Ring and ground
3. See functional holding current test circuit 2 ([Figure 6](#).)

Figure 2.

Table 4. Capacitance characteristics

CONFIGURATION	C _A (pF) max.	C _B (pF) max.	C _A - C _B (pF) max.
V _A = -1 V V _B = -56 V	45	15	30
V _A = -56 V V _B = -1 V	15	45	30

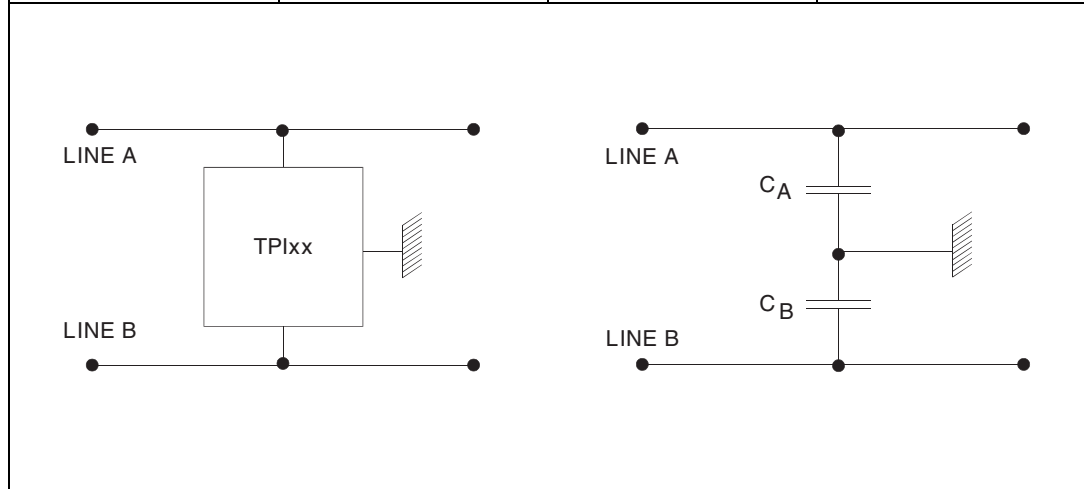


Figure 3. Pulse waveform (10/1000 μs)

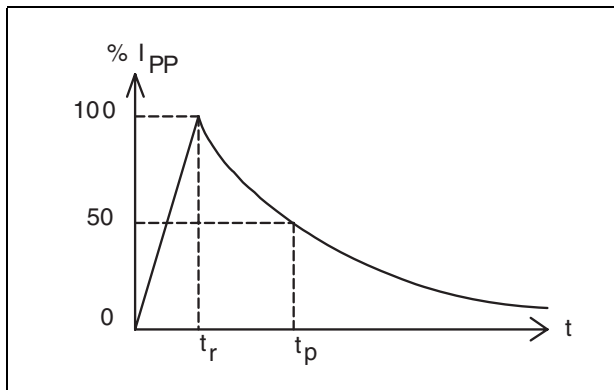


Figure 4. Surge peak current versus overload duration

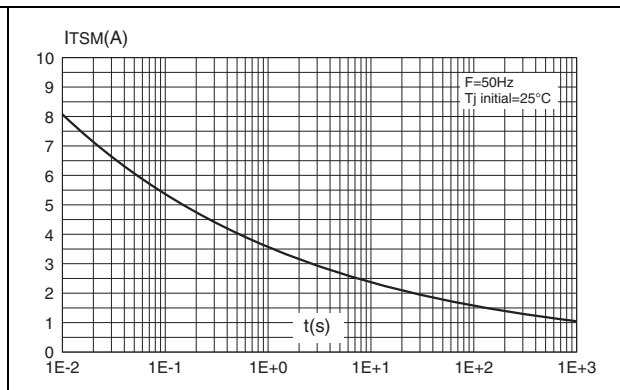


Figure 5. Reference test circuit 1

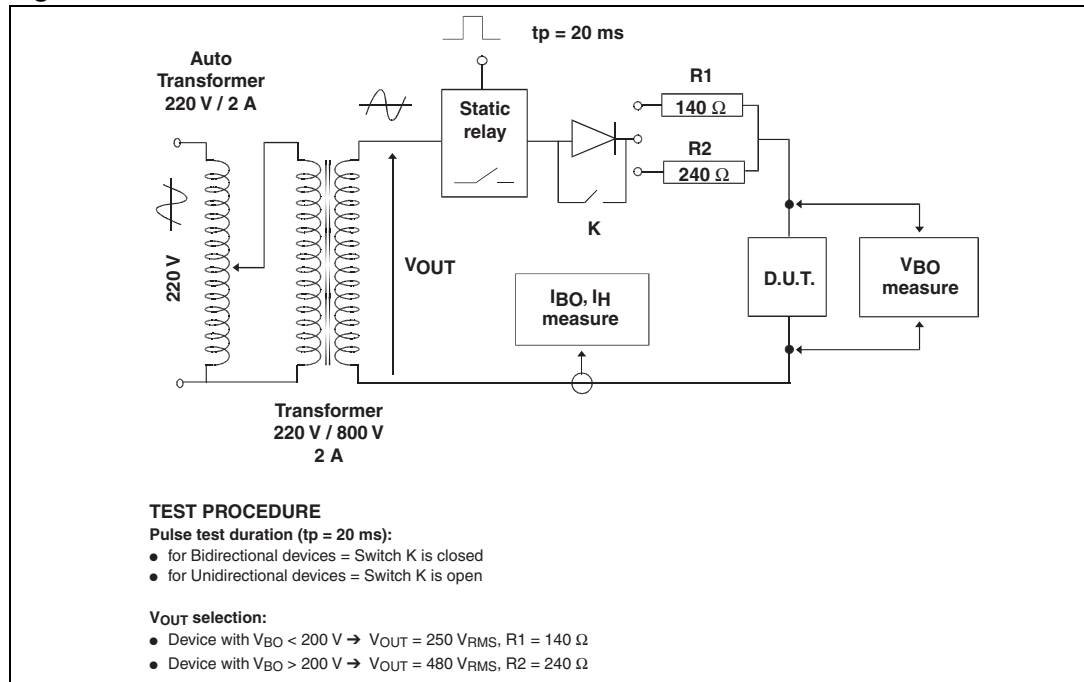
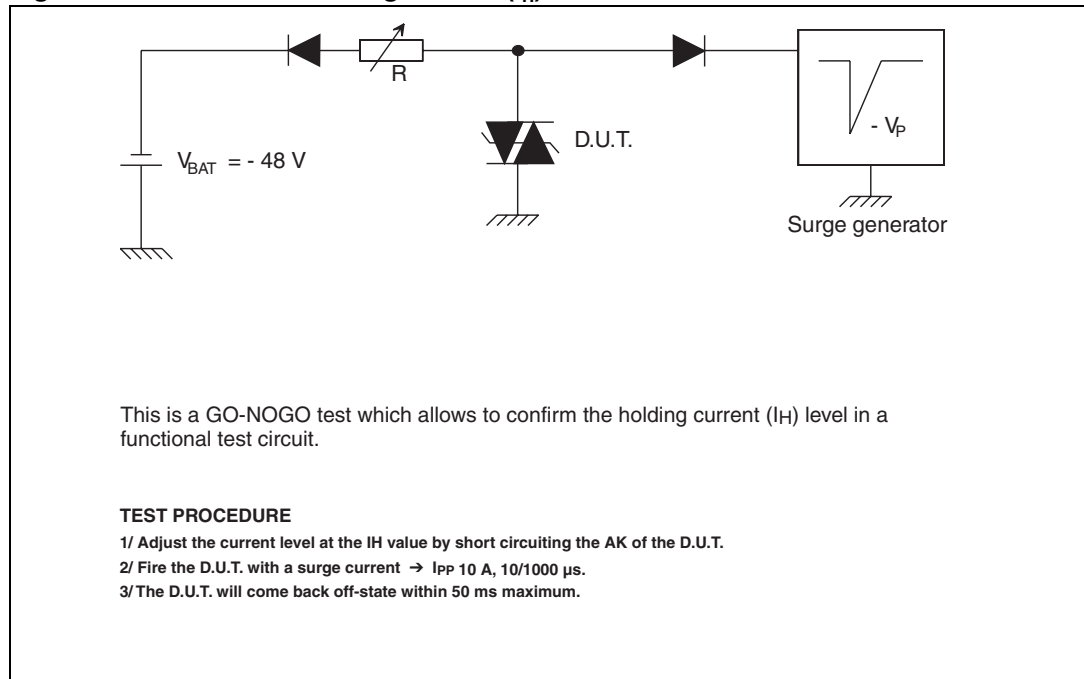


Figure 6. Functional holding current (I_H) test circuit 2



2 Application information

Figure 7. Application circuit - U interface protection

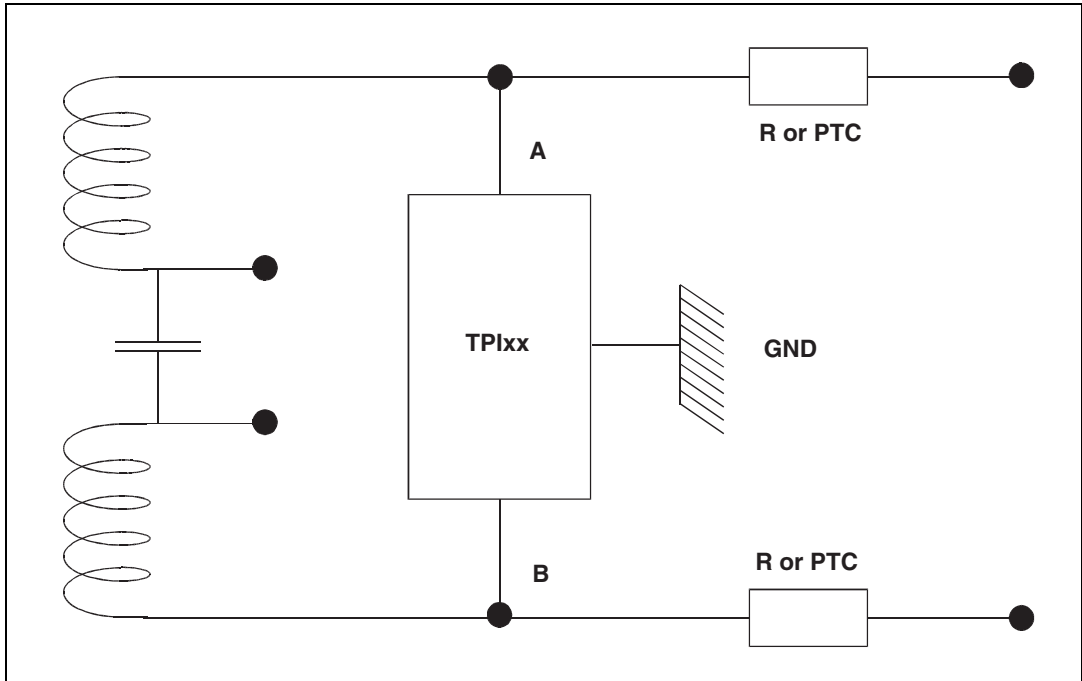
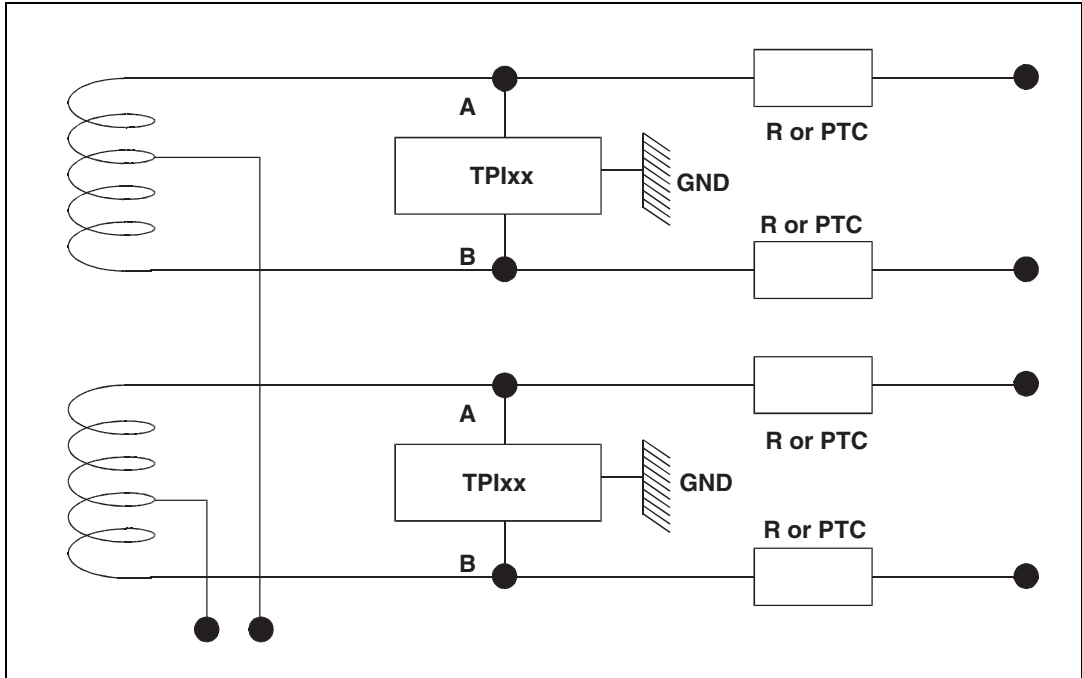
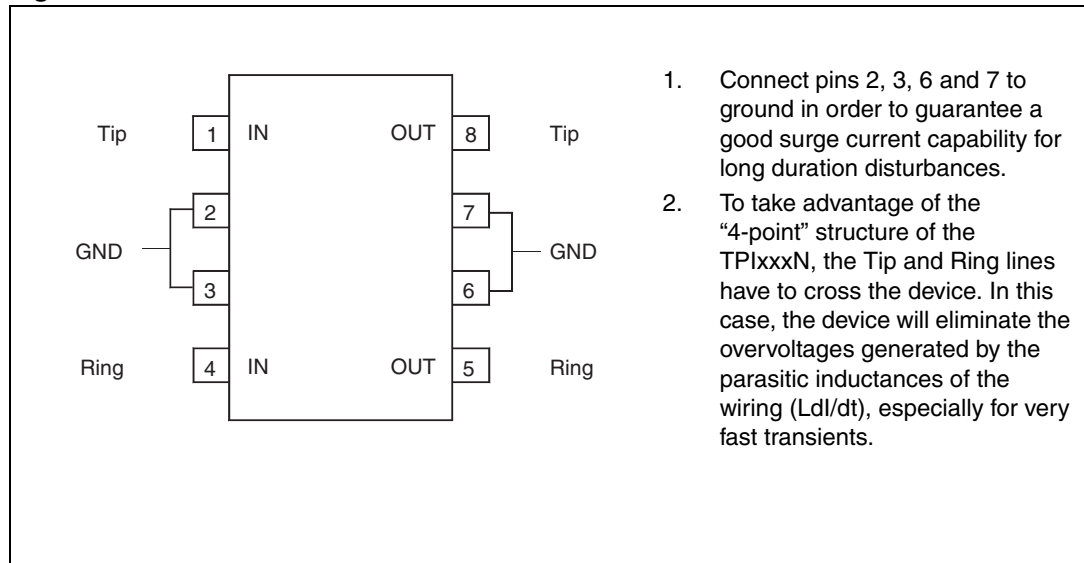


Figure 8. Application circuit - S interface protection



This component uses an internal structure resulting in symmetrical characteristics with a good balanced behaviour. Its topology ensures the same breakdown voltage level for positive and negative surges in differential and common mode.

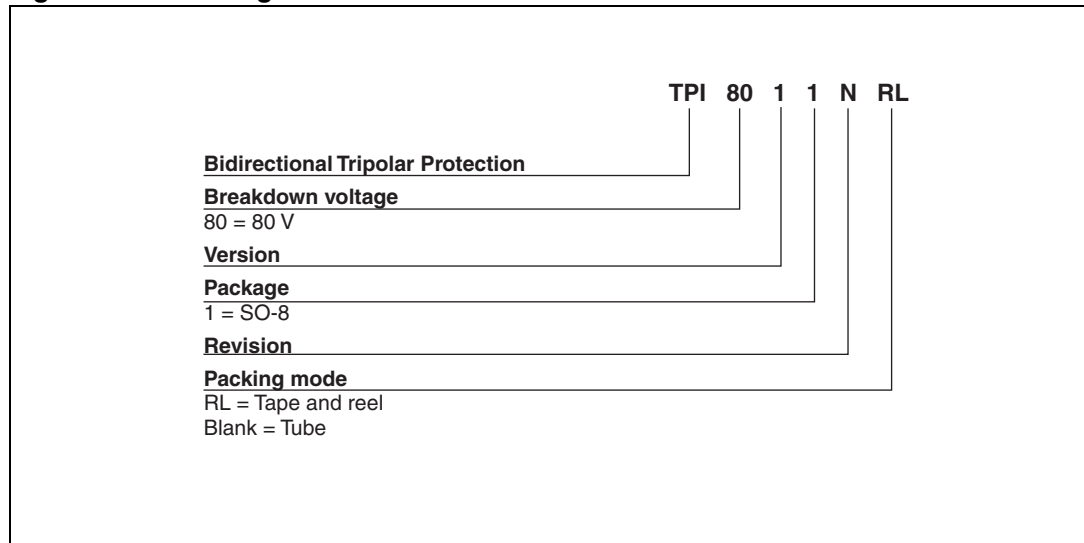
Figure 9. Connections



1. Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.
2. To take advantage of the "4-point" structure of the TPIxxxN, the Tip and Ring lines have to cross the device. In this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast transients.

3 Ordering information scheme

Figure 10. Ordering information scheme



4 Package information

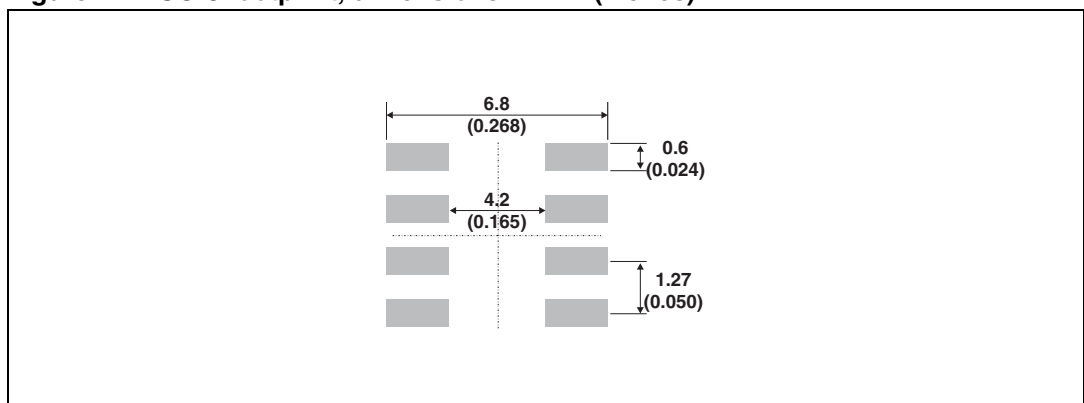
- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 5. SO-8 dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k	0°		8°	0°		8°
ppp			0.10			0.004

Figure 11. SO-8 footprint, dimensions in mm (inches)



5 Ordering Information

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
TPI8011N	TP80N	SO-8	0.08 g	100	Tube
TPI8011NRL ⁽¹⁾	TP80N			2500	Tape and reel
TPI12011N	TP120N			100	Tube
TPI12011NRL ⁽¹⁾	TP120N			2500	Tape and reel

1. Preferred device

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
August-2001	3A	Last update.
02-Aug-2004	4	V_{BO} dyn. (page 2) and capacitances (page 3) values update.
07-Nov-2007	5	Reformatted to current standards. Updated Package information .

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