



# THE DATASHEET OF STM703M6F



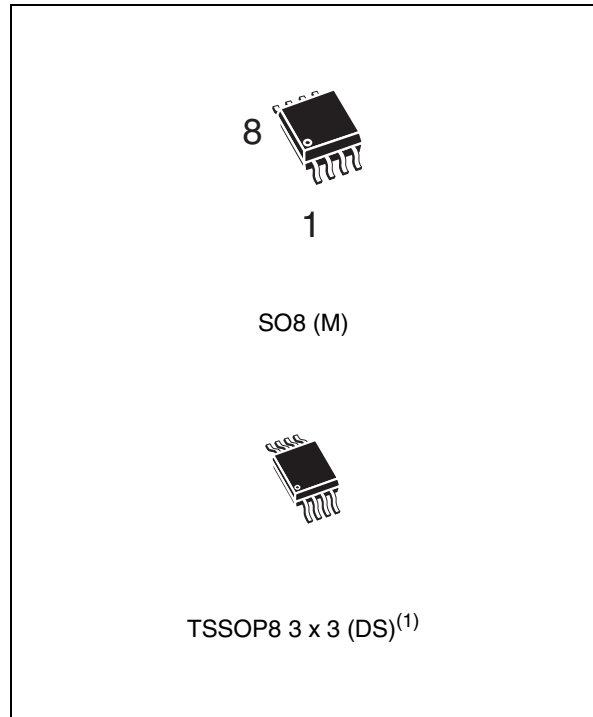


# STM690A, STM692A, STM703 STM704, STM802, STM805, STM817/8/9

## 5 V supervisor with battery switchover

### Features

- 5 V operating voltage
- NVRAM supervisor for external LPSRAM
- Chip-enable gating (STM818 only) for external LPSRAM (7 ns max prop delay)
- RST and  $\overline{\text{RST}}$  outputs
- 200 ms (typ)  $t_{\text{rec}}$
- Watchdog timer - 1.6 sec (typ)
- Automatic battery switchover
- Low battery supply current - 0.4  $\mu\text{A}$  (typ)
- Power-fail comparator (PFI/ $\overline{\text{PFO}}$ )
- Low supply current - 40  $\mu\text{A}$  (typ)
- Guaranteed  $\overline{\text{RST}}$  (RST) assertion down to  $V_{\text{CC}} = 1.0 \text{ V}$
- Operating temperature:  
-40 °C to +85 °C (industrial grade)
- RoHS compliance
  - Lead-free components are compliant with the RoHS directive



1. Contact local ST sales office for availability.

**Table 1. Device summary**

Part number	Watchdog input	Active-low RST <sup>(1)</sup>	Active-high RST	Manual reset input <sup>(1)</sup>	Battery switchover	Power-fail comparator	Chip-enable gating	Battery freshness seal
STM690A	✓	✓			✓	✓		
STM692A	✓	✓			✓	✓		
STM703		✓		✓	✓	✓		
STM704		✓		✓	✓	✓		
STM802L/M	✓	✓			✓	✓		
STM805L	✓		✓		✓	✓		
STM817L/M	✓	✓			✓	✓		✓
STM818L/M	✓	✓			✓		✓	✓
STM819L/M		✓		✓	✓	✓		✓

1. All  $\overline{\text{RST}}$  and RST outputs are push-pull.

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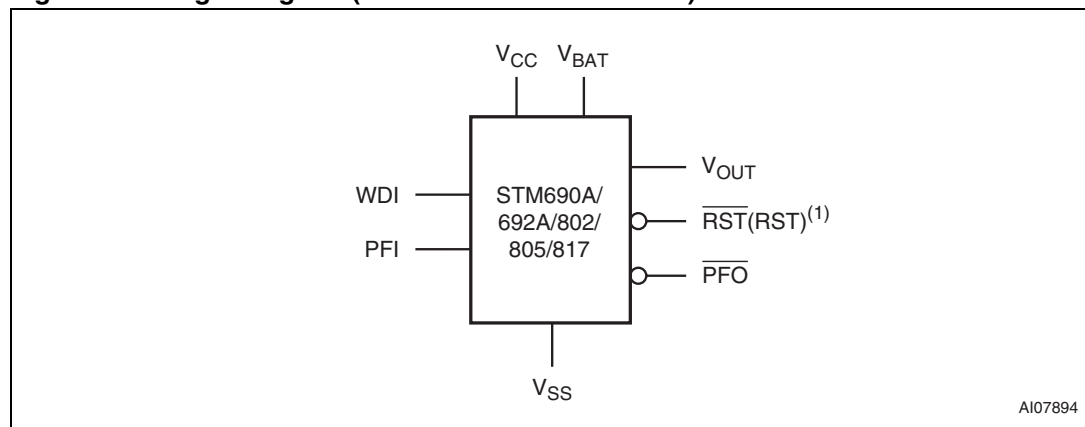
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# 1 Description

The STM690A/692A/703/704/802/805/817/818/819 supervisors are self-contained devices which provide microprocessor supervisory functions with the ability to non-volatize and write-protect external LPSRAM. A precision voltage reference and comparator monitors the  $V_{CC}$  input for an out-of-tolerance condition. When an invalid  $V_{CC}$  condition occurs, the reset output ( $\overline{RST}$ ) is forced low (or high in the case of RST). These devices also offer a watchdog timer (except for STM703/704/819) as well as a power-fail comparator (except for STM818) to provide the system with an early warning of impending power failure.

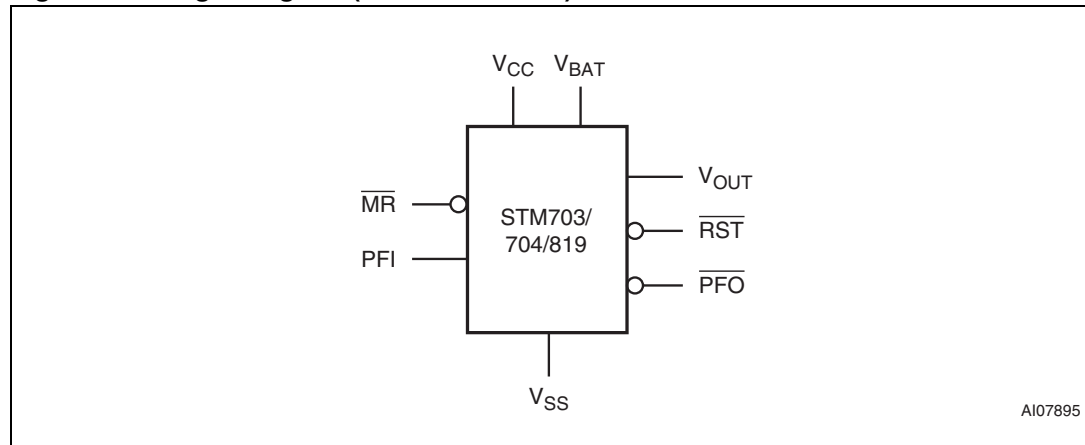
These devices are available in a standard 8-pin SOIC package or a space-saving 8-pin TSSOP package.

**Figure 1. Logic diagram (STM690A/692/802/805/817)**

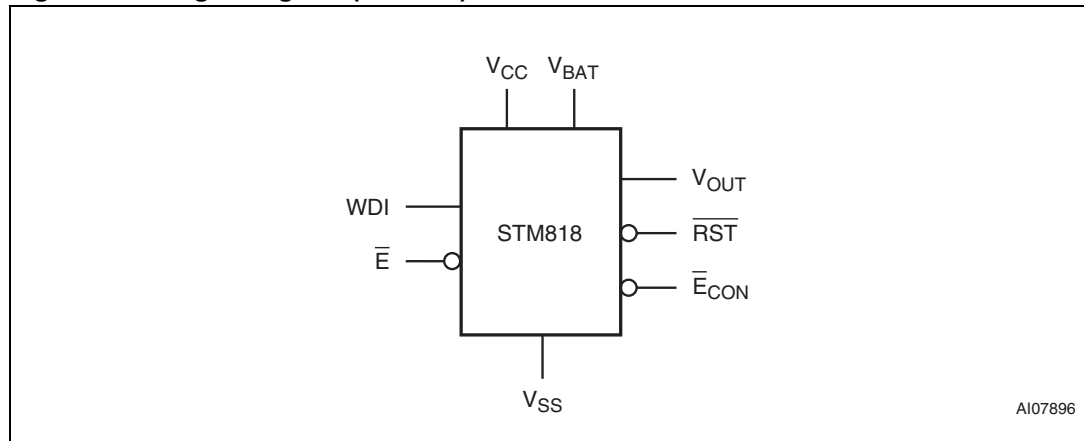


1. For STM805, reset output is active-high.

**Figure 2. Logic diagram (STM703/704/819)**



**Figure 3. Logic diagram (STM818)**



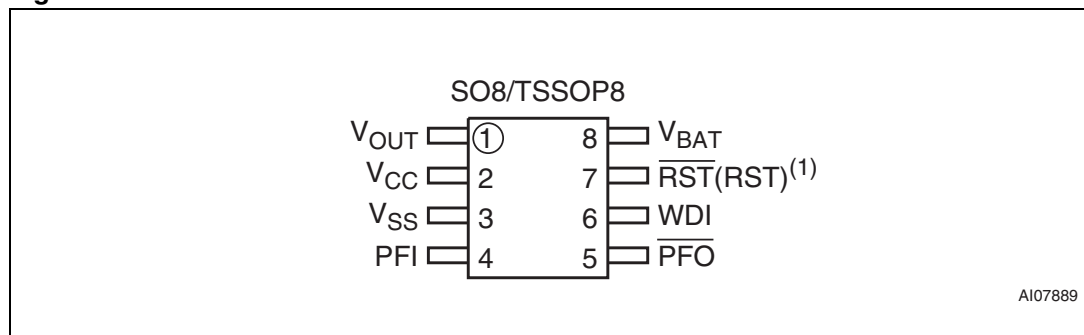
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**Table 2. Signal names**

$\overline{MR}$	Push-button reset input
WDI	Watchdog input
$\overline{RST}$	Active-low reset output
RST	Active-high reset output
$\overline{E}^{(1)}$	Chip-enable input
$\overline{E}_{CON}^{(1)}$	Conditioned chip-enable output
$V_{OUT}$	Supply voltage output
$V_{CC}$	Supply voltage
$V_{BAT}$	Backup supply voltage
PFI	Power-fail input
$\overline{PFO}$	Power-fail output
$V_{SS}$	Ground

1. STM818

**Figure 4. STM690A/692A/802/805/817 connections**



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1. For STM805, reset output is active-high.

Figure 5. STM703/704/819 connections

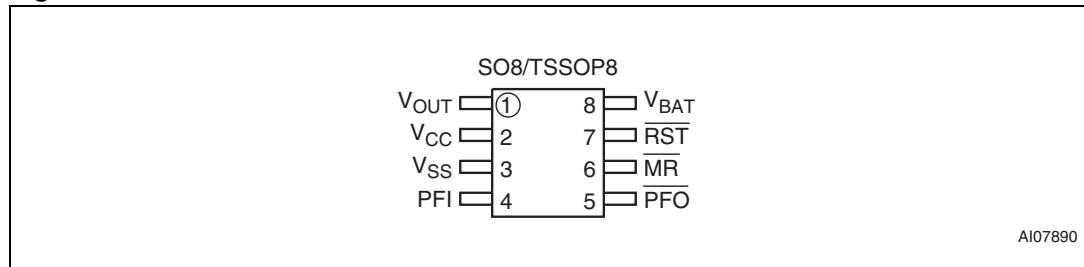
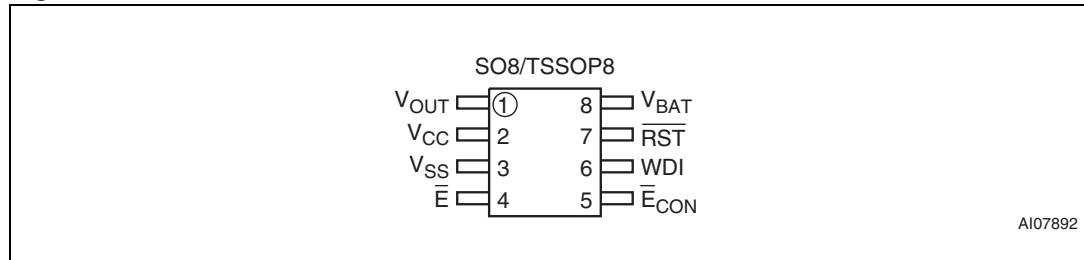


Figure 6. STM818 connections



## 1.1 Pin descriptions

### 1.1.1 $\overline{\text{MR}}$

A logic low on  $\overline{\text{MR}}$  asserts the reset output. Reset remains asserted as long as  $\overline{\text{MR}}$  is low and for  $t_{\text{rec}}$  after  $\overline{\text{MR}}$  returns high. This active-low input has an internal pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.

### 1.1.2 WDI

If WDI remains high or low for 1.6 sec, the internal watchdog timer runs out and reset is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge.

The watchdog function can be disabled by allowing the WDI pin to float.

### 1.1.3 $\overline{\text{RST}}$

Pulses low for  $t_{\text{rec}}$  when triggered, and stays low whenever  $V_{\text{CC}}$  is below the reset threshold or when  $\overline{\text{MR}}$  is a logic low. It remains low for  $t_{\text{rec}}$  after either  $V_{\text{CC}}$  rises above the reset threshold, the watchdog triggers a reset, or  $\overline{\text{MR}}$  goes from low to high.

### 1.1.4 RST

Pulses high for  $t_{\text{rec}}$  when triggered, and stays high whenever  $V_{\text{CC}}$  is above the reset threshold or when  $\overline{\text{MR}}$  is a logic high. It remains high for  $t_{\text{rec}}$  after either  $V_{\text{CC}}$  falls below the reset threshold, the watchdog triggers a reset, or  $\overline{\text{MR}}$  goes from high to low.

**1.1.5  $V_{OUT}$** 

When  $V_{CC}$  is above the switchover voltage ( $V_{SO}$ ),  $V_{OUT}$  is connected to  $V_{CC}$  through a P-channel MOSFET switch. When  $V_{CC}$  falls below  $V_{SO}$ ,  $V_{BAT}$  connects to  $V_{OUT}$ .

**1.1.6  $V_{BAT}$** 

When  $V_{CC}$  falls below  $V_{SO}$ ,  $V_{OUT}$  switches from  $V_{CC}$  to  $V_{BAT}$ . When  $V_{CC}$  rises above  $V_{SO} +$  hysteresis,  $V_{OUT}$  reconnects to  $V_{CC}$ .  $V_{BAT}$  may exceed  $V_{CC}$ . Connect to  $V_{CC}$  if no battery is used.

**1.1.7  $\bar{E}$** 

The input to the chip-enable gating circuit. Connect to ground if unused.

**1.1.8  $\bar{E}_{CON}$** 

$\bar{E}_{CON}$  goes low only when  $\bar{E}$  is low and reset is not asserted. If  $\bar{E}_{CON}$  is low when reset is asserted,  $\bar{E}_{CON}$  will remain low for 15  $\mu$ s or until  $\bar{E}$  goes high, whichever occurs first. In the disabled mode,  $\bar{E}_{CON}$  is pulled up to  $V_{OUT}$ .

**1.1.9  $PFI$** 

When  $PFI$  is less than  $V_{PFI}$  or when  $V_{CC}$  falls below 2.4 V (or  $V_{SO}$ ),  $\overline{PFO}$  goes low; otherwise,  $\overline{PFO}$  remains high. Connect to ground if unused.

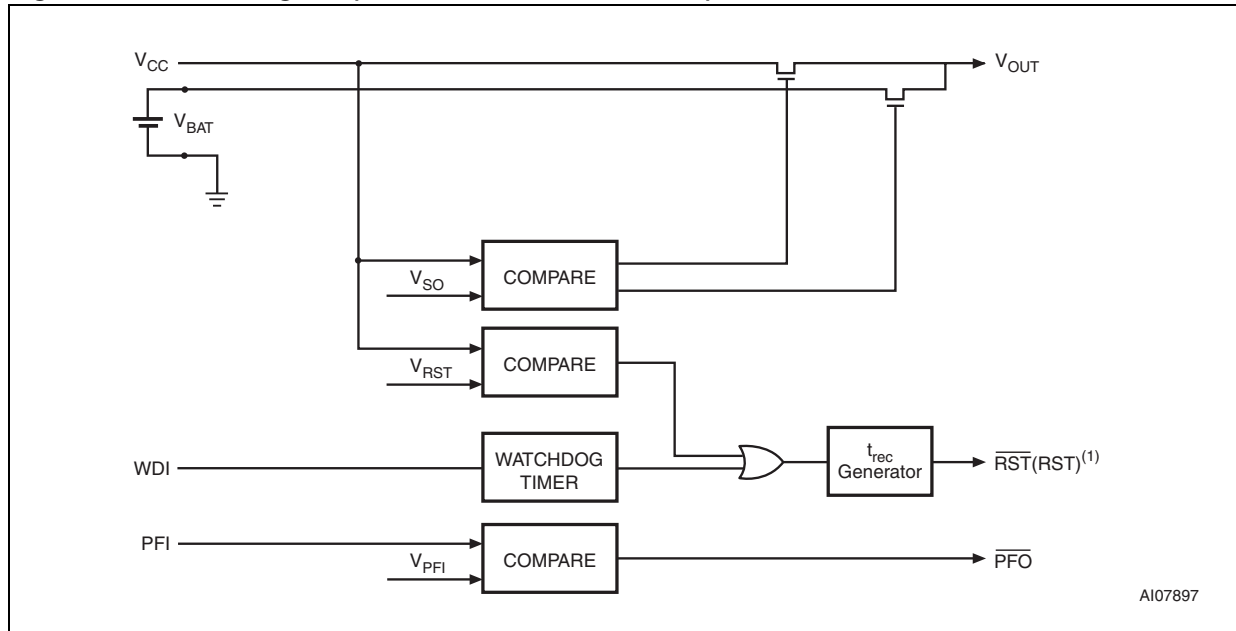
**1.1.10  $\overline{PFO}$** 

When  $PFI$  is less than  $V_{PFI}$ , or  $V_{CC}$  falls below 2.4 V (or  $V_{SO}$ ),  $\overline{PFO}$  goes low; otherwise,  $\overline{PFO}$  remains high. Leave open if unused. Output type is push-pull.

Table 3. Pin description

Pin				Name	Function
STM818	STM690A STM692A STM802 STM817	STM703 STM704 STM819	STM805		
-	-	6	-	$\overline{MR}$	Push-button reset input
6	6	-	6	WDI	Watchdog input
7	7	7	-	$\overline{RST}$	Active-low reset output
-	-	-	7	RST	Active-high reset output
1	1	1	1	$V_{OUT}$	Supply output for external LPSRAM
2	2	2	2	$V_{CC}$	Supply voltage
8	8	8	8	$V_{BAT}$	Backup battery input
4	-	-	-	$\overline{E}$	Chip-enable input
5	-	-	-	$\overline{E}_{CON}$	Conditioned chip-enable output
-	4	4	4	PFI	Power-fail input
-	5	5	5	$\overline{PFO}$	Power-fail output (push-pull)
3	3	3	3	$V_{SS}$	Ground

Figure 7. Block diagram (STM690A/692A/802/805/817)



1. For STM805, reset output is active-high.

Figure 8. Block diagram (STM703/704/819)

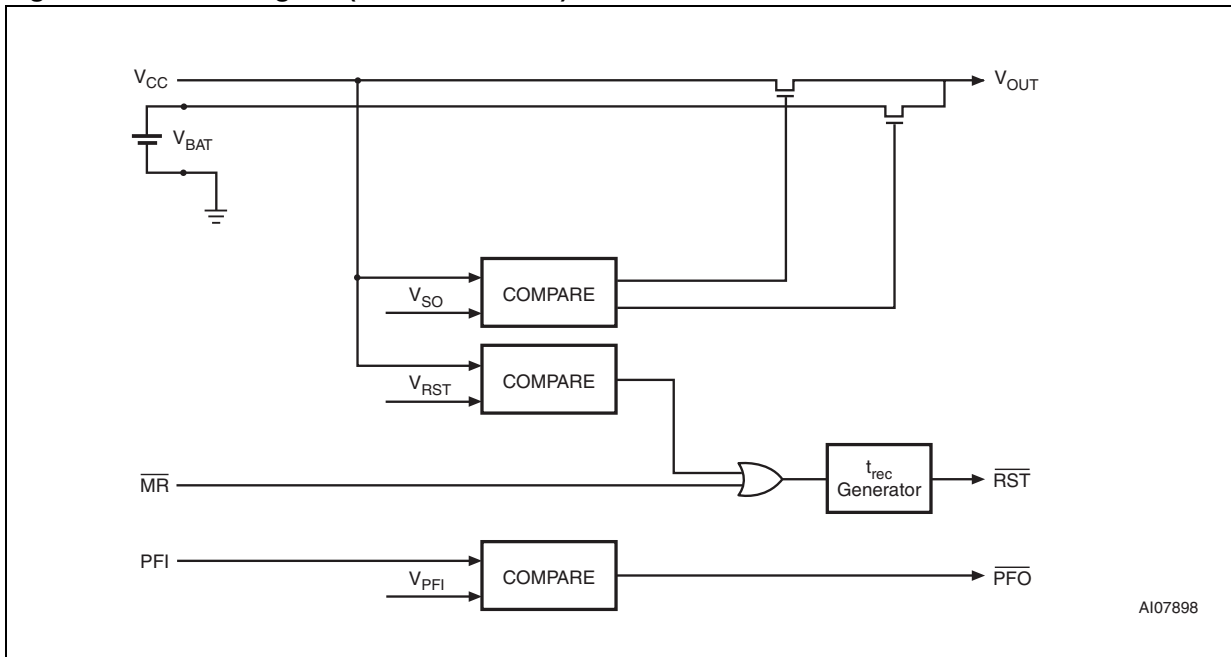
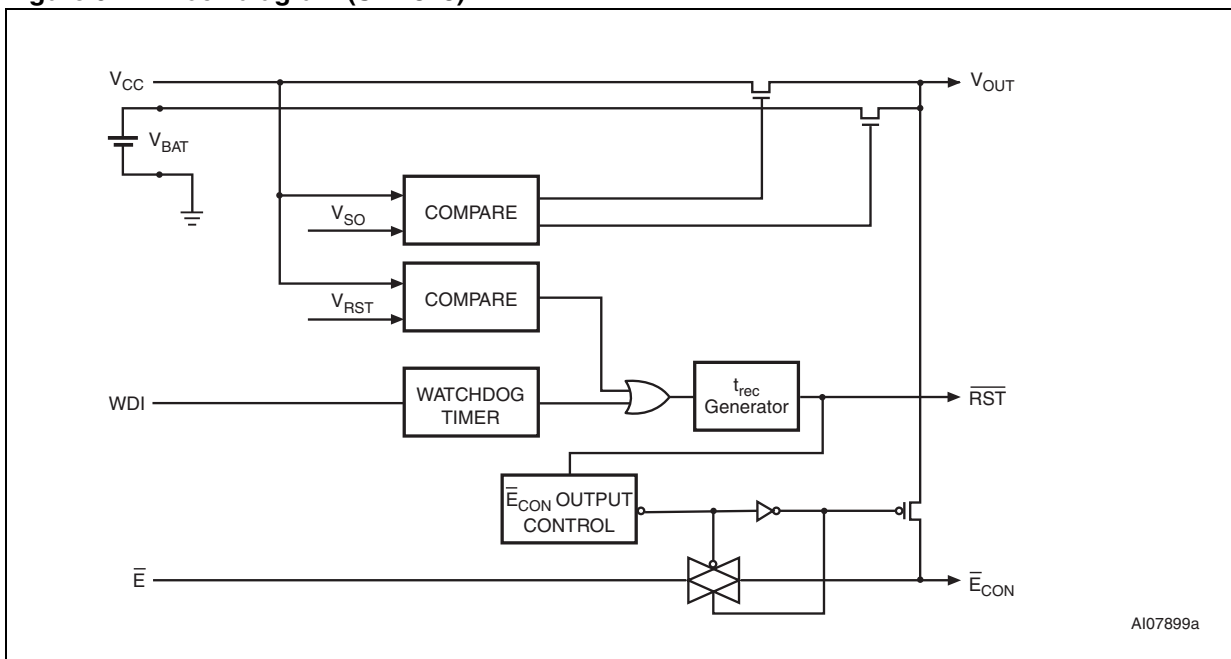


Figure 9. Block diagram (STM818)





## 2 Operation

### 2.1 Reset output

The STM690A/692A/703/704/802/805/817/818/819 Supervisor asserts a reset signal to the MCU whenever  $V_{CC}$  goes below the reset threshold ( $V_{RST}$ ), a watchdog time-out occurs, or when the Push-button Reset Input ( $\overline{MR}$ ) is taken low.  $\overline{RST}$  is guaranteed to be a logic low (logic high for STM805) for  $0V < V_{CC} < V_{RST}$  if  $V_{BAT}$  is greater than 1 V. Without a backup battery,  $\overline{RST}$  is guaranteed valid down to  $V_{CC} = 1V$ .

During power-up, once  $V_{CC}$  exceeds the reset threshold an internal timer keeps  $\overline{RST}$  low for the reset time-out period,  $t_{rec}$ . After this interval  $\overline{RST}$  returns high.

If  $V_{CC}$  drops below the reset threshold,  $\overline{RST}$  goes low. Each time  $\overline{RST}$  is asserted, it stays low for at least the reset time-out period ( $t_{rec}$ ). Any time  $V_{CC}$  goes below the reset threshold the internal timer clears. The reset timer starts when  $V_{CC}$  returns above the reset threshold.

### 2.2 Push-button reset input (STM703/704/819)

A logic low on  $\overline{MR}$  asserts reset. Reset remains asserted while  $\overline{MR}$  is low, and for  $t_{rec}$  (see [Figure 41](#)) after it returns high. The  $\overline{MR}$  input has an internal 40 k $\Omega$  pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{MR}$  to GND to create a manual reset function; external debounce circuitry is not required. If  $\overline{MR}$  is driven from long cables or the device is used in a noisy environment, connect a 0.1  $\mu F$  capacitor from  $\overline{MR}$  to GND to provide additional noise immunity.  $\overline{MR}$  may float, or be tied to  $V_{CC}$  when not used.

### 2.3 Watchdog input (NOT available on STM703/704/819)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the Watchdog Input (WDI) within  $t_{WD}$  (1.6 sec typ), the reset is asserted. The internal watchdog timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high-to-low or low-to-high), which can detect pulses as short as 50ns. If WDI is tied high or low, a reset pulse is triggered every 1.8 sec ( $t_{WD} + t_{rec}$ ).

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting (see [Figure 42](#)).

*Note:* 1 The watchdog function may be disabled by floating WDI or tri-stating the driver connected to WDI. When tri-stated or disconnected, the maximum allowable leakage current is 10  $\mu A$  and the maximum allowable load capacitance is 200 pF.

- 2 Input pulses less than 20 ns will be ignored.

## 2.4 Backup battery switchover

In the event of a power failure, it may be necessary to preserve the contents of external SRAM through  $V_{OUT}$ . With a backup battery installed with voltage  $V_{BAT}$ , the devices automatically switch the SRAM to the backup supply when  $V_{CC}$  falls.

*Note:* When the battery is first connected without  $V_{CC}$  power applied, the device does not immediately provide backup battery voltage on  $V_{OUT}$ . Only after  $V_{CC}$  exceeds  $V_{RST}$  will the switchover operate as described below. This mode allows a battery to be attached during manufacturing but not used until after the system has been activated for the first time. As a result, no battery power is consumed by the device during storage and shipment. For the STM81x devices, the battery freshness seal can be initiated again by following the procedure outlined in [Section 2.12](#). If the backup battery is not used, connect both  $V_{BAT}$  and  $V_{OUT}$  to  $V_{CC}$ .

Whenever  $V_{CC}$  falls below the switchover voltage,  $V_{SO}$ ,  $V_{OUT}$  is connected to  $V_{BAT}$  through a  $100\ \Omega$  switch.  $V_{SO}$  is the lesser of  $V_{BAT}$  and  $V_{RST}$ . Choosing the lesser allows the device to be powered by  $V_{CC}$  for as long as possible before switching over thereby maximizing the battery life.

Assuming  $V_{BAT} > 2.0\text{ V}$ , switchover at  $V_{SO}$  ensures that battery backup mode is entered before  $V_{OUT}$  gets too close to the 2.0 V minimum required to reliably retain data in most external SRAMs. When  $V_{CC}$  recovers, hysteresis is used to avoid oscillation around the  $V_{SO}$  point.  $V_{OUT}$  is connected to  $V_{CC}$  through a  $3\ \Omega$  PMOS power switch.

*Note:* The backup battery may be removed while  $V_{CC}$  is valid, assuming  $V_{BAT}$  is adequately decoupled ( $0.1\ \mu\text{F typ}$ ), without danger of triggering a reset.

**Table 4. I/O status in battery backup**

$V_{OUT}$	Connected to $V_{BAT}$ through internal switch
$V_{CC}$	Disconnected from $V_{OUT}$
PFI	Disabled
$\overline{\text{PFO}}$	Logic low
$\overline{\text{E}}$	High impedance
$\overline{\text{E}}_{\text{CON}}$	Logic high
WDI	Watchdog timer is disabled
$\overline{\text{MR}}$	Disabled
$\overline{\text{RST}}$	Logic low
RST	Logic high
$V_{BAT}$	Connected to $V_{OUT}$

## 2.5 Chip-enable gating (STM818 only)

Internal gating of the chip-enable ( $\bar{E}$ ) signal prevents erroneous data from corrupting the external CMOS RAM in the event of an undervoltage condition. The STM818 uses a series transmission gate from  $\bar{E}$  to  $\bar{E}_{CON}$  (see [Figure 11](#)). During normal operation (reset not asserted), the  $\bar{E}$  transmission gate is enabled and passes all  $\bar{E}$  transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short propagation delay from  $\bar{E}$  to  $\bar{E}_{CON}$  enables the STM818 to be used with most  $\mu$ Ps. If  $\bar{E}$  is low when reset asserts,  $\bar{E}_{CON}$  remains low for typically 15  $\mu$ s (or until  $\bar{E}$  goes high) to permit the current WRITE cycle to complete. Connect  $\bar{E}$  to  $V_{SS}$  if unused.

## 2.6 Chip-enable input (STM818 only)

The chip-enable transmission gate is disabled and  $\bar{E}$  is high impedance (disabled mode) while reset is asserted. During a power-down sequence when  $V_{CC}$  passes the reset threshold, the chip-enable transmission gate disables and  $\bar{E}$  immediately becomes high impedance if the voltage at  $\bar{E}$  is high. If  $\bar{E}$  is low when reset asserts, the chip-enable transmission gate will disable 15  $\mu$ s after reset asserts (see [Figure 12](#)). This permits the current WRITE cycle to complete during power-down.

Any time a reset is generated, the chip-enable transmission gate remains disabled and  $\bar{E}$  remains high impedance (regardless of  $\bar{E}$  activity) for the reset time-out period. When the chip-enable transmission gate is enabled, the impedance of  $\bar{E}$  appears as a 40  $\Omega$  resistor in series with the load at  $\bar{E}_{CON}$ . The propagation delay through the chip-enable transmission gate depends on  $V_{CC}$ , the source impedance of the drive connected to  $\bar{E}$ , and the loading on  $\bar{E}_{CON}$ . The chip-enable propagation delay is production tested from the 50% point on  $\bar{E}$  to the 50% point on  $\bar{E}_{CON}$  using a 50  $\Omega$  driver and a 50 pF load capacitance (see [Figure 39](#)). For minimum propagation delay, minimize the capacitive load at  $\bar{E}_{CON}$  and use a low-output impedance driver.

## 2.7 Chip-enable output (STM818 only)

When the chip-enable transmission gate is enabled, the impedance of  $\bar{E}_{CON}$  is equivalent to a 40  $\Omega$  resistor in series with the source driving  $\bar{E}$ . In the disabled mode, the transmission gate is off and an active pull-up connects  $\bar{E}_{CON}$  to  $V_{OUT}$  (see [Figure 11](#)). This pull-up turns off when the transmission gate is enabled.

Figure 11. Chip-enable gating

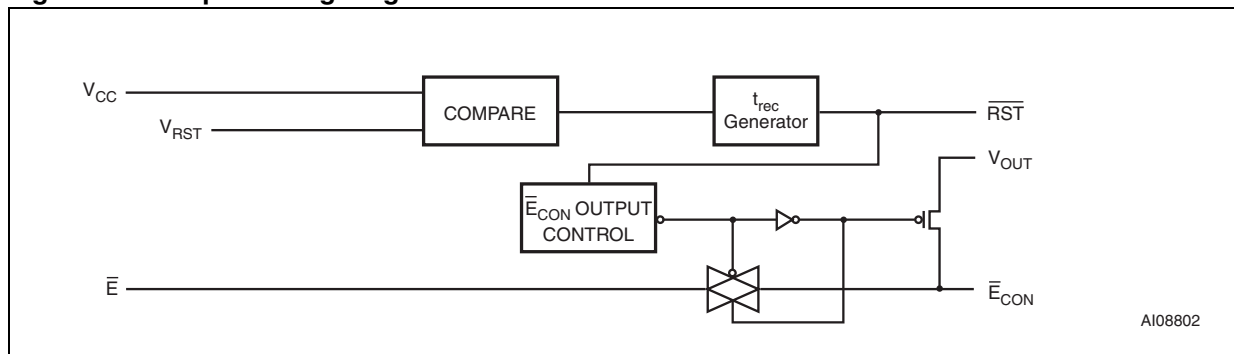
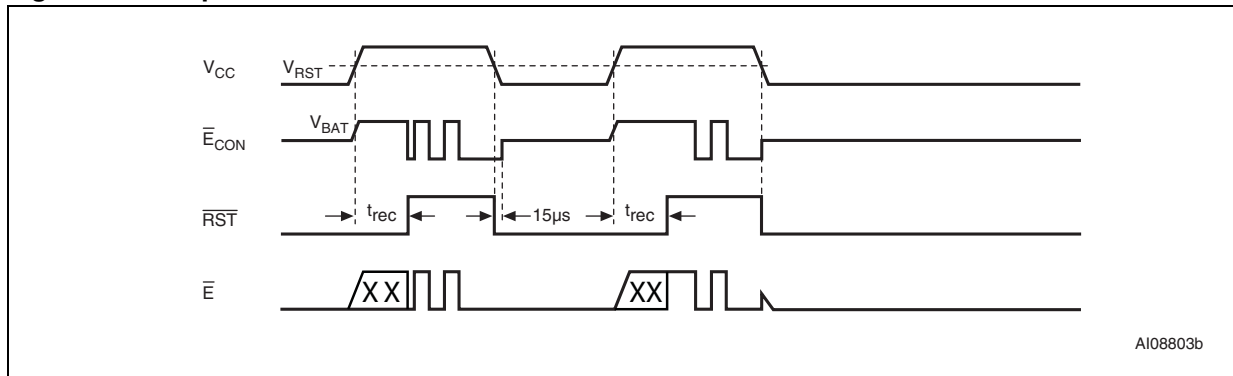


Figure 12. Chip-enable waveform



## 2.8 Power-fail input/output (NOT available on STM818)

The Power-fail Input (PFI) is compared to an internal reference voltage (independent from the  $V_{RST}$  comparator). If PFI is less than the power-fail threshold ( $V_{PFI}$ ), the Power-Fail Output ( $\overline{PFO}$ ) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see [Figure 12](#)) to either the unregulated DC input (if it is available) or the regulated output of the  $V_{CC}$  regulator. The voltage divider can be set up such that the voltage at PFI falls below  $V_{PFI}$  several milliseconds before the regulated  $V_{CC}$  input to the STM690A/692A/703/704/802/805/817/818/819 Supervisor or before the microprocessor drops below the minimum operating voltage. This provides several milliseconds of advanced warning that power is about to fail.

During battery backup, the power-fail comparator turns off and  $\overline{PFO}$  goes (or remains) low (see [Figure 13](#) below and [Figure 14](#)). This occurs after  $V_{CC}$  drops below 2.4 V (or  $V_{SO}$ ). When power returns,  $\overline{PFO}$  is forced high (STM817/819 only), irrespective of  $V_{PFI}$  for the WRITE protect time ( $t_{rec}$ ). At the end of this time, the power-fail comparator is enabled and  $\overline{PFO}$  follows PFI. If the comparator is unused, PFI should be connected to  $V_{SS}$  and  $\overline{PFO}$  left unconnected.  $\overline{PFO}$  may be connected to  $\overline{MR}$  on the STM703/704/818 so that a low voltage on PFI will generate a reset output.

## 2.9 Applications information

These supervisor circuits are not short-circuit protected. Shorting  $V_{OUT}$  to ground - excluding power-up transients such as charging a decoupling capacitor - destroys the device. Decouple both  $V_{CC}$  and  $V_{BAT}$  pins to ground by placing 0.1  $\mu\text{F}$  capacitors as close to the device as possible.

Figure 13. Power-fail comparator waveform (STM817/818/819)

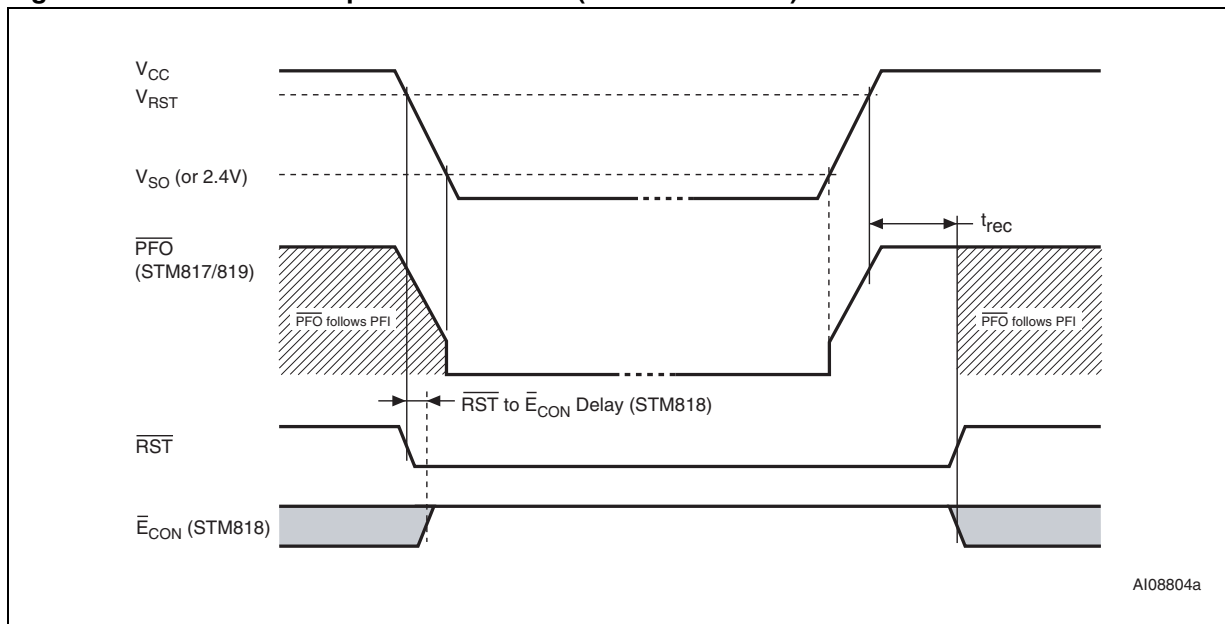
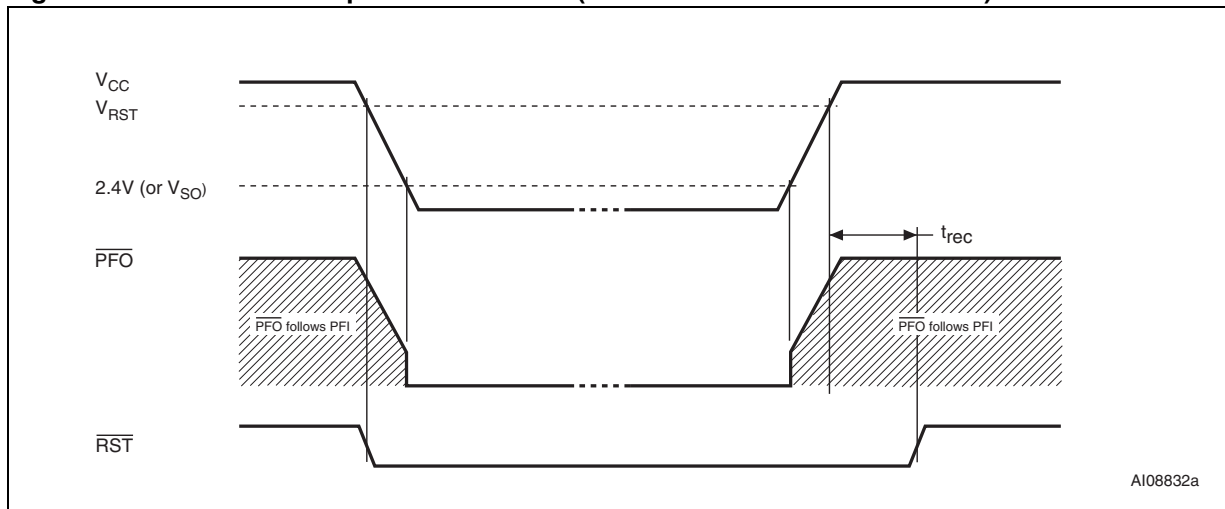


Figure 14. Power-fail comparator waveform (STM690A/692A/703/704/802/805)



## 2.10 Using a SuperCap™ as a backup power source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., 0.47 F) for their size. [Figure 15](#) shows how to use a SuperCap as a backup power source. The SuperCap may be connected through a diode to the 5 V supply. Since  $V_{BAT}$  can exceed  $V_{CC}$  while  $V_{CC}$  is above the reset threshold, there are no special precautions for using these supervisors with a SuperCap.

## 2.11 Negative-going $V_{CC}$ transients

The STM690A/692A/703/704/802/805/817/818/819 Supervisors are relatively immune to negative-going  $V_{CC}$  transients (glitches). [Figure 37](#) shows typical transient duration versus reset comparator overdrive (for which the STM690A/692A/703/704/802/805/817/818/819 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to  $V_{CC}$ , starting at  $V_{RST} + 0.3$  V and ending below the reset threshold by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative  $V_{CC}$  transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a  $V_{CC}$  transient that goes 100 mV below the reset threshold and lasts 40  $\mu$ s or less will not cause a reset pulse. A 0.1  $\mu$ F bypass capacitor mounted as close as possible to the  $V_{CC}$  pin provides additional transient immunity.

## 2.12 Battery freshness seal (STM817/818/819)

The battery freshness seal disconnects the backup battery from internal circuitry and  $V_{OUT}$  until it is needed. This allows an OEM to ensure that the backup battery connected to  $V_{BAT}$  will be fresh when the final product is put to use. To enable the freshness seal:

1. Connect a battery to  $V_{BAT}$
2. Ground  $\overline{PFO}$
3. Bring  $V_{CC}$  above the reset threshold and hold it there until reset is deasserted following the reset timeout period and
4. Bring  $V_{CC}$  down again (Figure 16)

Use the same procedure for the STM818, but ground  $\overline{ECON}$  instead of  $\overline{PFO}$ . Once the battery freshness seal is enabled (disconnecting the backup battery from internal circuitry and anything connected to  $V_{OUT}$ ), it remains enabled until  $V_{CC}$  is brought above  $V_{RST}$ .

Figure 15. Using a SuperCap™

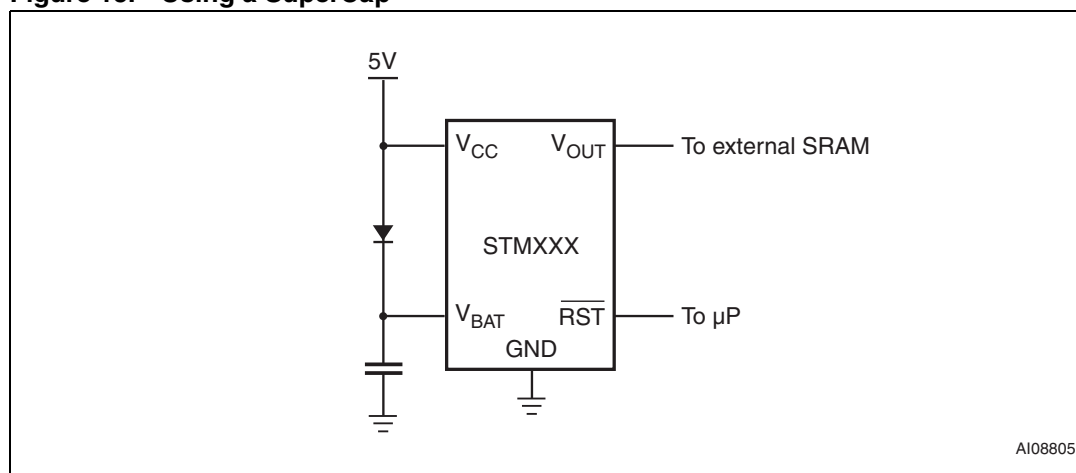
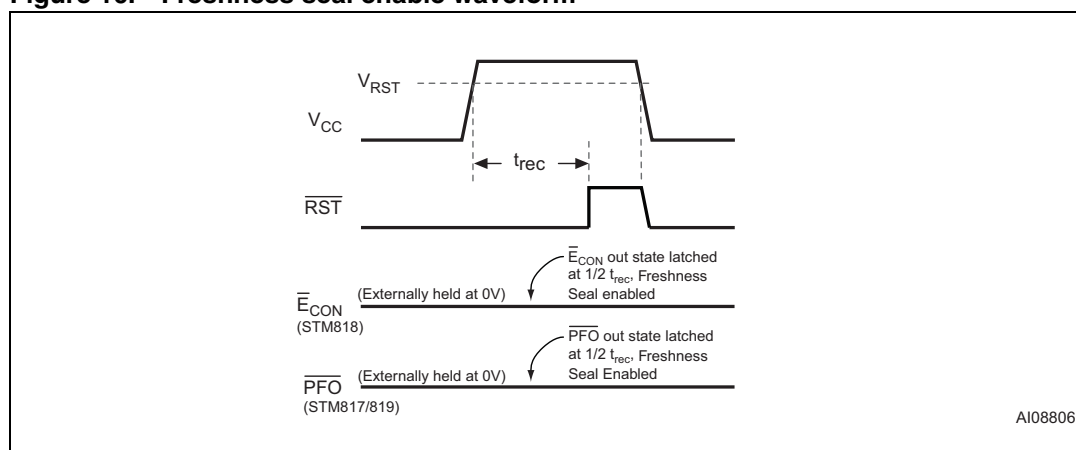


Figure 16. Freshness seal enable waveform



### 3 Typical operating characteristics

Note: Typical values are at  $T_A = 25^\circ\text{C}$ .

Figure 17.  $V_{CC}$  to  $V_{OUT}$  on-resistance vs. temperature

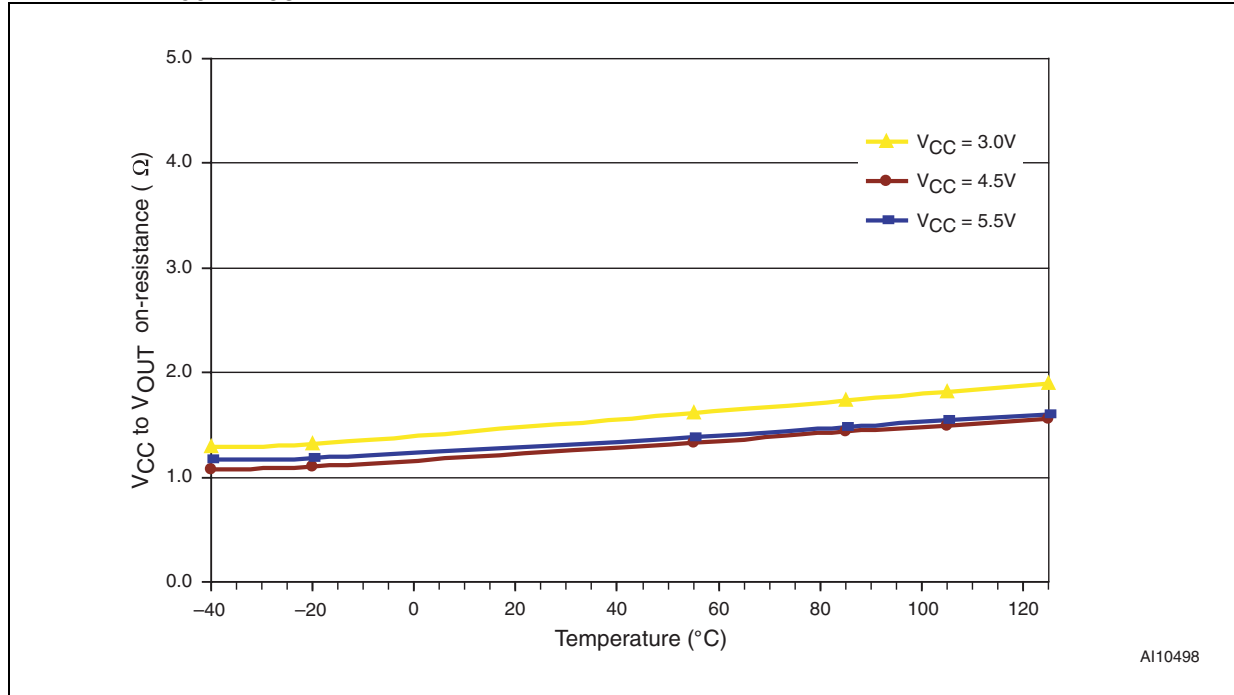


Figure 18.  $V_{BAT}$  to  $V_{OUT}$  on-resistance vs. temperature

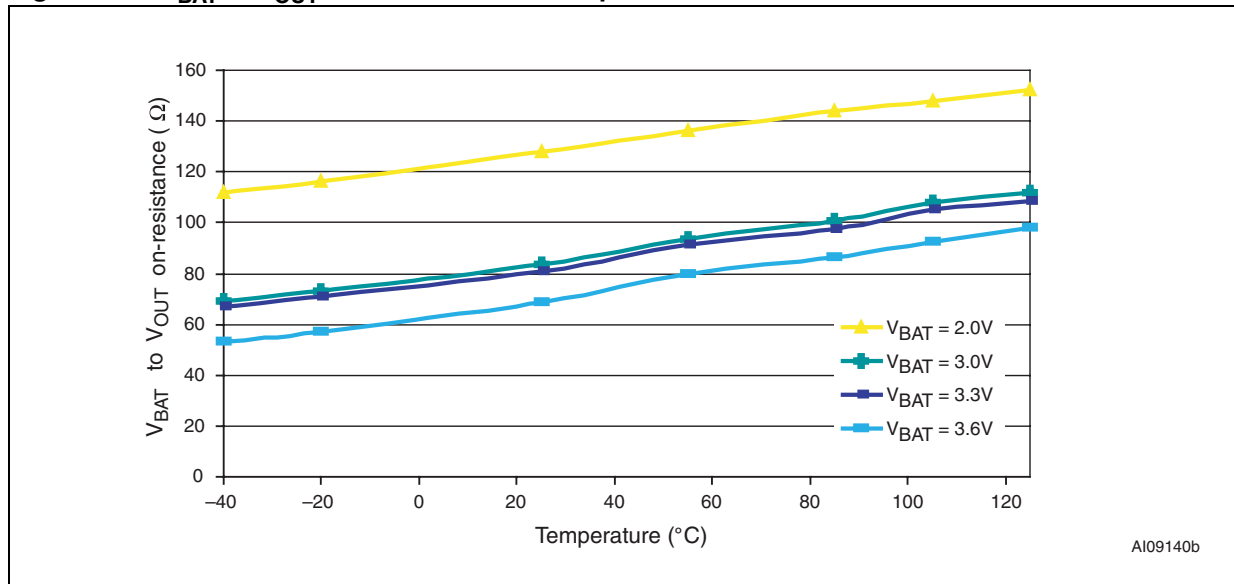


Figure 19. Supply current vs. temperature (no load)

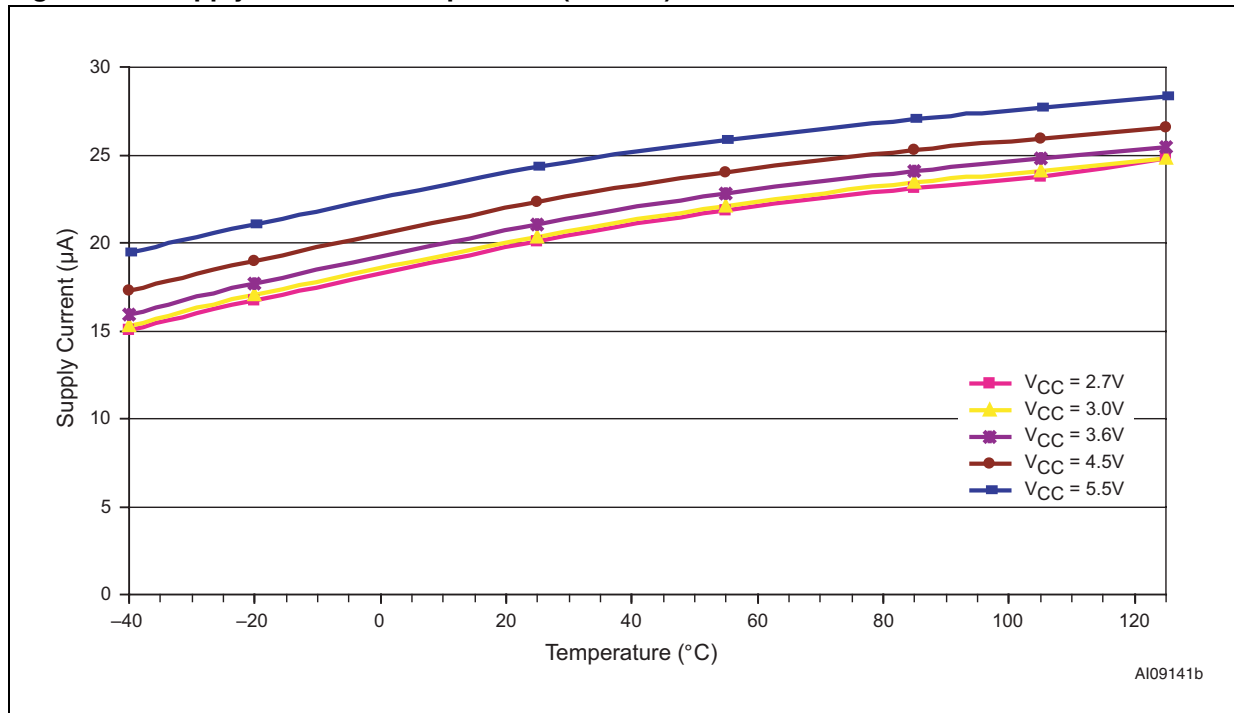


Figure 20. Battery current vs. temperature

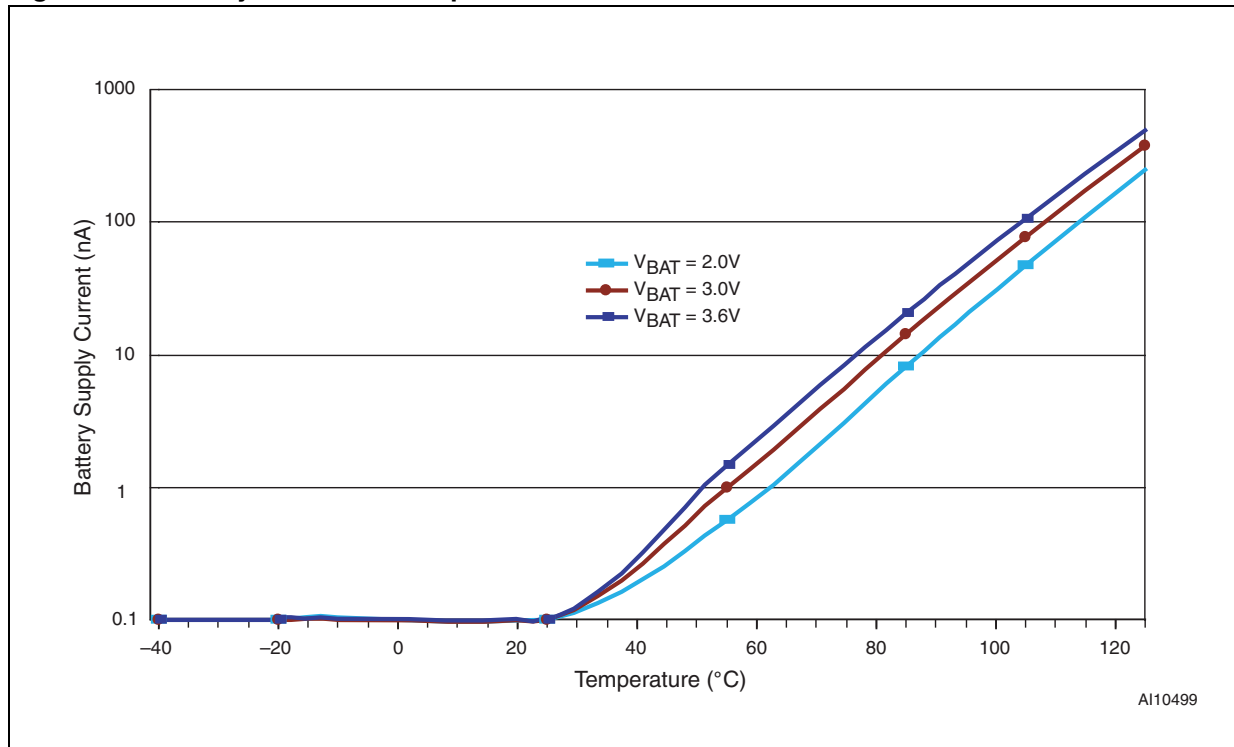


Figure 21.  $V_{PFI}$  threshold vs. temperature

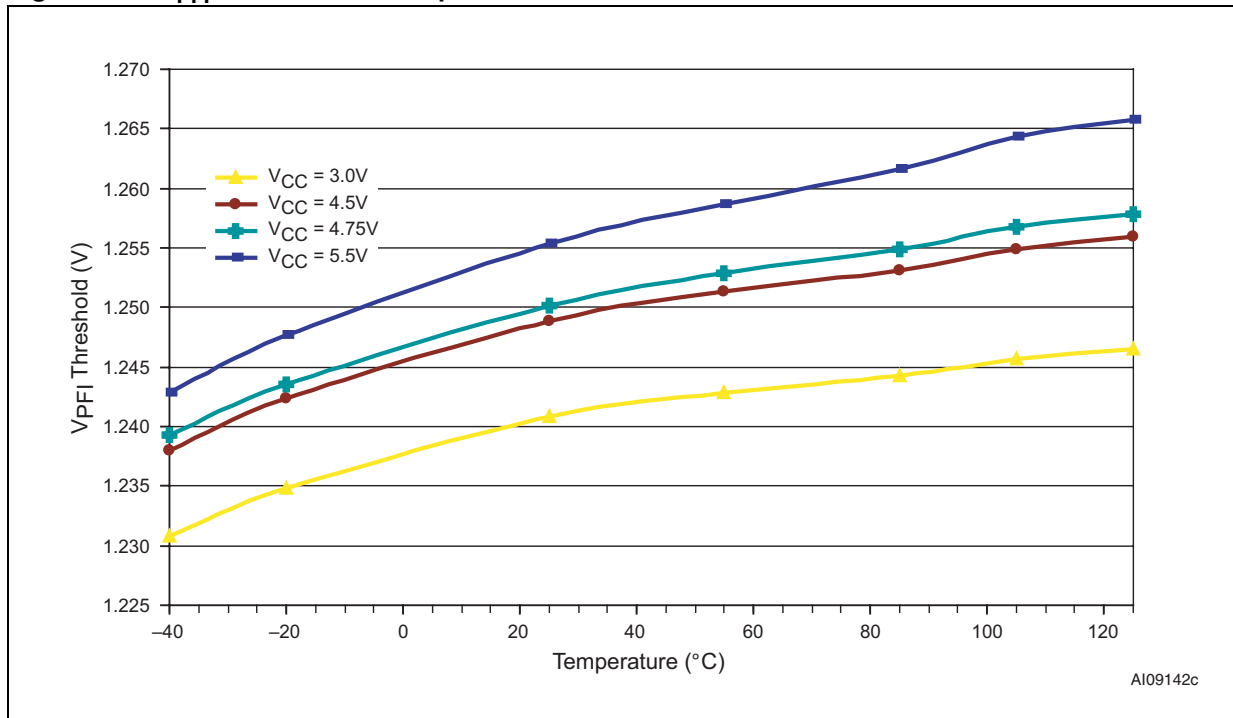


Figure 22. Reset comparator propagation delay vs. temperature (other than STM817/818/819)

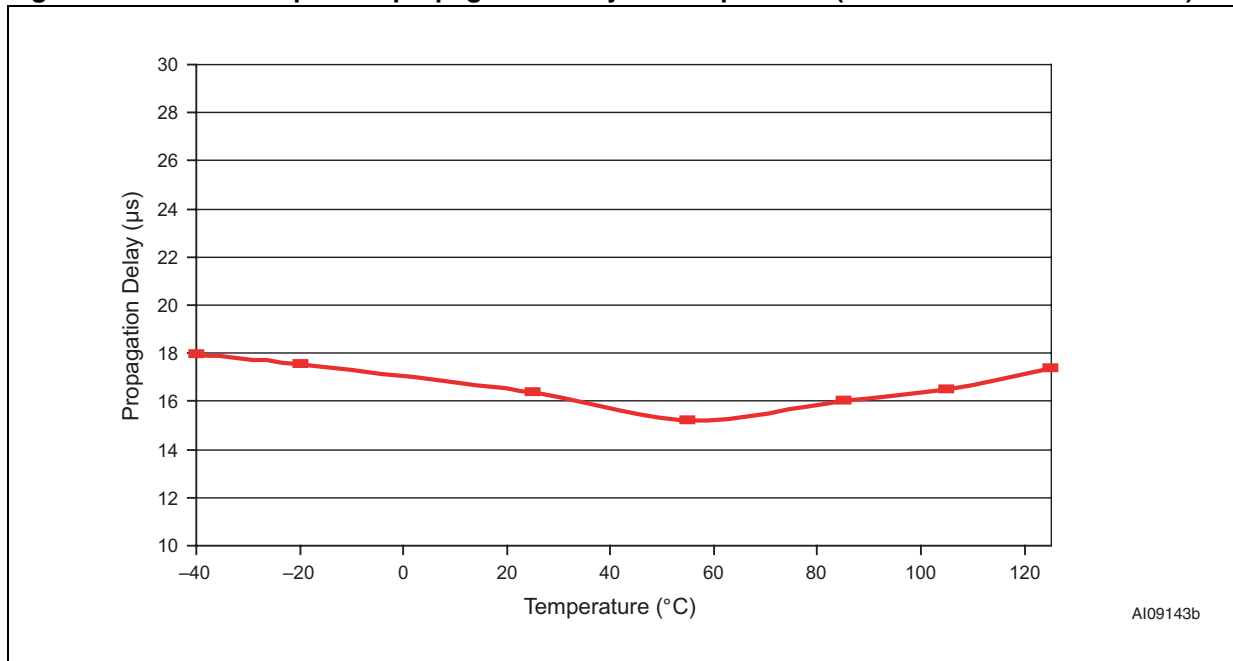


Figure 23. Reset comparator propagation delay vs. temperature ( $V_{BAT} = 3.0\text{ V}$ ; STM817/818/819)

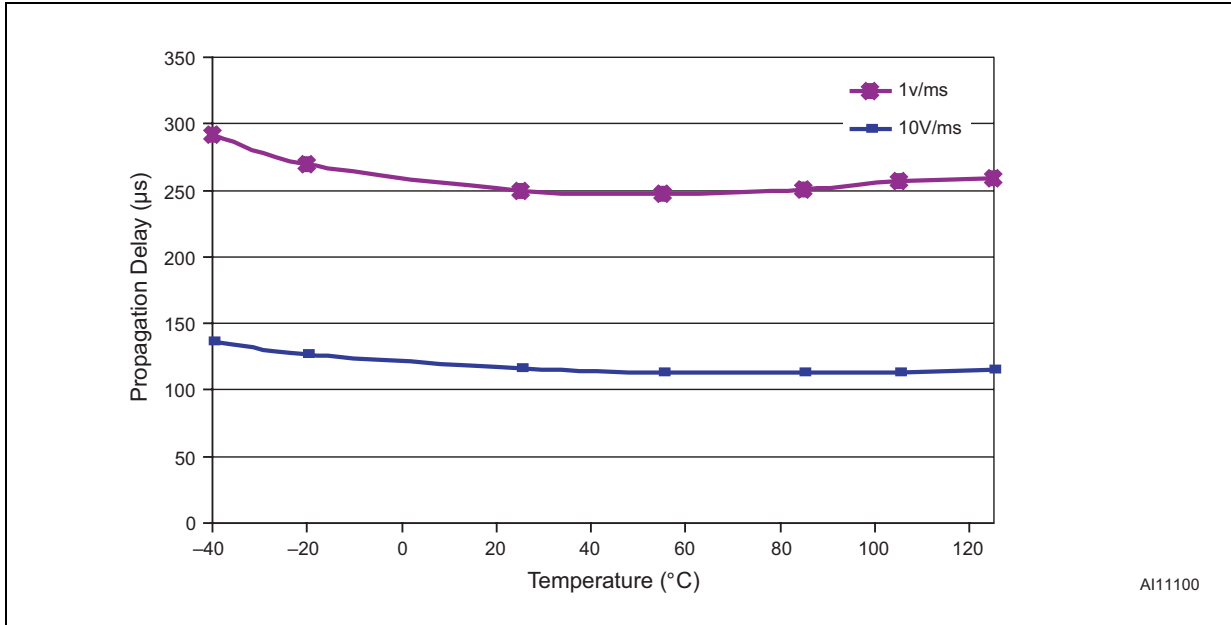


Figure 24. Power-up  $t_{REC}$  vs. temperature

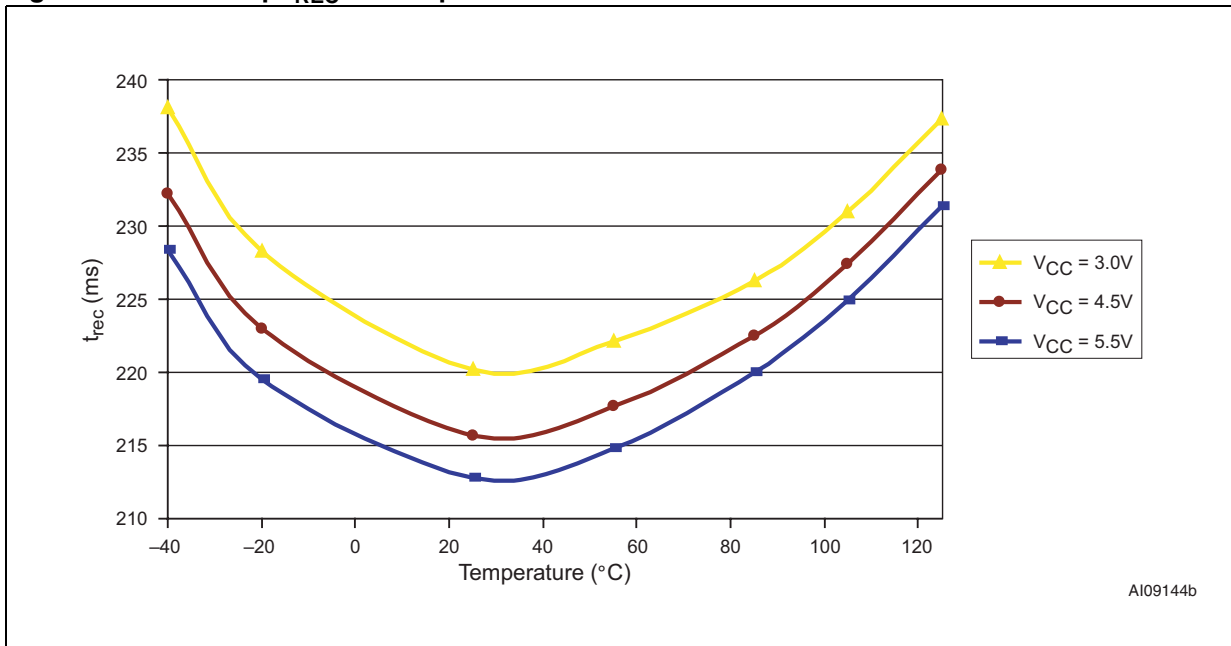


Figure 25. Normalized reset threshold vs. temperature

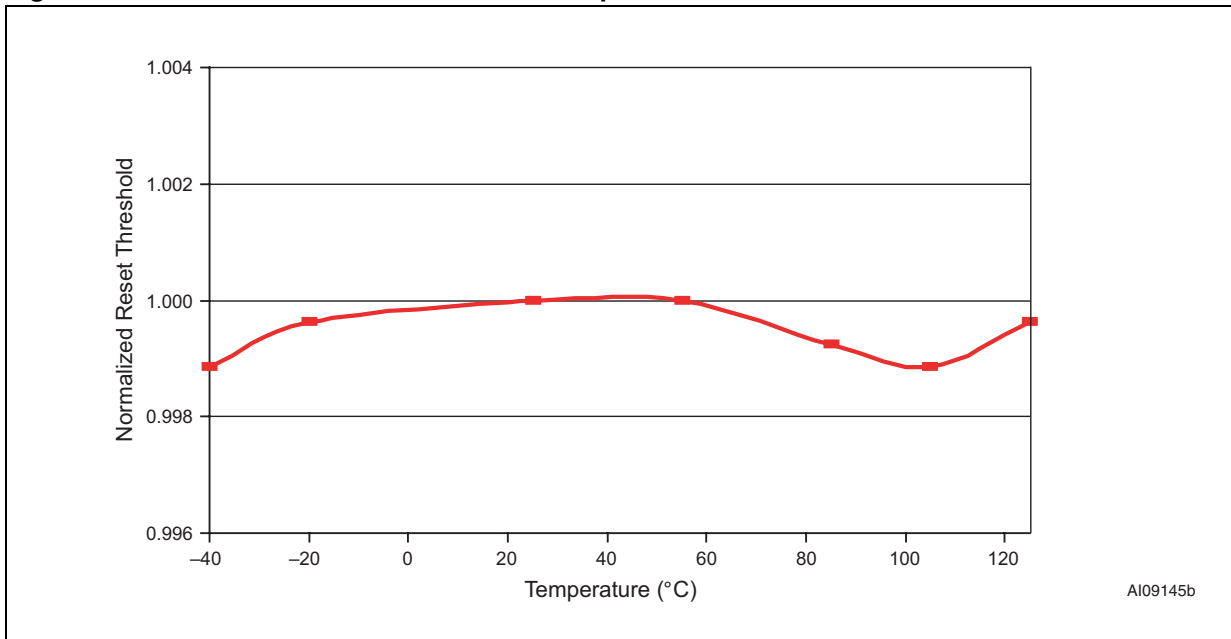


Figure 26. Watchdog time-out period vs. temperature

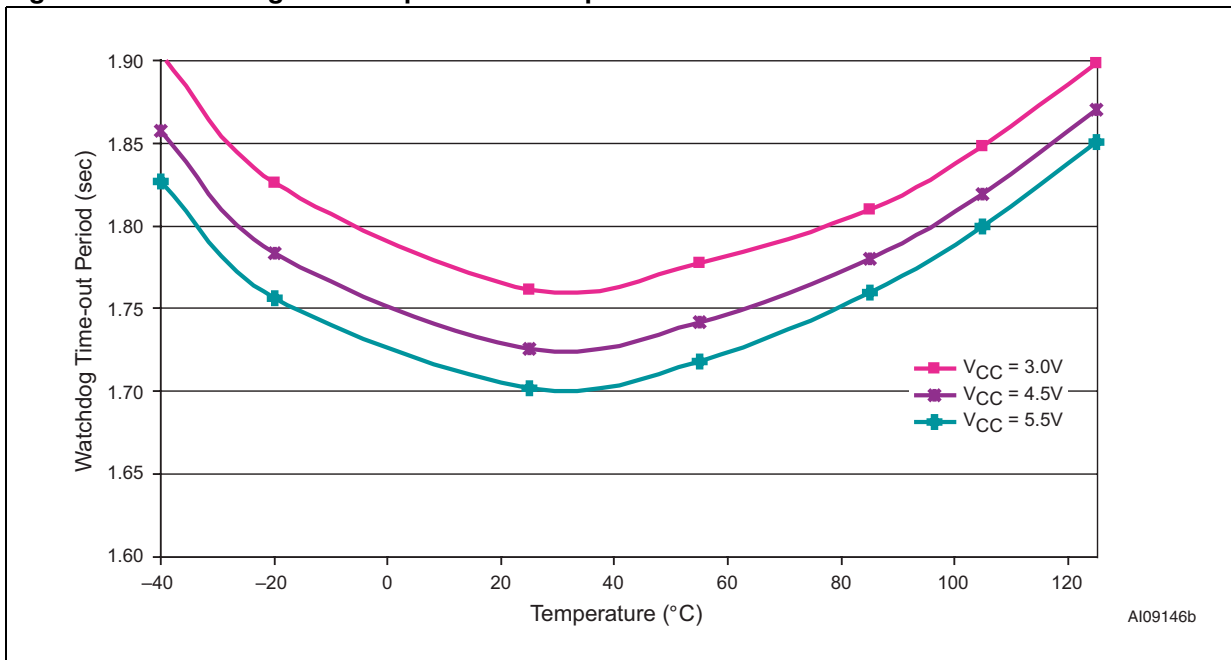


Figure 27.  $\bar{E}$  to  $\bar{E}_{CON}$  on-resistance vs. temperature

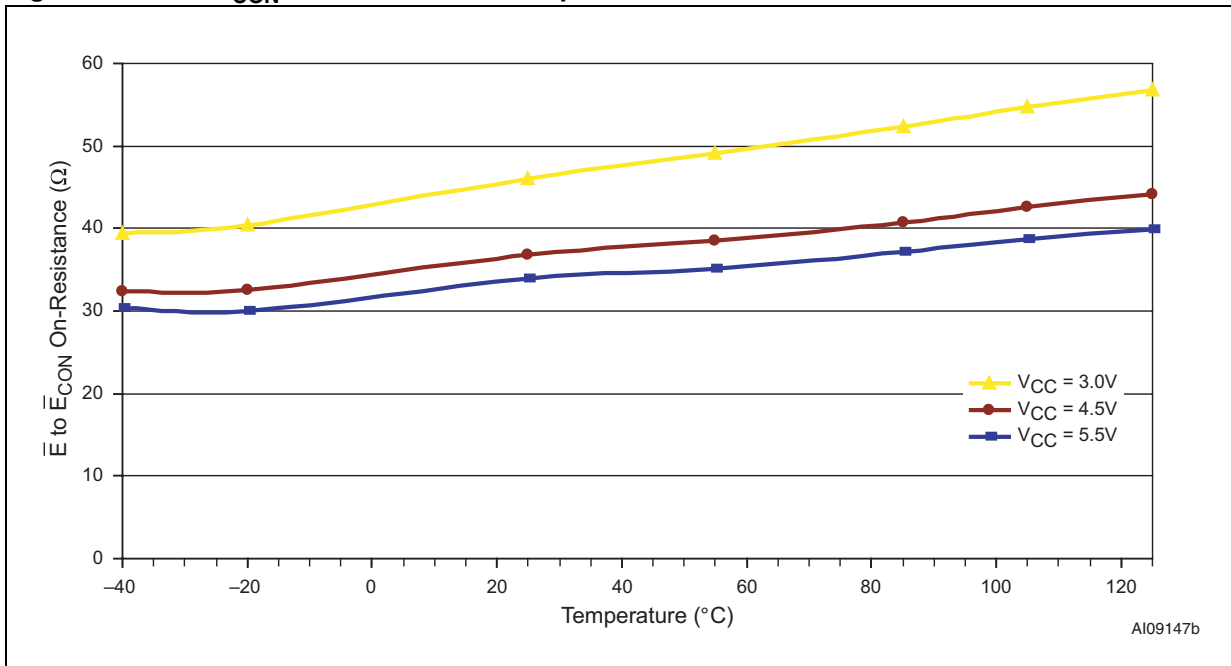


Figure 28. PFI to  $\bar{PFO}$  propagation delay vs. temperature

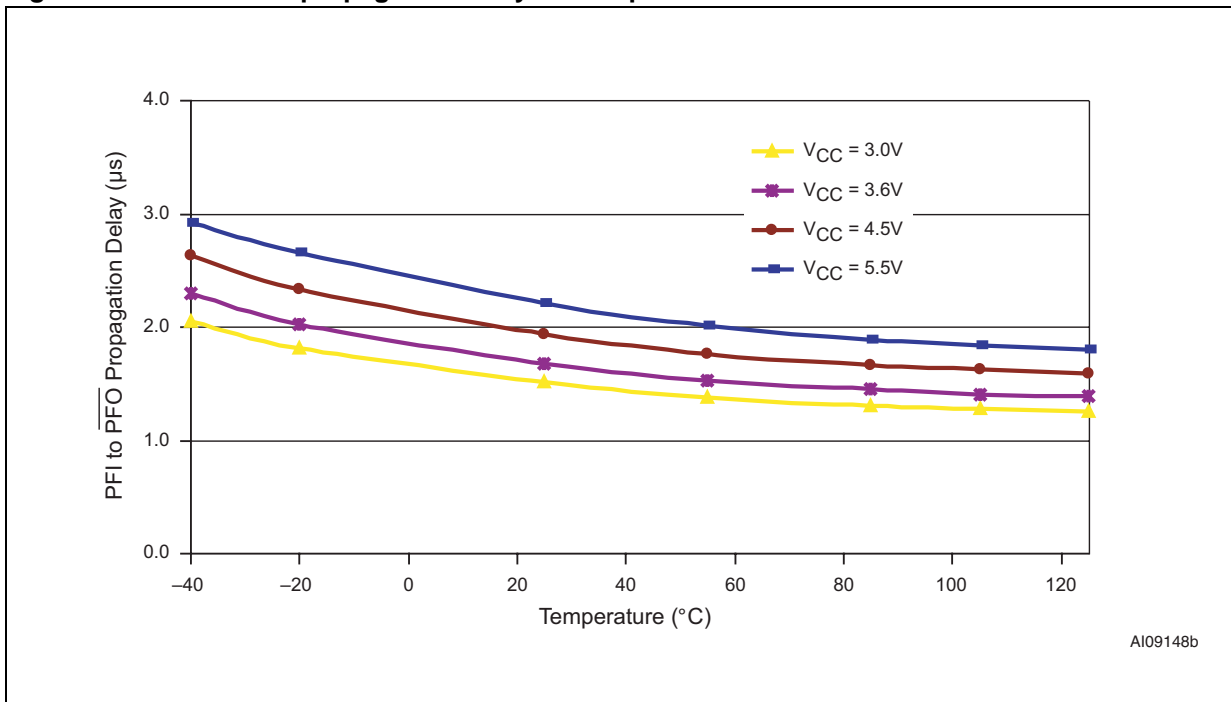


Figure 29. Output voltage vs. load current ( $V_{CC} = 5\text{ V}$ ;  $V_{BAT} = 2.8\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ )

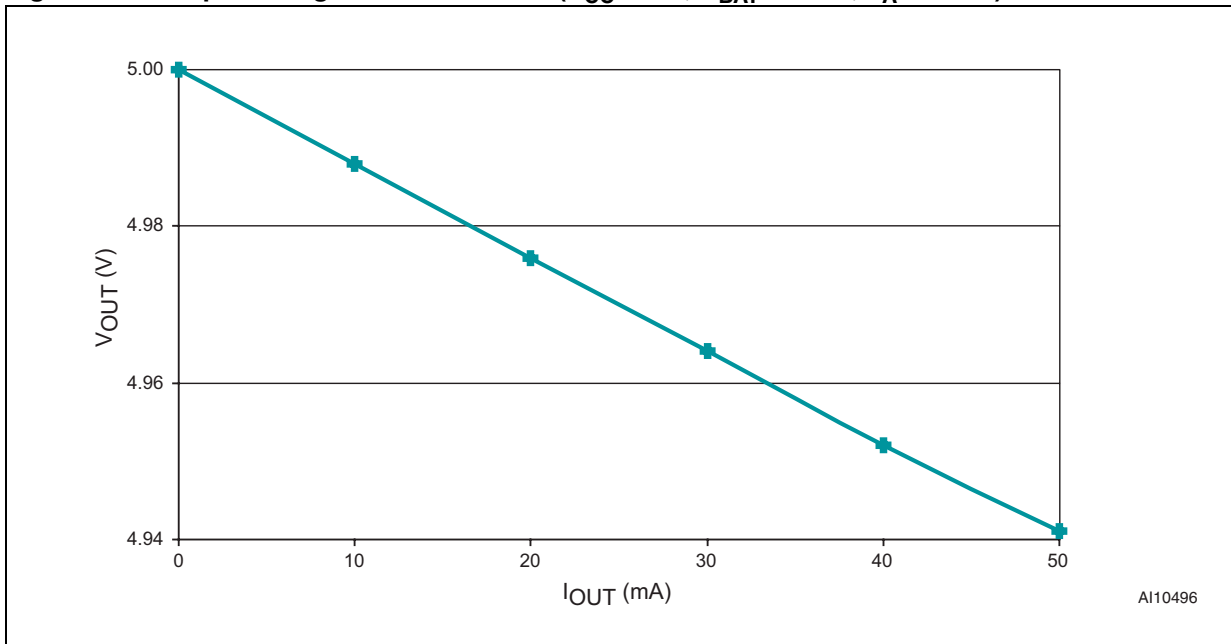


Figure 30. Output voltage vs. load current ( $V_{CC} = 0\text{ V}$ ;  $V_{BAT} = 2.8\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ )

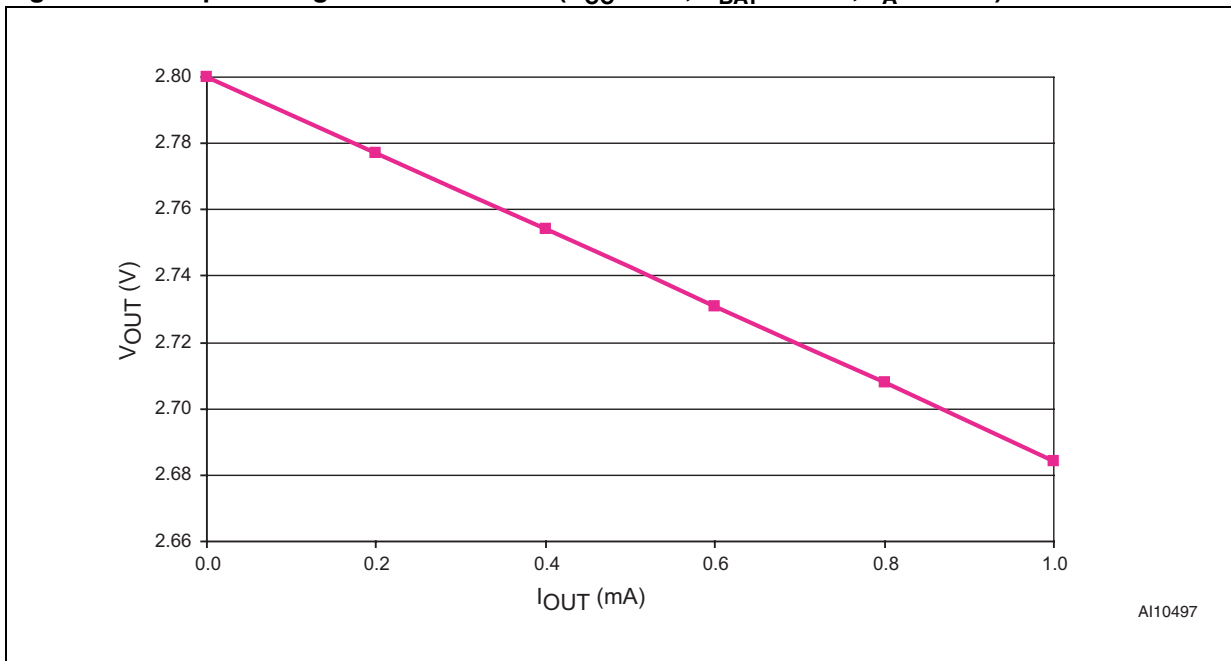


Figure 31.  $\overline{\text{RST}}$  output voltage vs. supply voltage

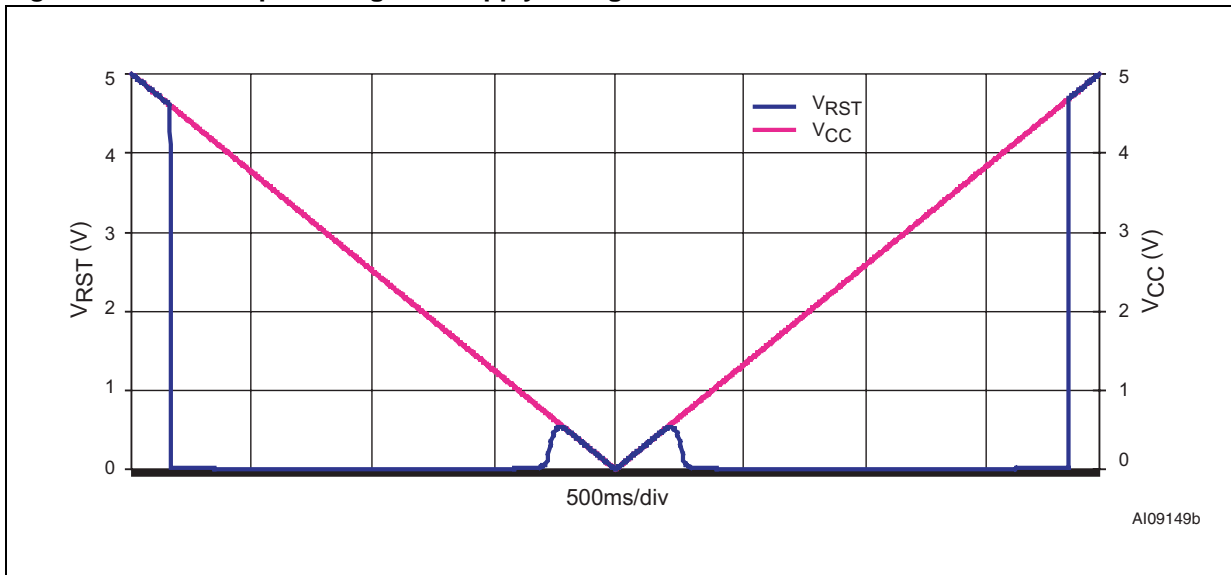


Figure 32. RST output voltage vs. supply voltage

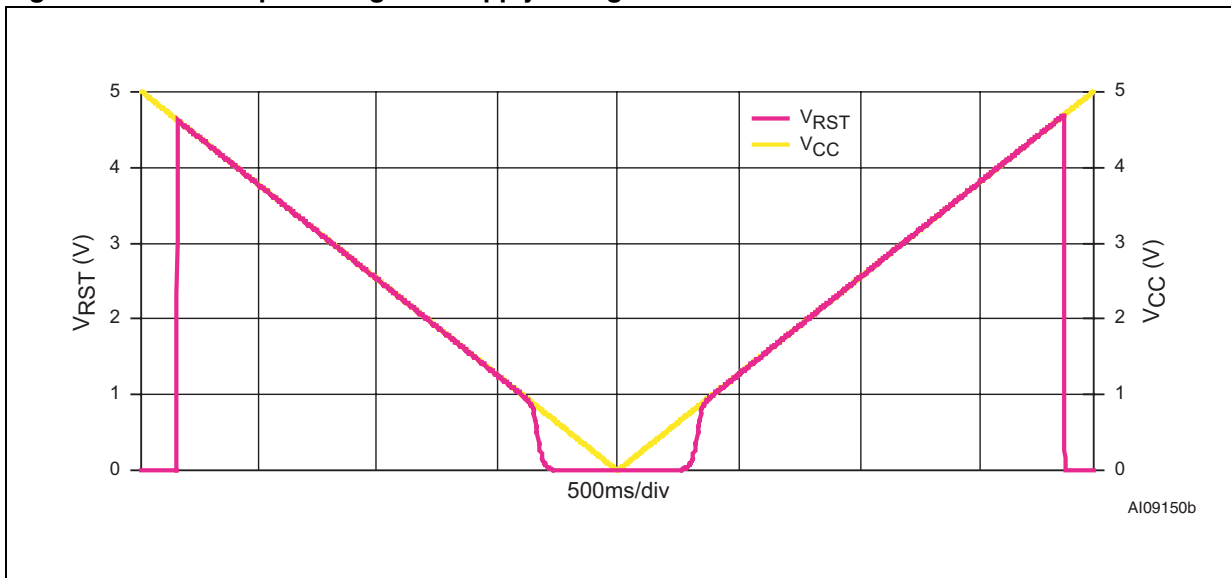


Figure 33.  $\overline{\text{RST}}$  response time (assertion)

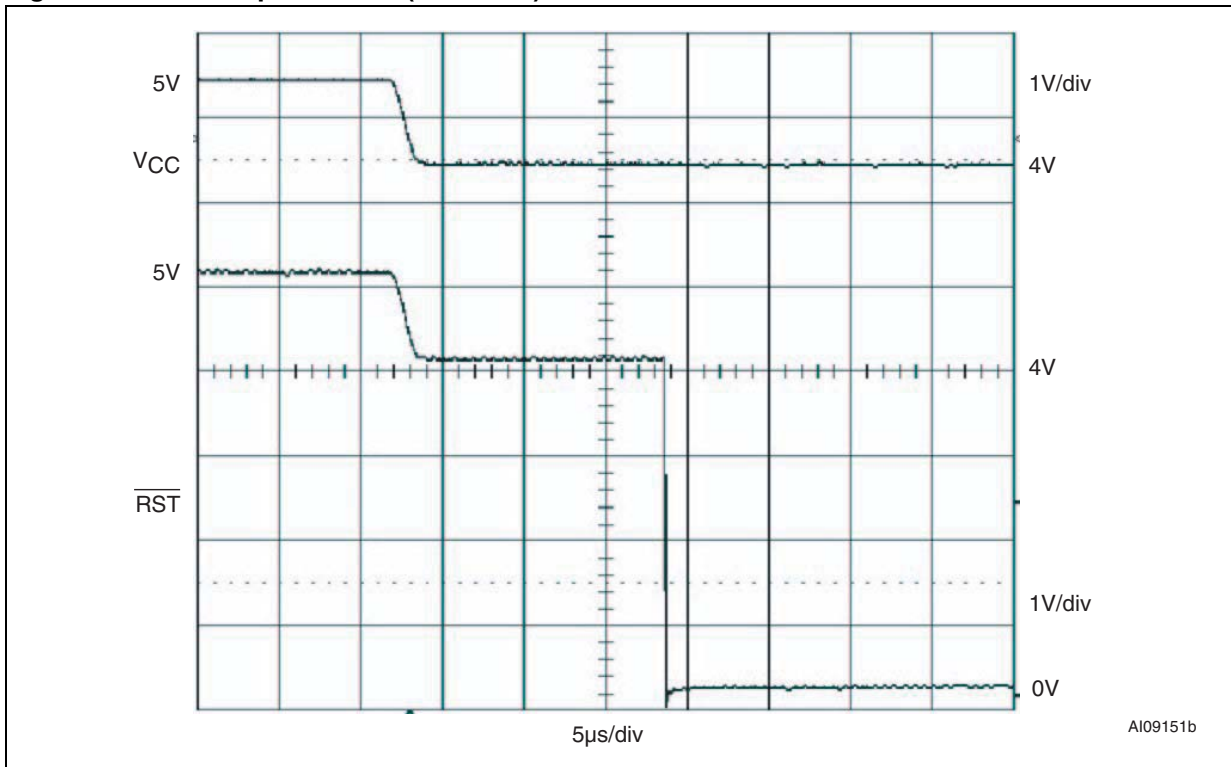


Figure 34. RST response time (assertion)

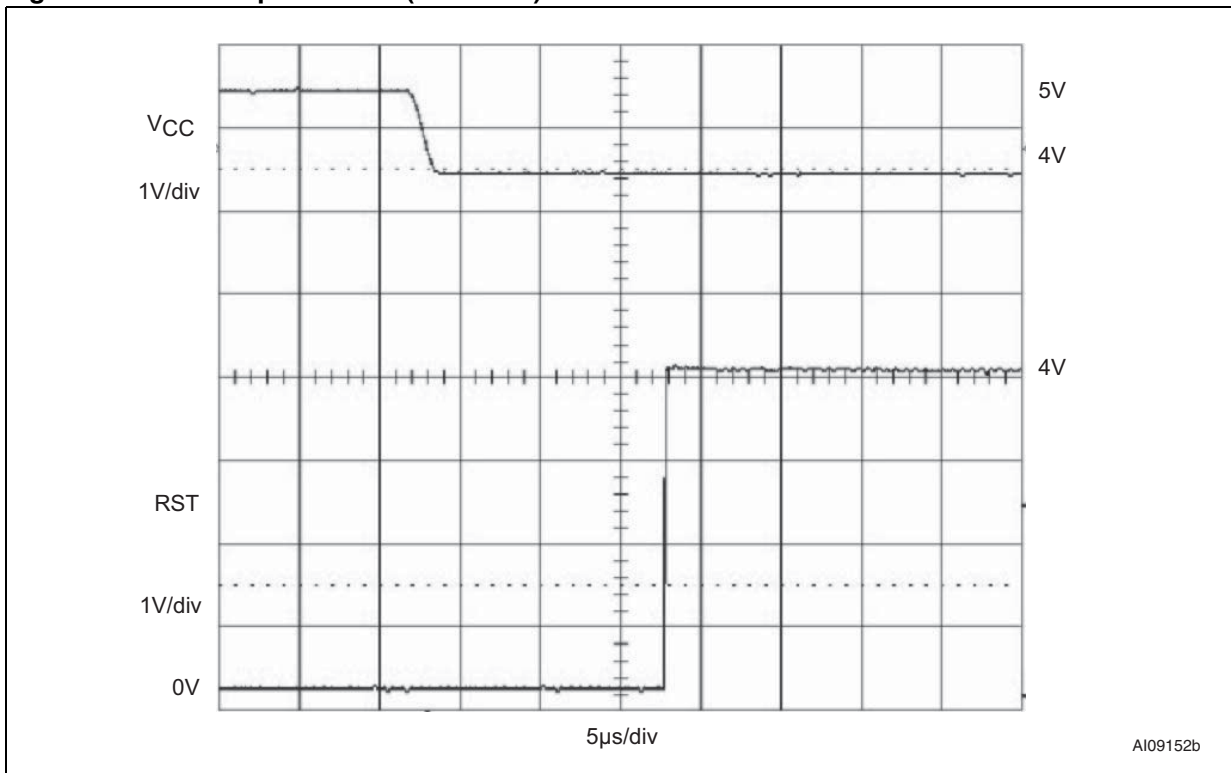


Figure 35. Power-fail comparator response time (assertion)

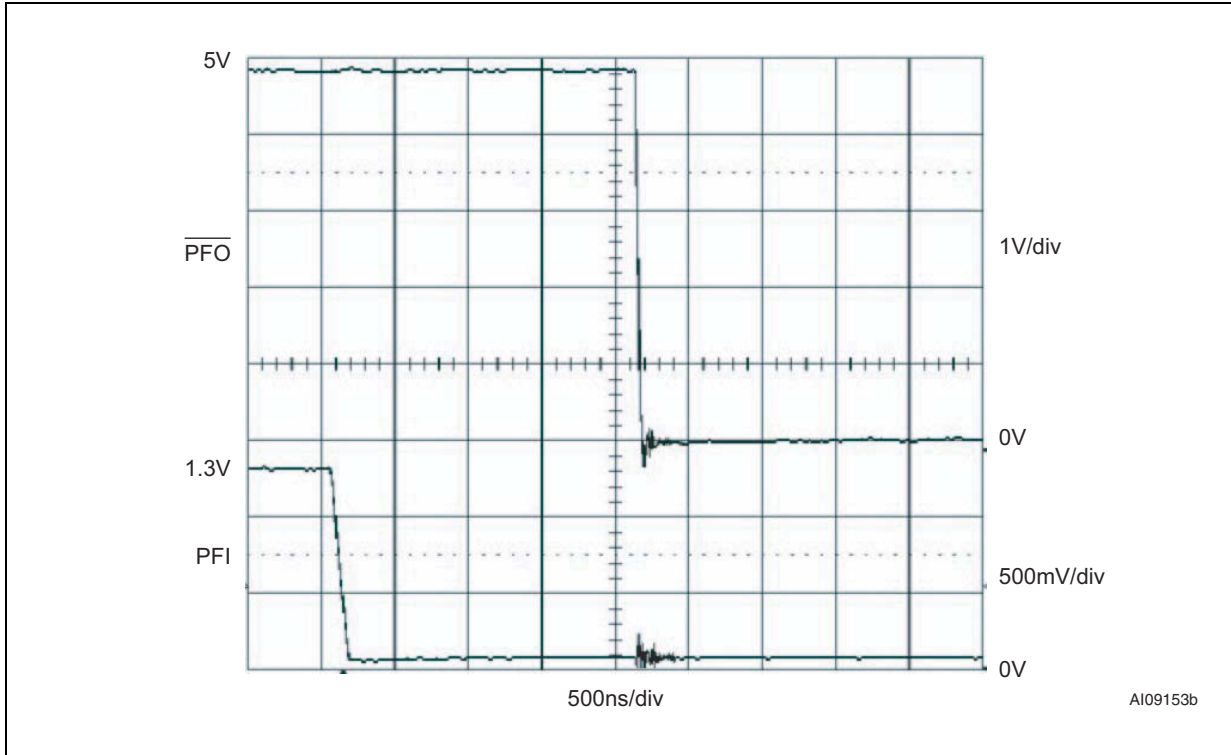


Figure 36. Power-fail comparator response time (de-assertion)

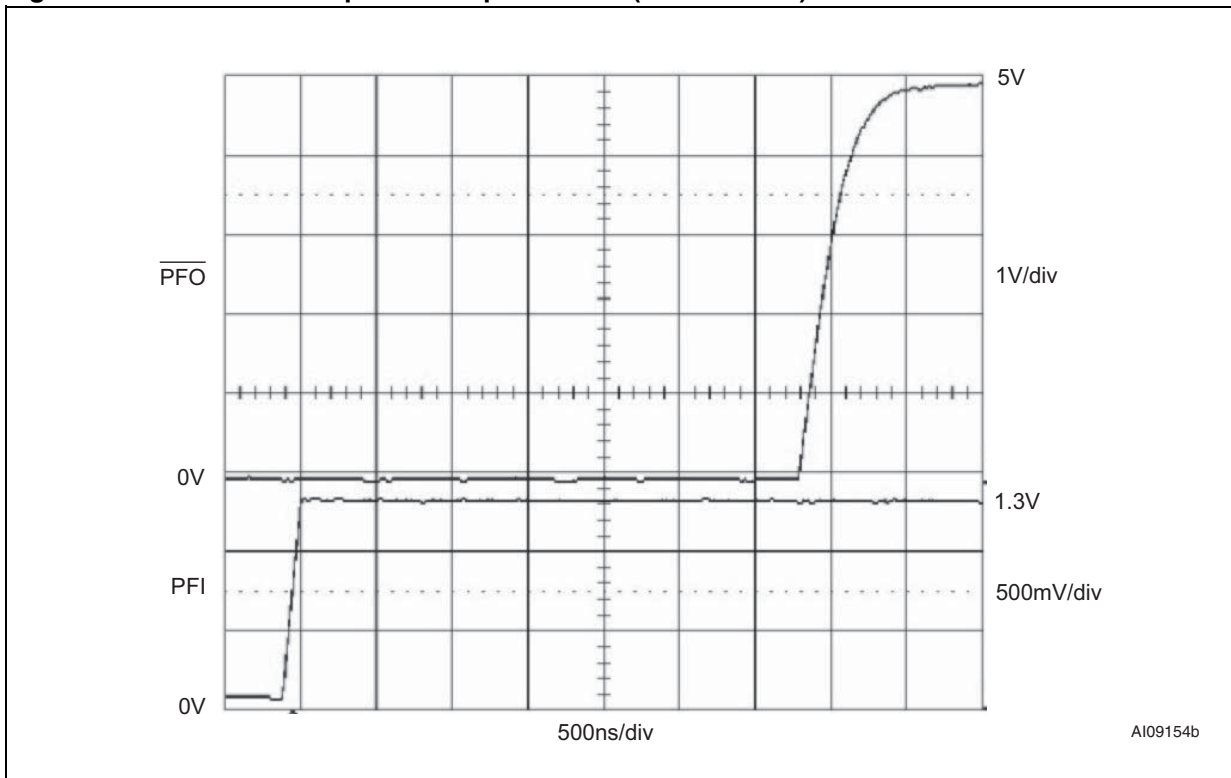


Figure 37. Maximum transient duration vs. reset threshold overdrive

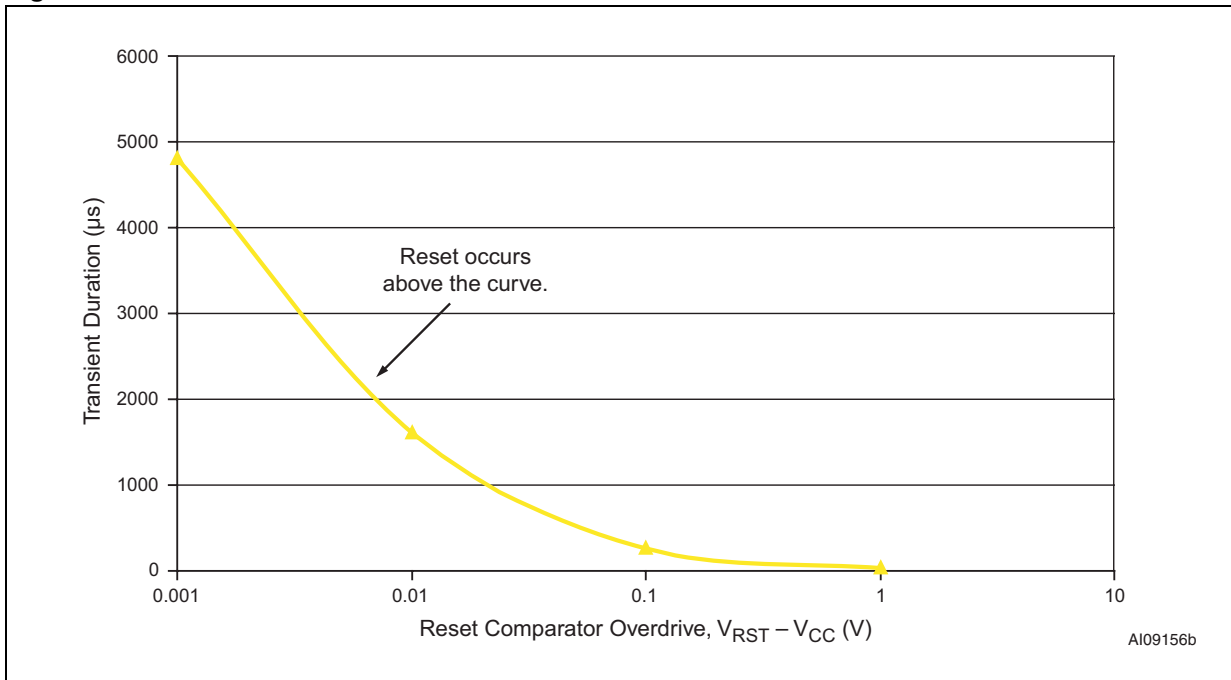
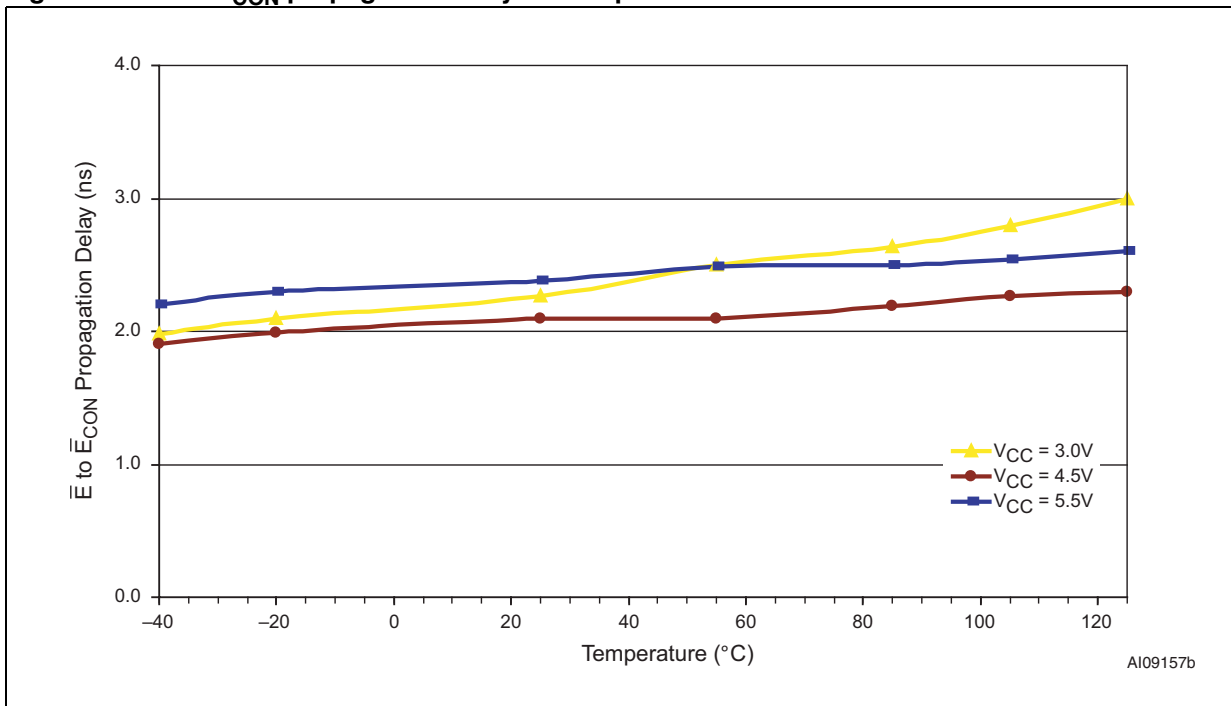


Figure 38.  $\bar{E}$  to  $\bar{E}_{CON}$  propagation delay vs. temperature



## 4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)	-55 to 150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
$V_{IO}$	Input or output voltage	-0.3 to $V_{CC} + 0.3$	V
$V_{CC}/V_{BAT}$	Supply voltage	-0.3 to 6.0	V
$I_O$	Output current	20	mA
$P_D$	Power dissipation	320	mW

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

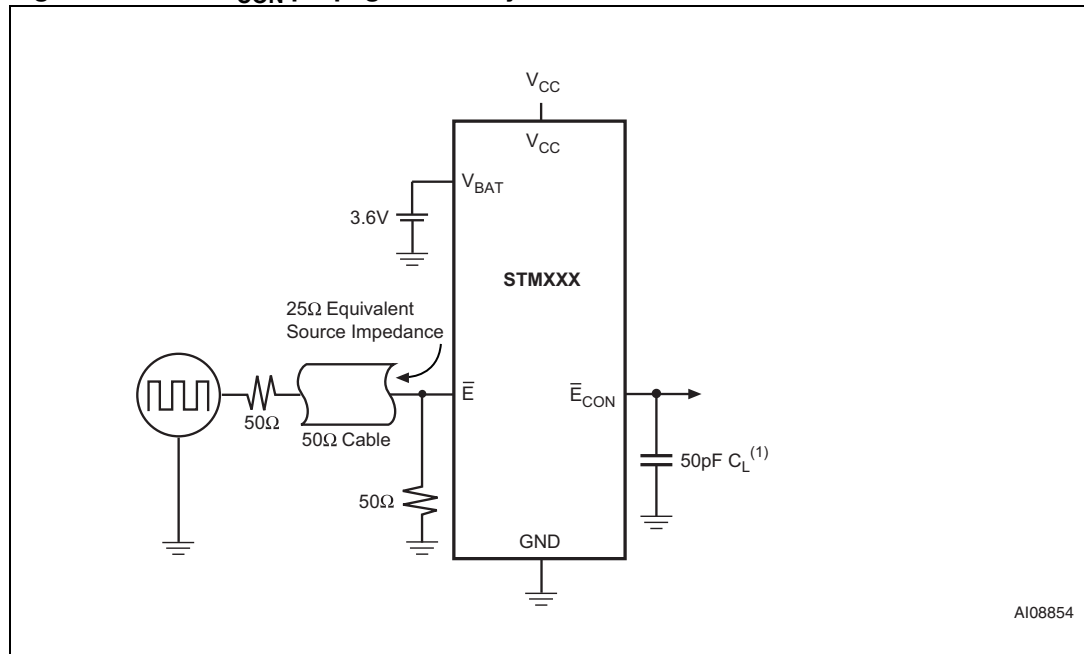
## 5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the measurement conditions summarized in [Table 6: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 6. Operating and AC measurement conditions**

Parameter	STM690A/692A/703/704/802/805/817/818/819	Unit
V <sub>CC</sub> /V <sub>BAT</sub> supply voltage	1.0 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	-40 to 85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8V <sub>CC</sub>	V
Input and output timing ref. voltages	0.3 to 0.7V <sub>CC</sub>	V

**Figure 39.  $\bar{E}$  to  $\bar{E}_{CON}$  propagation delay test circuit**



1. C<sub>L</sub> includes load capacitance and scope probe capacitance.

Figure 40. AC testing input/output waveforms

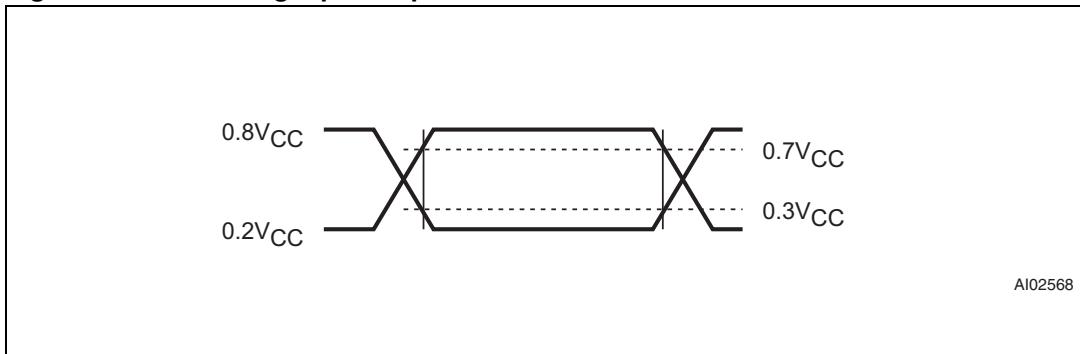
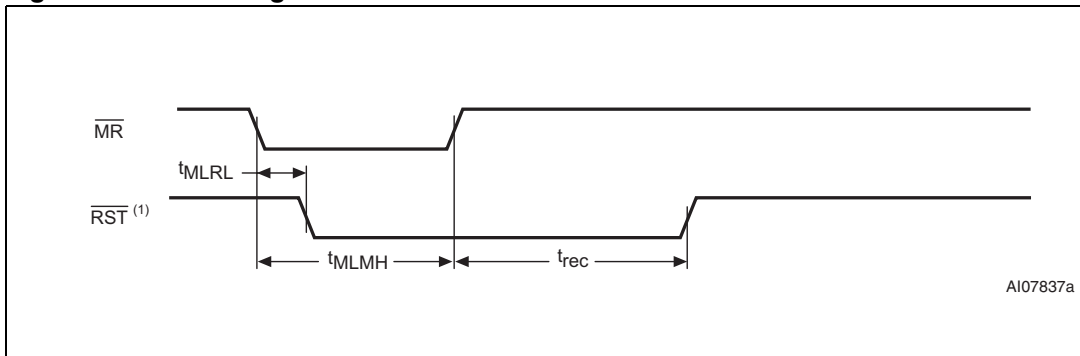


Figure 41.  $\overline{MR}$  timing waveform



1. RST for STM805.

Figure 42. Watchdog timing

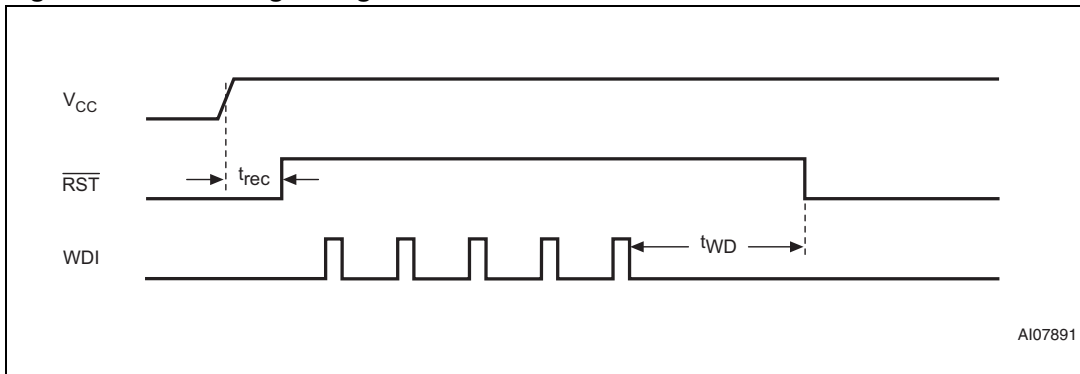


Table 7. DC and AC characteristics

Sym	Alternative	Description	Test condition <sup>(1)</sup>	Min	Typ	Max	Unit	
$V_{CC}, V_{BAT}^{(2)}$		Operating voltage	$T_A = -40$ to $+85$ °C	1.2 <sup>(3)</sup>		5.5	V	
$I_{CC}$		$V_{CC}$ supply current	Excluding $I_{OUT}$ ( $V_{CC} < 5.5$ V)		25	60	$\mu$ A	
		$V_{CC}$ supply current in battery backup mode	Excluding $I_{OUT}$ ( $V_{BAT} = 2.3$ V, $V_{CC} = 2.0$ V, $\overline{MR} = V_{CC}$ )		25	35	$\mu$ A	
$I_{BAT}^{(4)}$		$V_{BAT}$ supply current in battery backup mode	Excluding $I_{OUT}$ ( $V_{BAT} = 3.6$ V)		0.4	1.0	$\mu$ A	
$V_{OUT1}$		$V_{OUT}$ voltage (active)	$I_{OUT1} = 5$ mA <sup>(5)</sup>	$V_{CC} - 0.03$	$V_{CC} - 0.015$		V	
			$I_{OUT1} = 75$ mA	$V_{CC} - 0.3$	$V_{CC} - 0.15$		V	
			$I_{OUT1} = 250$ $\mu$ A, $V_{CC} > 2.5$ V <sup>(5)</sup>	$V_{CC} - 0.0015$	$V_{CC} - 0.0006$		V	
$V_{OUT2}$		$V_{OUT}$ voltage (battery backup)	$I_{OUT2} = 250$ $\mu$ A, $V_{BAT} = 2.3$ V	$V_{BAT} - 0.1$	$V_{BAT} - 0.034$		V	
			$I_{OUT2} = 1$ mA, $V_{BAT} = 2.3$ V		$V_{BAT} - 0.14$		V	
		$V_{CC}$ to $V_{OUT}$ on-resistance			3	4	$\Omega$	
		$V_{BAT}$ to $V_{OUT}$ on-resistance			100		$\Omega$	
$I_{LI}$		Input leakage current ( $\overline{MR}$ )	$4.5$ V $< V_{CC} < 5.5$ V	75	125	300	$\mu$ A	
		Input leakage current (PFI)	$0$ V $< V_{IN} < V_{CC}$	-25	2	+25	nA	
		Input leakage current (WDI) <sup>(6)</sup>	WDI = $V_{CC}$ , time average			120	160	$\mu$ A
			WDI = GND, time average		-20	-15		$\mu$ A
$V_{IH}$		Input high voltage ( $\overline{MR}$ )	$4.5$ V $< V_{CC} < 5.5$ V	2.0			V	
$V_{IH}$		Input high voltage (WDI)	$V_{RST}$ (max) $< V_{CC} < 5.5$ V	$0.7V_{CC}$			V	
$V_{IL}$		Input low voltage ( $\overline{MR}$ )	$4.5$ V $< V_{CC} < 5.5$ V			0.8	V	
$V_{IL}$		Input low voltage (WDI)	$V_{RST}$ (max) $< V_{CC} < 5.5$ V			$0.3V_{CC}$	V	
$V_{OL}$		Output low voltage ( $\overline{PFO}$ , $\overline{RST}$ , RST)	$V_{CC} = V_{RST}$ (max), $I_{SINK} = 3.2$ mA			0.3	V	
		Output low voltage ( $\overline{ECON}$ )	$V_{CC} = V_{RST}$ (max), $I_{OUT} = 1.6$ mA, $\overline{E} = 0$ V			$0.2V_{CC}$	V	
$V_{OL}$		Output low voltage ( $\overline{RST}$ )	$I_{SINK} = 50$ $\mu$ A, $V_{CC} = 1.0$ V, $V_{BAT} = V_{CC}$ , $T_A = 0$ °C to $85$ °C			0.3	V	
			$I_{SINK} = 100$ $\mu$ A, $V_{CC} = 1.2$ V, $V_{BAT} = V_{CC}$			0.3	V	

Table 7. DC and AC characteristics (continued)

Sym	Alternative	Description	Test condition <sup>(1)</sup>	Min	Typ	Max	Unit	
V <sub>OH</sub>		Output high voltage (RST, RST)	I <sub>SOURCE</sub> = 1 mA V <sub>CC</sub> = V <sub>RST</sub> (max)	2.4			V	
		Output high voltage (E <sub>CON</sub> )	V <sub>CC</sub> = V <sub>RST</sub> (max), I <sub>OUT</sub> = 1.6 mA, E <sub>CON</sub> = V <sub>CC</sub>	0.8V <sub>CC</sub>			V	
		Output high voltage (PFO)	I <sub>SOURCE</sub> = 75 μA, V <sub>CC</sub> = V <sub>RST</sub> (max)	0.8V <sub>CC</sub>			V	
V <sub>OH</sub>		Output high voltage	I <sub>SOURCE</sub> = 4 μA, V <sub>CC</sub> = 1.1 V, V <sub>BAT</sub> = V <sub>CC</sub> , T <sub>A</sub> = 0°C to 85°C			0.8	V	
			I <sub>SOURCE</sub> = 4 μA, V <sub>CC</sub> = 1.2 V, V <sub>BAT</sub> = V <sub>CC</sub>			0.9	V	
V <sub>OHB</sub>		V <sub>OH</sub> battery backup (RST, RST)	I <sub>SOURCE</sub> = 100 μA, V <sub>CC</sub> = 0, V <sub>BAT</sub> = 2.8 V	0.8V <sub>BAT</sub>			V	
		V <sub>OH</sub> battery backup (E <sub>CON</sub> )	I <sub>SOURCE</sub> = 75 μA, V <sub>CC</sub> = 0, V <sub>BAT</sub> = 2.8 V	0.8V <sub>BAT</sub>			V	
<b>Power-fail comparator (NOT available on STM818)</b>								
V <sub>PFI</sub>		PFI input threshold	PFI falling (V <sub>CC</sub> = 5 V)	All other versions	1.20	1.25	1.30	V
			STM802	1.225	1.250	1.275	V	
t <sub>PF</sub>		PFI to PFO propagation delay			2		μs	
I <sub>SC</sub>		PFO output short to GND current	V <sub>CC</sub> = 5 V, V <sub>PFO</sub> = 0 V	0.1	0.75	2.0	mA	
<b>Battery switchover</b>								
V <sub>SO</sub>		Battery backup switchover voltage <sup>(7)(8)</sup> (V <sub>CC</sub> < V <sub>BAT</sub> & V <sub>CC</sub> < V <sub>RST</sub> )	Power-down	V <sub>RST</sub> > V <sub>BAT</sub>		V <sub>BAT</sub>		V
				V <sub>RST</sub> < V <sub>BAT</sub>		V <sub>RST</sub>		V
			Power-up	V <sub>RST</sub> > V <sub>BAT</sub>		V <sub>BAT</sub>		V
				V <sub>RST</sub> < V <sub>BAT</sub>		V <sub>RST</sub>		V
		Hysteresis				40		mV
<b>Reset thresholds</b>								
V <sub>RST</sub>		Reset threshold <sup>(9)</sup>	STM690A/703, STM8XXL	4.50	4.65	4.75	V	
			STM692A/704, STM8XXM	4.25	4.40	4.50	V	
		Reset threshold hysteresis			25		mV	
		V <sub>CC</sub> to RST delay (from V <sub>RST</sub> , V <sub>CC</sub> falling at 10 V/ms)	STM817/818/819		100		μs	

Table 7. DC and AC characteristics (continued)

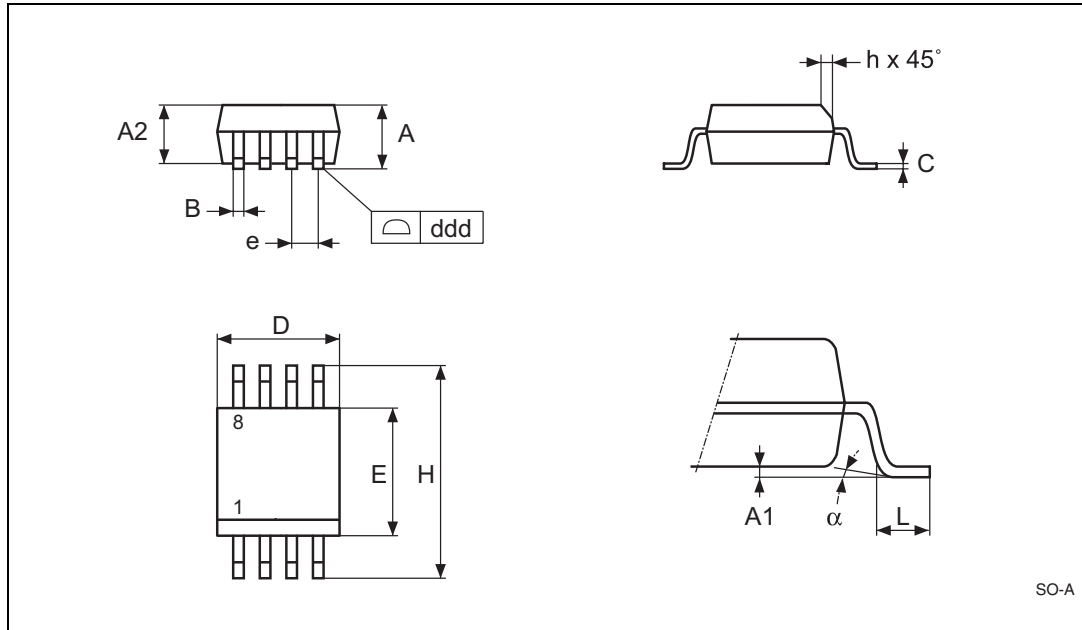
Sym	Alternative	Description	Test condition <sup>(1)</sup>	Min	Typ	Max	Unit
t <sub>REC</sub>		$\overline{RST}$ pulse width		140	200	280	ms
<b>Push-button reset input (STM703/704/819)</b>							
t <sub>MLMH</sub>	t <sub>MR</sub>	$\overline{MR}$ pulse width	STM703/704	150			ns
			STM819	1			μs
t <sub>MLMR</sub>	t <sub>MRD</sub>	$\overline{MR}$ to $\overline{RST}$ output delay	STM703/704			250	ns
			STM819		120		ns
		$\overline{MR}$ glitch immunity	STM819		100		ns
		$\overline{MR}$ pull-up resistor	$\overline{MR} = 0\text{ V}, V_{CC} = 5\text{ V}$	45	63	85	kΩ
<b>Watchdog timer (NOT available on STM703/704/819)</b>							
	t <sub>WD</sub>	Watchdog timeout period	$V_{RST}(\text{max}) < V_{CC} < 5.5\text{ V}$	1.12	1.60	2.24	s
		WDI pulse width	$V_{RST}(\text{max}) < V_{CC} < 5.5\text{ V}$	50			ns
<b>Chip-enable gating (STM818 only)</b>							
		$\overline{E}$ to $\overline{E}_{CON}$ resistance	$V_{CC} = V_{RST}(\text{max})$		40	150	Ω
		$\overline{E}$ to $\overline{E}_{CON}$ propagation delay	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$		2	7	ns
		Reset to $\overline{E}_{CON}$ high delay	(Power-down)		15		μs
		$\overline{E}_{CON}$ short circuit current	$V_{CC} = 5\text{ V}$ , disable mode, $\overline{E} = \text{logic high}, \overline{E}_{CON} = 0\text{ V}$	0.1	0.75	2.0	mA

- Valid for ambient operating temperature:  $T_A = -40$  to  $85\text{ °C}$ ;  $V_{CC} = 4.75\text{ V}$  to  $5.5\text{ V}$  for “L” versions;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$  for “M” versions; and  $V_{BAT} = 2.8\text{ V}$  (except where noted).
- $V_{CC}$  supply current, logic input leakage, watchdog functionality, push-button reset functionality, PFI functionality, state of  $\overline{RST}$  and  $RST$  tested at  $V_{BAT} = 3.6\text{ V}$ , and  $V_{CC} = 5.5\text{ V}$ . The state of  $\overline{RST}$  or  $RST$  and  $\overline{PFO}$  is tested at  $V_{CC} = V_{CC}(\text{min})$ . Either  $V_{CC}$  or  $V_{BAT}$  can go to  $0\text{ V}$  if the other is greater than  $2.0\text{ V}$ .
- $V_{CC}(\text{min}) = 1.0\text{ V}$  for  $T_A = 0\text{ °C}$  to  $+85\text{ °C}$ .
- Tested at  $V_{BAT} = 3.6\text{ V}$ ,  $V_{CC} = 3.5\text{ V}$  and  $0\text{ V}$ .
- Guaranteed by design.
- WDI input is designed to be driven by a three-state output device. To float WDI, the “high impedance mode” of the output device must have a maximum leakage current of  $10\text{ μA}$  and a maximum output capacitance of  $200\text{ pF}$ . The output device must also be able to source and sink at least  $200\text{ μA}$  when active.
- When  $V_{BAT} > V_{CC} > V_{RST}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below  $V_{RST}$ .
- When  $V_{RST} > V_{CC} > V_{BAT}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below the battery voltage ( $V_{BAT}$ ) –  $75\text{ mV}$ .
- For  $V_{CC}$  falling.

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Figure 43. SO8 - 8-lead plastic small outline, 150 mils body width, package mechanical drawing**

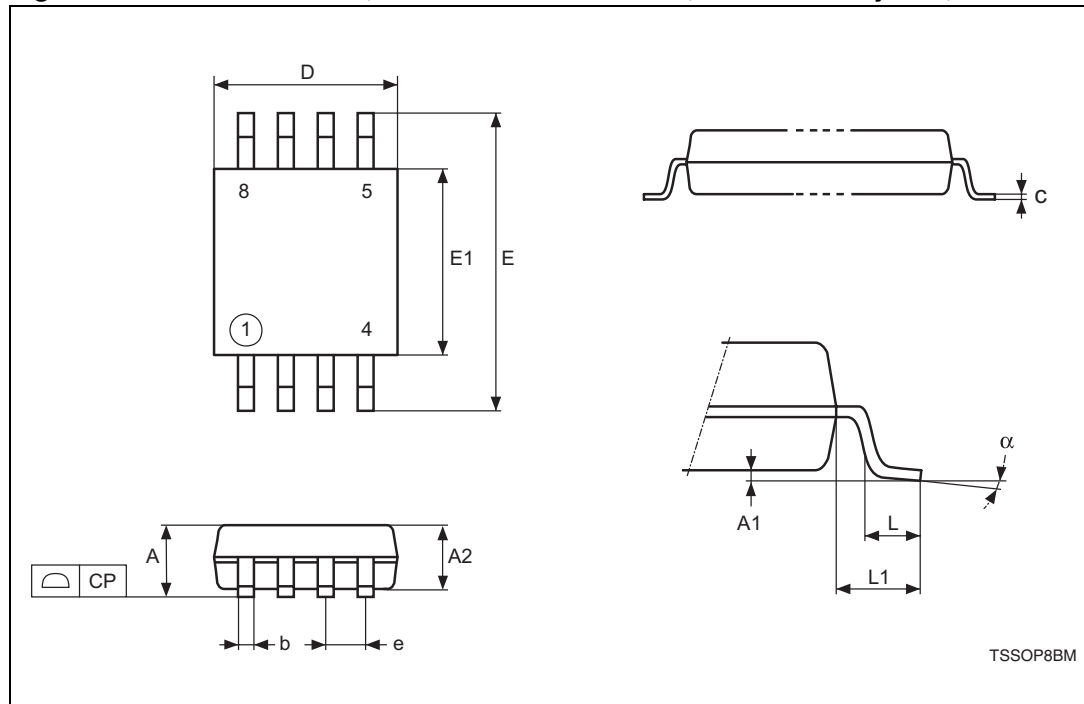


Note: Drawing is not to scale.

**Table 8. SO8 - 8-lead plastic small outline, 150 mils body width, package mechanical data**

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
B	-	0.33	0.51	-	0.013	0.020
C	-	0.19	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
ddd	-	-	0.10	-	-	0.004
E	-	3.80	4.00	-	0.150	0.157
e	1.27	-	-	0.050	-	-
H	-	5.80	6.20	-	0.228	0.244
h	-	0.25	0.50	-	0.010	0.020
L	-	0.40	0.90	-	0.016	0.035
α	-	0°	8°	-	0°	8°
N	8			8		

Figure 44. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, outline



Note: Drawing is not to scale.

Table 9. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	-	-	1.10	-	-	0.043
A1	-	0.05	0.15	-	0.002	0.006
A2	0.85	0.75	0.95	0.034	0.030	0.037
b	-	0.25	0.40	-	0.010	0.016
c	-	0.13	0.23	-	0.005	0.009
CP	-	-	0.10	-	-	0.004
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65	-	-	0.026	-	-
E	4.90	4.65	5.15	0.193	0.183	0.203
E1	3.00	2.90	3.10	0.118	0.114	0.122
L	0.55	0.40	0.70	0.022	0.016	0.030
L1	0.95	-	-	0.037	-	-
alpha	-	0°	6°	-	0°	6°
N	8			8		

# 7 Part numbering

**Table 10. Ordering information scheme**

Example:	STM690A	M	6	E
<b>Device type</b>	STM690A/692A/703/704/802/805/817/818/819			
<b>Threshold voltage</b>	STM690A, STM703: blank: $V_{RST} = 4.50\text{ V to }4.75\text{ V}$ STM692A, STM704: blank: $V_{RST} = 4.25\text{ V to }4.50\text{ V}$ STM8xx: L: $V_{RST} = 4.50\text{ V to }4.75\text{ V}$ M: $V_{RST} = 4.25\text{ V to }4.50\text{ V}$			
<b>Package</b>	M = SO8 DS <sup>(1)</sup> = TSSOP8			
<b>Temperature range</b>	6: -40 °C to 85 °C			
<b>Shipping method</b>	E = ECOPACK® package, tubes F = ECOPACK® package, tape & reel			

1. Contact local ST sales office for availability.

For other options or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 11. Marking description

Part number	Reset threshold	Package	Topside marking
STM690A	4.65 V	SO8	690A
STM692A	4.40 V	SO8	692A
STM703	4.65 V	SO8	703
STM704	4.40 V	SO8	704
STM802L	4.65 V	SO8	802L
STM802M	4.40 V	SO8	802M
STM805L	4.65 V	SO8	805L
STM817L	4.65 V	SO8	817L
		TSSOP8	
STM817M	4.40 V	SO8	817M
		TSSOP8	
STM818L	4.65 V	SO8	818L
		TSSOP8	
STM818M	4.40 V	SO8	818M
		TSSOP8	
STM819L	4.65 V	SO8	819L
		TSSOP8	
STM819M	4.40 V	SO8	819M
		TSSOP8	

## 8 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
Oct-2003	1	Initial release.
31-Oct-2003	1.1	Update DC characteristics ( <a href="#">Table 7</a> ).
22-Dec-2003	2	Reformatted; updated characteristics (cover page, <a href="#">Figure 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 16, Table 3, 4, 7, 9, 11</a> ).
16-Jan-2004	2.1	Add typical characteristics ( <a href="#">Figure 18, 19, 21, 22, 24, 25, 26, 27, 28, 31, 32, 33, 34, 35, 36, 37, 38</a> ).
08-Apr-2004	2.2	Update characteristics ( <a href="#">Figure 12, 22, 28, 32, 33, 34, 37; Table 1, 7</a> ).
25-May-2004	3	Remove references to “open drain” (cover page, <a href="#">4, 7; Table 2</a> ); update characteristics ( <a href="#">Table 3, 7</a> ).
05-Jul-2004	4	Update package availability, pin description; promote document (cover page, <a href="#">Figure 13, 14; Table 3, 7, 10</a> ).
29-Sep-2004	5	Clarify root part numbers, pin descriptions ( <a href="#">Figure 10, 12, 39; Table 7, 10</a> ).
01-Mar-2005	6	Update characteristics ( <a href="#">Figure 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38</a> ).
20-Jan-2006	7	Correct marking, update lead-free text ( <a href="#">Table 10, 11</a> )
21-Oct-2008	8	Reformatted, minor text changes; updated <a href="#">Table 3, 4, 7, 10, Figure 9, 10, 11, 12, 16, 39, Section 6: Package mechanical data</a> .
20-Nov-2009	9	Updated text in <a href="#">Section 6, Table 5</a> .
18-Aug-2010	10	Updated <a href="#">Section 2.4: Backup battery switchover</a> .

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