

# LB11862MC

## Fan Motor Driver, Single-Phase, Full-Wave



**ON Semiconductor**<sup>®</sup>  
www.onsemi.com

### Overview

Single-phase full-wave drive design and a compact package make these ICs optimal for small fans (especially CPU cooling fans). Low switching noise and effective motor drive are further advantages.

### Features

- Single-phase full-wave drive
- Built-in thermal shutdown circuit.
- Built-in lock protection and automatic recovery circuits

### Typical Applications

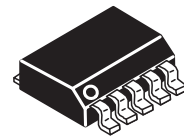
- PC power supply system
- CPU cooling fan system
- Refrigerator
- PC

### SPECIFICATION

#### ABSOLUTE MAXIMUM RATINGS at Ta = 25°C (Note 1)

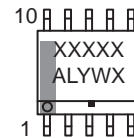
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub> max		17	V
Output current	I <sub>OUT</sub> max		0.8	A
Output withstand voltage	V <sub>OUT</sub> max		17	V
Output withstand voltage on RD output pin	V <sub>R</sub> max		17	V
RD output current	I <sub>R</sub> max		5	mA
HB output current	I <sub>B</sub> max		10	mA
Input voltage ST pin	V <sub>ST</sub> max		15	V
Allowable power dissipation	P <sub>d</sub> max	When mounted on a circuit board (Note 2)	0.75	W
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Specified circuit board : 114.3 × 76.1 × 1.6mm<sup>3</sup>, glass epoxy
3. Absolute maximum ratings represent the values which cannot be exceeded even for a moment
4. If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation



SOIC-10

#### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

#### ORDERING INFORMATION

Ordering Code:  
LB11862MC-AH

Package  
SOIC-10  
(Pb-Free / Halogen Free)

Shipping (Qty / packing)  
2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.  
[http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

# LB11862MC

## Recommended Operating Conditions at $T_a = 25^\circ\text{C}$ (Note 5)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		3.8 to 16.8	V
ST input High-level voltage	$V_{STH}$		3 to 14	V
ST input Low-level voltage	$V_{STL}$		-0.3 to 0.4	V
Hall input common-mode input voltage range	VICM		0.2 to $V_{CC}-1.5$	V

5. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## Electrical Characteristics Unless otherwise specified $T_a = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$ (Note 6)

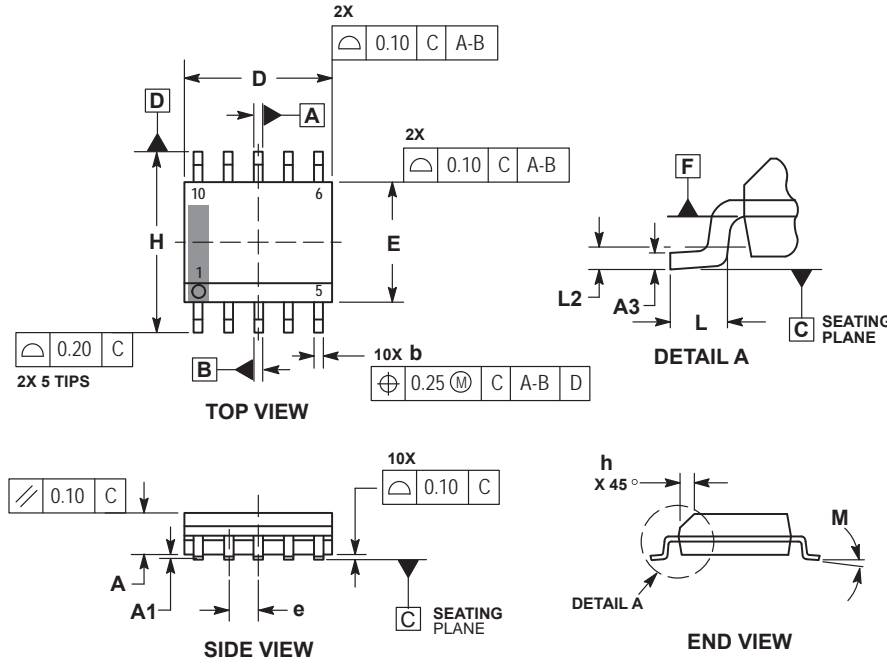
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC1}$	Operation mode (CT=L, ST=L)		12	17	mA
	$I_{CC2}$	Lock protection mode (CT=H, ST=L)		2.5	4.0	mA
	$I_{CC2}$	Standby mode (ST=H)		110	150	$\mu\text{A}$
Lock detection capacitor charging current	$I_{CT1}$	$V_{CT} = 0.2\text{V}$	1.5	2.1	3.0	$\mu\text{A}$
Capacitor discharging current	$I_{CT2}$	$V_{CT} = 3.0\text{V}$	0.21	0.35	0.50	$\mu\text{A}$
Capacitor charging / discharging current ratio	$R_{CT}$	$R_{CD} = I_{CT1}/I_{CT2}$	5.0	6.0	8.0	
CT charging voltage	$V_{CT1}$		2.55	2.75	2.95	V
CT discharging voltage	$V_{CT2}$		1.6	1.8	2.0	V
Output Low-level voltage	$V_{OL}$	$I_O = 200\text{mA}$		0.2	0.3	V
Output High-level voltage	$V_{OH}$	$I_O = 200\text{mA}$	3.9	4.1		V
Hall input sensitivity	$V_{HN}$	Zero peak value (including offset hysteresis)		7	15	mA
RD output pin Low-level voltage	$V_{RD\text{L}}$	$I_{RD} = 5\text{mA}$		0.1	0.3	V
RD output pin leakage current	$I_{RD\text{L}}$	$V_{RD} = 15\text{V}$			30	$\mu\text{A}$
HB output Low-level voltage	$V_{HBL}$	$I_{HB} = 5\text{mA}$		1.0	1.3	V
ST pin input current	$I_{ST}$	$V_{ST} = 5\text{V}$		75	100	$\mu\text{A}$

6. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Package Dimensions**

unit : mm

**SOIC-10 NB**  
CASE 751BQ  
ISSUE B

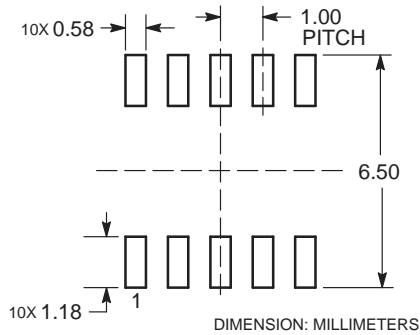


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

MILLIMETERS		
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	0.80
L2	0.25 BSC	
M	0°	8°

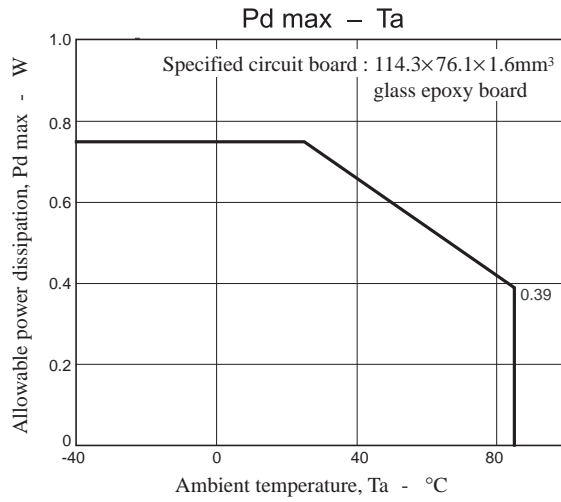
**RECOMMENDED SOLDERING FOOTPRINT\***



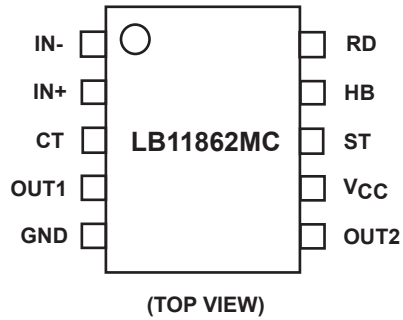
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# LB11862MC

## Pdmax-Ta graph



## Pin Assignment



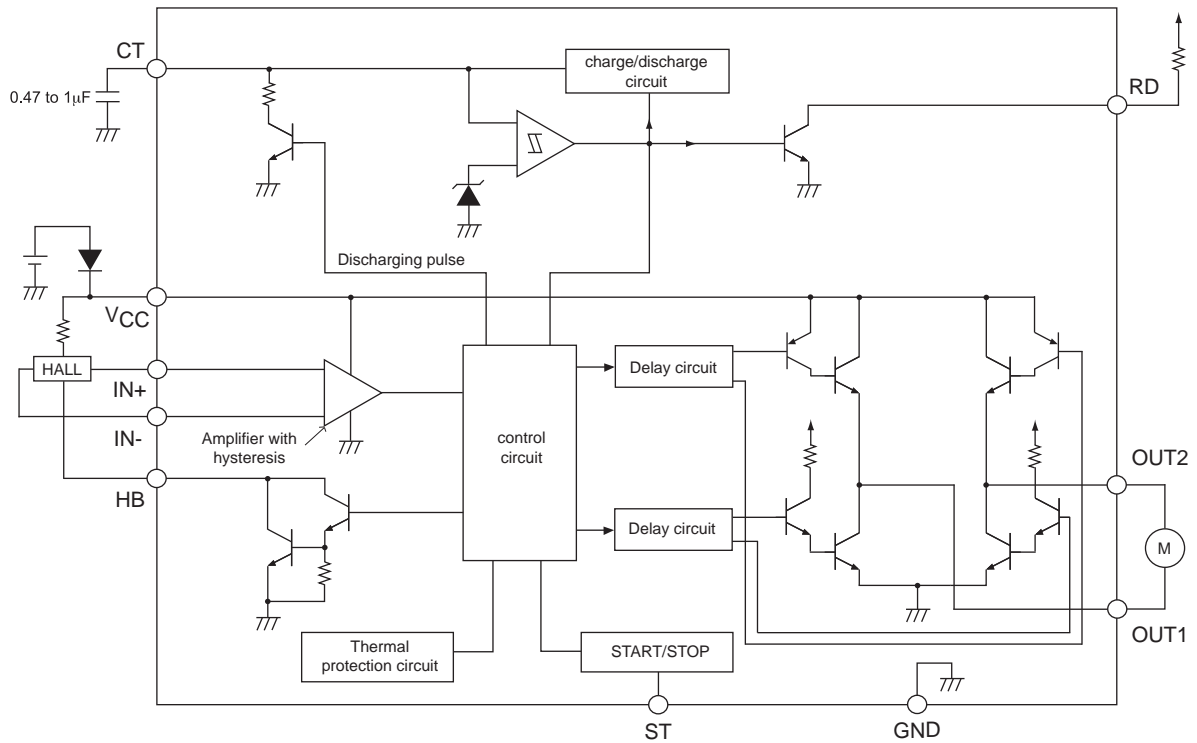
## Truth Table

ST	IN-	IN+	CT	OUT1	OUT2	RD	HB	Mode
High	-	-	-	OFF	OFF	OFF	OFF	Standby
Low	High	Low	Low	High	Low	Low	Low	Operating
	Low	High		Low	High			
			High	OFF	OFF	OFF	Low	Lock protection

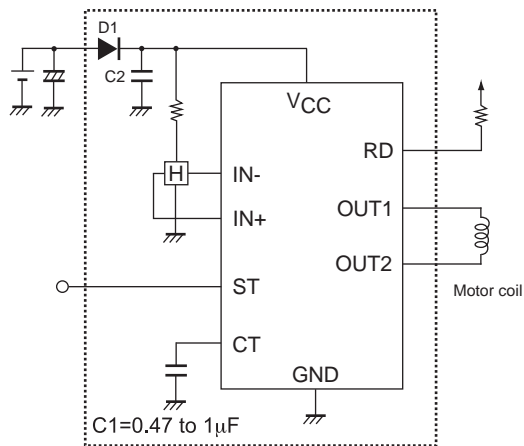
(The RD output is latched at "Low"-level in operating mode and "High"-level in stop mode.)

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## Block Diagram



## Application Circuit Example





1. D1 is for protection against breakdown in case of reverse connection of power supply and mat is deleted when there is no problem.
2. C2 is necessary to allow the kick-back regenerative current to flow when C2 is to be used with the coil current of 500mA or more.
3. CT to be connected to GND when not used.
4. RD, ST and HB pins to be OPEN when not used.

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