



**THE DATASHEET OF  
TSU6111ARSVR**



## USB Port SP2T Switch Supports USB & UART

 Check for Samples: [TSU6111A](#)

### FEATURES

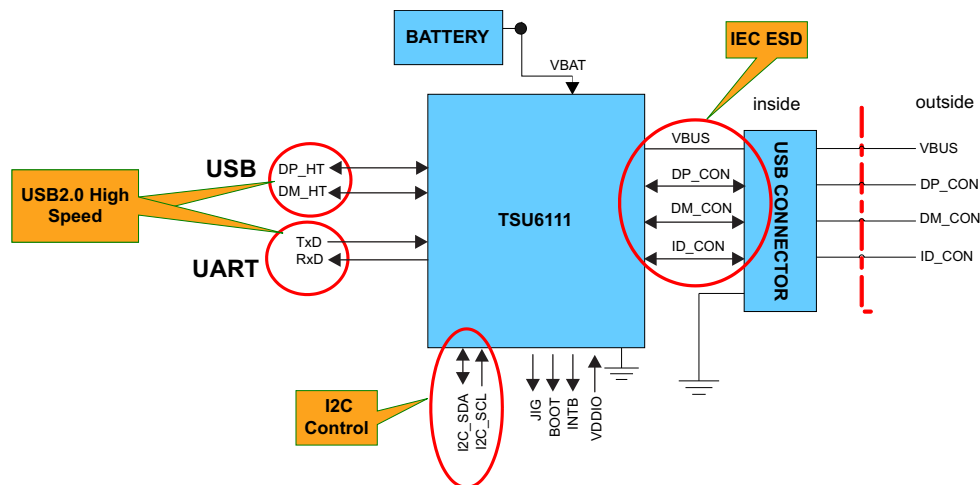
- **Switch Matrix**
  - USB
  - UART Supports USB 2.0 High Speed
- **Charger Detection**
  - USB BCDv1.1 Compliant
  - VBUS Detection
  - Data Contact Detection
  - Primary and Secondary Detection
- **Compatible Accessories**
  - USB Chargers (DCP, CDP)
  - Factory Cable
- **Additional Features**
  - I<sup>2</sup>C Interface with Host Processor
  - Switches Controlled by Automatic Detection or Manual Control
  - Interrupts Generated for Plug/Unplug
  - Support Control Signals used In Manufacturing (JIG, BOOT)

- **Max Voltage**
  - 28V VBUS rating
- **ESD Performance Tested Per JESD 22**
  - 5000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **IEC ESD Performance**
  - ±8kV Contact Discharge (IEC 61000-4-2) for VBUS/DP\_CON/DM\_CON/ID\_CON to GND
- **Surge Protection on VBUS/DP\_CON/DM\_CON**
  - USB Connector Pins Without External Component

### APPLICATIONS

- Cell Phones and Smart Phones
- Tablet PCs
- Digital Cameras and Camcorders
- GPS Navigation Systems
- Micro USB interface with USB/UART

### TYPICAL APPLICATION DIAGRAM



### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	uQFN 0.4-mm pitch – RSV Tape and Reel	TSU6111ARSVR	ZTN

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



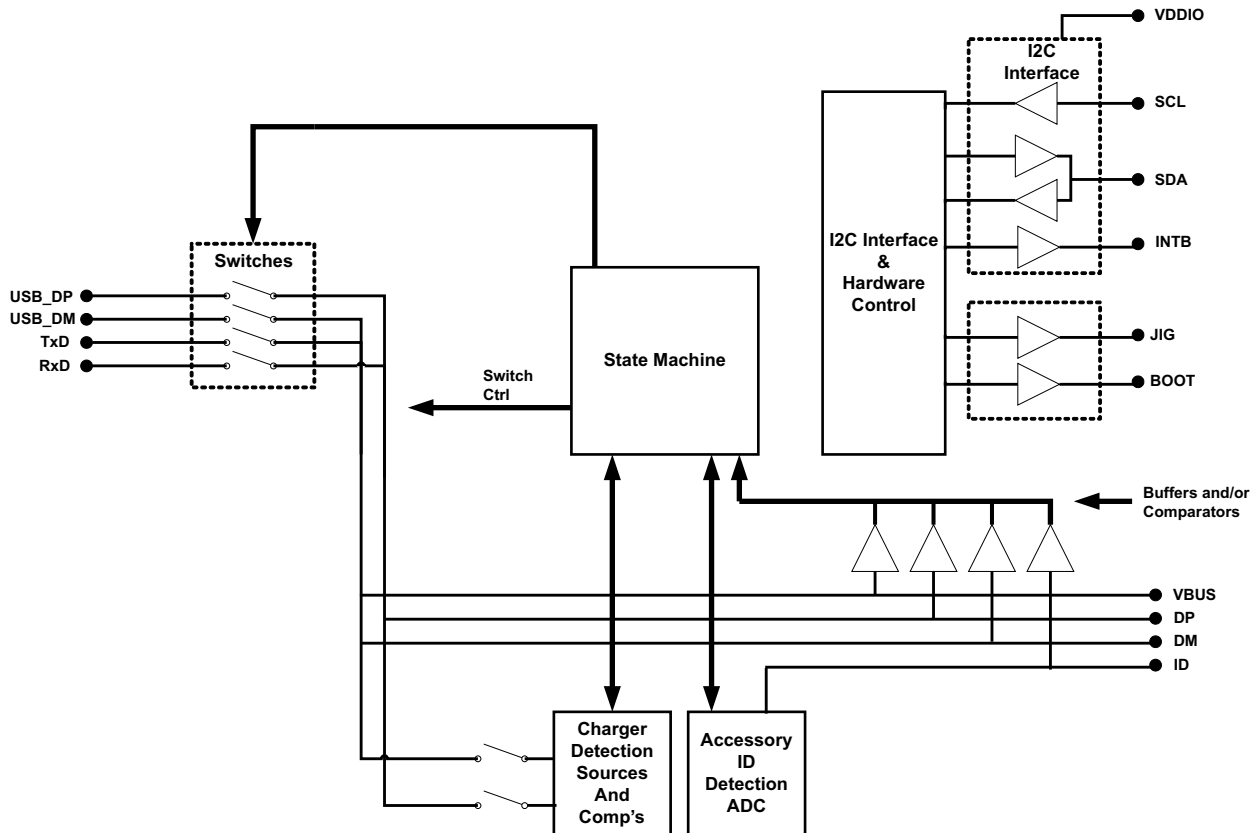
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### DESCRIPTION

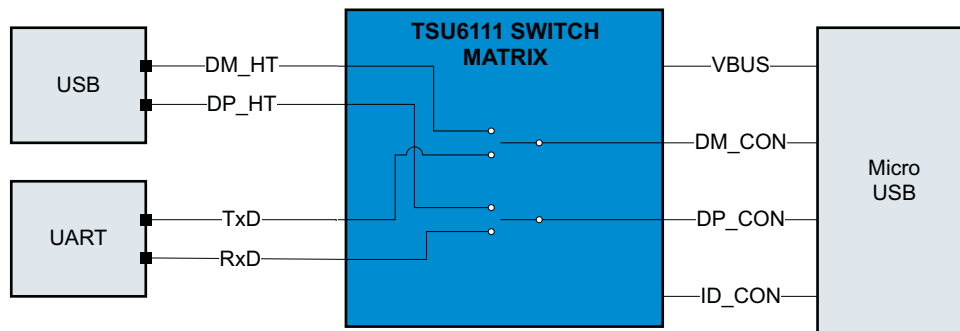
The TSU6111A is a high performance differential autonomous SP2T switch with impedance detection. The switch supports the detection of various accessories that are attached through DP, DM, and ID. The charger detection satisfies USB charger specification v1.1 and  $V_{BUS\_IN}$  has a 28V tolerance to eliminate the need for external protection. Power for this device is supplied through VBAT of the system or through  $V_{BUS\_IN}$  when attached to a charger.

The SP2T switch is controlled by the automatic detection logic or through manual configuration of the I<sup>2</sup>C. JIG and BOOT pins are used when a USB or UART JIG cable is used to test the device in the development and manufacturing. TSU6111A has open-drain JIG output (active low).

### BLOCK DIAGRAM

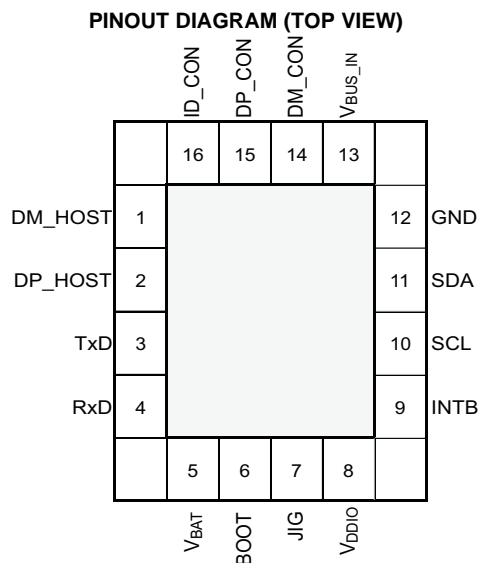


### SWITCH MATRIX





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



**PIN FUNCTIONS**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DM_HOST	I/O	USB DM connected to host
2	DP_HOST	I/O	USB DP connected to host
3	TxD	I/O	UART Tx
4	RxD	I/O	UART Rx
5	VBAT	I	Connected to battery
6	BOOT	O	BOOT mode out (push-pull). Used for factory test modes.
7	JIG	O	JIG detection JIG detection (Open-drain). Used for factory test modes
8	VDDIO	O	I/O voltage reference
9	INTB	O	Interrupt to host (push-pull)
10	SCL	I	I2C clock
11	SDA	I/O	I2C data
12	GND		Ground
13	VBUS_IN	I	VBUS connected to USB receptacle
14	DM_CON	I/O	USB DM connected to USB receptacle
15	DP_CON	I/O	USB DP connected to USB receptacle
16	ID_CON	I/O	USB ID connected to USB receptacle

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>BUS</sub>	Supply voltage from USB connector	-0.5	28	V	
V <sub>BAT</sub>	Supply voltage from battery	-0.5	6.0		
V <sub>DDIO</sub>	Logic supply voltage	-0.5	4.6	V	
V <sub>ID_CON</sub>	ID Connector voltage	-0.5	V <sub>BAT</sub> +0.5	V	
V <sub>USBIO</sub>	Switch I/O voltage range	USB Switch	-0.5	V <sub>BAT</sub> +0.5	V
V <sub>UARTIO</sub>	Switch I/O voltage range	UART Switch	-0.5	V <sub>BAT</sub> +0.5	V
V <sub>JIG</sub>	JIG voltage	-0.5	V <sub>BAT</sub> +0.5	V	
V <sub>LOGIC_O</sub>	Voltage applied to logic output (SCL, SDA, INTB, BOOT)	-0.5	4.6	V	
I <sub>K</sub>	Analog port diode current	-50	50	mA	
I <sub>SW-DC</sub>	ON-state continuous switch current	-60	60	mA	
I <sub>SW</sub>	ON-state peak switch current PEAK	-150	150	mA	
I <sub>IK</sub>	Digital logic input clamp current	V <sub>DDIO</sub> < 0	-50	mA	
I <sub>LOGIC_O</sub>	Continuous current through logic output (SCL, SDA, INTB, BOOT)	-50	50	mA	
I <sub>GND</sub>	Continuous current through GND		100	mA	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**THERMAL IMPEDANCE RATINGS**

			UNIT
θ <sub>JA</sub>	Package thermal impedance	RSV package	184 °C/W

**SUMMARY OF TYPICAL CHARACTERISTICS**

AMBIENT TEMPERATURE = 25°C	USB/UART PATH
Number of channels	2
ON-state resistance ( $r_{on}$ )	8 $\Omega$
ON-state resistance match ( $\Delta r_{on}$ )	0.5 $\Omega$
ON-state resistance flatness ( $r_{on(flat)}$ )	0.5 $\Omega$
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	95 $\mu$ s/ 3.5 $\mu$ s
Bandwidth (BW)	920 MHz
OFF isolation ( $O_{ISO}$ )	-26 dB at 250 MHz
Crosstalk ( $X_{TALK}$ )	-32 dB at 250 MHz
Leakage current ( $I_{IO(ON)}$ )	50 nA

**RECOMMENDED OPERATING CONDITIONS**

		MIN	MAX	UNIT
$V_{BUS\_IN}$	VBUS voltage	4.0	6.5	V
$V_{BAT}$	VBAT voltage	3.0	4.4	V
$V_{DDIO}$	VDDIO voltage	1.65	3.6	V
ID_CON_Cap	ID_CON capacitance		1	nF
USB_I/O	USB path signal range	0	3.6	V
Temperature	Operating Temperature	-40	85	°C

## ELECTRICAL SPECIFICATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
<b>DIGITAL SIGNALS – I2C INTERFACE (SCL and SDA)</b>					
V <sub>DDIO</sub>	Logic and I/O supply voltage		1.65	3.6	V
V <sub>IH</sub>	High-level input voltage		V <sub>DDIO</sub> × 0.7	V <sub>DDIO</sub>	V
V <sub>IL</sub>	Low-level input voltage		0	V <sub>DDIO</sub> × 0.3	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –3 mA	V <sub>DDIO</sub> × 0.7		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 3 mA		0.4	V
f <sub>SCL</sub>	SCL frequency			400	kHz
<b>JIG OUTPUT (TSU6111A – OPEN-DRAIN OUTPUT, ACTIVE LOW)</b>					
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 10 mA, V <sub>BAT</sub> = 3.0 V		0.5	V
<b>INTB AND BOOT (PUSH-PULL OUTPUT)</b>					
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –4 mA, V <sub>DDIO</sub> = 1.65 V	1.16	V <sub>DDIO</sub>	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, V <sub>DDIO</sub> = 1.65 V	0	0.33	V

## ELECTRICAL SPECIFICATIONS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TOTAL SWITCH CURRENT CONSUMPTION</b>						
I <sub>BAT(Standby)</sub>	V <sub>BAT</sub> Standby current consumption	V <sub>BUS</sub> = 0 V, Idle state		25	30	μA
I <sub>DD(Operating)</sub>	V <sub>BAT</sub> Operating current consumption	V <sub>BUS_IN</sub> = 0 V, USB switches ON		45	75	μA
<b>VOLTAGE PROTECTION</b>						
V <sub>VBUS_UVLO</sub>	V <sub>BUS</sub> under voltage +	Voltage is rising		2.85		V
	V <sub>BUS</sub> under voltage–	Voltage is falling		2.55		
V <sub>VBAT_UVLO</sub>	V <sub>BUS</sub> under voltage +	Voltage is rising		2.65		V
	V <sub>BUS</sub> under voltage–	Voltage is falling		2.45		
V <sub>VDDIO_UVLO</sub>	V <sub>BUS</sub> under voltage +	Voltage is rising		1.30		V
	V <sub>BUS</sub> under voltage–	Voltage is falling		1.05		

(1) V<sub>O</sub> is equal to the asserted voltage on DP\_CON and DM\_CON pins. V<sub>I</sub> is equal to the asserted voltage on DP\_HT and DM\_HT pins. I<sub>O</sub> is equal to the current on the DP\_CON and DM\_CON pins. I<sub>I</sub> is equal to the current on the DP\_HT and DM\_HT pins.

**USB AND UART SWITCH ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>						
$V_{\text{USBIO}}$	Analog signal range		0		$V_{\text{BAT}}$	V
$r_{\text{ON}}$	ON-state resistance	DM_HT, DP_HT, DM_CON, DP_CON		8	15	$\Omega$
$\Delta r_{\text{ON}}$	ON-state resistance match between channels	DM_HT, DP_HT, DM_CON, DP_CON		0.5	2	$\Omega$
$r_{\text{ON(flat)}}$	ON-state resistance flatness	DM_HT, DP_HT, DM_CON, DP_CON		0.5	2	$\Omega$
$I_{\text{IO(OFF)}}$	$V_{\text{I}}$ or $V_{\text{O}}$ OFF leakage current			45	200	nA
$I_{\text{IO(ON)}}$	$V_{\text{O}}$ ON leakage current			50	200	nA
<b>DYNAMIC</b>						
$t_{\text{ON}}$	Turn-ON time	From receipt of I <sup>2</sup> C ACK bit		95		$\mu\text{s}$
$t_{\text{OFF}}$	Turn-OFF time	From receipt of I <sup>2</sup> C ACK bit		3.5		$\mu\text{s}$
$C_{\text{I(OFF)}}$	$V_{\text{I}}$ OFF capacitance			4		pF
$C_{\text{O(OFF)}}$	$V_{\text{O}}$ OFF capacitance			7		pF
$C_{\text{I(ON)}}$ , $C_{\text{O(ON)}}$	$V_{\text{I}}$ , $V_{\text{O}}$ ON capacitance			9		pF
BW	Bandwidth			920		MHz
$O_{\text{ISO}}$	OFF Isolation			-26		dB
$X_{\text{TALK}}$	Crosstalk			-32		dB

(1)  $V_{\text{O}}$  is equal to the asserted voltage on DP\_CON and DM\_CON pins.  $V_{\text{I}}$  is equal to the asserted voltage on DP\_HT and DM\_HT pins.  $I_{\text{O}}$  is equal to the current on the DP\_CON and DM\_CON pins.  $I_{\text{I}}$  is equal to the current on the DP\_HT and DM\_HT pins.

## GENERAL OPERATION

The TSU6111A will automatically detect accessories plugged into the phone via the mini/micro USB 5 pin connector. The type of accessory detected will be stored in I<sup>2</sup>C registers within the TSU6111A for retrieval by the host. The TSU6111A has a network of switches that are automatically opened and closed based on the accessory detection. See [Table 1](#) for details of which switches are open during each mode of operation. The TSU6111A also offers a manual switching mode that allows the host processor to decide which switches should be opened and closed. The manual switching settings are executed through the I<sup>2</sup>C interface.

## STANDBY MODE

Standby mode is the default mode upon power up and occurs when no accessory has been detected. During this mode, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is inserted. Power consumption is minimal during standby mode.

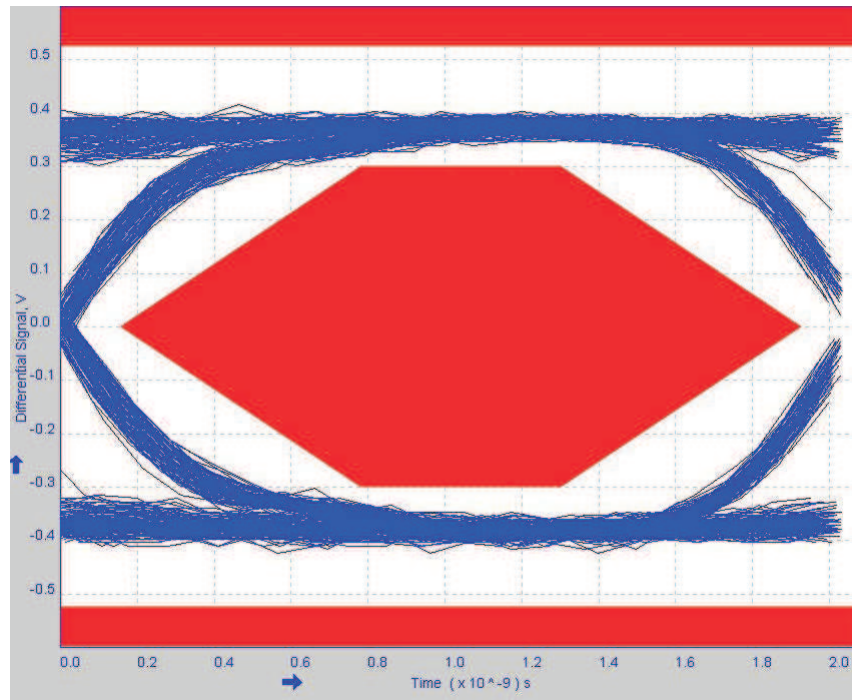
## POWER SUPERVISOR

TSU6111A uses VBAT as the primary supply voltage. VBUS is the secondary supply. VDDIO is used for I<sup>2</sup>C communication.

**Table 1. Function Table**

TSU6111A					
VBAT	VBUS	VDDIO	DETECTION	I2C	COMMENTS
Yes	No	No	Enabled	Not enabled	VBAT is supply
Yes	Yes	No	Enabled	Not enabled	VBAT is supply
Yes	No	Yes	Enabled	Enabled	VBAT is supply
Yes	Yes	Yes	Enabled	Enabled	VBAT is supply
No	Yes	No	Enabled	Not enabled	VBUS is supply
No	Yes	Yes	Not valid		
No	No	Yes	Not valid		
No	No	No	Power Down Reset		

### EYE DIAGRAM USB 2.0 HIGH SPEED



## ACCESSORY ID DETECTION

If  $V_{BUS\_IN}$  is high and the attachment is not a charger, then determine the impedance on the ID pin. If  $V_{BUS\_IN}$  is low and an accessory is attached, then use an ADC for impedance sensing on the ID pin to identify which accessory is attached.

## IMPEDANCE BUCKETS FOR EACH ACCESSORY

In order to implement ID detection, each accessory should contain a ID impedance resistor value (refer to [Table 2](#)) which has a 5% tolerance accuracy.

**Table 2. Accessory ID and Switch States**

ACCESSORY	DETECTED IMPEDANCE ON ID	RESISTOR TOLERANCE (%)	ADC VALUE	SWITCH STATE		FACTORY CABLE	
				DP/DM		JIG	BOOT
				USB	UART		
OTG	0	—	0	ON	OFF	OFF	OFF
MHL	1K	5%	0	OFF	OFF	OFF	OFF
Audio Device Type 3	28.7K	5%	1110	OFF	OFF	OFF	OFF
Reserved Accessory #1	34K	5%	1111	OFF	OFF	OFF	OFF
Reserved Accessory #2	40.2K	5%	10000	OFF	OFF	OFF	OFF
Reserved Accessory #3	49.9K	5%	10001	OFF	OFF	OFF	OFF
Reserved Accessory #4	64.9K	5%	10010	OFF	OFF	OFF	OFF
Audio Device Type 2	80.27K	5%	10011	OFF	OFF	OFF	OFF
Phone Powered Device	102K	5%	10100	OFF	ON	OFF	OFF
TTY Converter	121K	5%	10101	OFF	OFF	OFF	OFF
UART Cable	150K	5%	10110	OFF	ON	OFF	OFF
Type 1 Charger	200K	5%	10111	OFF	OFF	OFF	OFF
Factory Mode Cable - Boot Off USB	255K	5%	11000	ON	OFF	ON	OFF
Factory Mode Cable - Boot On USB	301K	5%	11001	ON	OFF	ON	ON
Audio/Video Cable	365K	5%	11010	OFF	OFF	OFF	OFF
Type 2 Charger	442K	5%	11011	OFF	OFF	OFF	OFF
Factory Mode Cable - Boot Off UART	523K	5%	11100	OFF	ON	ON	OFF
Factory Mode Cable - Boot On UART	619K	5%	11101	OFF	ON	ON	ON
Stereo Headset with Remote (Audio Device Type 1)	1000.07K	10%	11110	OFF	OFF	OFF	OFF
Mono/Stereo Headset (Audio Device Type 1)	1002K	10%	11110	OFF	OFF	OFF	OFF
No ID	—	—	11111	OFF	OFF	OFF	OFF
USB Standard Downstream Port	—	—	11111	ON	OFF	OFF	OFF
USB Charging Downstream Port	—	—	11111	ON	OFF	OFF	OFF
Dedicated Charging Port	—	—	11111	OFF	OFF	OFF	OFF

### Power-On Reset

When power (from 0 V) is applied to  $V_{BAT}$ , an internal power-on reset holds the TSU6111A in a reset condition until  $V_{BAT}$  has reached  $V_{POR}$ . Once  $V_{BAT}$  has reached  $V_{POR}$ , the reset condition is released, and the TSU6111A registers and I<sup>2</sup>C state machine initialize to their default states.

After the initial power-up phase,  $V_{BAT}$  must be lowered to below 0.2 V and then back up to the operating voltage ( $V_{DDIO}$ ) for a power-reset cycle.

### Software Reset

The TSU6111A has software reset feature.

- Hold low both I<sup>2</sup>C\_SCL and I<sup>2</sup>C\_SDA for more than 30ms to reset digital logic of the TSU6111A.

After resetting the digital logic, INTB will keep low until INT\_Mask bit of Control register (0x02) is cleared.

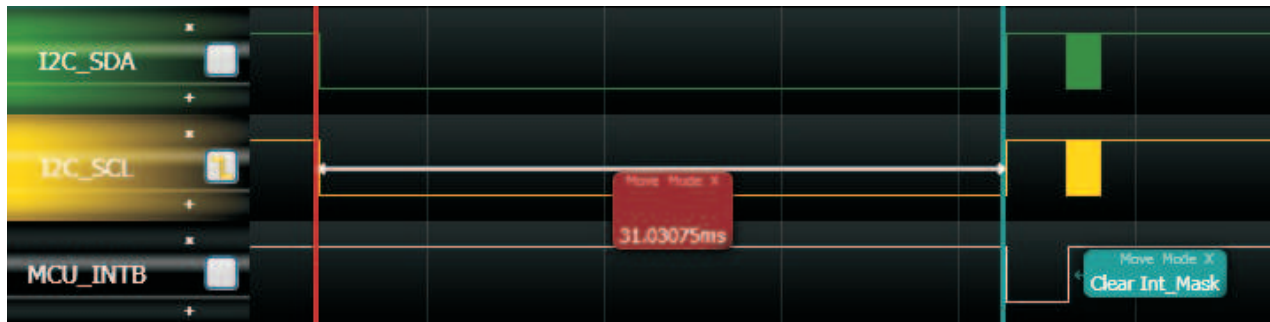
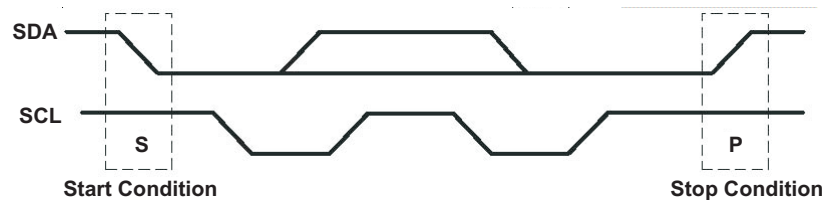


Figure 1. Software Reset

## Standard I<sup>2</sup>C Interface Details

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. The SCL and SDA lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

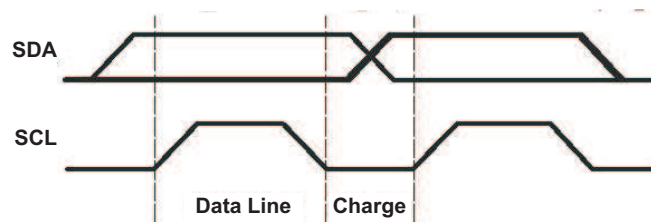
I<sup>2</sup>C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 2](#)). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, the device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.



**Figure 2. Definition of Start and Stop Conditions**

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data is sent only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP, see [Figure 3](#)).



**Figure 3. Bit Transfer**

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 2](#)).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver address must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 4](#)). Setup and hold times must be taken into account.

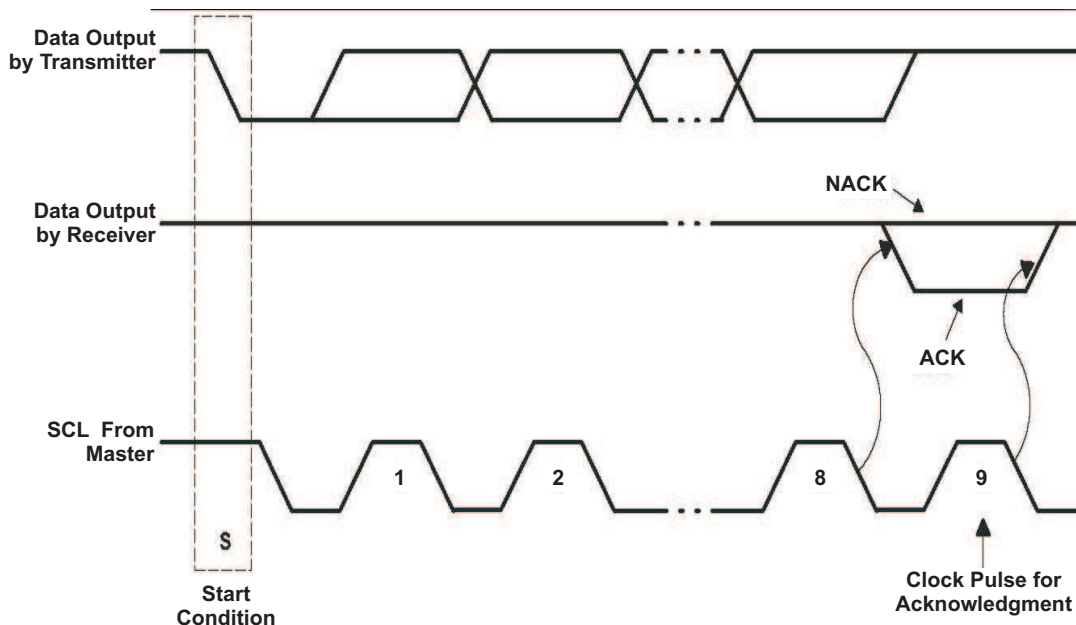


Figure 4. Acknowledgment on I<sup>2</sup>C Bus

**Writes**

Data is transmitted to the TSU6111A by sending the device slave address and setting the LSB to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

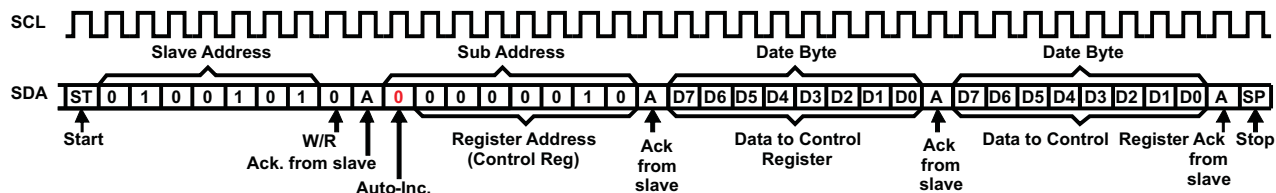


Figure 5. Repeated Data Write to a Single Register

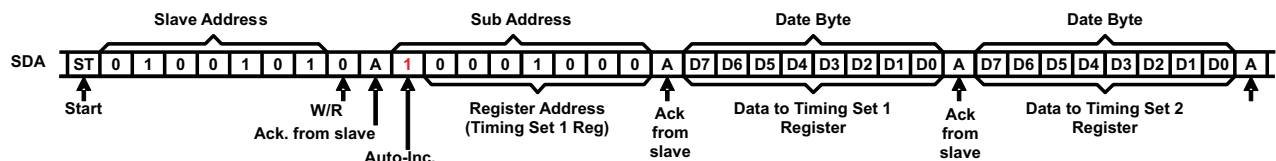


Figure 6. Burst Data Write to Multiple Registers

**Reads**

The bus master must first send the TSU6111A slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU6111A. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse (See Figure 7).

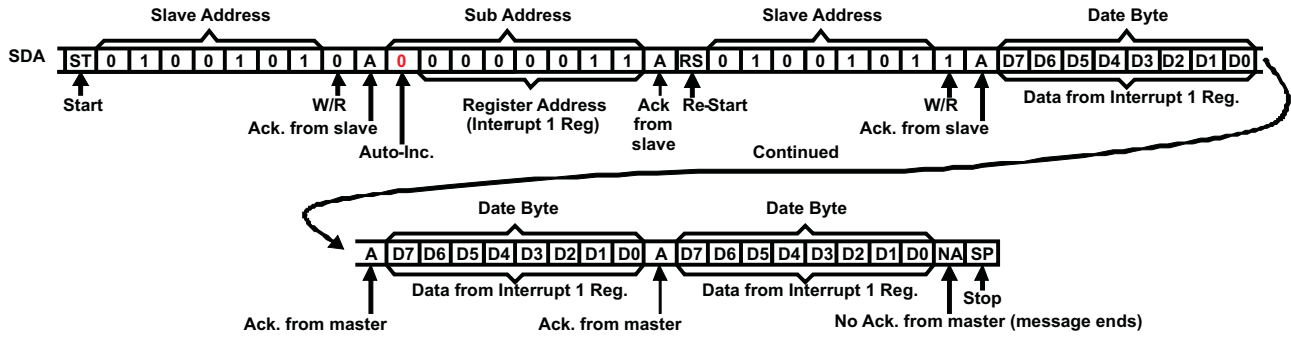


Figure 7. Repeated Data Read from a Single Register – Combined Mode

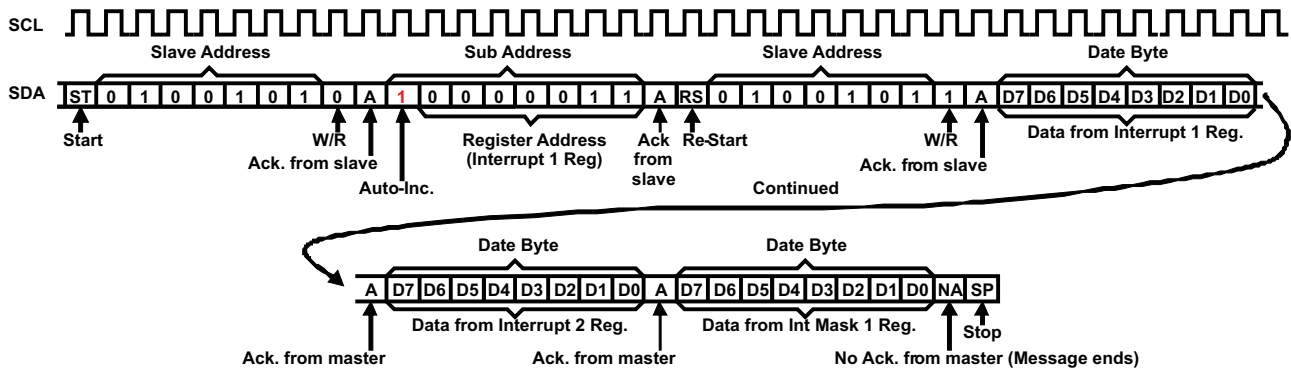


Figure 8. Burst Data Read from Multiple Registers – Combined Mode

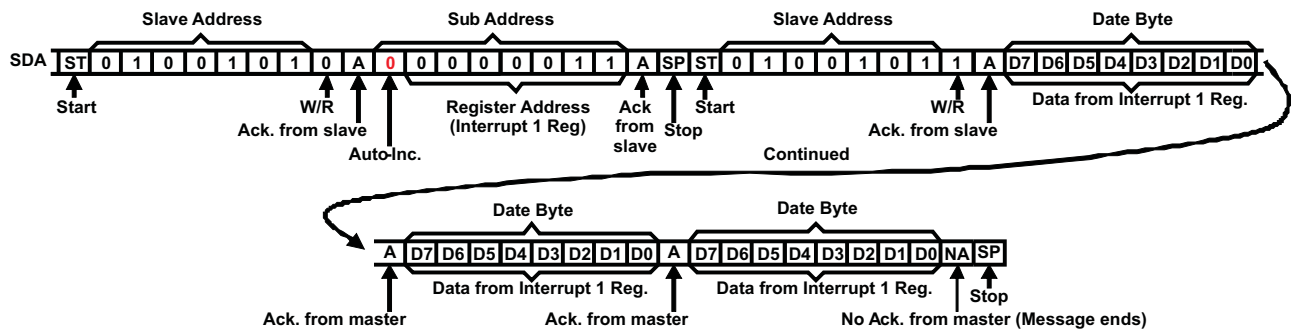


Figure 9. Repeated Data Read from a Single Register – Split Mode

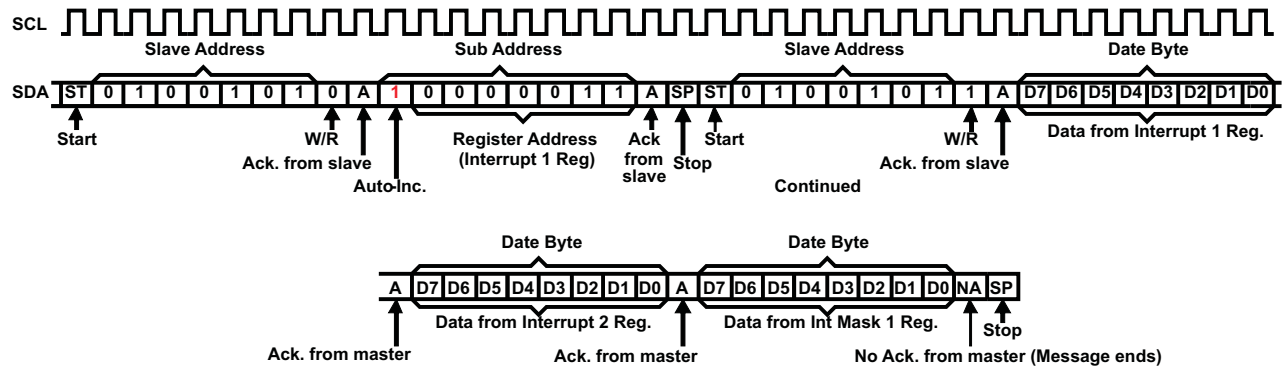


Figure 10. Burst Data Read from Multiple Registers – Split Mode

**Notes (Applicable to Figure 5–Figure 10):**

- SDA is pulled low on Ack. from slave or Ack. from master.
- Register writes always require sub-address write before first data byte.
- Repeated data that writes to a single register continues indefinitely until a Stop or a Re-Start.
- Repeated data reads from a single register continues indefinitely until No Ack. from master.
- Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur; however, no data is changed by the writes. After register 14h is written, writing resumes to register 01h and continues until a Stop or a Re-Start.
- Burst data reads starts at the specified register address, then advances to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No Ack. from master.

**I<sup>2</sup>C Register Map<sup>(1)(2)(3)</sup>**

ADDR	REGISTER	TYPE	RESET VALUE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
01h	Device ID	R	00010010	Version ID				Vendor ID				
02h	Control	R/W	xxx11111				Switch Open	Raw Data	Manual S/W	Wait	INT Mask	
03h	Interrupt 1	R	xxxxxx00							Detach	Attach	
04h	Interrupt 2	R	xx0xx000				CONNECT			ADC_Change	Reserved_Attach	Charging_AV
05h	Interrupt Mask 1	R/W	xxxxxx00							Detach	Attach	
06h	Interrupt Mask 2	R/W	xx0xx000				CONNECT			ADC_Change	Reserved_Attach	Charging_AV
07h	ADC	R	xxx11111								ADC Value	
08h	Timing Set 1	R/W	xxxx0000					Device Wake Up				
09h	Timing Set 2	R/W	0000xxxx	Switching Wait								
0Ah	Device Type 1	R	00000000	USG OTG	DCP	CDP			UART	USG	Audio Type2	Audio Type1
0Bh	Device Type 2	R	00000000	Audio Type3	Audio/Video	TTY	PPD	JIG_UART_OFF	JIG_UART_ON	JIG_USB_OFF	JIG_USB_ON	
0Ch	Button 1	R	00000000	7	6	5	4	3	2	1	Send_End	
0Dh	Button 2	R	x0000000	Unknown		Error	12	11	10	9	8	
13h	Manual S/W 1	R/W	000000xx	D- Switching				D+ Switching				
14h	Manual S/W 2	R/W	xxxx00xx					BOOT_SW	JIG-ON			
15h	Device Type 3	R	xxxxxx00							VBUS	MHL	

- (1) Do not use blank register bits.
- (2) Write "0" to the blank register bits.
- (3) Values read from the blank register bits are not defined and invalid.

**Slave Address**

NAME	SIZE (BITS)	DESCRIPTION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Slave address	8	0	1	0	0	1	0	1	R/W

**Device ID**

Address: 01h

Reset Value: 00010010

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	Vendor ID	3	A unique number for vendor 010 for Texas Instruments
7-3	Version ID	5	A unique number for chip version 00001b for TSU6111A

**Control**

Address: 02h

Reset Value: xxx11111

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	INT Mask	1	0: Unmask interrupt 1: Mask interrupt
1	Wait	1	0: Wait until host re-sets this bit(WAIT bit) high 1: Wait until Switching timer is expired
2	Manual S/W	1	0: Manual Switching 1: Automatic Switching
3	RAW Data	1	0: Report the status changes on ID to Host 1: Don't report the status changes on ID
4	Switch Open	1	0: Open all Switches 1: Automatic Switching by accessory status
7-5	Reserved		

**Interrupt 1**

Address: 03h

Reset Value: xxxxxx00

Type: Read and Clear

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	Attach	1	1: Accessory is attached
1	Detach	1	1: Accessory is detached
7-2	Unused	6	Unused

**Interrupt 2**

Address: 04h

Reset Value:xx0xx000

Type: Read and Clear

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	Charging_A/V	1	1: Charger detected when A/V cable is attached
1	Reserved_Attach	1	1: Reserved Device is attached
2	ADC_Change	1	1: ADC value is changed when RAW data is enabled
4-3	Unused	2	
5	Connect	1	1: Switch is connected(closed)
7-6	Unused	2	

**Interrupt Mask 1**

Address: 05h

Reset Value:xxxxxx00

Type: Read/Write

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	Attach	1	0: Unmask Attach Interrupt 1: Mask Attach Interrupt
1	Detach	1	0: Unmask Key press Interrupt 1: Mask Detach Interrupt
7-2	Unused	6	Unused

**Interrupt Mask 2**

Address: 06h

Reset Value:xx0xx000

Type: Read/Write

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	Charging_A/V	1	0: Unmask A/V_Charging Interrupt 1: Mask A/V_Charging Interrupt
1	Reserved_Attach	1	0: Unmask Reserved_Attach Interrupt 1: Mask Reserved_Attach Interrupt
2	ADC_Change	1	0: Unmask ADC_Change Interrupt 1: Mask ADC_Change Interrrupt
4-3	Unused	2	
5	Connect	1	0: Unmask Connect Interrupt 1: Mask Connect Interrupt
7-6	Unused	2	

**ADC Value**

Address: 07h

Reset Value: xxx11111

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
4-0	ADC value	5	ADC value read from ID
7-5	Unused	3	

**Timing Set 1**

Address: 08h

Reset Value: xxxx0000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Device Wake Up	4	Device wake up duration
7-4	Unused	4	

**Timing Set 2**

Address: 09h

Reset Value: 0000xxxx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Unused	4	
7-4	Switching wait	4	Waiting duration before switching

**Time Table<sup>(1)</sup>**

SETTING VALUE	DEVICE WAKE UP	SWITCHING WAIT
0000	50 ms	10 ms
0001	100 ms	30 ms
0010	150 ms	50 ms
0011	200 ms	70 ms
0100	300 ms	90 ms
0101	400 ms	110 ms
0110	500 ms	130 ms
0111	600 ms	150 ms
1000	700 ms	170 ms
1001	800 ms	190 ms
1010	900 ms	210 ms
1011	1000 ms	–
1100	–	–
1101	–	–
1110	–	–
1111	–	–

(1) Maximum variation of these timing is ±20%

**Device Type 1**

Address: 0Ah

Reset Value: 00000000

Type: Read

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	Audio type 1	1	Audio device type 1
1	Audio type 2	1	Audio device type 2
2	USB	1	USB host
3	UART	1	UART
4	Unused	1	Unused
5	CDP	1	Charging Downstream Port (USB Host Hub Charger)
6	DCP	1	Dedicated Charging Port
7	USB OTG	1	USB on-the-go device

**Device Type 2**

Address: 0Bh

Reset Value: 00000000

Type: Read

<b>BIT NO.</b>	<b>NAME</b>	<b>SIZE (BITS)</b>	<b>DESCRIPTION</b>
0	JIG_USB_ON	1	Factory mode cable
1	JIG_USB_OFF	1	Factory mode cable
2	JIG_UART_ON	1	Factory mode cable
3	JIG_UART_OFF	1	Factory mode cable
4	PPD	1	Phone-powered device
5	TTY	1	TTY converter
6	Audio/Video	1	A/V cable
7	Audio type 3	1	Audio device type 3

**Button 1**

Address: 0Ch

Reset Value: 00000000

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Send_End	1	Send_End key is pressed
1	1	1	Number 1 key is pressed
2	2	1	Number 2 key is pressed
3	3	1	Number 3 key is pressed
4	4	1	Number 4 key is pressed
5	5	1	Number 5 key is pressed
6	6	1	Number 6 key is pressed
7	7	1	Number 7 key is pressed

**Button 2**

Address: 0Dh

Reset Value:x0000000

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	8	1	Number 8 key is pressed
1	9	1	Number 9 key is pressed
2	10	1	Number 10 key is pressed
3	11	1	Number 11 key is pressed
4	12	1	Number 12 key is pressed
5	Error	1	Error key is pressed
6	Unknown	1	Unknown key is pressed
7	Unused		

**Manual S/W 1**

Address: 13h

Reset Value: 000000xx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	Unused	2	
4-2	D+ Switching	3	000: Open all switch 001: D+ is connected to D+ of USB port 010: Open all switch 011: D+ is connected to RxD of UART
7-5	D– Switching	3	000: Open all switch 001: D– is connected to D– of USB port 010: Open all switch 011: D– is connected to TxD of UART

**Manual S/W 2**

Address: 14h

Reset Value: xxxx00xx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	Unused	2	
2	JIG	1	TSU6111A: 0: High Impedance 1: GND
3	BOOT	1	0: Low 1: High
7-4	Unused	4	

**Device Type 3**

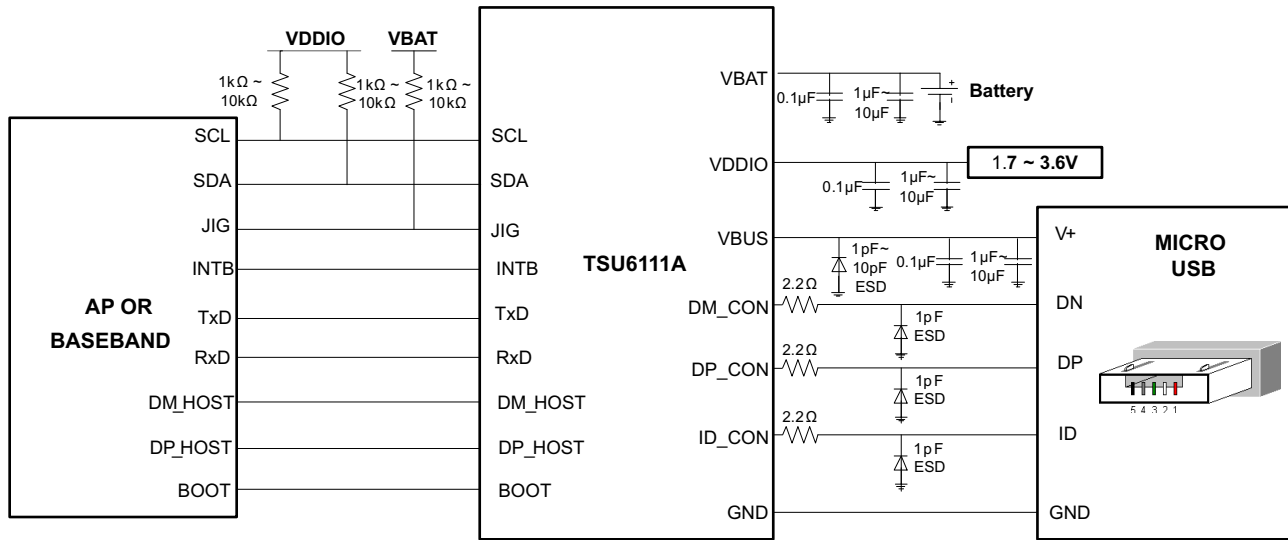
Address: 15h

Reset Value: xxxxxx00

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	MHL	2	MHL device
1	VBUS	1	VBUS valid
7-1	Unused	7	Unused

**APPLICATION SCHEMATIC**



PIN NAME	PIN NO.	CRITICAL COMPONENT
V <sub>BUS_IN</sub>	13	1μF~10μF
		ESD Protection Diode
		0.1μF
V <sub>DDIO</sub>	8	1μF~10μF
		0.1μF
V <sub>BAT</sub>	5	1μF~10μF
		Battery
Jig	7	1kΩ
SCL	10	1kΩ
SDA	11	1kΩ
DM_CON	14	2.2Ω
		ESD Protection Diode
DP_CON	15	2.2Ω
		ESD Protection Diode
ID_CON	16	2.2Ω <sup>(1)</sup>
		ESD Protection Diode

(1) Optional components

## SCHEMATIC GUIDELINES

1.  $V_{BUS\_IN}$ ,  $V_{DDIO}$ , and  $V_{BAT}$  require  $1\mu\text{F}$ – $10\mu\text{F}$  and  $0.1\mu\text{F}$  decoupling capacitors to reduce noise from circuit elements. The capacitors act as a shunt to block off the noise. The  $0.1\mu\text{F}$  capacitor smoothes out high frequencies and has a lower series inductance. The  $1\mu\text{F}$ – $10\mu\text{F}$  capacitors smoothes out the lower frequencies and has a much higher series inductance. Placing both capacitors will provide better load regulation across the frequency spectrum.
2. JIG is an open-drain output and therefore requires a  $1\text{k}\Omega$  ~  $10\text{k}\Omega$  pull-up resistor to VBAT.
3. SCL and SDA require  $1\text{k}\Omega$  ~  $10\text{k}\Omega$  pull-up resistors to VDDIO to prevent floating inputs.
4.  $V_{BUS\_IN}$ , DM\_CON, and DP\_CON are recommended to have an external resistor  $2.2\Omega$  to provide extra ballasting to protect the chip and internal circuitry.
  - (a) For ID\_CON, if there is less stress on the ID pin then the external  $2.2\Omega$  resistor is optional.
5. DM\_CON, DP\_CON, and ID\_CON are recommended to have a  $1\text{pF}$  external ESD Protection Diode rated for 8kV IEC protection to prevent failure in case of an 8kV IEC contact discharge.
6. VBUS\_IN is recommended to have a  $1\text{pF}$  ~  $10\text{pF}$  external ESD Protection Diode rated for 8kV IEC protection to prevent failure in case of an 8kV IEC contact discharge.

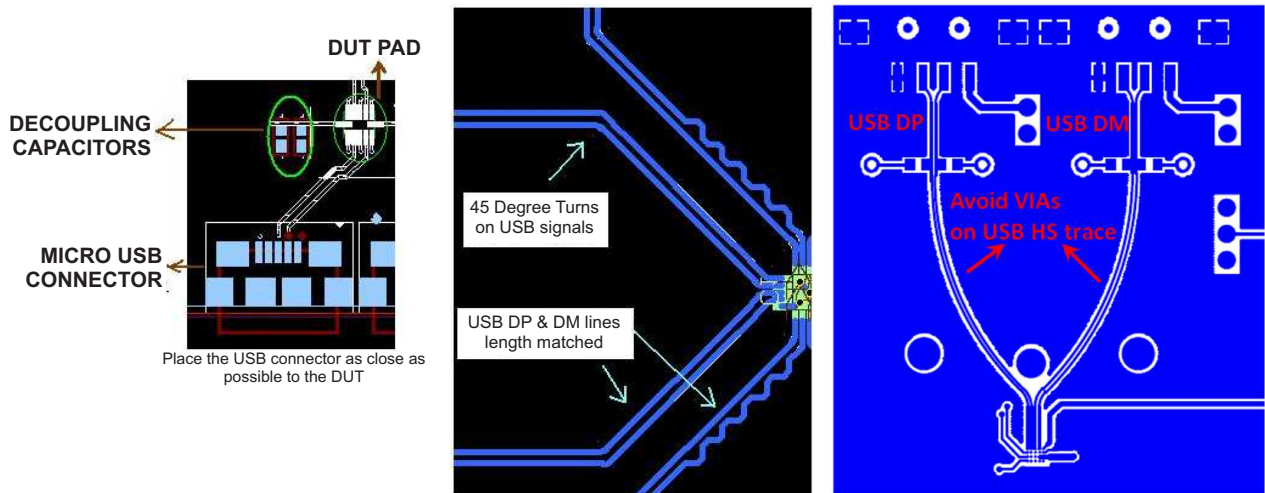
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$V_{BUS\_IN}$	VBUS voltage	4.0	6.5	V
$V_{BAT}$	VBAT voltage	3.0	4.4	V
$V_{DDIO}$	VDDIO voltage	1.65	3.6	V
ID_CON_Cap	ID_CON capacitance		1	nF
USB_I/O	USB path signal range	0	3.6	V
Temperature	Operating Temperature	-40	85	°C

## PCB ROUTING GUIDELINES

### Routing Guidelines for USB Signal Integrity

1. All the USB lines DP\_CON, DM\_CON, DP\_HT, DM\_HT, TxD, and RxD
  - Must have 45Ω single ended characteristic impedance
  - Must have 90Ω differential ended impedance
  - To fulfill USB 2.0 requirements
2. TSU6111A location
  - Close to the USB connector as possible
  - Keep the distance between the USB controller and the device less than 1 inch
  - Shortening the length of the trace will reduce effect of stray noise and radiate less EMI
3. Minimize use of VIAs for USB related signals
  - Differential transmission lines should be matched as close as possible
  - For optimum USB2.0 performance, use no VIAs



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**REVISION HISTORY**

<b>Changes from Original (February 2012) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"><li>Updated ORDERABLE PART NUMBER and TOP-SIDE MARKING in the ORDERING INFORMATION table. ....</li></ul>	<b>1</b>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU6111ARSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

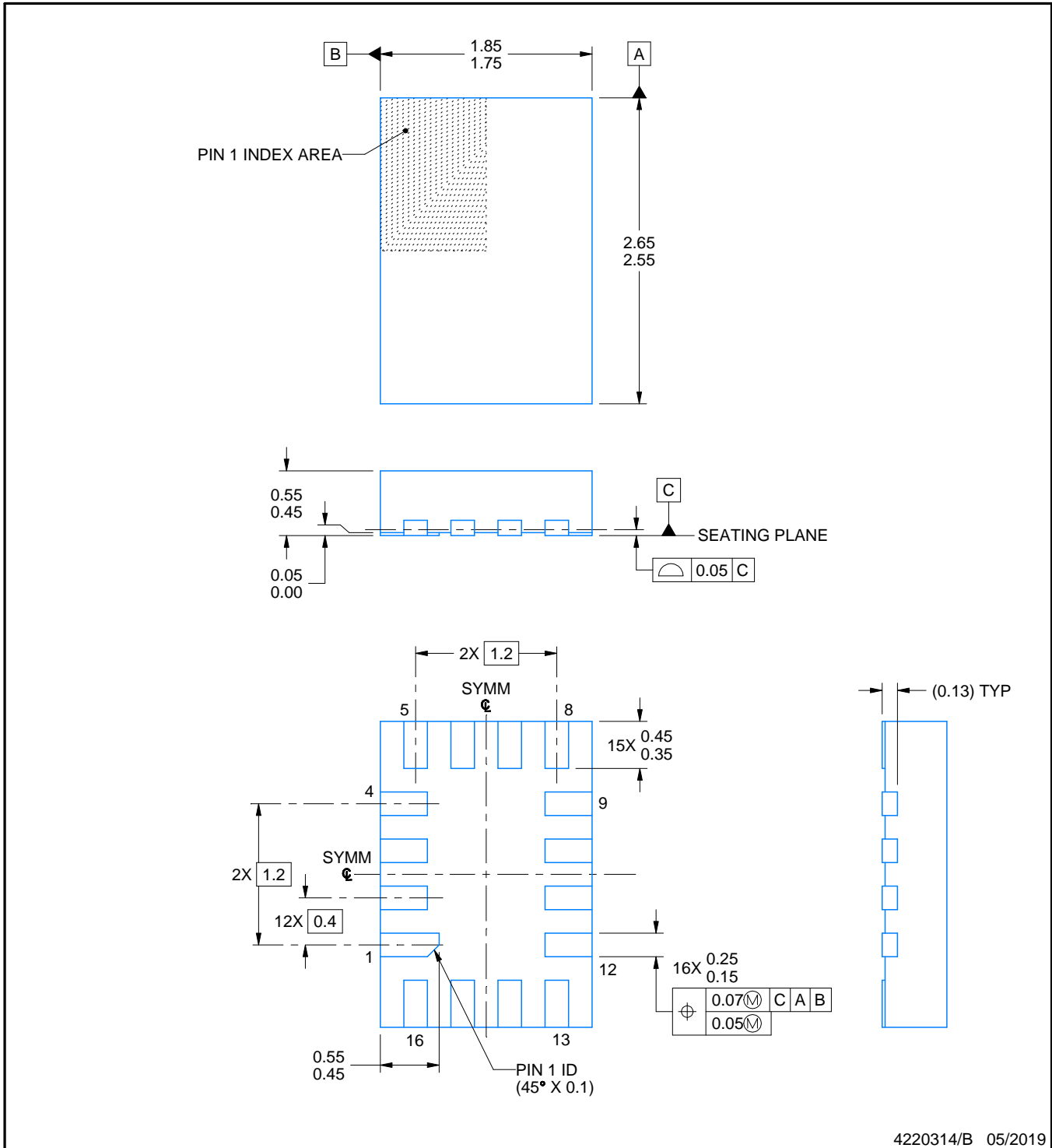
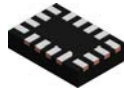
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU6111ARSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU6111ARSVR	UQFN	RSV	16	3000	202.0	201.0	28.0



4220314/B 05/2019

NOTES:

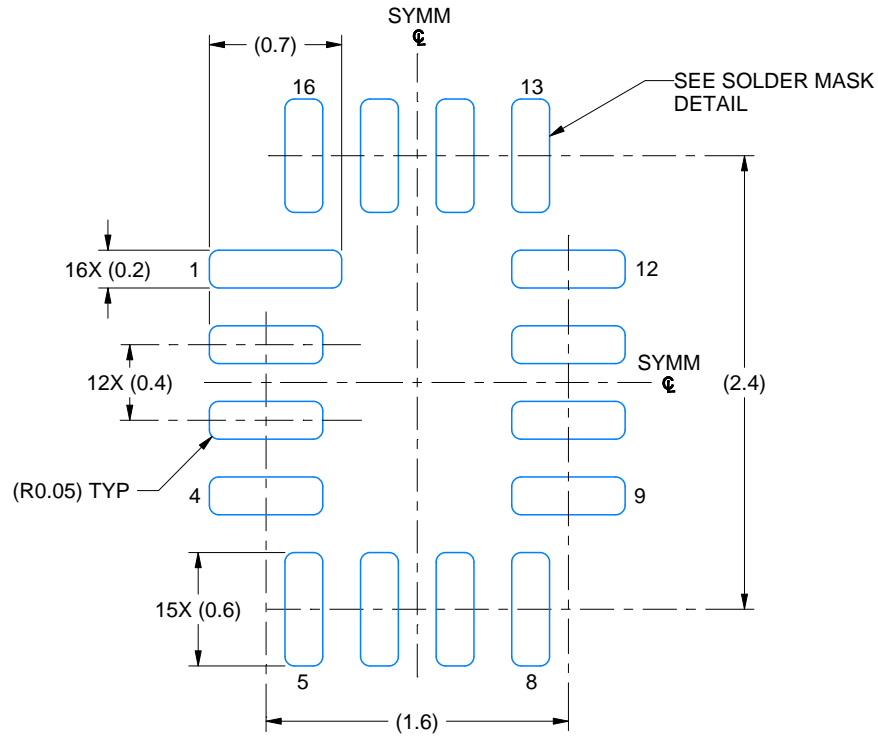
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

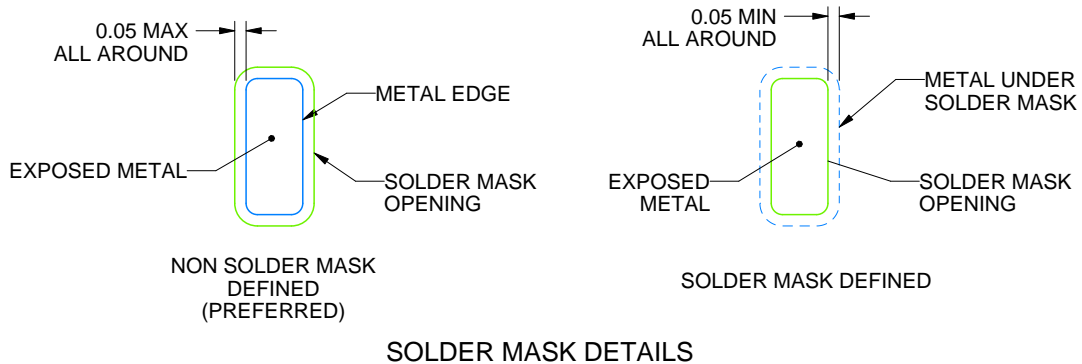
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS

4220314/B 05/2019

NOTES: (continued)

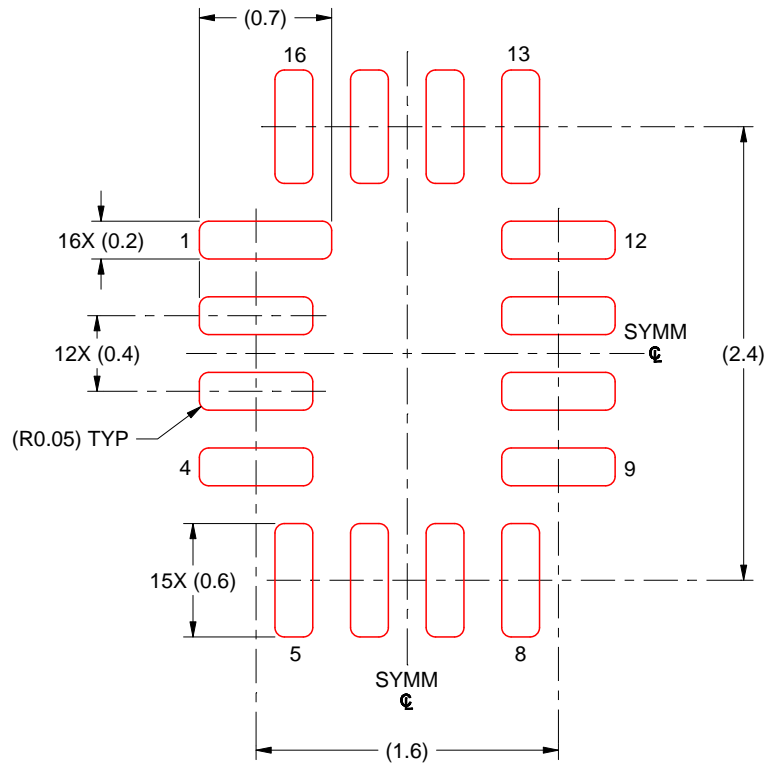
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/B 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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