



**THE DATASHEET OF
74LVT14PW,118**



74LVT14

3.3 V hex inverter Schmitt trigger

Rev. 3 — 6 April 2018

Product data sheet

1 General description

The 74LVT14 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. It is capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, it has a greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going inputs. The threshold differential (typically 600 mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

2 Features and benefits

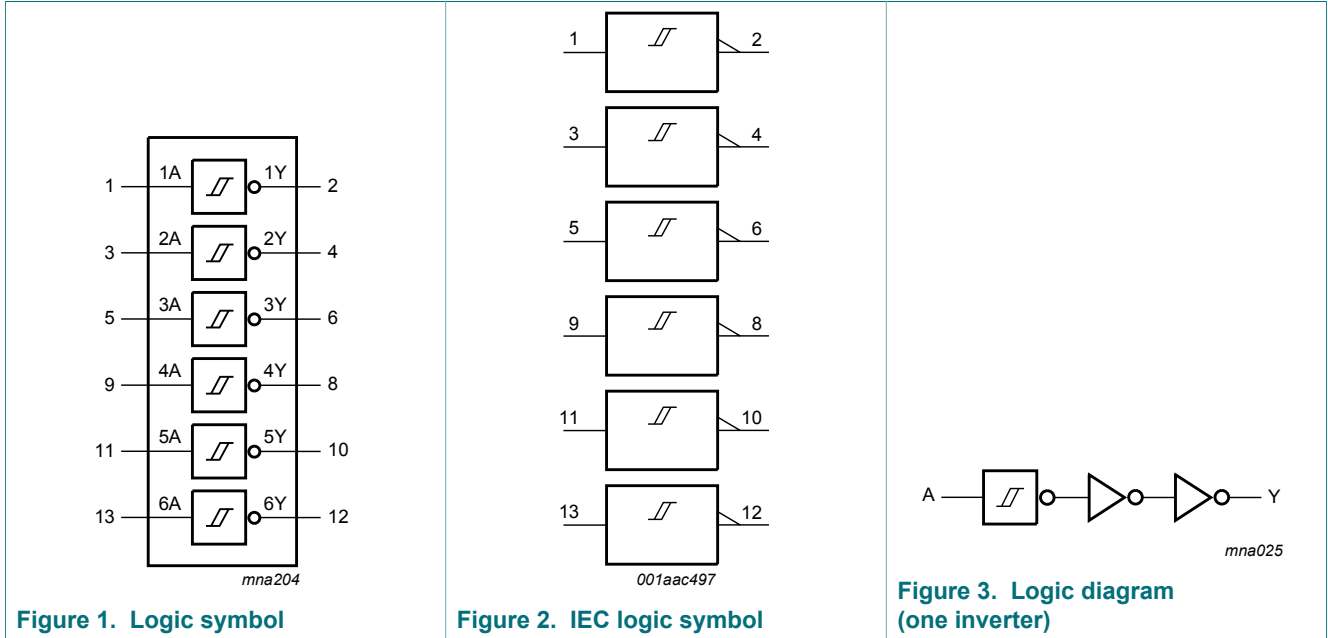
- Different positive and negative going input threshold voltages
- Tolerant of slow input transitions
- High noise immunity
- TTL input and output switching levels
- Output capability: +32 mA/-20 mA
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3 Ordering information

Table 1. Ordering information

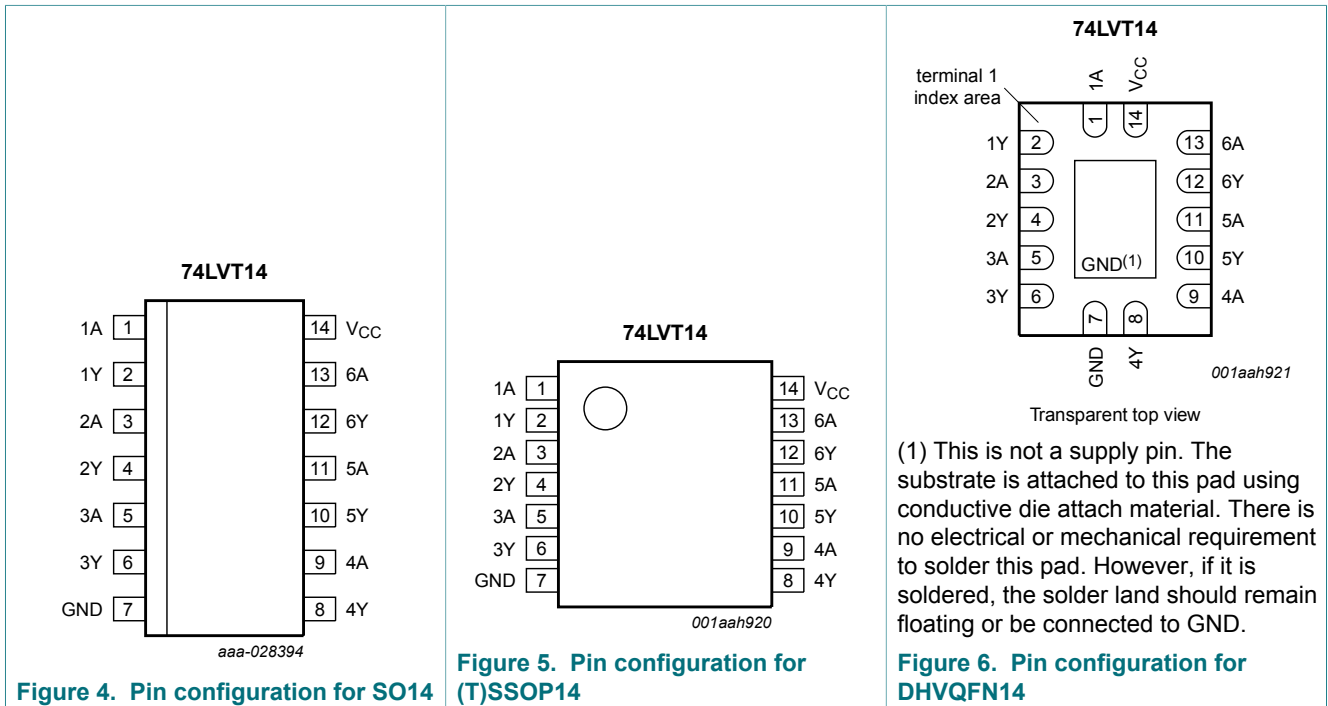
Type number	Package			Version
	Temperature range	Name	Description	
74LVT14D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 7.5 mm	SOT108-1
74LVT14DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT14PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT14BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 4.5 × 0.85 mm	SOT762-1

4 Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	positive supply voltage

6 Functional description

Table 3. Function selection ^[1]

Inputs	Output
nA	nY
L	H
H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[1] -0.5	+7.0	V
V _O	output voltage	output in OFF or HIGH state	^[1] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW state	-	64	mA
		output in HIGH state	-32	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		^[2] -	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	^[3] -	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-20	-	-	mA
I_{OL}	LOW-level output current		-	-	32	mA
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	0	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
V_{T+}	positive-going threshold voltage	$V_{CC} = 3.3$ V; see Figure 7	1.5	1.7	2.0	V
V_{T-}	negative-going threshold voltage	$V_{CC} = 3.3$ V; see Figure 7	0.9	1.1	1.3	V
V_H	hysteresis voltage	$V_{CC} = 3.3$ V; see Figure 7	0.4	0.6	-	V
V_{IK}	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	-1.2	-	-	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ μ A	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7$ V; $I_{OH} = -6$ mA	2.4	-	-	V
		$V_{CC} = 3.0$ V; $I_{OH} = -20$ mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7$ V; $I_{OL} = 100$ μ A	-	-	0.2	V
		$V_{CC} = 2.7$ V; $I_{OL} = 24$ mA	-	-	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 32$ mA	-	-	0.5	V
I_I	input leakage current	$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	-	-	10	μ A
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	-	-	± 1	μ A
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 0$ V to 4.5 V	-	-	± 100	μ A
I_{CC}	supply current	$V_{CC} = 3.6$ V; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0$ A				
		outputs HIGH	-	-	0.02	mA
		outputs LOW	-	1.5	3	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0$ V to 3.6 V; one input = $V_{CC} - 0.6$ V and other inputs at V_{CC} or GND ^[2]	-	-	0.2	mA
C_I	input capacitance	$V_I = 0$ V or 3.0 V	-	3	-	pF

[1] All typical values are measured at $V_{CC} = 3.3$ V (unless stated otherwise) and $T_{amb} = 25$ °C.

[2] This is the increase in the supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{PLH}	LOW to HIGH propagation delay	nA to nY; see Figure 8				
		V _{CC} = 2.7 V	-	-	6.9	ns
		V _{CC} = 3.3 V + 0.3 V	1.0	3.8	5.7	ns
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 8				
		V _{CC} = 2.7 V	-	-	4.1	ns
		V _{CC} = 3.3 V + 0.3 V	1.0	3.2	4.5	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

10.1 Waveforms and test circuit

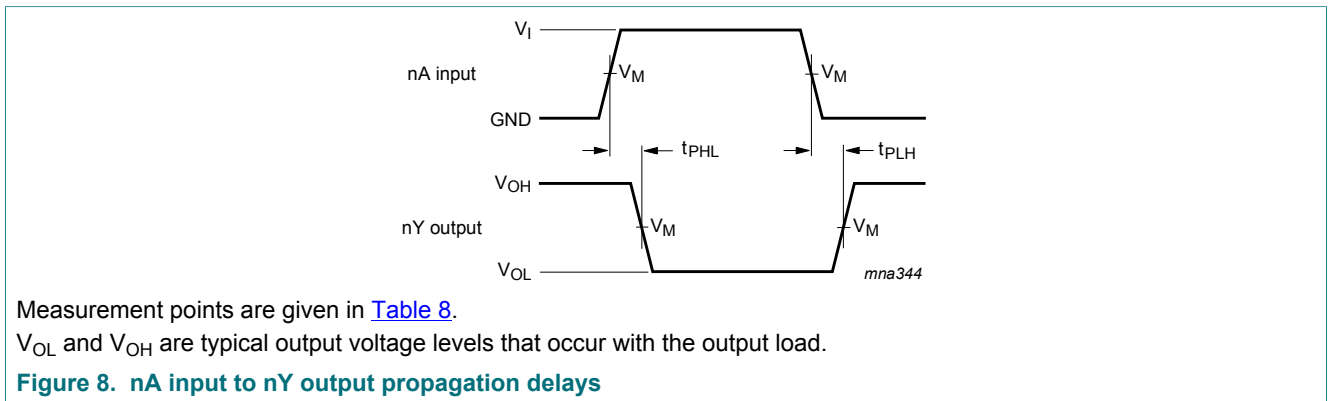
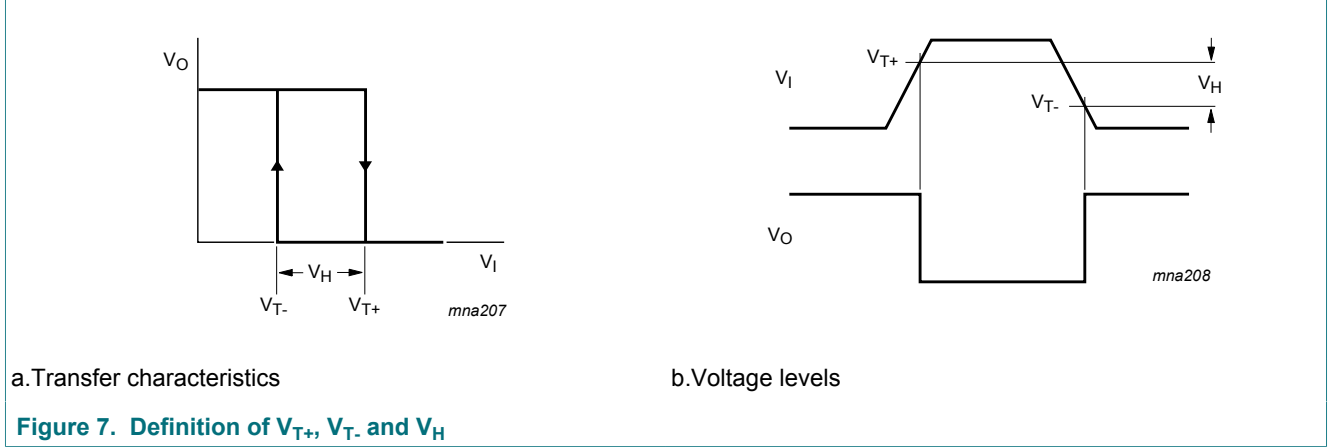
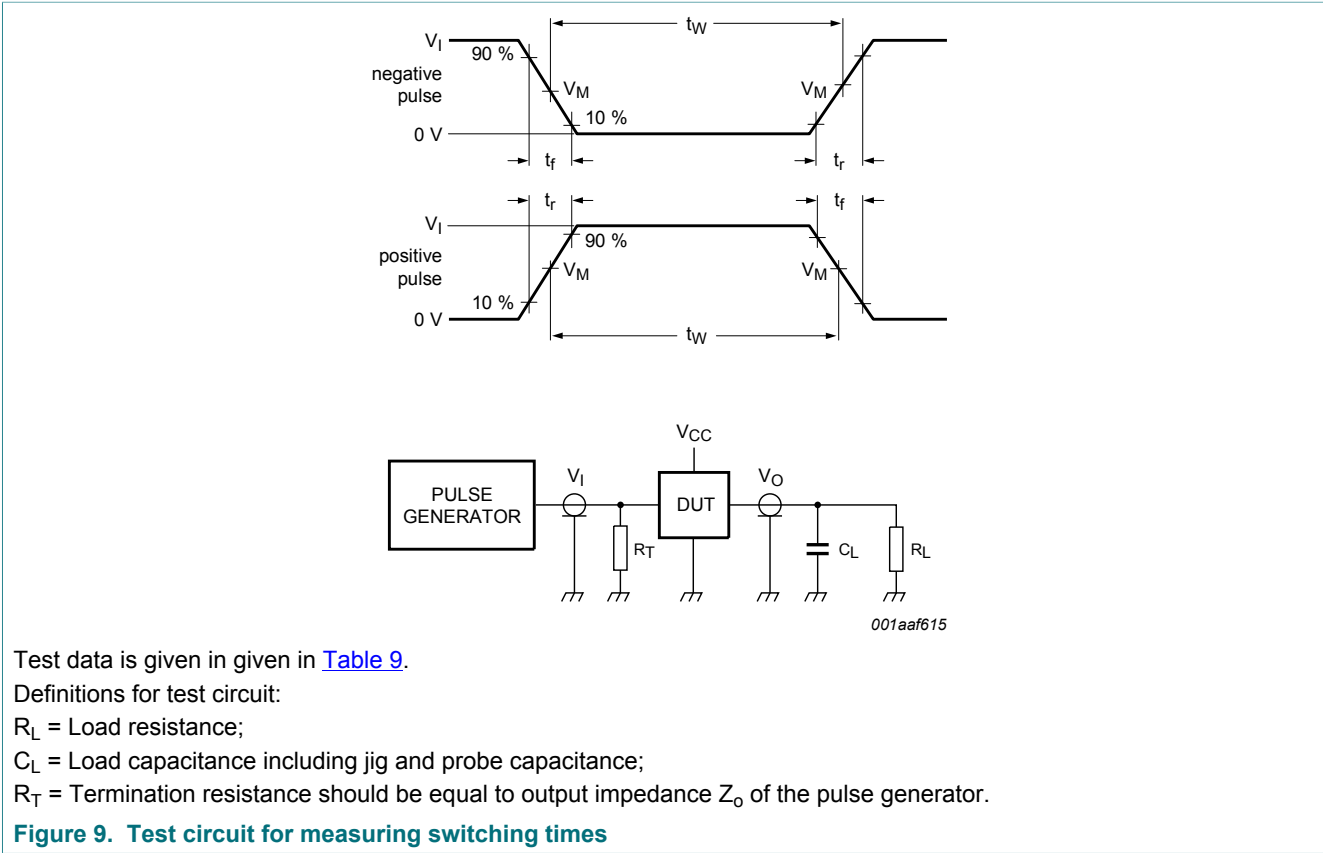


Table 8. Measurement points

V_{CC}	Input	Output
	V_M	V_M
2.7 V to 3.6 V	1.5 V	1.5 V



Test data is given in given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Figure 9. Test circuit for measuring switching times

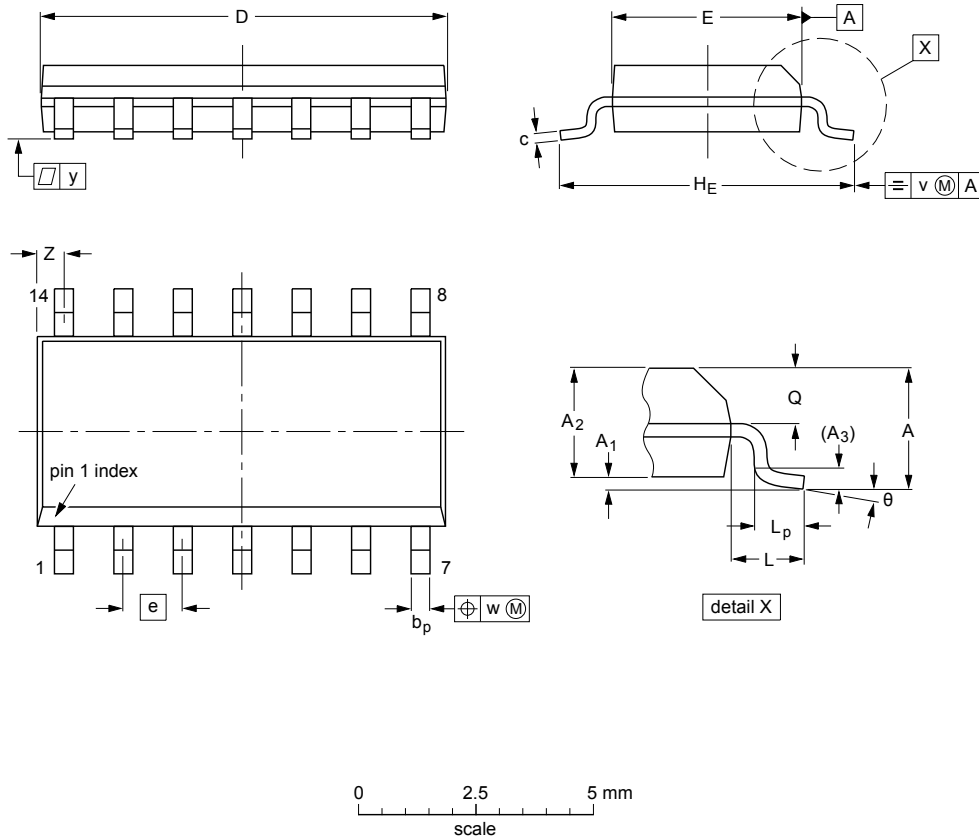
Table 9. Test data

Supply	Input				Load	
V_{CC}	V_I	f_i	t_w	t_r, t_f	R_L	C_L
2.7 V to 3.3 V	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

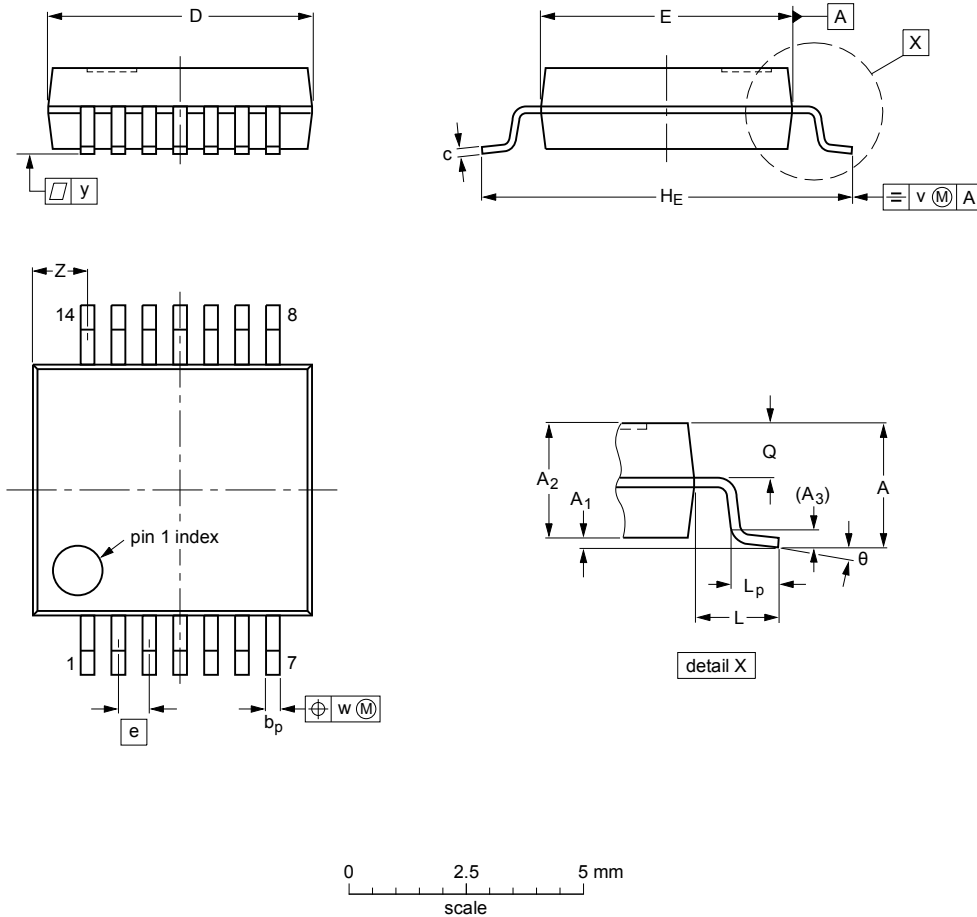
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

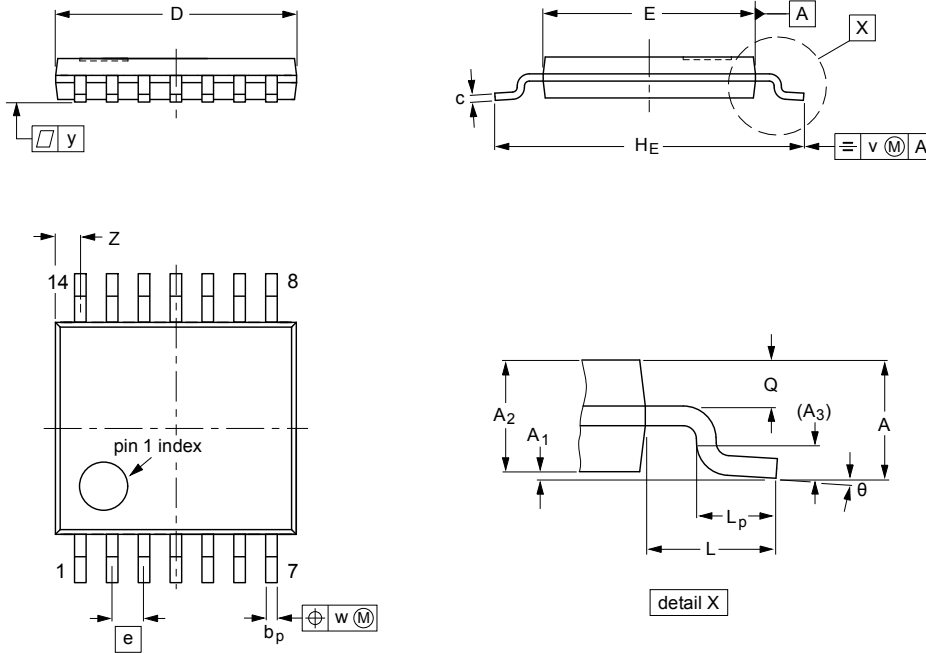
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				-99-12-27 03-02-19

Figure 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

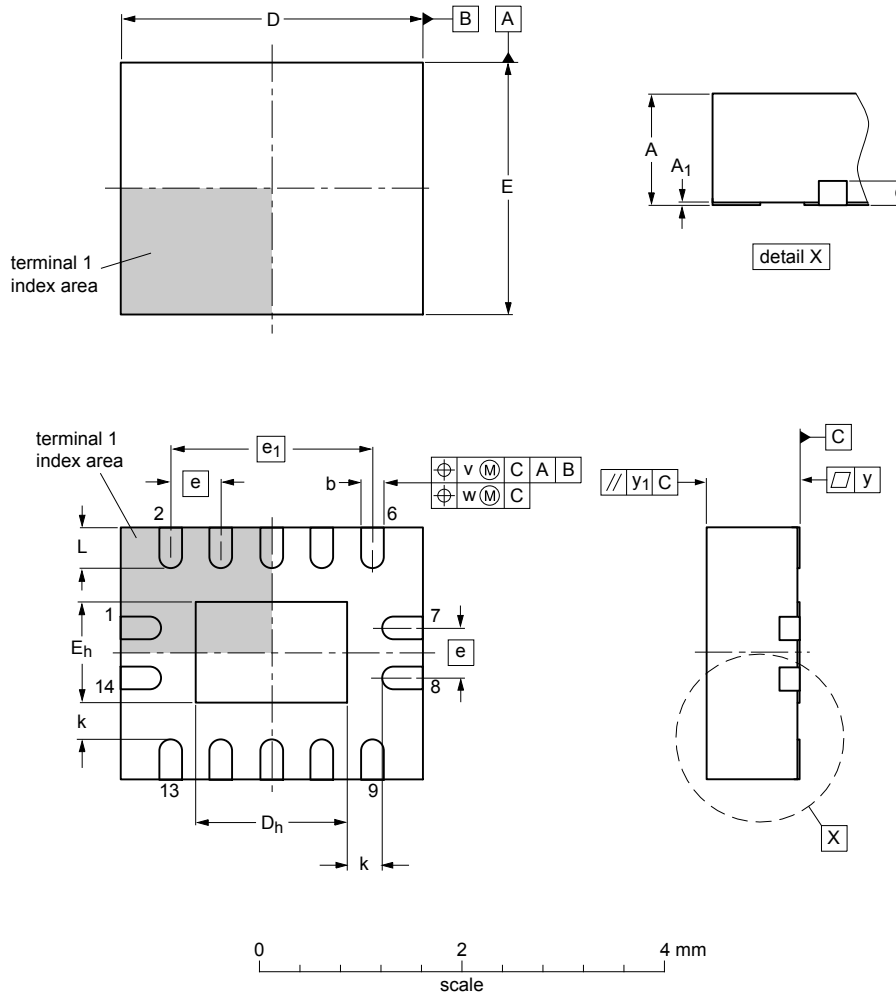
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Figure 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Figure 13. Package outline SOT762-1 (DHVQFN14)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT14 v.3	20180406	Product data sheet	-	74LVT14 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVT14 v.2	20080425	Product data sheet	-	74LVT14 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Quick reference section removed. DHVQFN14 package added to Section 3 and Section 11. Section 12 added. 			
74LVT14 v.1	19960828	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 6 April 2018
Document identifier: 74LVT14

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