THE DATASHEET OF

BQ24381DSGR

bq2438x Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC With LDO Mode

1 Features

- Input Overvoltage Protection
- Accurate Battery Overvoltage Protection
- Output Short-Circuit Protection
- Soft-Start to Prevent Inrush Currents
- Soft-Stop to Prevent Voltage Spikes
- Maximum Input Voltage of 30 V
- Supports up to 1.7-A Load Current
- Thermal Shutdown
- Enable Function
- Fault Status Indication
- Small 2 mm × 2 mm 8-Pin WSON Package

2 Applications

- Smart Phones, Mobile Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

3 Description

The bq2438x family of devices are charger front-end integrated circuits (ICs) designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage and battery voltage. The device operates like a linear regulator, maintaining a 5.5-V (bq24380) or 5-V (bq24381, bq24382) output with input voltages up to the Input overvoltage threshold. During input overvoltage conditions, the device immediately turns off the internal pass FET disconnecting the charging circuit from the damaging input source. Additionally, if the battery voltage rises to unsafe levels while charging, power is removed from the system. The device checks for short-circuit or overload conditions at its output when turning the pass FET on, and if it finds unsafe conditions, it switches off and then rechecks the conditions. Additionally, the device also monitors its die temperature and switches off if it exceeds 140°C.

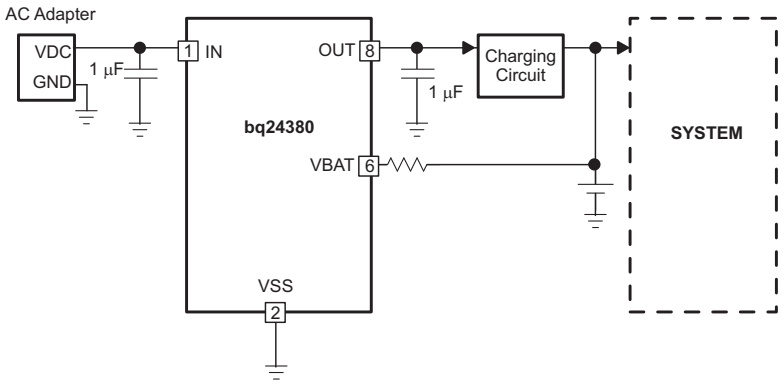
When the device is controlled by a processor, the device provides status information about fault conditions to the host.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24380	WSON (8)	2.00 mm × 2.00 mm
bq24381		
bq24382		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2009) to Revision C — **Page**

- Added *ESD Ratings* table, *Thermal Information*, *Timing Requirements*, *Functional Block Diagram*, *Design Requirements*, *Application Curves*, *Power Supply Recommendations*, *Layout Example*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* ... 1
- Changed SON to WSON throughout the document ... 1
- Changed From: "the bq2430x $\overline{CE}$ pin." To: "the bq2438x $\overline{CE}$ pin." in *Selection of $R_{(BAT)}$* ... 13
- Moved Figures 1 through 8 from *Typical Characteristics* to *Application Curves* section ... 13

Changes from Revision A (May 2008) to Revision B — **Page**

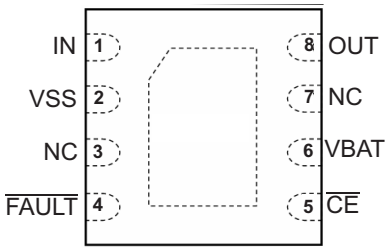
- Added device bq24382 to the datasheet ... 1
- Added the bq24382 option to I_{DD} in the *Electrical Characteristics*. ... 5
- Added the bq24382 option to $V_{O(REG)}$ in the *Electrical Characteristics* ... 5
- Added the bq24382 option to V_{OVP} in the *Electrical Characteristics* ... 5
- Added the bq24382 option to $V_{hys(OVP)}$ in the *Electrical Characteristics* ... 5

Changes from Original (April 2008) to Revision A — **Page**

- Changed Figure 4 ... 7
- Changed Figure 5 ... 7
- Added Figure 9 ... 7

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CE}$	5	I	Active-low chip enable input. Connect $\overline{CE}$ = HI to turn the input pass FET off. Connect $\overline{CE}$ = LOW to turn the internal pass FET on and connect the input to the charging circuitry. $\overline{CE}$ is Internally pulled down, approximately 200 kΩ.
$\overline{FAULT}$	4	O	Open-drain device status output. $\overline{FAULT}$ is pulled to VSS internally when the input pass FET has been turned off due to input overvoltage or output short-circuit conditions, an overtemperature condition, or because the battery voltage is outside safe limits. $\overline{FAULT}$ is high impedance during normal operation.
IN	1	I	Input power, connected to external DC supply. Bypass IN to VSS with a ceramic capacitor (1 µF minimum)
NC	3, 7		Do not connect to any external circuits. These pins may have internal connections used for test purposes.
OUT	8	O	Output terminal to the charging system. Bypass OUT to VSS with a ceramic capacitor (1 µF minimum)
VBAT	6	I	Battery voltage sense input. Connected to pack positive terminal through a 100-kΩ resistor.
VSS	2	–	Ground terminal. Connect to the thermal pad and to the ground rail of the circuit.
Thermal PAD			There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) All voltage values are with respect to the network ground terminal unless otherwise noted.(1)

			MIN	MAX	UNIT
V_I	Input voltage	IN (with respect to VSS)	–0.3	30	V
		OUT (with respect to VSS)	–0.3	12	
		$\overline{FAULT}$, $\overline{CE}$, VBAT (with respect to VSS)	–0.3	7	
I_{OUT}max	Output source current	OUT		2	A
	Output sink current	$\overline{FAULT}$		15	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	IN voltage range	3.3		30	V
I_O	Output current, OUT pin			1.7	A
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq2438x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

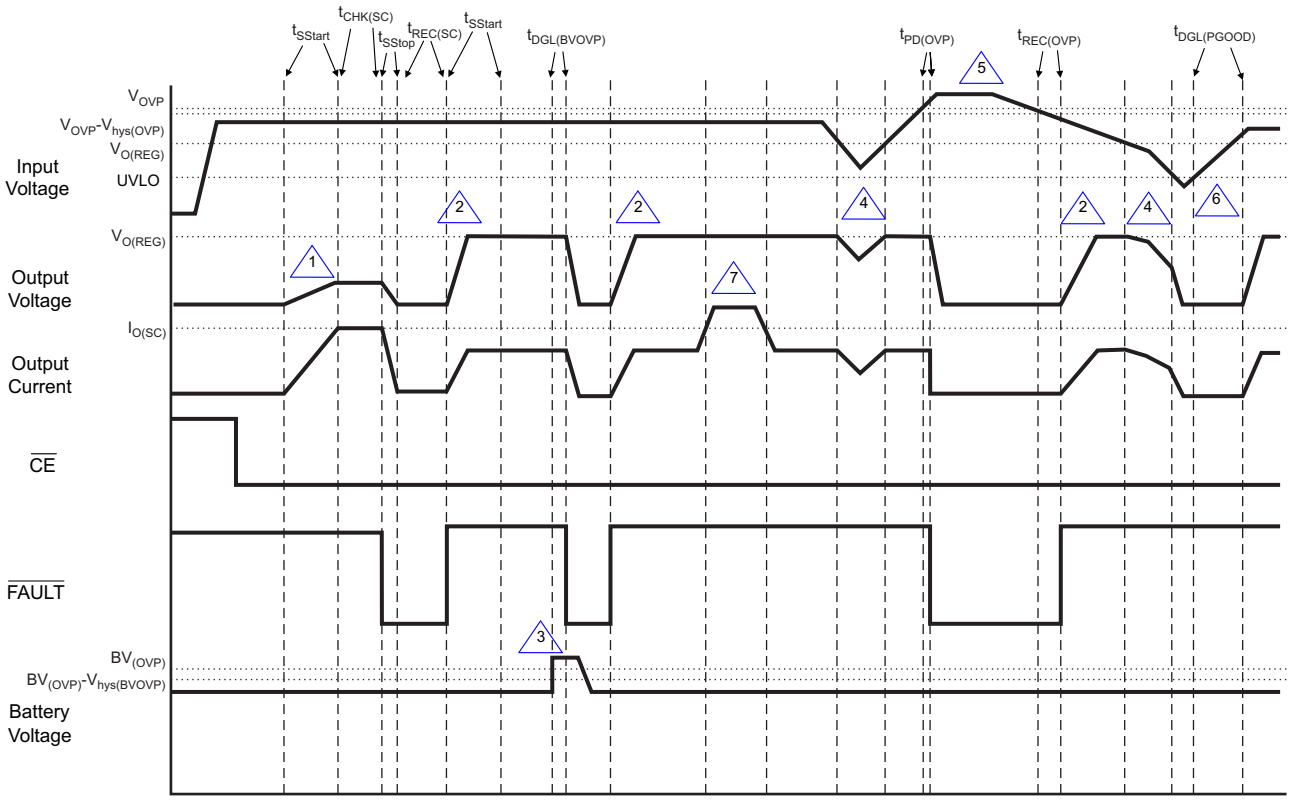
Over junction temperature range –40°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IN							
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{CE}$ = LO or HI, V_{IN}: 0 V → 3 V		2.5		2.8	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	$\overline{CE}$ = LO or HI, V_{IN}: 3 V → 0 V		200		300	mV
I_{DD}	Operating current	$\overline{CE}$ = LO, no load on OUT pin, V_{IN} = 5 V	bq24380			250	µA
			bq24381			300	
			bq24382			300	
I_{STDBY}	Standby current	$\overline{CE}$ = HI, V_{IN} = 5.5 V				100	µA
INPUT-TO-OUTPUT CHARACTERISTICS							
V_{DO}	Dropout voltage IN to OUT	$\overline{CE}$ = LO, V_{IN} = 5 V, $I_{(OUT)}$ = 1 A				280	mV
I_{OFF}	Q1 off-state leakage current	$\overline{CE}$ = HI, V_{IN} = 5.5 V				10	µA
INPUT OVERVOLTAGE PROTECTION							
$V_{O(REG)}$	Output voltage	$\overline{CE}$ = LO, V_{IN} = 6 V	bq24380	5.3	5.5	5.7	V
			bq24381	4.8	5	5.2	
			bq24382	4.8	5	5.2	
V_{OVP}	Input overvoltage protection threshold	$\overline{CE}$ = LO, V_{IN}: 5 V → 8 V	bq24380	6.1	6.3	6.5	V
			bq24831	6.88	7.1	7.31	
			bq24382	10.17	10.5	10.83	
$V_{hys(OVP)}$	Hysteresis on OVP	$\overline{CE}$ = LO or HI, V_{IN}: 7 V → 5 V	bq24380	25		110	mV
		$\overline{CE}$ = LO or HI, V_{IN}: 8 V → 5 V	bq24831	25		120	
			bq24382	150		300	
OUTPUT SHORT-CIRCUIT PROTECTION (ONLY at START-UP)							
$I_{O(SC)}$	Short-circuit detection threshold	3 V < V_{IN} < V_{OVP} - $V_{hys(OVP)}$		1.3	1.5	1.7	A
$t_{REC(SC)}$	Retry interval if short-circuit detected				64		ms
BATTERY OVERVOLTAGE PROTECTION							
BV_{OVP}	Battery overvoltage protection threshold	V_{IN} > 4.5 V, $\overline{CE}$ = LO		4.3	4.35	4.4	V
$V_{hys(BVovp)}$	Hysteresis on $BV_{(OVP)}$	V_{IN} > 4.5 V, $\overline{CE}$ = LO		200		320	mV
$I_{(VBAT)}$	Input bias current on VBAT pin	T_J = 25°C				10	nA
THERMAL PROTECTION							
$T_{J(OFF)}$	Thermal shutdown temperature				140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis				20		°C
LOGIC LEVELS ON $\overline{CE}$							
V_{IL}	Logic LOW input voltage			0		0.4	V
V_{IH}	Logic HIGH input voltage			1.4			V
I_{IL}						1	µA
I_{IH}		$V_{\overline{CE}}$ = 1.8 V				15	µA
LOGIC LEVELS ON $\overline{FAULT}$							
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA				0.2	V
I_{lkg}	Off-state leakage current, HI-Z	$V_{\overline{FAULT}}$ = 5 V				10	µA

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
IN						
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = LO or HI. Time measured from V_{IN} 0 V → 5 V 1-µs rise-time		8		ms
INPUT OVERVOLTAGE PROTECTION						
$t_{PD(OVP)}$ (1)	Input OV propagation delay	V_{IN}: 5 V → 10 V		200		ns
$t_{REC(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = LO. Time measured from V_{IN}: 7 V → 5 V, 1-µs fall-time		8		ms
BATTERY OVERVOLTAGE PROTECTION						
$t_{DGL(BVovp)}$	Deglitch time, battery overvoltage detected	V_{IN} > 4.5 V, $\overline{CE}$ = LO, Time measured from V_{VSAT} rising from 4.1 V to 4.4 V to $\overline{FAULT}$ going low.		176		µs

(1) Not tested. Specified by design



1. Short-circuit during start-up
2. Normal start-up condition
3. Battery overvoltage event
4. $V_{UVLO} < V_{IN} < V_{(OREG)} – V_{OUT}$ tracks V_{IN}
5. Input overvoltage event
6. Input below UVLO
7. High-current event during normal operation

Figure 1. Timing Diagram

6.7 Typical Characteristics

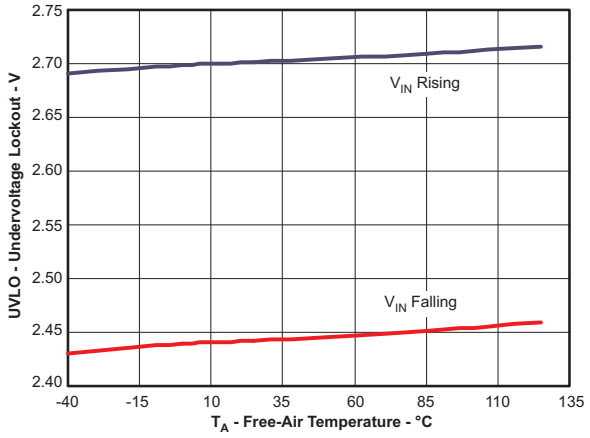


Figure 2. UVLO vs Free-Air Temperature

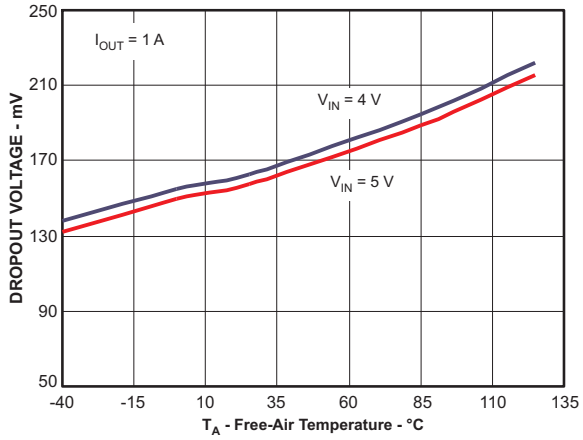


Figure 3. Dropout Voltage vs Free-Air Temperature

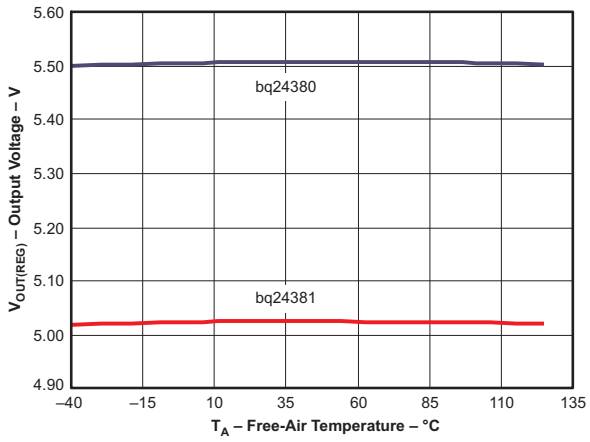


Figure 4. Output Voltage Regulation, $V_{O(REG)}$ vs Free-Air Temperature

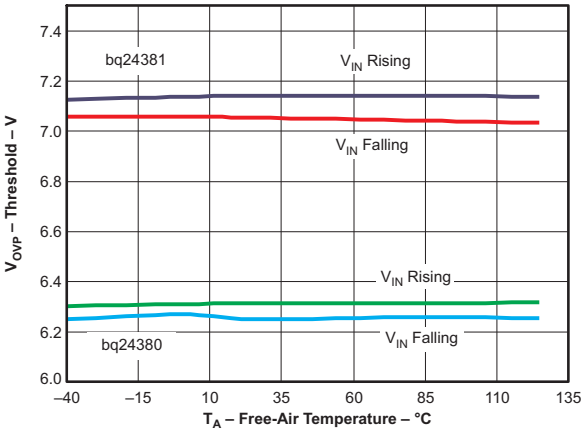


Figure 5. OVP Threshold vs Free-Air Temperature

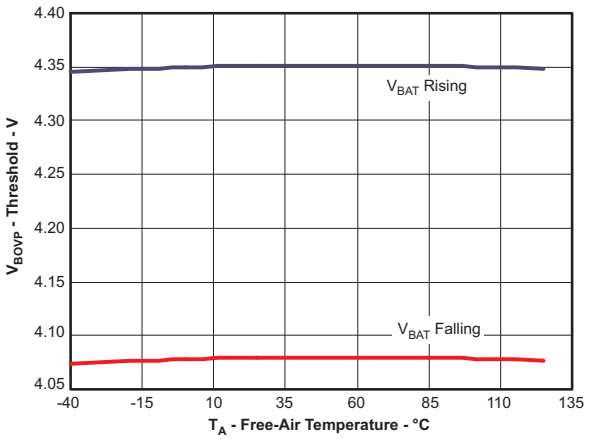


Figure 6. OVP Threshold, V_{BOVP} vs Free-Air Temperature

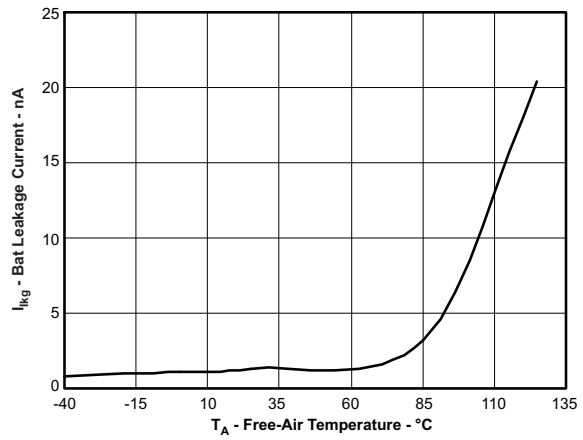


Figure 7. Leakage Current (VBAT PIN) vs Free-Air Temperature

Typical Characteristics (continued)

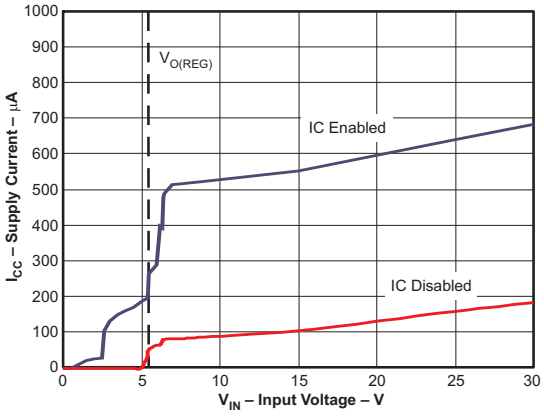


Figure 8. Supply Current vs Input Voltage (bq24380)

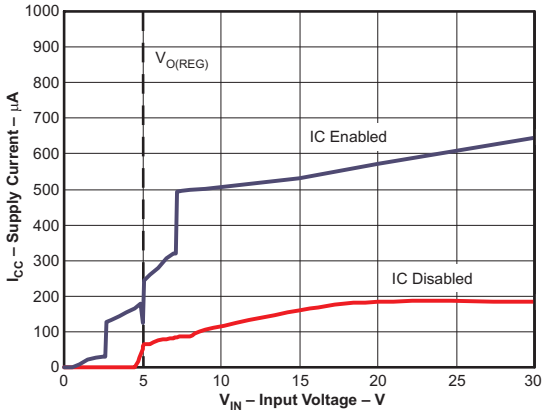


Figure 9. Supply Current vs Input Voltage (bq24381)

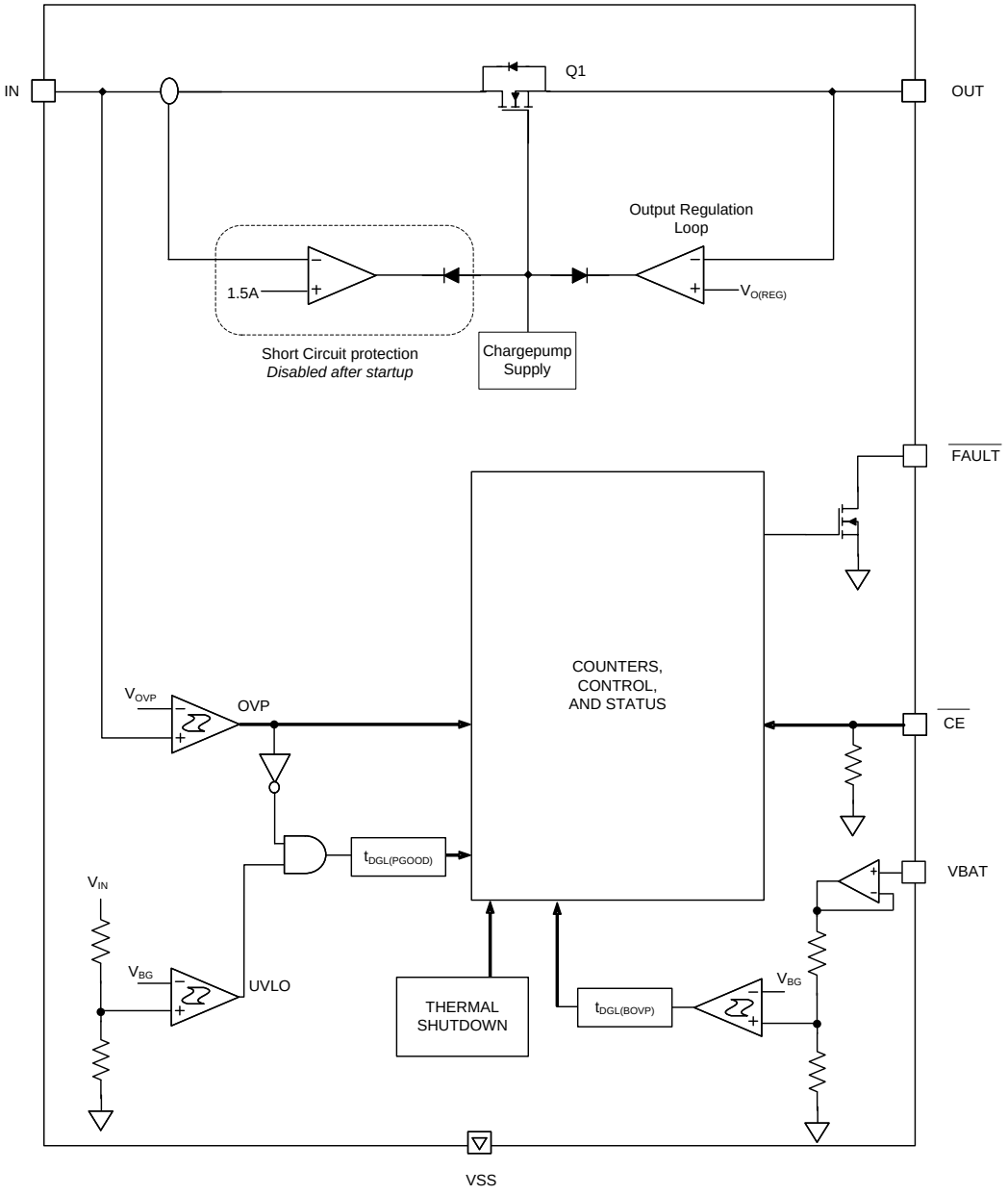
7 Detailed Description

7.1 Overview

The bq2438x is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit and the input source. The device continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.5-V (bq24380) or 5-V (bq24381, bq24382) output with input voltages up to the input overvoltage threshold (V_{OVP}). If the input voltage exceeds V_{OVP}, the device shuts off the pass FET and disconnects the system from input power. Additionally, if the battery voltage rises above 4.35 V, the device switches off the pass FET, removing the power from the system until the battery voltage falls to safe levels. The device also monitors its die temperature and switches the pass FET off if it exceeds 140°C.

The device can be controlled by a processor, and also provides status information about fault conditions to the host.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Overvoltage Protection

The OUT output of the bq2438x operates similar to a linear regulator. While the input voltage is less than $V_{O(REG)}$ and above the UVLO, the output voltage tracks the input voltage (less the drop caused by $R_{DS(on)}$ of the pass FET). When the input voltage is greater than $V_{O(REG)}$ (plus the $R_{DS(on)}$ drop) and less than V_{OVP}, the output voltage is regulated to $V_{O(REG)}$. $V_{O(REG)}$ is 5.5 V for the bq24380 and 5 V for both the bq24381 and bq24382. If the input voltage is increased above V_{OVP}, the internal pass FET is turned off, removing power from the charging circuitry connected to OUT. The $\overline{FAULT}$ output is then asserted low. When the input voltage drops below $V_{OVP} - V_{hys(OVP)}$ (but is still above UVLO), the pass FET is turned on after a deglitch time of $t_{REC(OVP)}$ to ensure that the input supply has stabilized. The *condition 5* in Figure 1 illustrates an input overvoltage event.

7.3.2 Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35 V for the bq2438x. *Condition 3* in Figure 1 illustrates a battery overvoltage event. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BVovp)}$, the pass FET is turned off (using soft-stop), and $\overline{FAULT}$ is asserted low. The pass FET is turned on (using the soft-start sequence) once the battery voltage drops to $BV_{OVP} - V_{hys(BVovp)}$.

7.3.3 Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the pass FET is turned off and the $\overline{FAULT}$ output is asserted low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

7.3.4 Start-Up Short-Circuit Protection

The bq2438x features overload current protection during start-up. The *condition 1* in Figure 1 illustrates start-up into an overload condition. If after the eight soft-start steps are complete and the current limit is exceeded, the device initiates a short-circuit check timer ($t_{CHK(SC)}$). During this check, the current is clamped to $I_{O(SC)}$. If the 5-ms $t_{CHK(SC)}$ timer expires and the current remains clamped by the current limit, the internal pass FET is turned off using the soft-stop method, $\overline{FAULT}$ is pulled low, and the $t_{REC(SC)}$ timer begins. Once the $t_{REC(SC)}$ timer expires, $\overline{FAULT}$ becomes high impedance and the soft-start sequence restarts. The device repeats the start/fail sequence until the overload condition is removed. Once the overload condition is removed, the current-limit circuitry is disabled and the device enters normal operation. Additionally, if the current is not limited after the completion of the soft-start sequence, the $t_{CHK(SC)}$ timer does not start and the current limit circuitry is disabled for normal operation.

7.3.5 Enable Function

The device has an enable pin which is used to enable and disable the device. Connect the $\overline{CE}$ pin high to turn off the internal pass FET. Connect the $\overline{CE}$ pin low to turn on the internal pass FET and enter the start-up routine. The $\overline{CE}$ pin has an internal pulldown resistor and can be left unconnected. The $\overline{FAULT}$ pin is high impedance when the $\overline{CE}$ pin is high.

7.3.6 Fault Indication

The $\overline{FAULT}$ pin is an active-low, open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{CE}$ high. With $\overline{CE}$ low, the $\overline{FAULT}$ pin goes low whenever any of these events occurs:

1. Output short-circuit at power-on
2. Input overvoltage
3. Battery overvoltage
4. IC overtemperature

See Figure 1 for an example of $\overline{FAULT}$ conditions during these events. Connect the $\overline{FAULT}$ pin to the desired logic-level voltage rail through a resistor between 1 kΩ and 50 kΩ.

7.4 Device Functional Modes

7.4.1 OPERATION Mode

The bq2438x device continuously monitors the input voltage and the battery voltage. As long as the input voltage is less than V_{OVP}, the output voltage tracks the input voltage (less the drop caused by $R_{DS}ON$ of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

7.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO) of 2.8 V. The FET connected between the IN and OUT pins is off, and the status output, $\overline{FAULT}$, is set to HI-Z.

7.4.3 POWER-ON RESET Mode

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. During power-on reset, the device waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are within operation limits, the pass FET is turned ON. The device has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input due to the resonant circuit formed by the parasitic inductance of the adapter cable and the input bypass capacitor. During the soft-start time, t_{SStart}, the current limit is stepped up in 8 equal steps every 625 µs. Each step is one-eighth of the $I_{O(SC)}$. After the soft-start sequence is over, the device samples the load current. If the load current exceeds $I_{O(SC)}$, the device initiates short circuit protection. See the *Startup Short-Circuit Protection* section for details. If no overcurrent event is measured, the current-monitoring circuitry is disabled for normal operation.

In the event a short-circuit is detected at power-on, to prevent the input voltage from spiking up when the pass FET is switched off (due to the inductance of the input cable), The pass FET is turned off by gradually reducing its gate-drive, resulting in a *soft-stop* (t_{SStop}).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq2438x device protects against overvoltage and battery overvoltage events that occur due to faulty adapter or incorrect input sources. If either of these faults occur, the bq2438x device isolates the downstream devices from the input source and alerts the host controller with the $\overline{\text{FAULT}}$ open-drain output.

8.2 Typical Application

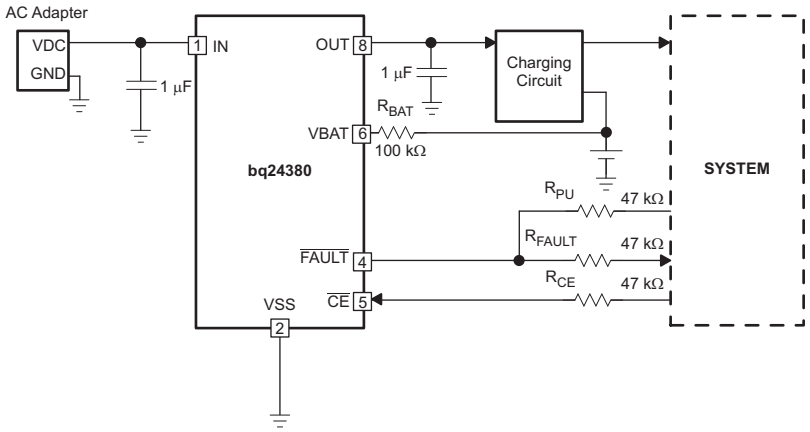


Figure 10. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

PARAMETER	VALUE
Voltage	5 V
Current	< 1.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Selection of $R_{(BAT)}$

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the device, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery may cause failure of the device and can be hazardous. Connecting the VBAT pin through $R_{(BAT)}$ prevents a large current from flowing into the battery in the event of failure of the device. For safety, $R_{(BAT)}$ must have a high value. The problem with a large $R_{(BAT)}$ is that the voltage drop across this resistor because of the VBAT bias current, $I_{(VBAT)}$, causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35-V BV_{OVP} threshold.

Choosing $R_{(BAT)}$ in the range from 100 kΩ to 470 kΩ is a good compromise. If the device fails with $R_{(BAT)}$ equal to 100 kΩ, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 kΩ = 246 µA, which is low enough to be absorbed by the bias currents of the system components. $R_{(BAT)}$ equal to 100 kΩ results in a worst-case voltage drop of $R_{(BAT)} \times I_{(VBAT)}$ = 1 mV. This is negligible compared to the internal tolerance of 50 mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin must be connected to VSS.

8.2.2.2 Selection of $R_{(CE)}$

The $\overline{CE}$ pin can be used to enable and disable the device. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

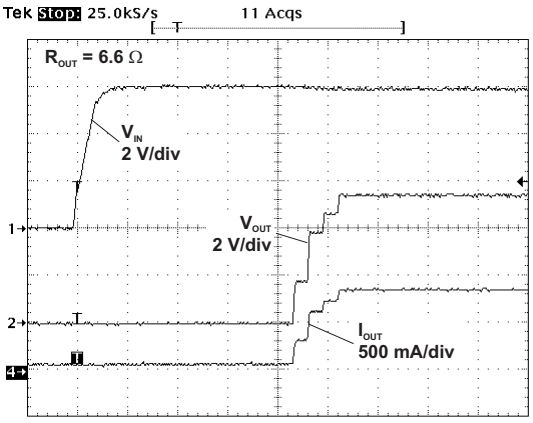
In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As with the VBAT pin (see previous discussion), the $\overline{CE}$ pin must be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor must be greater than V_{IH} of the bq2438x $\overline{CE}$ pin. The drop across the resistor is given by $R_{(CE)} \times I_{IH}$.

8.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 10 is for decoupling and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1 µF be used at the input of the device. It must be located in close proximity to the IN pin.

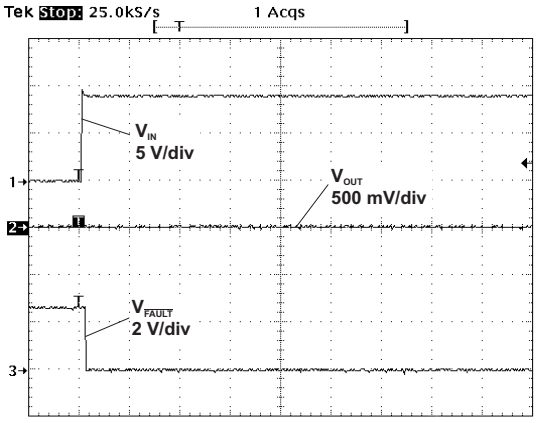
C_{OUT} in Figure 10 is also important. During an overvoltage transient, this capacitance limits the output overshoot until the power FET is turned off by the overvoltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 1 µF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection device.

8.2.3 Application Curves



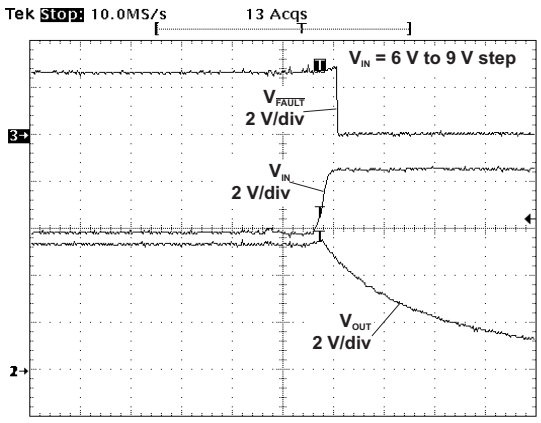
t - Time - 2 ms/div

Figure 11. Normal Power-On vs Showing Soft-Start (bq24380)



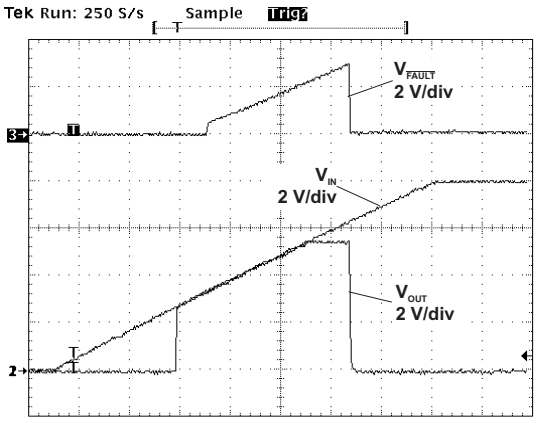
t - Time - 2 ms/div

Figure 12. OVP at Power-On



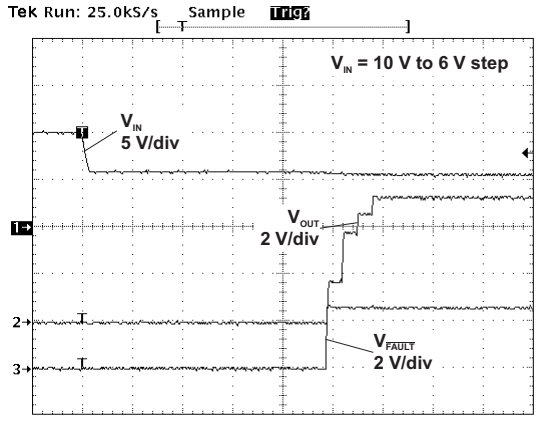
t - Time - 5 μs/div

Figure 13. OVP Response for Input Step (bq24380)



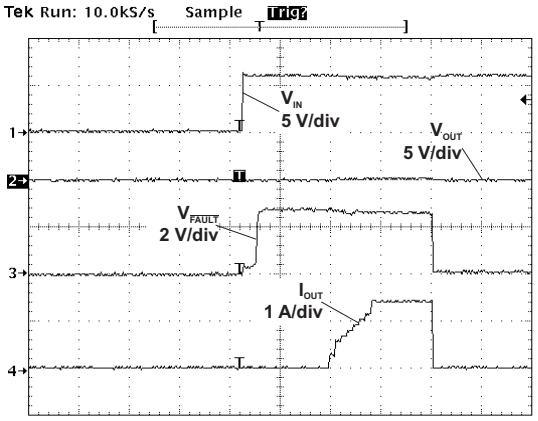
t - Time - 200 ms/div

Figure 14. Slow Input Ramp into OVP Event (bq24380)



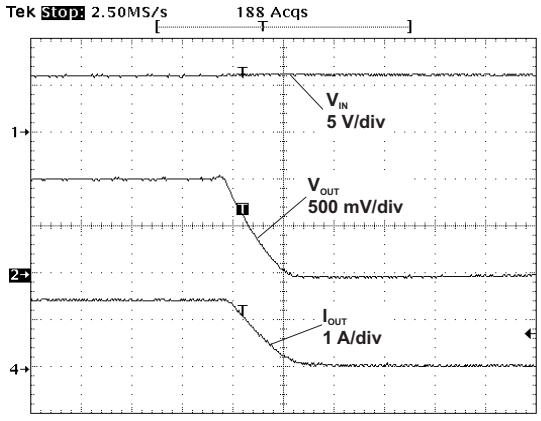
t - Time - 2 ms/div

Figure 15. Recovery from OVP (bq24380)



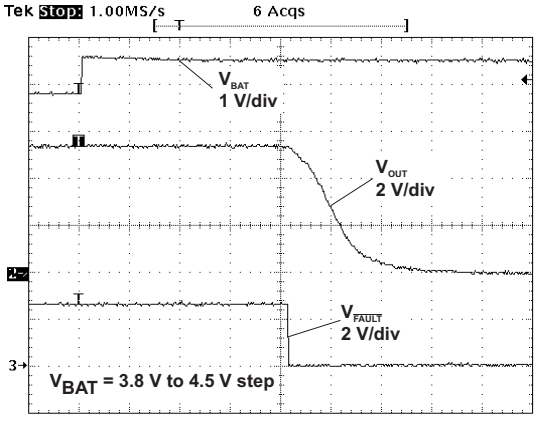
t - Time - 5 ms/div

Figure 16. Power Up into Short Circuit



t - Time - 20 μs/div

Figure 17. Soft-Stop During OCP Event (bq24380)



t - Time - 50 μs/div

Figure 18. Battery OVP Event (bq24380)

9 Power Supply Recommendations

The intention is for the bq2438x device to operate with 5-V adapters with a maximum current rating of 1.5 A. The device operates from sources from 3 V to 5.7 V. Outside of this range, the output is disconnected due to either UVLO or the OVP function.

10 Layout

10.1 Layout Guidelines

- This device is a protection device and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this device. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system. See Figure 19.
- The device uses WSON packages with a thermal pad. For good thermal performance, the thermal pad must be thermally coupled with the PCB ground plane (GND). In most applications, this requires a copper pad directly under the device. This copper pad must be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} should be located close to the device. Other components like $R_{(BAT)}$ should also be located close to the device.

10.2 Layout Example

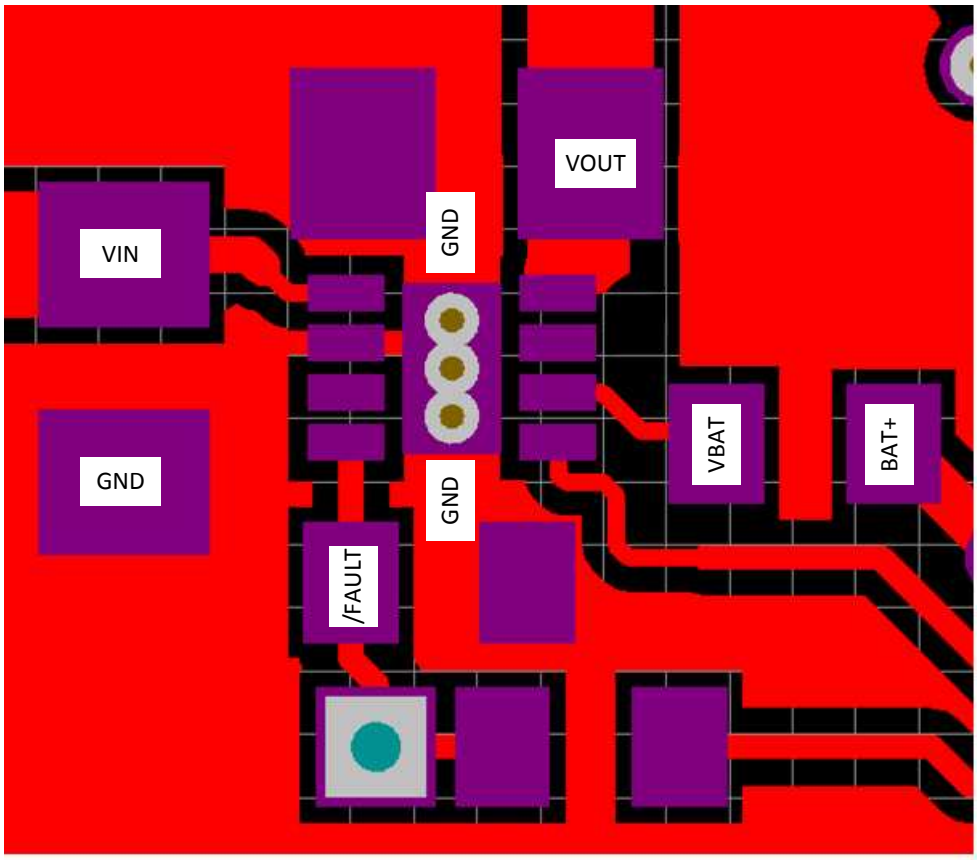


Figure 19. Layout Example Recommendation

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24380	Click here	Click here	Click here	Click here	Click here
bq24381	Click here	Click here	Click here	Click here	Click here
bq24382	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24380DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFE	Samples
BQ24380DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFE	Samples
BQ24381DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFW	Samples
BQ24381DSGRG4	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFW	Samples
BQ24381DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFW	Samples
BQ24382DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBE	Samples
BQ24382DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

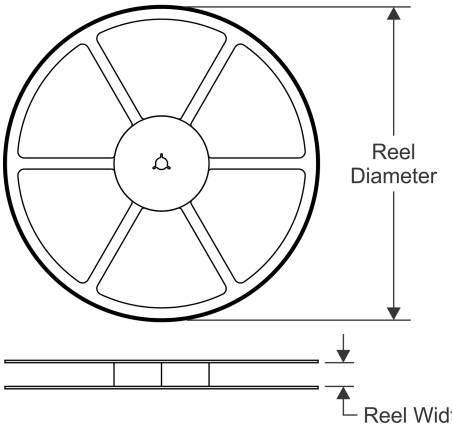
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

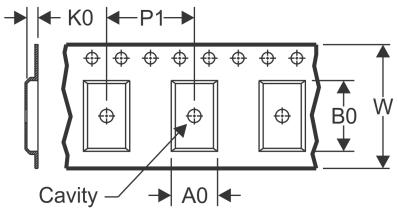
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

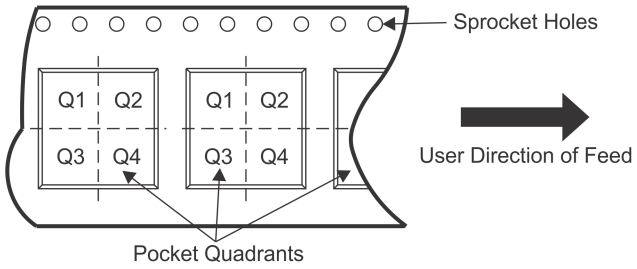


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

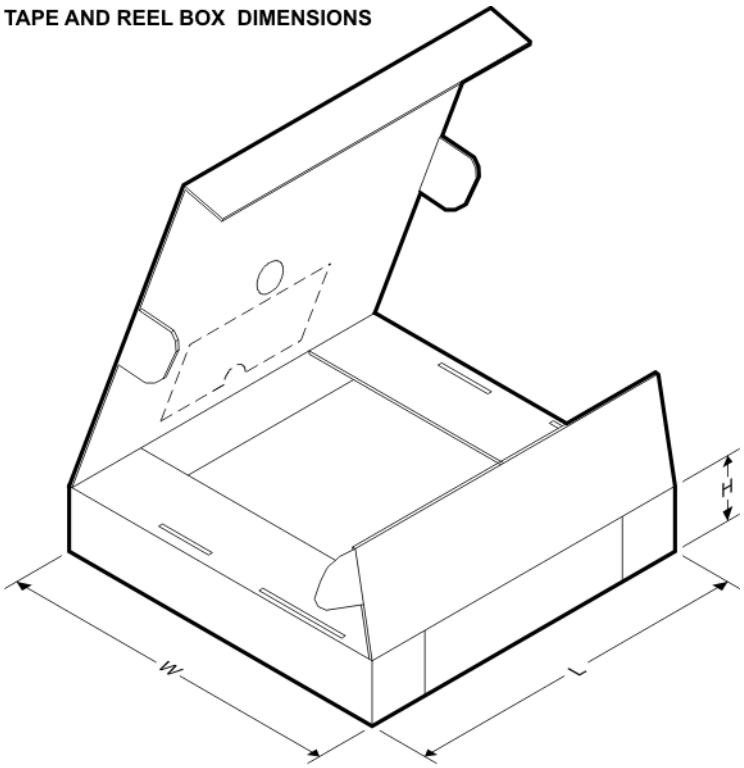
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24380DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24380DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24380DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
BQ24380DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24381DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24381DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24382DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24382DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24380DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24380DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
BQ24380DSGT	WSON	DSG	8	250	205.0	200.0	33.0
BQ24380DSGT	WSON	DSG	8	250	195.0	200.0	45.0
BQ24381DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24381DSGT	WSON	DSG	8	250	195.0	200.0	45.0
BQ24382DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24382DSGT	WSON	DSG	8	250	195.0	200.0	45.0

GENERIC PACKAGE VIEW

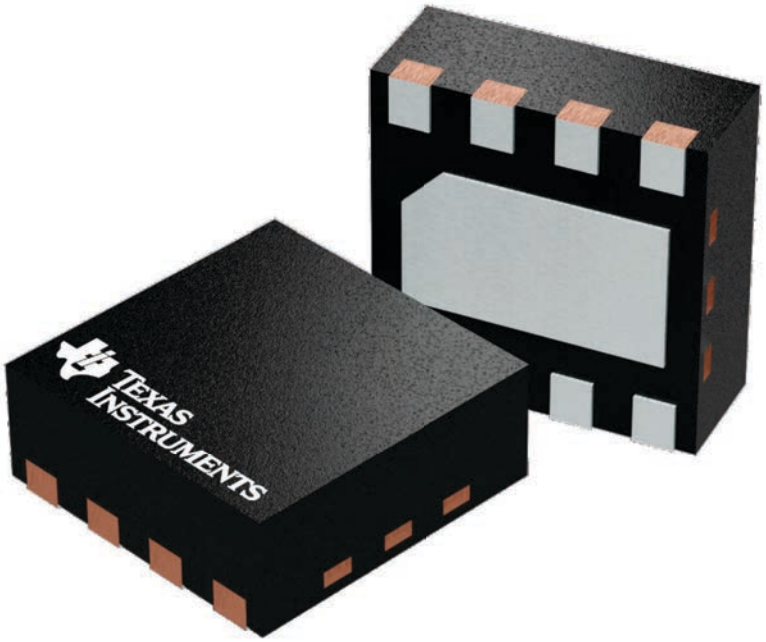
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



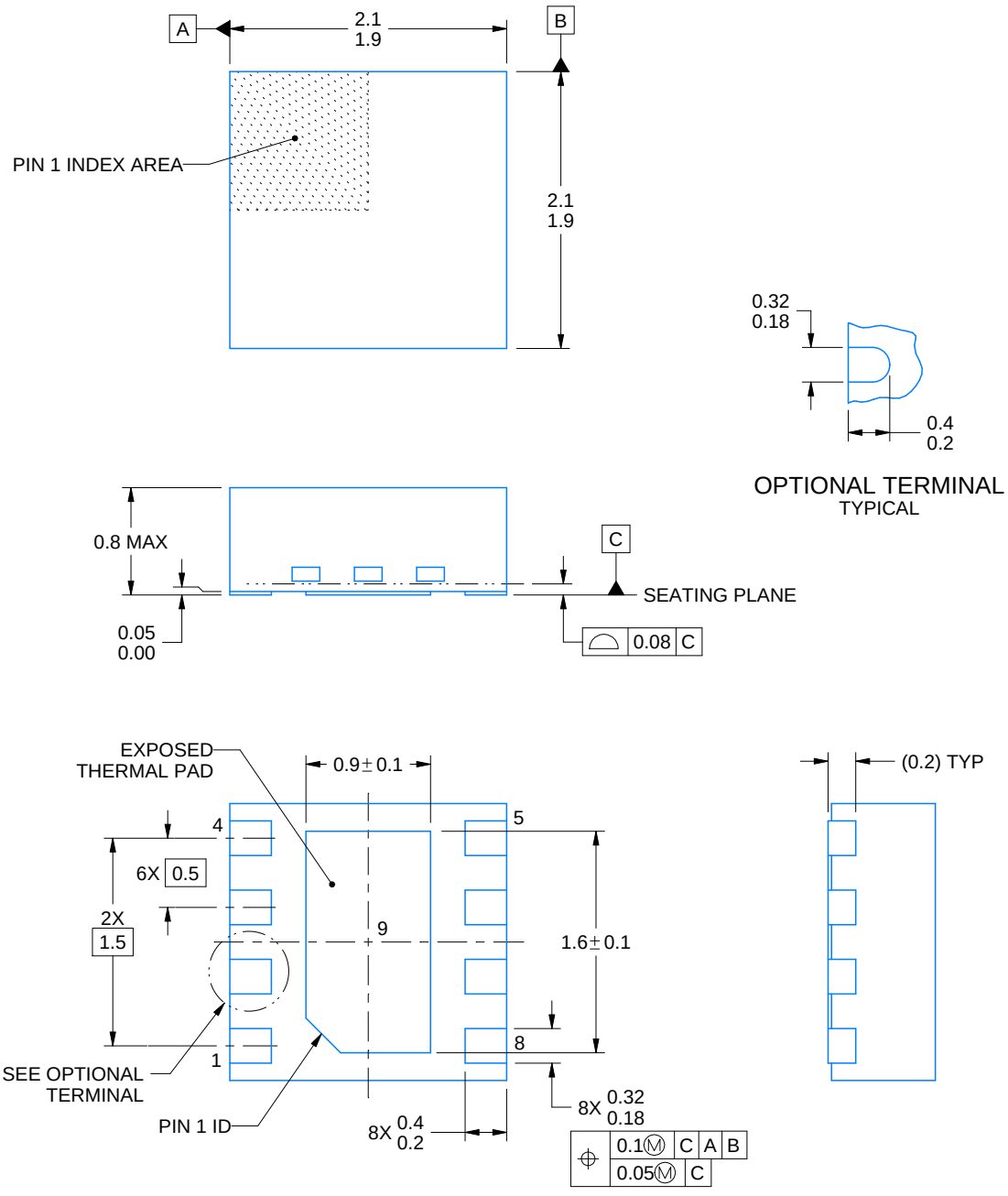
4224783/A

PACKAGE OUTLINE

DSG0008A

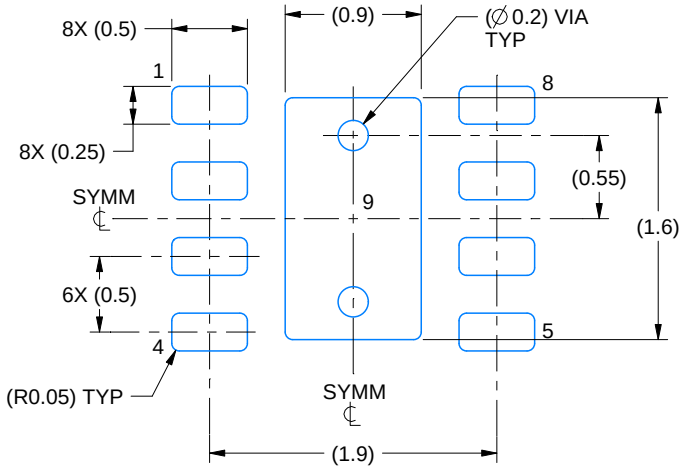
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

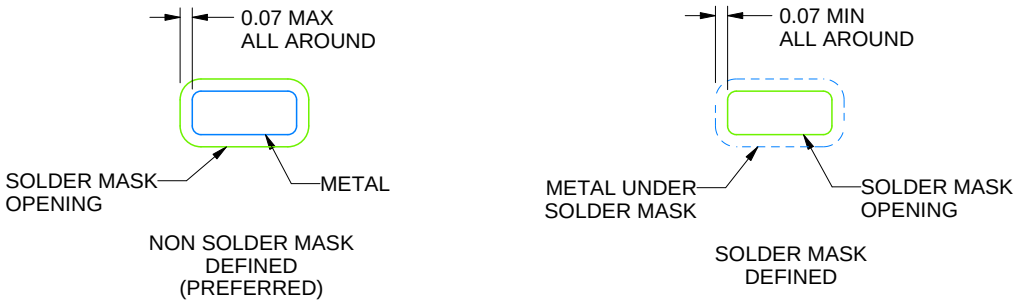


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

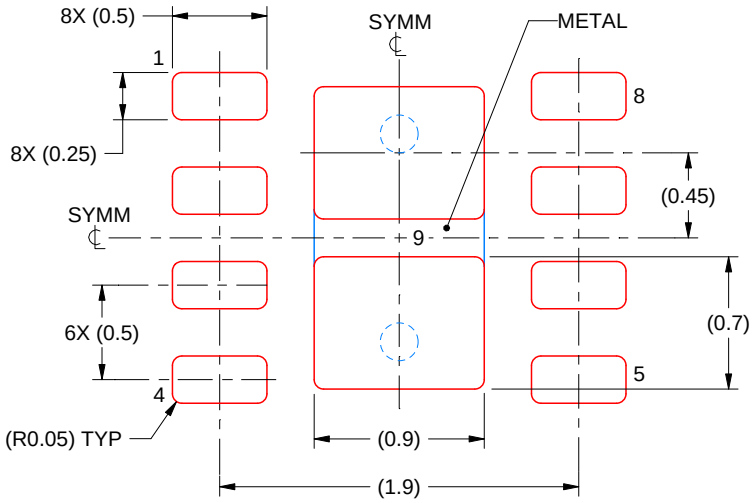


SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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