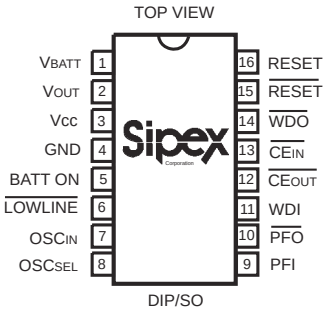
THE DATASHEET OF

UD2-5NU

Low Power Microprocessor Supervisory with Battery Switch-Over

FEATURES

- Precision 4.65V/4.40V Voltage Monitoring
- 200ms Or Adjustable Reset Time
- 100ms, 1.6s Or Adjustable Watchdog Time
- 60μA Maximum Operating Supply Current
- 2.0μA Maximum Battery Backup Current
- 0.1μA Maximum Battery Standby Current
- Power Switching
  250mA Output in Vcc Mode (0.6Ω)
  25mA Output in Battery Mode (5Ω)
- On-Board Gating of Chip-Enable Signals
  Memory Write-Cycle Completion
  6ns CE Gate Propagation Delay
- Voltage Monitor for Power-Fail or Low Battery
- Backup-Battery Monitor
- RESET Valid to Vcc=1V
- 1% Accuracy Guaranteed (**SP800L/800M**)
- Pin Compatible Upgrade to MAX691A/693A/800L/800M



Now Available in Lead Free Packaging

DESCRIPTION

The **SP691A/693A/800L/800M** is a microprocessor (μP) supervisory circuit that integrates a myriad of components involved in discrete solutions to monitor power-supply and battery-control functions in μP and digital systems. The **SP691A/693A/800L/800M** offers complete μP monitoring and watchdog functions. The **SP691A/693A/800L/800M** is ideal for a low-cost battery management solution and is well suited for portable, battery-powered applications with its supply current of 35μA. The 6ns chip-enable propagation delay, the 25mA current output in battery-backup mode, and the 250mA current output in standard operation also makes the **SP691A/693A/800L/800M** suitable for larger scale, high-performance equipment.

Part Number	RESET Threshold	RESET Accuracy	PFI Accuracy	Backup-Battery Switch
SP691A	4.65V	±125mV	±4%	YES
SP693A	4.40V	±125mV	±4%	YES
SP800L	4.65V	±50mV	±1%	YES
SP800M	4.40V	±50mV	±1%	YES

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Terminal Voltages (with respect to GND)
V_{CC}.....-0.3V to +6V
V_{BATT}.....-0.3V to +6V
All Other Inputs.....-0.3V to (V_{CC} +0.3V)

Input Currents
V_{CC} Peak.....1.0A
V_{CC} Continuous.....250mA
V_{BATT} Peak.....250mA
V_{BATT} Continuous.....25mA
GND, BATT ON.....100mA
All Other Inputs.....25mA

Enhanced ESD Specifications.....±4kV Human Body Model

Power Dissipation Per Package
16-pin PDIP (derate 14.3mW/°C above +70°C).....1150mW
16-pin Narrow SOIC (derate 13.6mW/°C above 70°C).....1090mW
16-pin Wide SOIC (derate 11.2mW/°C above 70°C).....900mW

Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering,10 sec).....+300°C

ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75V to +5.5V for the **SP691A/800L**, V_{CC} = +4.5V to +5.5V for the **SP693A/800M**, V_{BATT} = +2.8V, and T_{AMB} = T_{MIN} to T_{MAX} unless otherwise noted. Typical values apply at T_{AMB}=+25°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, V_{CC} or V_{BATT}, NOTE 1	0		5.5	V	
Output Voltage, V_{OUT} in Normal Operating Mode	V_{CC}-0.05 V_{CC}-0.3 V_{CC}-0.2	V_{CC}-0.015 V_{CC}-0.15 V_{CC}-0.09		V	V_{CC}=4.5V, I_{OUT}=25mA V_{CC}=4.5V, I_{OUT}=250mA V_{CC}=3.0V, V_{BATT}=2.8V, I_{OUT}=100mA
V_{CC}-to-V_{OUT} On-Resistance		0.6 0.9	1.2 2.0	Ω	V_{CC}=4.5V V_{CC}=3.0V
V_{OUT} in Battery-Backup Mode	V_{BATT}-0.3 V_{BATT}-0.25 V_{BATT}-0.15	V_{BATT}-0.1 V_{BATT}-0.07 V_{BATT}-0.05		V	V_{BATT}=4.5V, I_{OUT}=20mA V_{BATT}=2.8V, I_{OUT}=10mA V_{BATT}=2.0V, I_{OUT}=5mA
V_{BATT}-to-V_{OUT} On-Resistance		5 7 10	15 25 30	Ω	V_{BATT}=4.5V V_{BATT}=2.8V V_{BATT}=2.0V
Supply Current in Normal Operating Mode, I_{Vcc}		35	60	µA	V_{CC}>(V_{BATT}-1V), excluding I_{OUT}
Supply Current in Battery-Backup Mode, I_{BATT}, NOTE 2		0.001	2.0	µA	V_{CC}<(V_{BATT}-1.2V), V_{BATT}=2.8V, excluding I_{OUT}
V_{BATT} Standby Current, I_{BATT}, NOTE 3	-0.1		0.02	µA	V_{CC}≥(V_{BATT}+0.2V), excluding I_{OUT}
Battery Switchover Threshold		V_{BATT}+0.03 V_{BATT}-0.03		V	power-up power-down
Battery Switchover Hysteresis		60		mV	Peak to Peak

ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75V to +5.5V for the **SP691A/800L**, V_{CC} = +4.5V to +5.5V for the **SP693A/800M**, V_{BATT} = +2.8V, and T_{AMB} = T_{MIN} to T_{MAX} unless otherwise noted. Typical values apply at T_{AMB}=+25°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BATT ON Output Low Voltage		0.1 0.7	0.4 1.5	V	I_{SINK}=3.2mA I_{SINK}=25mA
BATT ON Output Short Circuit Current	 1	60 15	 100	mA µA	sink current source current
RESET, LOWLINE, AND WATCHDOG TIMER					
Reset Threshold Voltage	4.50 4.25 4.60 4.35	4.65 4.40 4.65 4.40	4.75 4.50 4.70 4.45	V	**SP691A** **SP693A** **SP800L** **SP800M**
Reset Threshold Hysteresis		15		mV	center-to-peak
V_{CC} to $\overline{\text{RESET}}$ Delay		80		µs	power down
$\overline{\text{LOWLINE}}$ to $\overline{\text{RESET}}$ Delay		800		ns	power down
Reset Active Timeout Period for the Internal Oscillator	140	200	280	ms	power-up
Reset Active Timeout Period for the External Clock, NOTE 4		2048		clock cycles	power-up
Watchdog Timeout Period for the Internal Oscillator	1.0 70	1.6 100	2.25 140	sec ms	long period short period
Watchdog Timeout Period for the External Clock, NOTE 4		4096 1024		clock cycles	long period short period
Minimum Watchdog Input Pulse Width	100			ns	V_{IL}=0.8V,V_{IH}=0.75xV_{CC}
$\overline{\text{RESET}}$ Output Voltage	 3.5	0.004 0.1	0.3 0.4	V	I_{SINK}=50µA, V_{CC}=1V, V_{CC} falling I_{SINK}=3.2mA, V_{CC}=4.25V I_{SOURCE}=1.6mA, V_{CC}=5V
$\overline{\text{RESET}}$ Output Short-Circuit Current		7	20	mA	output source current
RESET Output Voltage Low, NOTE 5		0.1	0.4	V	I_{SINK}=3.2mA
$\overline{\text{LOWLINE}}$ Output Voltage	 3.5	0.1	0.4	V	I_{SINK}=3.2mA, V_{CC}=4.25V I_{SOURCE}=1µA, V_{CC}=5V
$\overline{\text{LOWLINE}}$ Output Short Circuit Current		15	100	µA	output source current
$\overline{\text{WDO}}$ Output Voltage	 3.5	0.1	0.4	V	I_{SINK}=3.2mA I_{SOURCE}=500µA, V_{CC}=5V
$\overline{\text{WDO}}$ Output Short-Circuit Current		3	10	mA	output source current

V_{CC} = +4.75V to +5.5V for the **SP691A/800L**, V_{CC} = +4.5V to +5.5V for the **SP693A/800M**, V_{BATT} = +2.8V, and T_{AMB} = T_{MIN} to T_{MAX} unless otherwise noted. Typical values apply at T_{AMB}=+25°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
WDI Threshold Voltage, NOTE 6	0.75xV_{CC}		0.8	V	V_{IH} V_{IL}
WDI Input Current	-50	-10 20	50	µA	WDI=0V WDI=V_{OUT}
POWER-FAIL COMPARATOR					
PFI Input Threshold	1.237 1.225	1.25 1.25	1.263 1.275	V	**SP691A/693A**, V_{CC}=5V **SP800L/800M**, V_{CC}=5V
PFI Leakage Current		±0.01	±25	nA	
$\overline{PFO}$ Output Voltage	 3.5	0.1	0.4	V	I_{SINK}=3.2mA I_{SOURCE}=1µA, V_{CC}=5V
$\overline{PFO}$ Short Circuit Current	 1	60 15	 100	mA µA	output sink current output source current
PFI-to-$\overline{PFO}$ Delay		25 60		µs	V_{OD}=15mV V_{OD}=15mV
CHIP-ENABLE GATING					
$\overline{CE_{IN}}$ Leakage Current		±0.005	±1	µA	disable mode
$\overline{CE_{IN}}$ to $\overline{CE_{OUT}}$ Resistance, NOTE 7		65	150	Ω	enable mode
$\overline{CE_{OUT}}$ Short-Circuit Current (RESET Active)	0.1	0.75	2.0	mA	disable mode, $\overline{CE_{OUT}}$=0V
$\overline{CE_{IN}}$ to $\overline{CE_{OUT}}$ Propagation Delay, NOTE 8		6	10	ns	50Ω source impedance driver, C_{LOAD}=50pF
$\overline{CE_{OUT}}$ Output Voltage High (RESET Active)	3.5 2.7			V	V_{CC}=5V, I_{OUT}= 100µA V_{CC}=0V, V_{BATT}=2.8V, I_{OUT}=1µA
RESET to $\overline{CE_{OUT}}$ Delay		12		µs	power-down
INTERNAL OSCILLATOR					
OSC_{IN} Leakage Current		0.10	±5.0	µA	OSC_{SEL}=0V
OSC_{IN} Input Pull-Up Current		10	100	µA	OSC_{SEL}=V_{OUT} or floating, OSC_{IN}=0V
OSC_{SEL} Input Pull-Up Current		10	100	µA	OSC_{SEL}=0V
OSC_{IN} Frequency Range		200		kHz	OSC_{SEL}=0V
OSC_{IN} External Oscillator Threshold Voltage	V_{OUT}-0.3	V_{OUT}-0.6 3.65	 2.0	V	V_{IH} V_{IL}
OSC_{IN} Frequency with External Capacitor		2		kHz	OSC_{SEL}=0V, C_{OSC}=47pF

ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75V to +5.5V for the **SP691A/800L**, V_{CC} = +4.5V to +5.5V for the **SP693A/800M**, V_{BATT} = +2.8V, and $T_{AMB} = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values apply at T_{AMB}=+25°C.

NOTE 1: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.

NOTE 2: The supply current drawn by the **SP691A/693A/800L/800M** from the battery (excluding I_{OUT}) typically goes to 5µA when (V_{BATT} - 1V) < V_{CC} < V_{BATT}. In most applications, this is a brief period as V_{CC} falls through this region.

NOTE 3: "+" = battery-discharging current, "-" = battery-charging current.

NOTE 4: Although presented as typical values, the number of clock cycles for the reset and watchdog timeout periods are fixed and do not vary with process or temperature.

NOTE 5: RESET is an open-drain output and sinks current only.

NOTE 6: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

NOTE 7: The chip-enable resistance is tested with V_{CC} = +4.75V for the **SP691A/800L** and V_{CC} = +4.5V for the **SP693A/800M**. $\overline{CE_{IN}} = \overline{CE_{OUT}} = V_{CC}/2$.

NOTE 8: The chip-enable propagation delay is measured from the 50% point at $\overline{CE_{IN}}$ to the 50% point at $\overline{CE_{OUT}}$.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_{AMB} = 25°C, unless otherwise noted)

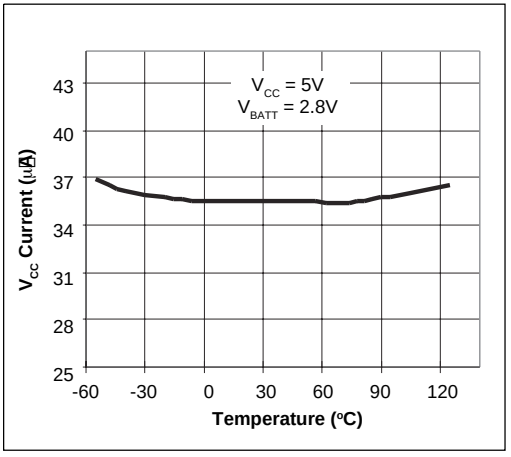


Figure 1. V_{CC} Supply Current vs. Temperature (Normal Operating Mode)

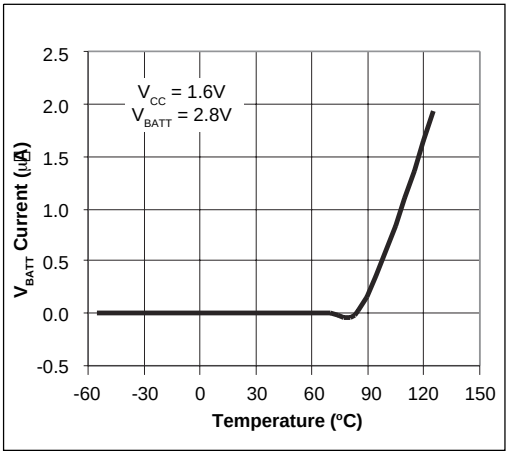


Figure 2. Battery Supply Current vs. Temperature (Battery-Backup Mode)

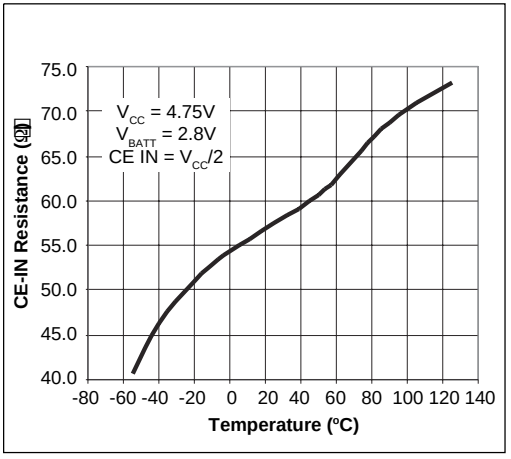


Figure 3. Chip-Enable On-Resistance vs. Temperature

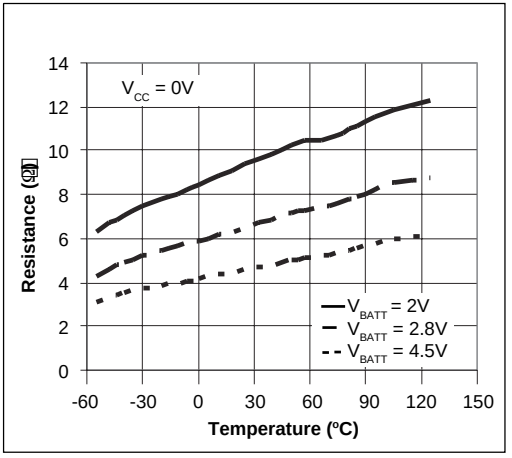


Figure 4. V_{BATT} to V_{OUT} On-Resistance vs. Temperature

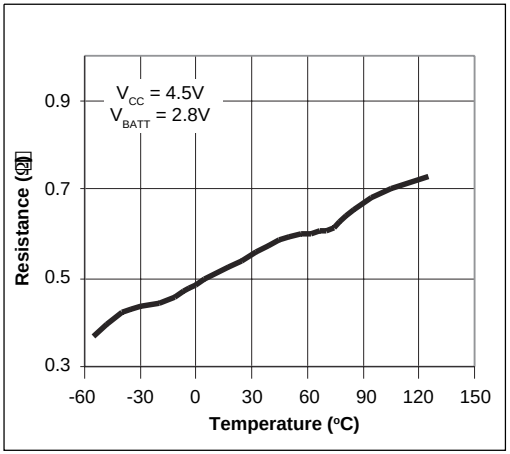


Figure 5. V_{CC} to V_{OUT} On-Resistance vs. Temperature

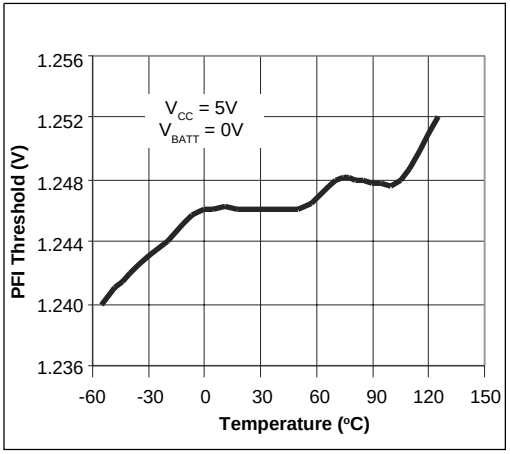


Figure 6. PFI Threshold vs. Temperature

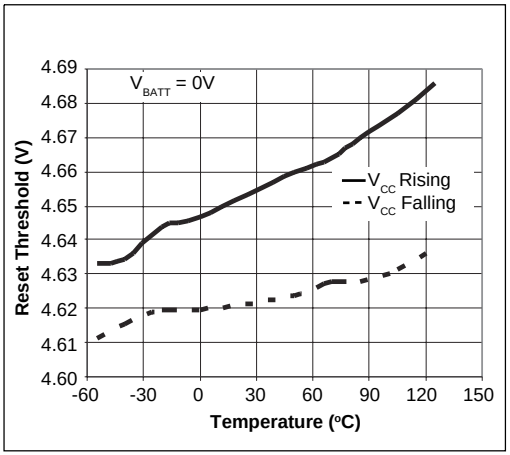


Figure 7. Reset Threshold vs. Temperature

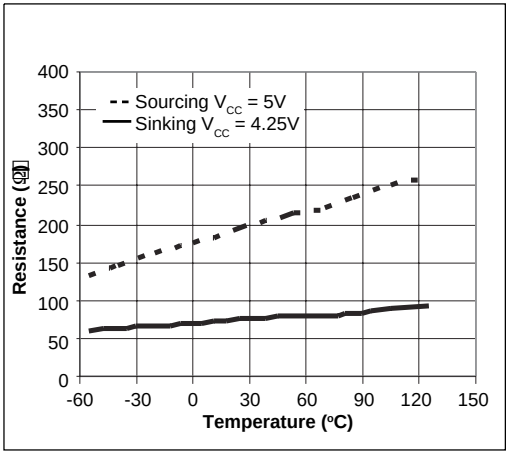


Figure 8. $\overline{RESET}$ Output Resistance vs. Temperature

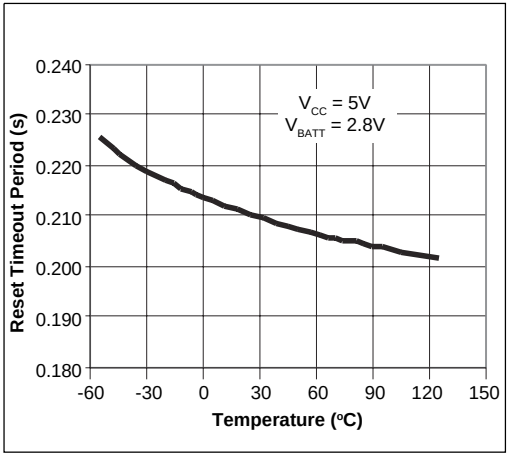


Figure 9. Reset Delay vs. Temperature

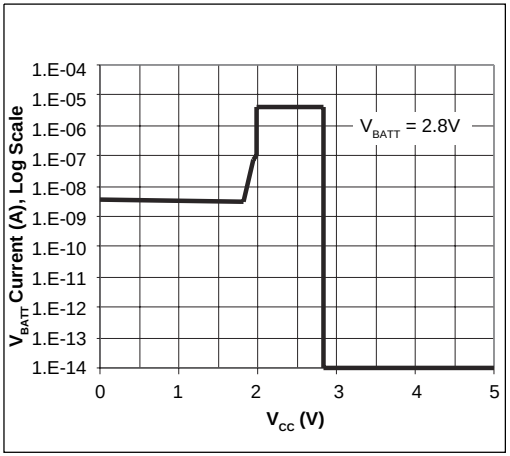


Figure 10. Battery Current vs. Input Supply Voltage

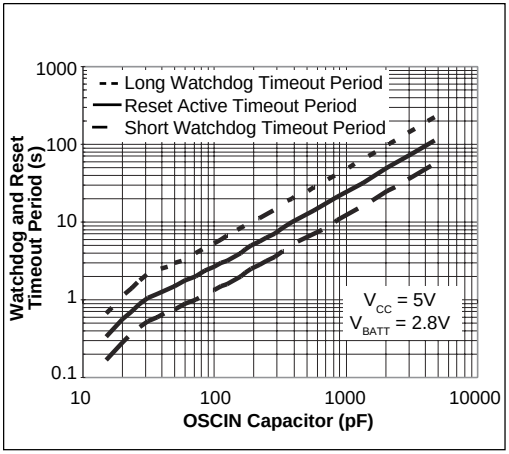


Figure 11. Watchdog and Reset Timeout Period vs. OSC_{IN} Timing Capacitor (C_{OSC})

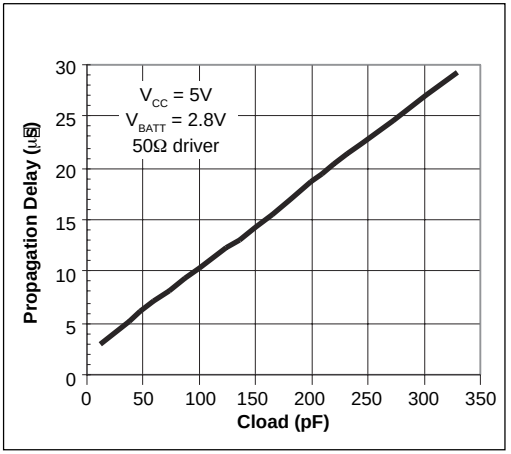


Figure 12. Chip-Enable Propagation Delay vs. $\overline{CE_{OUT}}$ Load Capacitance

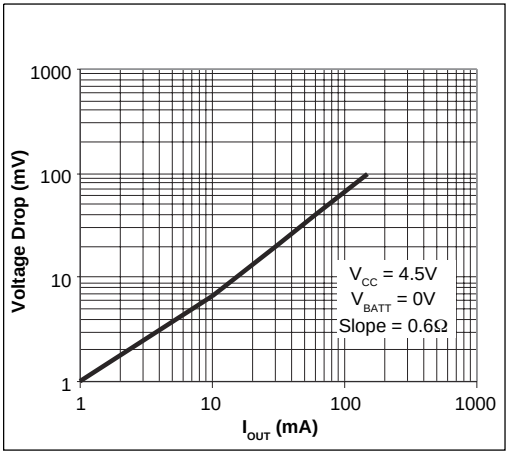


Figure 13. V_{CC} to V_{OUT} vs. Output Current (Normal Operating Mode)

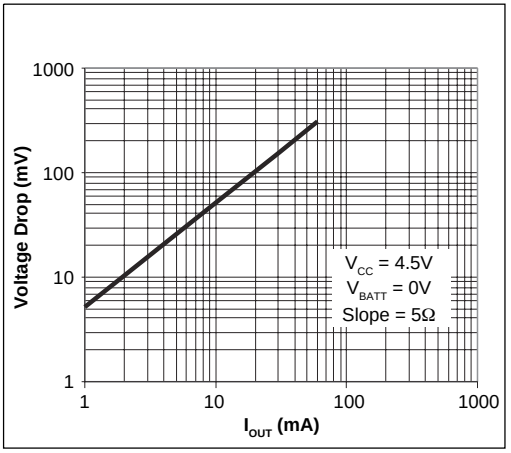


Figure 14. V_{BATT} to V_{OUT} vs. Output Current (Battery-Backup Mode)

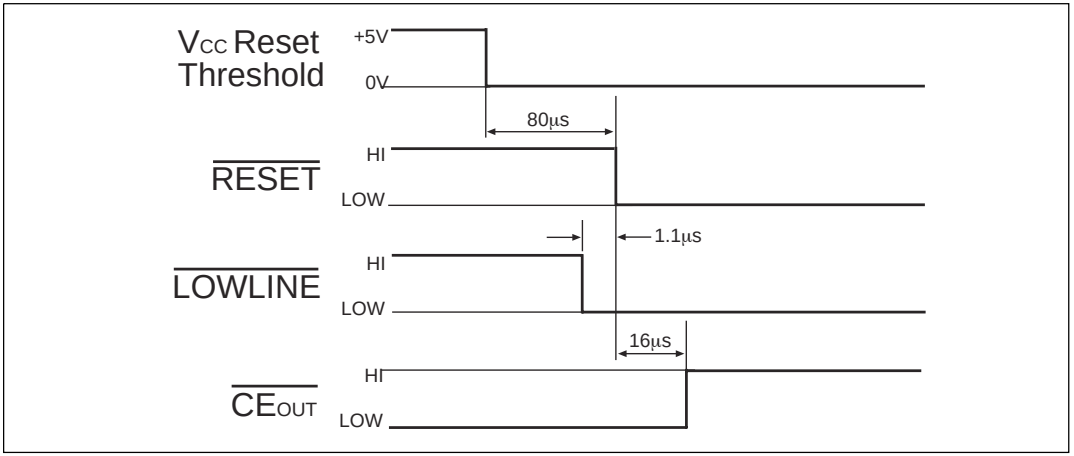
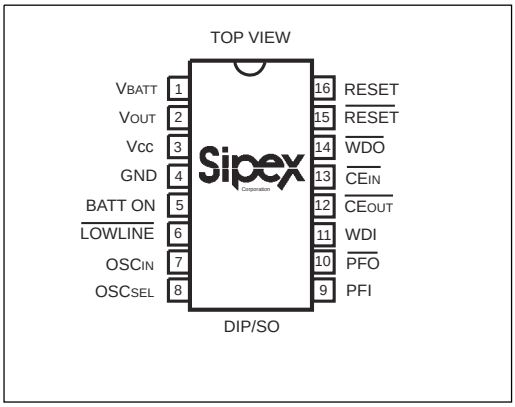


Figure 15. V_{CC} to $\overline{LOWLINE}$ and $\overline{CE_{OUT}}$ Delay

PINOUT



PIN ASSIGNMENTS

Pin 1 — V_{BATT} — Battery-Backup Input. Connect to the external battery supply or supercharging capacitor and charging circuit. If a backup battery is not provided, connect this pin to ground.

Pin 2 —V_{OUT} — Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than V_{BATT} and V_{CC} is above the reset threshold. When V_{CC} falls below V_{BATT} and V_{CC} is below the reset threshold, V_{OUT} connects to V_{BATT}. Connect a 0.1µF capacitor from V_{OUT} to GND.

Pin 3 — V_{CC} — +5V Input Supply Voltage.

Pin 4 — GND — Ground reference for all signals.

Pin 5 — BATT ON — Battery On Output. Goes high when V_{OUT} switches to V_{BATT}. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.

Pin 6 — LOWLINE — Low Line Output. This output pin goes LOW when V_{CC} falls below the reset threshold voltage. This output pin returns to its HIGH output as soon as V_{CC} rises above the reset threshold voltage.

Pin 7 — OSC_{IN} — External Oscillator Input. When OSC_{SEL} is unconnected or driven HIGH, a 10µA pull-up connects from V_{OUT} to this input pin, the internal oscillator sets the reset and watchdog timeout periods, and this input pin selects between fast and slow watchdog timeout periods. When OSC_{SEL} is driven LOW, the reset and watchdog timeout periods may be set either by a capacitor from this input pin to ground or by an external clock at this pin (refer to *Figure 21*).

Pin 8 — OSC_{SEL} — Oscillator Select. When OSC_{SEL} is unconnected or driven HIGH, the internal oscillator sets the reset delay and watchdog timeout period. When OSC_{SEL} is driven LOW, the external oscillator input pin, OSC_{IN}, is enabled (refer to *Table 1*). This input pin has a 10µA internal pull-up.

Pin 9 — PFI — Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.

Pin 10 — $\overline{PFO}$ — Power-Fail Output. This is the output of the power-fail comparator. PFO goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.

Pin 11 — WDI — Watchdog Input. This is a three-level input pin. If WDI remains either HIGH or LOW for longer than the watchdog timeout period, $\overline{WDO}$ goes LOW and $\overline{RESET}$ is asserted for the reset timeout period. $\overline{WDO}$ remains LOW until the next transition at this input pin. Leaving this input pin unconnected disables the watchdog function. This input pin connects to an internal voltage divider between V_{OUT} and ground, which sets it to mid-supply when left unconnected.

Pin 12 — $\overline{CE_{OUT}}$ — Chip-Enable Output. This output pin goes LOW only when $\overline{CE_{IN}}$ is LOW and V_{CC} is above the reset threshold voltage. If $\overline{CE_{IN}}$ is LOW when RESET is asserted, this output pin will stay low for 16µs or until $\overline{CE_{IN}}$ goes HIGH, whichever occurs first.

Pin 13 — $\overline{CE_{IN}}$ — Chip-Enable Input. This is the input pin to the chip-enable gating circuit. If this input pin is not used, connect it to ground or V_{OUT}.

Pin 14 — $\overline{WDO}$ — Watchdog Output. If WDI remains HIGH or LOW longer than the watchdog timeout period, this output pin goes LOW and RESET is asserted for the reset timeout period. This output pin returns HIGH on the next transition at WDI. This output pin remains HIGH if WDI is unconnected.

Pin 15 — $\overline{RESET}$ — Active LOW Reset Output. This output pin goes LOW whenever V_{CC} falls below the reset threshold. This output pin will remain low typically for 200ms after V_{CC} crosses the reset threshold voltage on power-up.

Pin 16 — RESET — Active HIGH Reset Output. This output pin is open drain and the inverse of RESET.

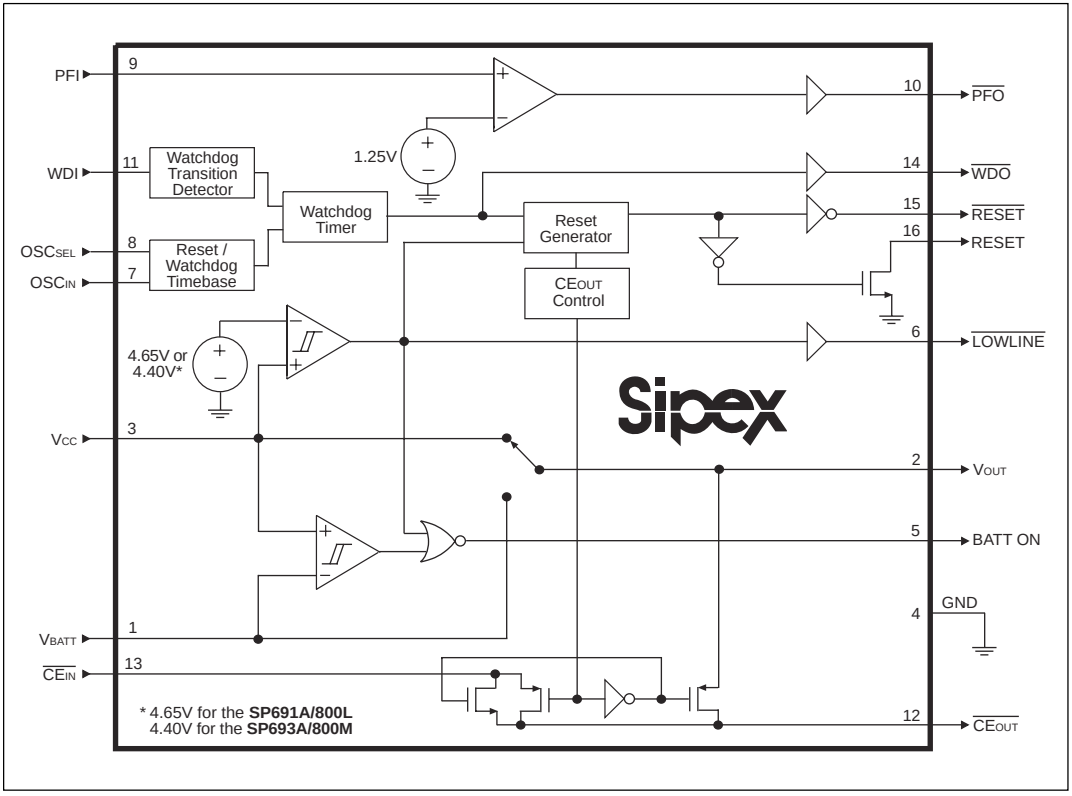


Figure 16. Internal Block Diagram of the SP691A/693A/800L/800M

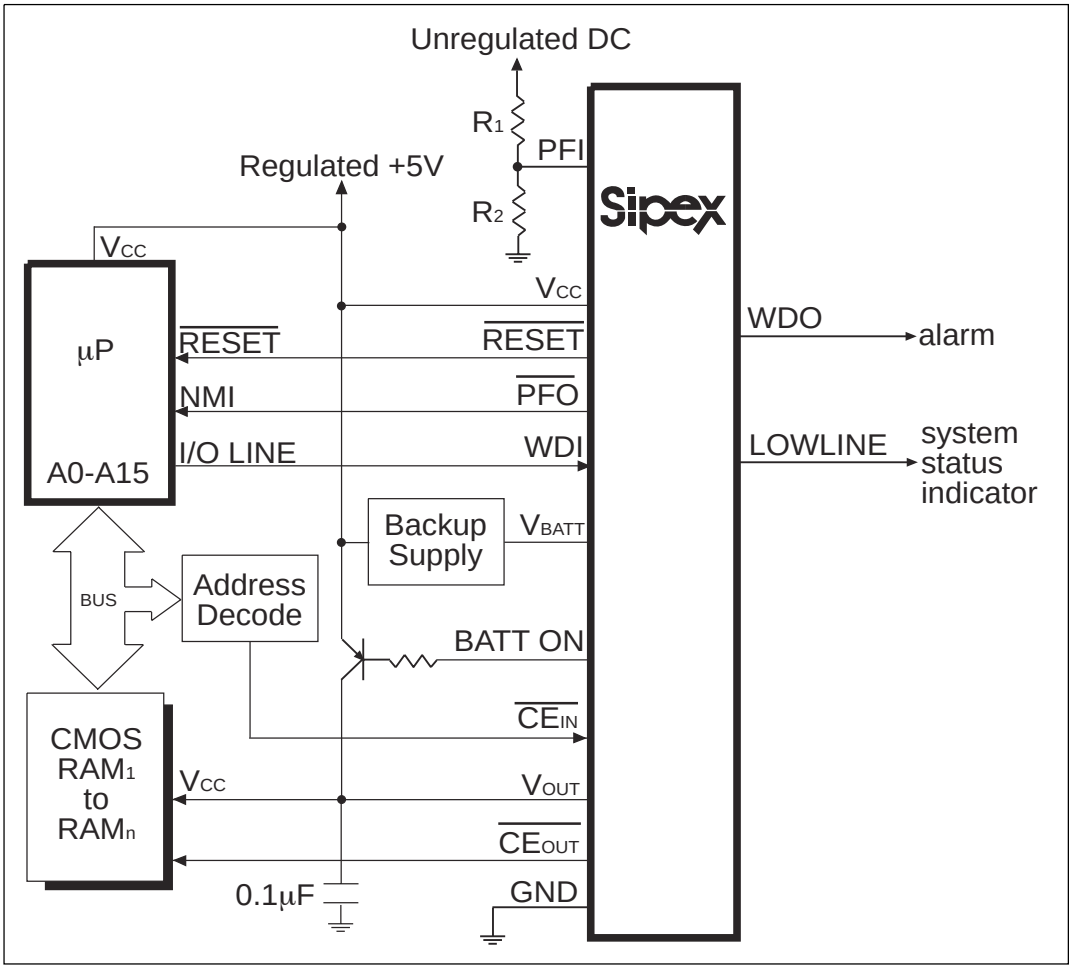


Figure 17. Typical Application Circuit of the SP691A/693A/800L/800M

FEATURES

The **SP691A/693A/800L/800M** devices are microprocessor (μP) supervisory circuits that monitor the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The **SP691A/693A/800L/800M** series is an ideal solution for portable, battery-powered equipment that require power supply monitoring. The **SP691A/693A/800L/800M** watchdog functions will continuously oversee the operational status of a system. Implementing the **SP691A/693A/800L/800M** series will reduce the number of components and overall complexity in a design that requires power supply monitoring circuitry. The operational features and benefits of this series are described in more detail below.

THEORY OF OPERATION

The **SP691A/693A/800L/800M** series is a complete μP supervisor IC and provides the following main functions:

1) μP reset ➡ Reset output is asserted during power fluxiations such as power-up, power-down, and brown out conditions, and is guaranteed to be in the correct state for VCC down to 1V, even with no battery in the circuit.

2) μP reset ➡ Reset output is pulsed if the optional watchdog timer has not been toggled within a specified time.

3) Power Fail Comparator ➡ Provides for power-fail warning and low-battery detection, or monitors another power supply.

4) Watchdog function ➡ Monitors µP activity where the watchdog output goes to a logic LOW state if the watchdog input is not toggled for greater than the timeout period.

5) Internal switch ➡ Switches over from V_{CC} to V_{BATT} if the V_{CC} falls below the reset threshold.

$\overline{\text{RESET}}$ and RESET Outputs

The **SP691A/693A/800L/800M** devices' $\overline{\text{RESET}}$ and RESET outputs ensure that the µP powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The $\overline{\text{RESET}}$ output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, $\overline{\text{RESET}}$ sources 1.6mA at typically VOUT – 0.5V. RESET output is open drain, active high, and typically sinks 3.2mA with a saturation voltage of 0.1V. When no backup battery is used, $\overline{\text{RESET}}$ output is guaranteed to be valid down to VCC = 1V, and an external 10kΩ pull-down resistor on $\overline{\text{RESET}}$ ensures that $\overline{\text{RESET}}$ will be valid with VCC down to GND as shown on *Figure 18*. As VCC goes below 1V, the gate drive to the $\overline{\text{RESET}}$ output switch reduces accordingly, increasing the R_{DS}(ON) and the saturation voltage. The 10kΩ pull-down resistor ensures the parallel combination of switch plus resistor is around

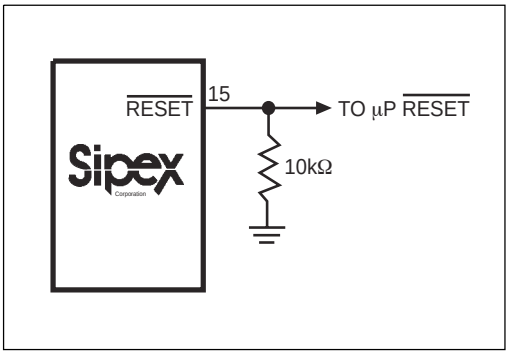


Figure 18. External Pull-down Resistor Ensures $\overline{\text{RESET}}$ is Valid with V_{CC} Down to Ground.

10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for the $\overline{\text{RESET}}$ output with Vcc = 4.75V is 4.5V typical. For battery voltages less than or equal to 2V connected to VBATT, $\overline{\text{RESET}}$ and RESET remains valid for VCC from 0V to 5.5V.

$\overline{\text{RESET}}$ and RESET are asserted when V_{CC} falls below the reset threshold and remain asserted for the Reset Timeout Period (200ms nominal) after V_{CC} rises above the reset threshold voltage on power-up. Refer to *Figure 19*. The devices' battery-switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

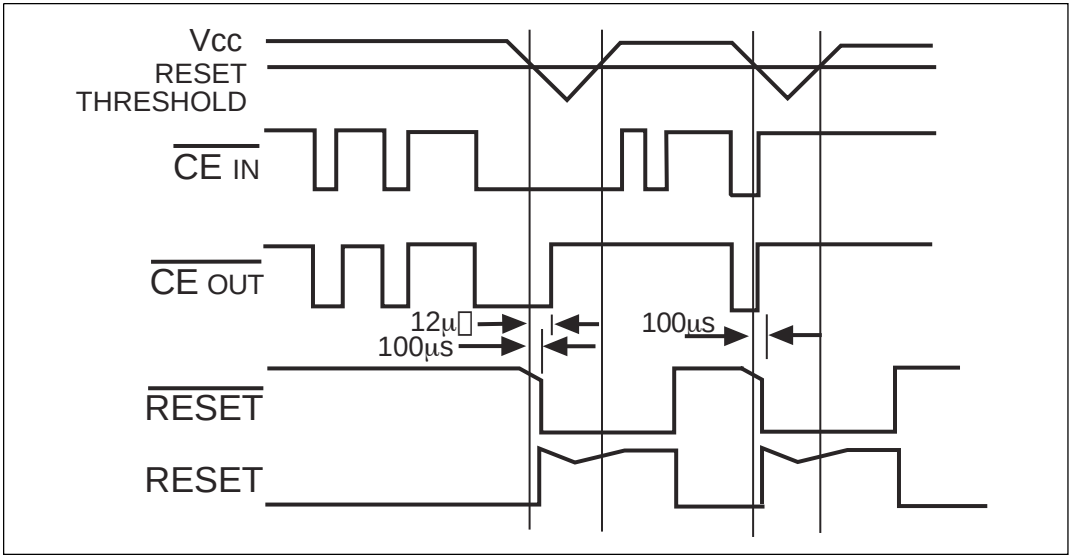


Figure 19. Reset and Chip-Enable Timing

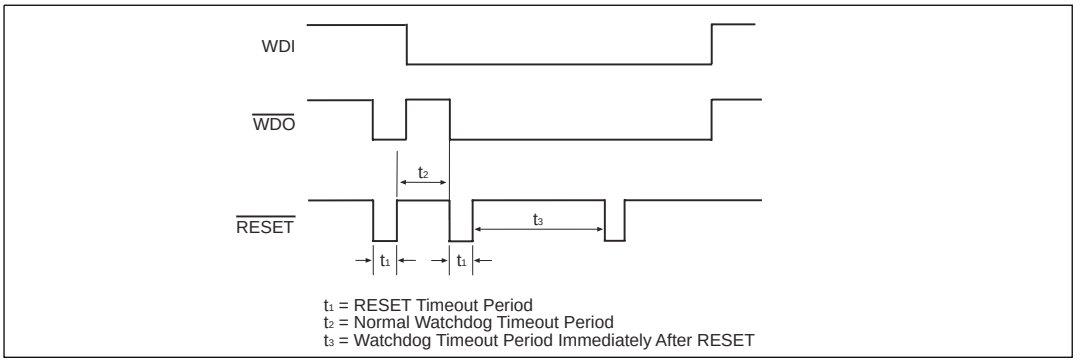


Figure 20. Watchdog Timeout Period and Reset Active Time

Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, $\overline{\text{RESET}}$ and RESET are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6s nominal). $\overline{\text{WDO}}$, $\overline{\text{RESET}}$, and RESET are asserted, indicating a software fault or idle conditions. Refer to **$\overline{\text{RESET}}$ and RESET Outputs** and **Watchdog Output** sections.

Watchdog Input

A change of logic state (minimum 100ns duration) at WDI during the watchdog period will reset the watchdog timer. The watchdog default timout is 1.6sec.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When Vcc is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

$\overline{\text{WDO}}$ remains high if there is activity (transition or pulse) at WDI during the watchdog-timeout period. The watchdog function is disabled and $\overline{\text{WDO}}$ is a logic high when V_{CC} is less than the reset threshold or when WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog-timeout period,

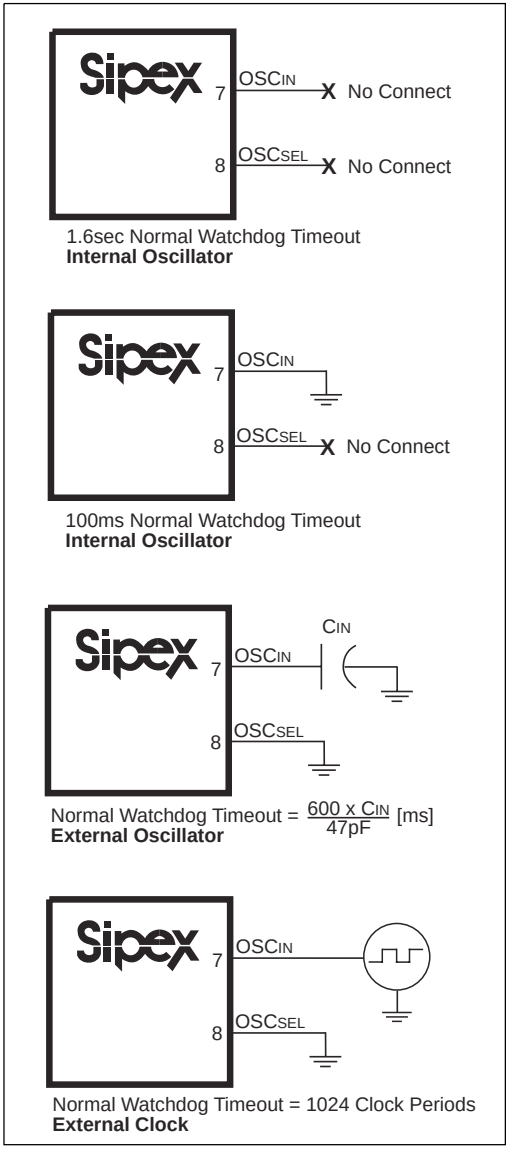


Figure 21. Selecting Timeout Periods

OSC_{SEL}	OSC_{IN}	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
LOW	External Clock Input	1024 clocks	4096 clocks	2048 clocks
LOW	External Capacitor	(600/47pF x C) ms	(2.4/47 pf x C) sec	(1200/47pF x C) ms
Floating	LOW	100 ms	1.6 s	200 ms
Floating	Floating	1.6 s	1.6 s	200 ms

Table 1. Reset Pulse Width and Watchdog Timeout Selections

$\overline{RESET}$ and RESET are asserted for the reset timeout period (200ms nominal). $\overline{WDO}$ goes to logic low and remains low until the next transition at WDI. Refer to *Figure 20*. If WDI is held high or low indefinitely, $\overline{RESET}$ and RESET will generate 200ms pulses every 1.6s. $\overline{WDO}$ has a 2 x TTL output characteristic.

Selecting an Alternative Watchdog Timeout Period

The OSC_{SEL} and OSC_{IN} inputs control the watchdog are reset timeout periods. Floating OSC_{SEL} and OSC_{IN} or tying them both to V_{OUT} selects the nominal 1.6s watchdog timeout period and 200ms reset timout period. Connecting OSC_{IN} to ground and floating or connecting OSC_{SEL} to V_{OUT} selects a 100ms normal watchdog timeout period and a 1.6s timeout period immediately after reset. The reset timeout period remains 200ms. Refer to *Figure 20*. Select alternative timeout periods by connecting OSC_{SEL} to ground and connecting a capacitor between OSC_{IN} and ground, or by externally driving OSC_{IN} . A synopsis of this control can be found in *Figure 21* and *Table 1*.

Chip-Enable Signal Gating

The **SP691A/693A/800L/800M** devices provide internal gating of chip-enable (CE) signals, to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The **SP691A/693A/800L/800M** devices use a series transmission gate from $\overline{CE_{IN}}$ to $\overline{CE_{OUT}}$. Refer to *Figure 16.*

The 10ns maximum CE propagation from $\overline{CE_{IN}}$ to $\overline{CE_{OUT}}$ enables the **SP691A/693A/800L/800M** devices to be used with most µPs.

Chip-Enable Input

$\overline{CE_{IN}}$ is in high impedance (disabled mode) while $\overline{RESET}$ and/or RESET are asserted.

During a power-down sequence where V_{CC} falls below the reset threshold, $\overline{CE_{IN}}$ assumes a high impedance state when the voltage at $\overline{CE_{IN}}$ goes high or 12µs after RESET is asserted, whichever occurs first. Refer to *Figure 19*. During a power-up sequence, CE_{IN} remains high impedance until RESET is deasserted.

In the high-impedance mode, the leakage currents into $\overline{CE_{IN}}$ are <1µA over temperature. In the low-impedance mode, the impedance of $\overline{CE_{IN}}$ appears as a 65Ω resistor in series with the load at $\overline{CE_{OUT}}$.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE_{IN}}$ and the capacitive loading on $\overline{CE_{OUT}}$ (see the Chip-Enable Propagation Delay vs. $\overline{CE_{OUT}}$ Load Capacitance graph in the **Typical Performance Characteristics** section). The CE propagation delay is defined from the 50% point on $\overline{CE_{IN}}$ to the 50% point on $\overline{CE_{OUT}}$ using a 50Ω driver and 50pF of load capacitance as in *Figure 22*. For minimum propagation delay, minimize the capacitive load at $\overline{CE_{OUT}}$ and use a low output-impedance driver.

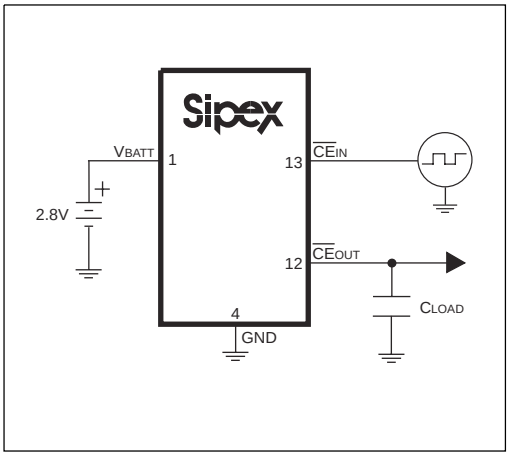


Figure 22. Chip Enable Propagation Delay Test Circuit

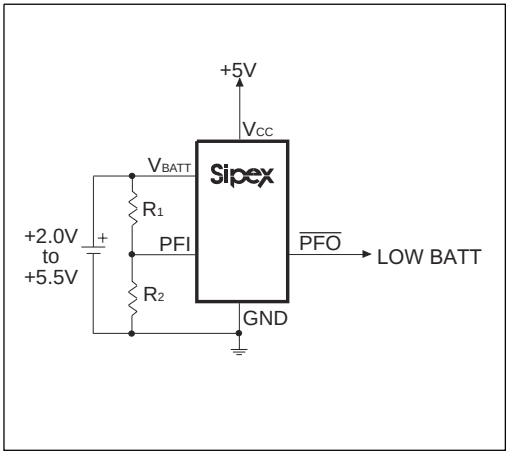


Figure 23. Low-Battery Indicator Circuit

Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}_{OUT}$ is equivalent to 65Ω in series with the source driving $\overline{CE}_{IN}$. In the disabled mode, the 65Ω transmission gate is off and $\overline{CE}_{OUT}$ is actively pulled to VOUT. This source turns off when the transmission gate is enabled.

$\overline{\text{LOWLINE}}$ Output

$\overline{\text{LOWLINE}}$ is the buffered output pin of the reset threshold comparator. Refer to *Figure 16*. $\overline{\text{LOWLINE}}$ typically sinks 3.2mA at 0.1V. For normal operation where V_{CC} is above the reset threshold, $\overline{\text{LOWLINE}}$ is pulled to V_{OUT}.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the **SP691A/693A/800L/800M** devices. Common uses include low battery detection, as found in *Figure 23*, and early power-fail detection when the unregulated power is easily accessible as shown in *Figure 17*.

Power-Fail Input

The Power-Fail Input (PFI) has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 25µs from VIL to VOL (power failing), and 60µs from VIH to VOH (power being restored). Connect this input to ground if PFI is not used.

Power-Fail Output

The Power-Fail Output ($\overline{\text{PFO}}$) goes low when PFI goes below 1.25V. It sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, PFO is actively pulled to VOUT. PFO can be used to generate an NMI for the µP, as shown in *Figure 17*.

Battery-Backup Mode

The **SP691A/693A/800L/800M** requires two conditions to switch to battery-backup mode: 1) VCC must be below the reset threshold; 2) VCC must be below VBATT. *Table 2* lists the status of the inputs and outputs in battery-backup mode.

Battery-On Output

The Battery On Output (BATT ON) indicates the status of the internal VCC/battery-switchover comparator, which controls the internal VCC and VBATT switches. For VCC greater that VBATT (ignoring the small hysteresis effect), BATT ON is a logic low. For V_{CC} less than V_{BATT}, BATT ON is a logic high. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications. Refer to *Figure 17*.

NAME	STATUS	PIN NUMBER
V_{BATT}	Supply current is 1µA maximum when V_{CC}<(V_{BATT}-1.2V).	1
V_{OUT}	V_{OUT} connected to V_{BATT} through an internal PMOS switch.	2
V_{CC}	Battery switchover comparator monitors V_{CC} for active switchover. V_{CC} is disconnected from V_{OUT}.	3
GND	0V reference for all signals.	4
BATT ON	Logic HIGH. The open-circuit output voltage is equal to V_{OUT}.	5
$\overline{\text{LOWLINE}}$	Logic LOW.	6
OSC_{IN}	OSC_{IN} is ignored and is at high-Z.	7
OSC_{SEL}	OSC_{SEL} is ignored and is at high-Z.	8
PFI	The power-fail comparator is disabled.	9
$\overline{\text{PFO}}$	The power-fail comparator is disabled. PFO is forced to logic LOW.	10
WDI	WDI is ignored and is at high-Z.	11
$\overline{CE_{OUT}}$	Logic HIGH. The open-circuit output voltage is equal to V_{OUT}.	12
$\overline{CE_{IN}}$	High-Z.	13
$\overline{\text{WDO}}$	Logic HIGH. The open-circuit output voltage is equal to V_{OUT}.	14
$\overline{\text{RESET}}$	Logic LOW.	15
RESET	High-Z.	16

Table 2. Input and Output Status in Battery-Backup Mode; to enter the Battery-Backup Mode, V_{CC} must be less than the reset threshold and less than V_{BATT}.

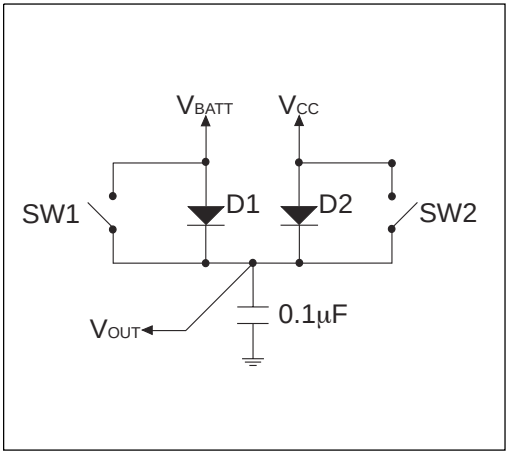


Figure 24. V_{CC} and V_{BATT} to V_{OUT} Switch

Input Supply Voltage

The Input Supply Voltage (VCC) should be a regulated +5V source. VCC connects to VOUT via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each. Refer to *Figure 24*. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to VCC, except the PMOS switch and parallel diode are much smaller. Refer to *Figure 24*. Accordingly, the on-resistances of the diode and the switch are each approximately 10Ω.

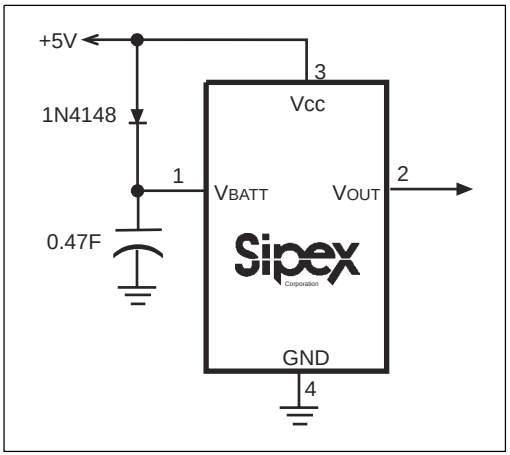


Figure 25. High Capacity Capacitor on V_{BATT}

Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage.

Output Supply Voltage

The Output Supply Voltage (VOUT) supplies all the current to the external system and internal circuitry. All open-circuit outputs will assume the VOUT voltage in their high states rather than the VCC voltage. At the maximum source current of 250mA, VOUT will typically be 150mV below VCC. VOUT should be decoupled with 0.1µF capacitor.

TYPICAL APPLICATIONS

The **SP691A/693A/800L/800M** devices are not short-circuit protected. Shorting VOUT to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. All open-circuit outputs swing between VOUT and GND rather than VCC and GND. If long leads connect to the chip inputs, ensure that these lines are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered from V_{CC}. Typical supply current from V_{CC} is 35µA, while only leakage currents flow from the battery.

2) Battery-backup mode where V_{CC} is typically within 0.7V below V_{BATT}. All circuitry is powered from V_{BATT} and the supply current from the battery is typically less than 5µA.

3) Battery-backup mode where V_{CC} is less than V_{BATT} by at least 0.7V. V_{BATT} supply current is less than 1µA max.

Using High Capacity Capacitor with the SP691A/693A/800L/800M Series

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typically +30mV centered at VBATT, allowing use of a capacitor and a simple charging circuit as a backup source. Refer to *Figure 25*.

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to VOUT and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC.

Leakage current through the capacitor charging diode and **SP691A/693A/800L/800M** internal power diode eventually discharges the capacitor to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the capacitor on VBATT discharges through VCC until VBATT reaches the reset threshold; the **SP691A/693A/800L/800M** devices then switch to battery-backup mode.

Using Separate Power Supplies for V_{BATT} and V_{CC}

If using separate power supplies for VCC and VBATT, VBATT must be less than 0.3V above VCC when VCC is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at VCC, current flows continuously from VBATT to VCC via the VBATT-to-VOUT diode and the VOUT-to-VCC switch until the circuit is broken. Refer to *Figure 24*.

Alternative Chip-Enable Gating

Using memory devices with CE and $\overline{CE}$ inputs allows the CE loop of the **SP691A/693A/800L/800M** series to be bypassed. To do this, connect $\overline{CE}_{IN}$ to ground, pull up $\overline{CE}_{OUT}$ to VOUT,

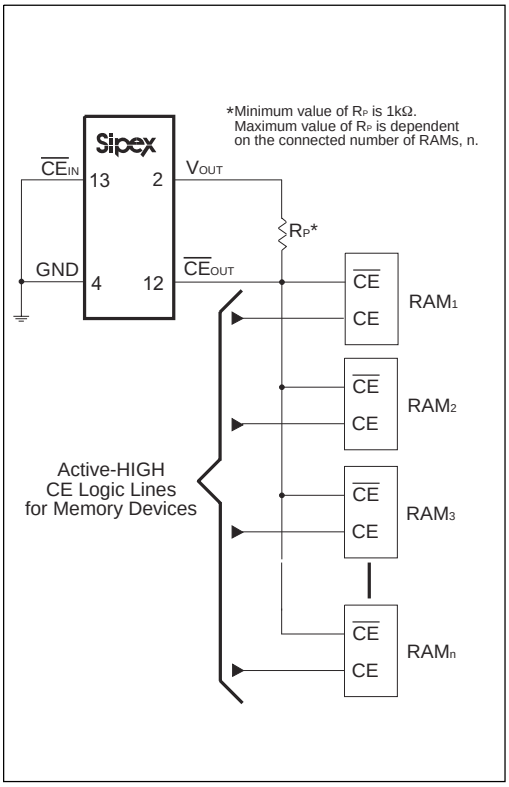


Figure 26. Alternate Chip Enable Gating

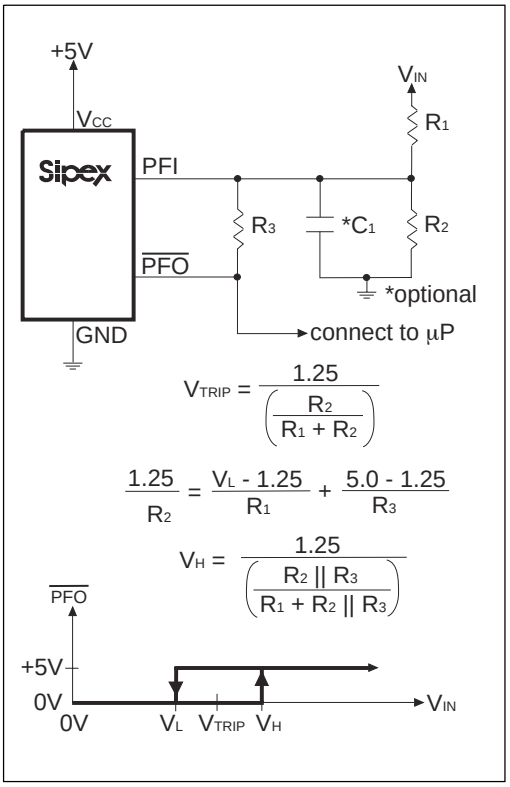


Figure 27. Adding Hysteresis to the Power-Fail Comparator

and connect $\overline{CE_{OUT}}$ to the $\overline{CE}$ input of each memory device as shown in *Figure 26*. The CE input of each part then connects directly to the chip-select logic, which does not have to gated by the **SP691A/693A/800L/800M** devices.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when V_{IN} is near the power-fail comparator trip point. *Figure 27* shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in *Figure 28*. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

Backup-Battery Replacement

The backup battery may be disconnected while V_{CC} is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

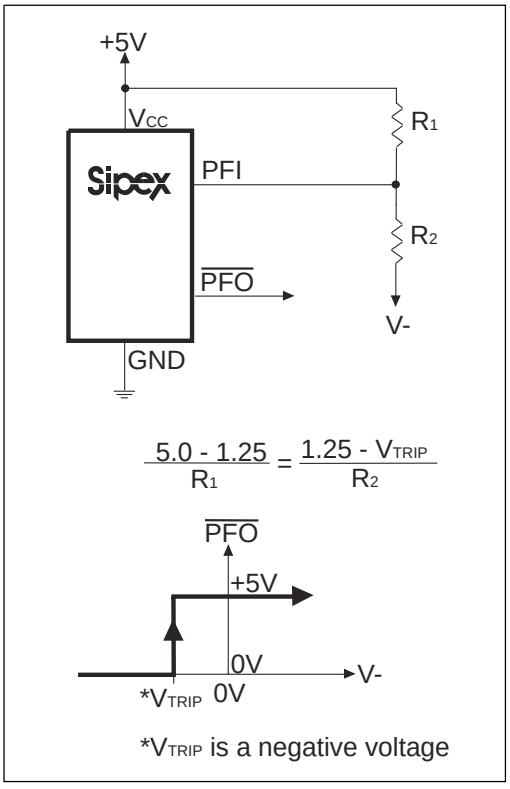


Figure 28. Monitoring a Negative Voltage

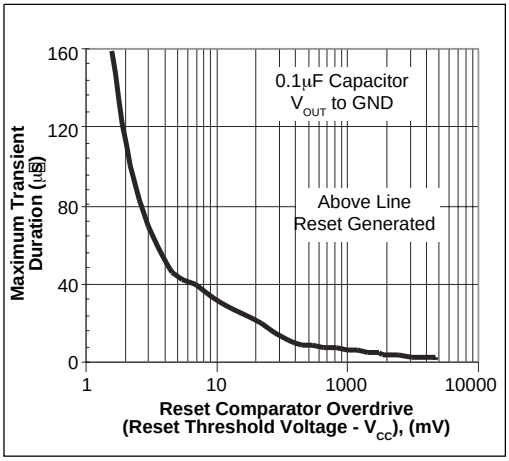


Figure 29. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

Negative-Going V_{CC} Transients

While asserting resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going VCC transients. It is usually undesirable to reset the µP when VCC experiences only small glitches.

Refer to *Figure 29* for a graph of the maximum transient duration vs. the reset-comparator overdrive for which reset pulses are not generated. The graph was produced using negative-going pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going VCC transient may typically have without causing a reset pulse to be issued.

As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued. A 100nF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

Connecting a Timing Capacitor to OSC_{IN}

When OSC_{SEL} is connected to ground, OSC_{IN} disconnects from its internal 10µA pull-up and is internally connected to a ±100nA current source. When a capacitor is connected from OSC_{IN} to ground (to select an alternative watchdog timeout period), the current source charges and discharges the timing capacitor to create the oscillator that controls the reset and watchdog timeout period. To prevent timing errors, minimize external current leakage sources at this pin, and locate the capacitor as close to OSC_{IN} as possible. The sum of any PC board leakage plus the OSC capacitor leakage must be small compared to ±100nA.

Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 30 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subrouting or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

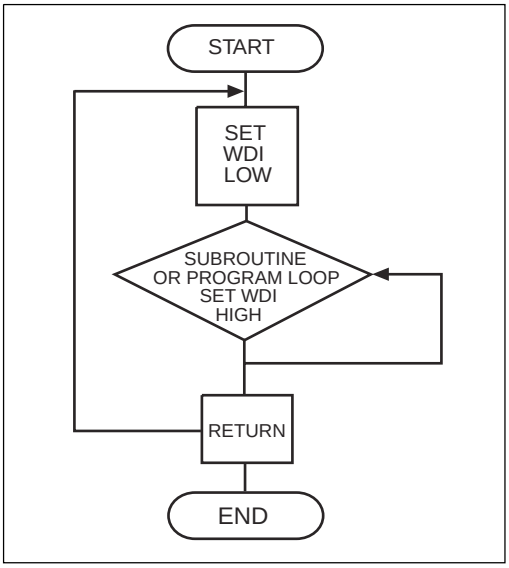
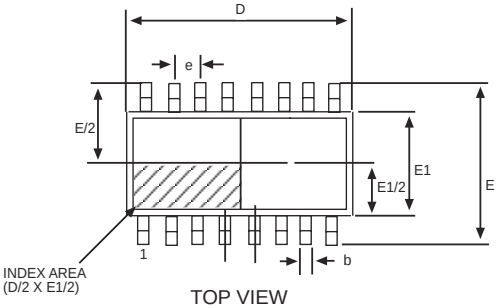


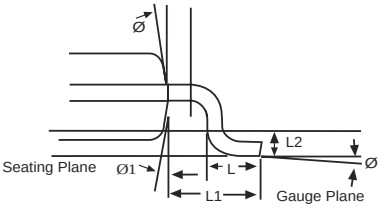
Figure 30. Watchdog Flow Diagram

Maximum V_{CC} Fall Time

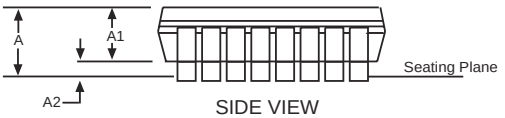
The VCC fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule of thumb for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial VCC fall rate is just the inverse of 1A/100µF = 0.01V/µs. The VCC fall rate decreases with time as VCC falls exponentially, which more than satisfies the maximum fall-time requirement.



TOP VIEW



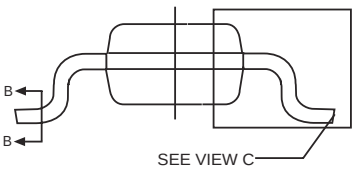
VIEW C

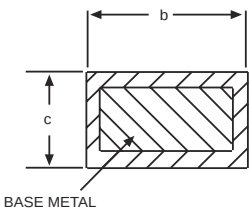


SIDE VIEW

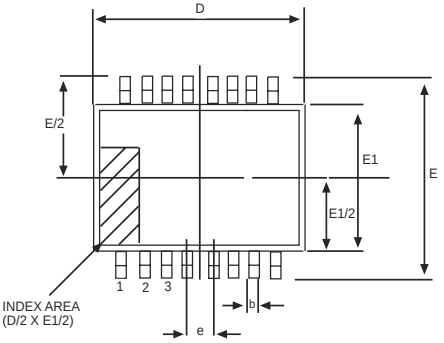
16 Pin NSOIC JEDEC MO-012 (AC) Variation			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.1	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D		9.90 BSC	
E		6.00 BSC	
E1		3.90 BSC	
e		1.27 BSC	
L	0.4	-	1.27
L1		1.04 REF	
L2		0.25 BSC	
ø	0º	-	8º
ø1	5º	-	15º

Note: Dimensions in (mm)

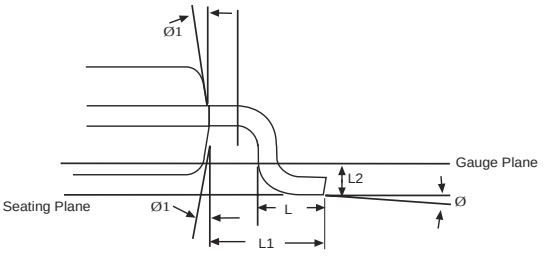




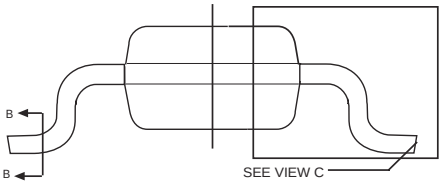
SECTION B-B
WITH PLATING



TOP VIEW

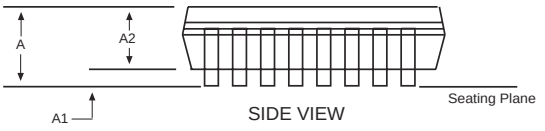


VIEW C

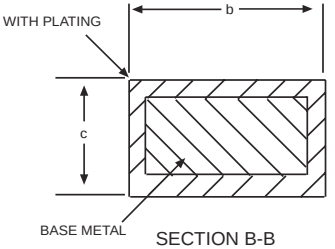


16 Pin SOIC JEDEC MS-013 (AA) Variation			
SYMBOL	MIN	NOM	MAX
A	2.35	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.55
b	0.31	-	0.51
c	0.2	-	0.33
D	10.30 BSC		
E	10.30 DSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.4	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
ø	0º	-	8º
ø1	5º	-	15º

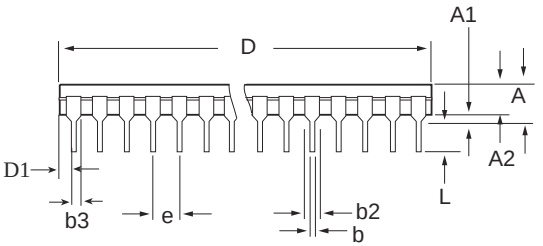
Note: Dimensions in (mm)

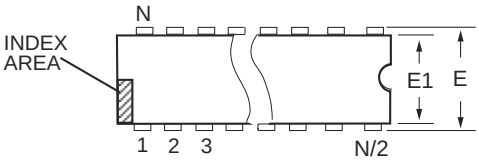


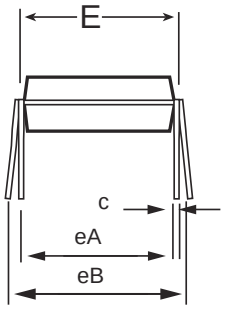
SIDE VIEW



SECTION B-B

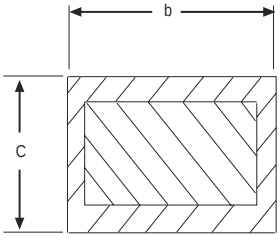






16 PIN PDIP JEDEC MS-001 (BB) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	0.21
A1	0.15	-	-
A2	0.115	0.13	0.195
b	0.014	0.018	0.022
b2	0.045	0.06	0.07
b3	0.3	0.039	0.045
c	0.008	0.01	0.014
D	0.735	0.75	0.755
D1	0.005	-	-
E	0.3	0.31	0.325
E1	0.24	0.25	0.28
e	.100 BSC		
eA	.300 BSC		
eB	-	-	0.43
L	0.115	0.13	0.15

Note: Dimensions in (mm)



ORDERING INFORMATION

Part Number	Temperature Range	Package Type
SP691ACP	0°C to +70°C	16-Pin PDIP
SP691ACN	0°C to +70°C	16-Pin NSOIC
SP691ACN/TR	0°C to +70°C	16-Pin NSOIC
SP691ACT	0°C to +70°C	16-Pin WSOIC
SP691ACT/TR	0°C to +70°C	16-Pin WSOIC
SP691AEP	-40°C to +85°C	16-Pin PDIP
SP691AEN	-40°C to +85°C	16-Pin NSOIC
SP691AEN/TR	-40°C to +85°C	16-Pin NSOIC
SP691AET	-40°C to +85°C	16-Pin WSOIC
SP691AET/TR	-40°C to +85°C	16-Pin WSOIC
SP693ACP	0°C to +70°C	16-Pin PDIP
SP693ACN	0°C to +70°C	16-Pin NSOIC
SP693ACN/TR	0°C to +70°C	16-Pin NSOIC
SP693ACT	0°C to +70°C	16-Pin WSOIC
SP693ACT/TR	0°C to +70°C	16-Pin WSOIC
SP693AEP	-40°C to +85°C	16-Pin PDIP
SP693AEN	-40°C to +85°C	16-Pin NSOIC
SP693AEN/TR	-40°C to +85°C	16-Pin NSOIC
SP693AET	-40°C to +85°C	16-Pin WSOIC
SP693AET/TR	-40°C to +85°C	16-Pin WSOIC

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP691AEN/TR = standard; SP691AEN-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for NSOIC and WSOIC.

CLICK HERE TO ORDER SAMPLES

Sipex Corporation

ANALOG EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Part Number	Temperature Range	Package Type
SP800LCP	0°C to +70°C	16-Pin PDIP
SP800LCN	0°C to +70°C	16-Pin NSOIC
SP800LCN/TR	0°C to +70°C	16-Pin NSOIC
SP800LCT	0°C to +70°C	16-Pin WSOIC
SP800LCT/TR	0°C to +70°C	16-Pin WSOIC
SP800LEP	-40°C to +85°C	16-Pin PDIP
SP800LEN	-40°C to +85°C	16-Pin NSOIC
SP800LEN/TR	-40°C to +85°C	16-Pin NSOIC
SP800LET	-40°C to +85°C	16-Pin WSOIC
SP800LET/TR	-40°C to +85°C	16-Pin WSOIC
SP800MCP	0°C to +70°C	16-Pin PDIP
SP800MCN	0°C to +70°C	16-Pin NSOIC
SP800MCN/TR	0°C to +70°C	16-Pin NSOIC
SP800MCT	0°C to +70°C	16-Pin WSOIC
SP800MCT/TR	0°C to +70°C	16-Pin WSOIC
SP800MEP	-40°C to +85°C	16-Pin PDIP
SP800MEN	-40°C to +85°C	16-Pin NSOIC
SP800MEN/TR	-40°C to +85°C	16-Pin NSOIC
SP800MET	-40°C to +85°C	16-Pin WSOIC
SP800MET/TR	-40°C to +85°C	16-Pin WSOIC

Available in lead free packaging. To order add “-L” suffix to part number.

Example: SP800MEN/TR = standard; SP800MEN-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for NSOIC and WSOIC.

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