



**THE DATASHEET OF  
LMV393QDRQ1**

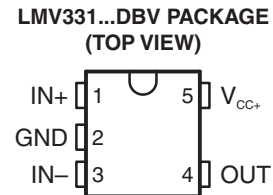
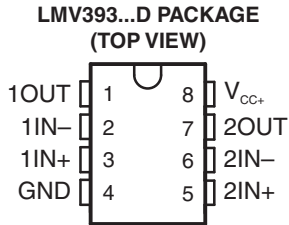


## GENERAL-PURPOSE LOW-VOLTAGE COMPARATORS

 Check for Samples: [LMV331-Q1 SINGLE](#), [LMV393-Q1 DUAL](#)

### FEATURES

- Qualified for Automotive Applications
- 2.7-V and 5-V Performance
- Low Supply Current
  - LMV331 . . . 60  $\mu$ A Typ
  - LMV393 . . . 100  $\mu$ A Typ
- Input Common-Mode Voltage Range Includes Ground
- Low Output Saturation Voltage . . . 200 mV Typ
- Open-Collector Output for Maximum Flexibility



### DESCRIPTION/ORDERING INFORMATION

The LMV393-Q1 device is a low-voltage (2.7 V to 5.5 V) version of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331-Q1 is the single-comparator version.

The LMV331-Q1 and LMV393-Q1 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

### ORDERING INFORMATION<sup>(1)</sup>

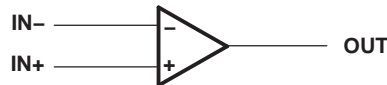
$T_A$	PACKAGE <sup>(2)</sup>			ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 125°C	Single	SOT23-5 – DBV	Reel of 3000	LMV331QDBVRQ1	LADQ
	Dual	SOIC – D	Reel of 2500	LMV393QDRQ1	V393Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

Figure 1. SYMBOL (EACH COMPARATOR)



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## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>		5.5	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±5.5	V
V <sub>I</sub>	Input voltage range (either input)	0	5.5	V
θ <sub>JA</sub>	Package thermal impedance <sup>(4) (5)</sup>	D (8-pin) package		°C/W
		D (14-pin) package		
		DBV package		
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V<sub>CC+</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Selecting the maximum of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage (single-supply operation)	2.7	5.5	V
V <sub>OUT</sub>	Output voltage		V <sub>CC+</sub> + 0.3	V
T <sub>A</sub>	Operating free-air temperature	–40	125	°C

**Electrical Characteristics**

at specified free-air temperature,  $V_{CC+} = 2.7\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		1.7	7	mV
$\alpha V_{IO}$	Average temperature coefficient of input offset voltage		-40°C to 125°C		5		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	Input bias current		25°C		10	250	nA
			-40°C to 125°C			400	
$I_{IO}$	Input offset current		25°C		5	50	nA
			-40°C to 125°C			150	
$I_O$	Output current (sinking)	$V_O \leq 1.5\text{ V}$	25°C	5	23		mA
	Output leakage current		25°C		0.003		$\mu\text{A}$
			-40°C to 125°C			1	
$V_{ICR}$	Common-mode input voltage range		25°C		-0.1 to 2		V
$V_{SAT}$	Saturation voltage	$I_O \leq 1\text{ mA}$	25°C		200		mV
$I_{CC}$	Supply current	LMV331	25°C		40	100	$\mu\text{A}$
		LMV393 (both comparators)			70	140	
		LMV339 (all four comparators)			140	200	

**Switching Characteristics**

$T_A = 25^\circ\text{C}$ ,  $V_{CC+} = 2.7\text{ V}$ ,  $R_L = 5.1\text{ k}\Omega$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$t_{PHL}$	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV	1000	ns
		Input overdrive = 100 mV	350	
$t_{PLH}$	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV	500	ns
		Input overdrive = 100 mV	400	

## Electrical Characteristics

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		1.7	7	mV
			–40°C to 125°C			9	
$\alpha V_{IO}$	Average temperature coefficient of input offset voltage		25°C		5		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	Input bias current		25°C		25	250	nA
			–40°C to 125°C			400	
$I_{IO}$	Input offset current		25°C		2	50	nA
			–40°C to 125°C			150	
$I_O$	Output current (sinking)	$V_O \leq 1.5\text{ V}$	25°C	10	84		mA
	Output leakage current		25°C		0.003		$\mu\text{A}$
			–40°C to 125°C			1	
$V_{ICR}$	Common-mode input voltage range		25°C		–0.1 to 4.2		V
$A_{VD}$	Large-signal differential voltage gain		25°C	20	50		V/mV
$V_{SAT}$	Saturation voltage	$I_O \leq 4\text{ mA}$	25°C		200	400	mV
			–40°C to 125°C			700	
$I_{CC}$	Supply current	LMV331	25°C		60	120	$\mu\text{A}$
			–40°C to 125°C			150	
		LMV393 (both comparators)	25°C		100	200	
			–40°C to 125°C			250	
		LMV339 (all four comparators)	25°C		170	300	
			–40°C to 125°C			350	

## Switching Characteristics

 $T_A = 25^\circ\text{C}$ ,  $V_{CC+} = 5\text{ V}$ ,  $R_L = 5.1\text{ k}\Omega$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$t_{PHL}$	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV	600	ns
		Input overdrive = 100 mV	200	
$t_{PLH}$	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV	450	ns
		Input overdrive = 100 mV	300	

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV331QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LADQ	<a href="#">Samples</a>
LMV393QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V393Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LMV331-Q1, LMV393-Q1 :**

- Catalog: [LMV331](#), [LMV393](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

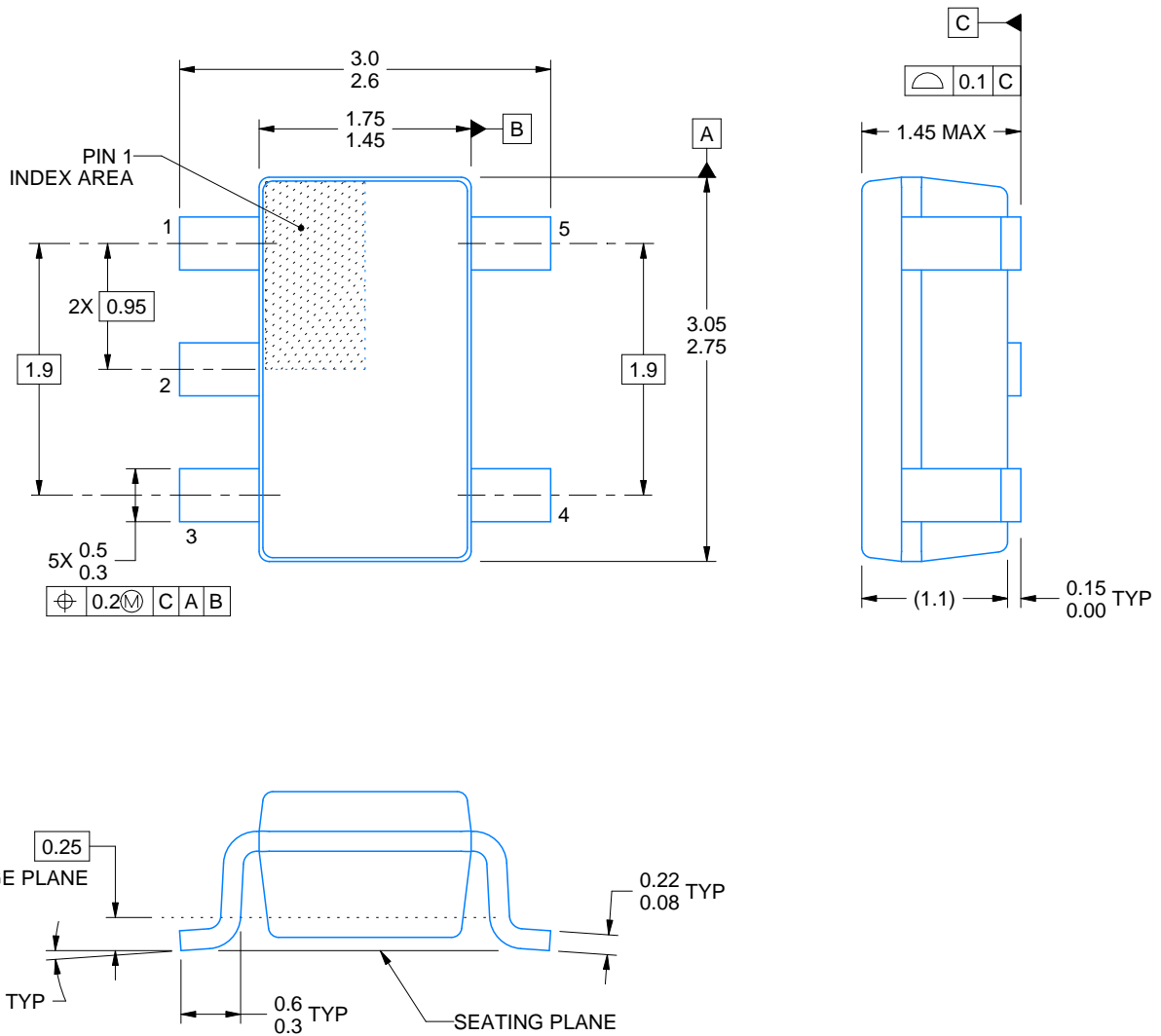
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

## NOTES:

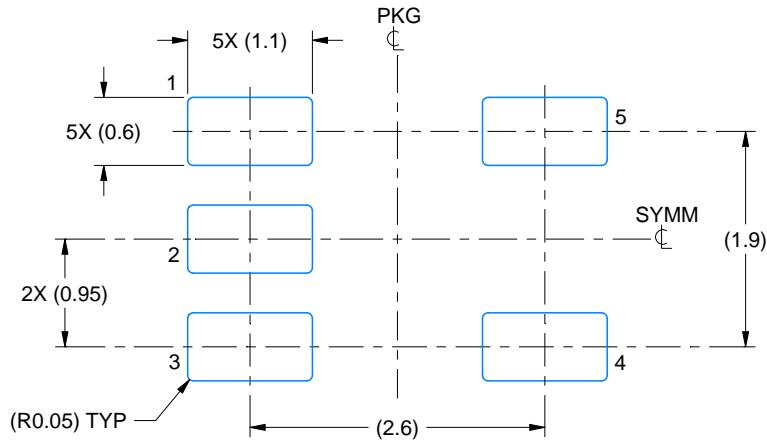
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

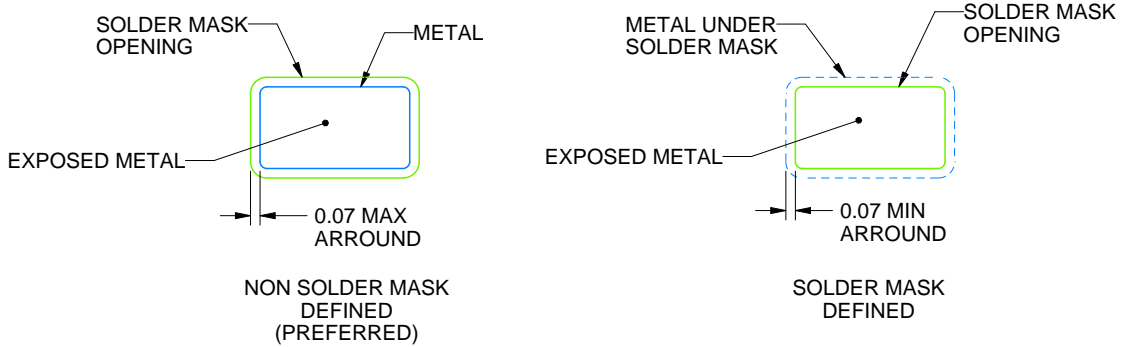
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

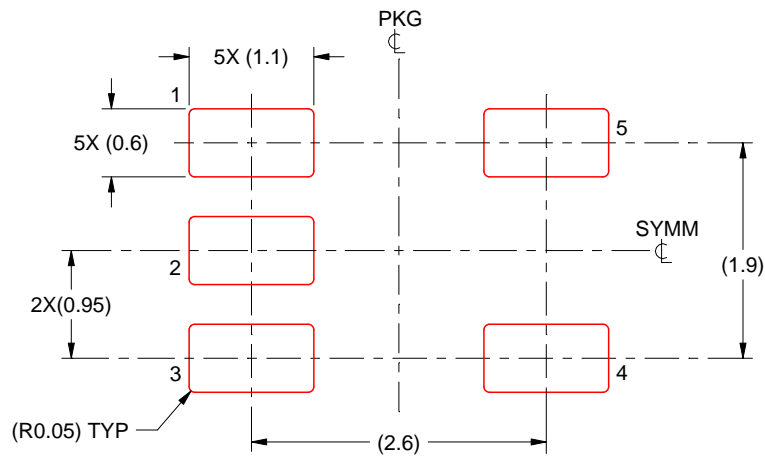
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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