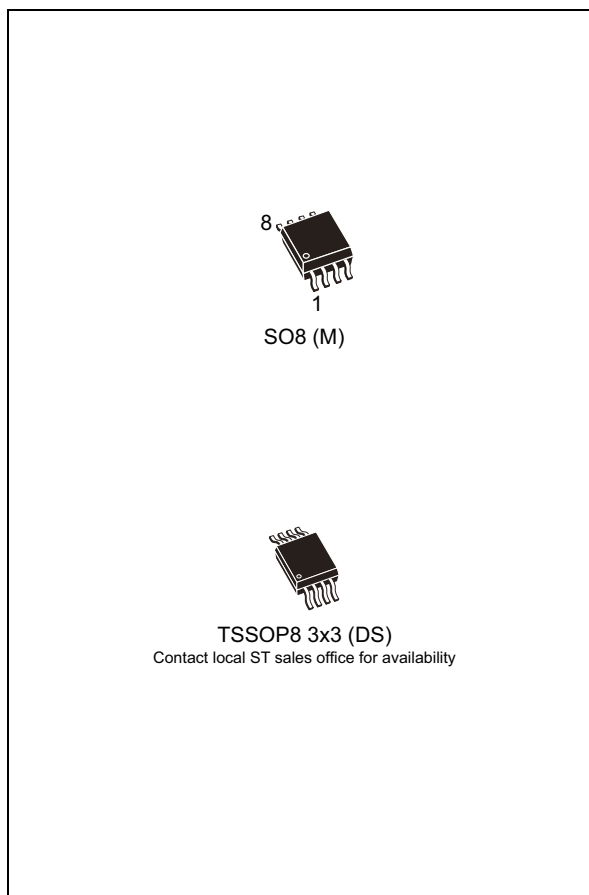




THE DATASHEET OF STM706RM6E





Features

- Precision V_{CC} monitor
 - T: $3.00\text{ V} \leq V_{RST} \leq 3.15\text{ V}$
 - S: $2.88\text{ V} \leq V_{RST} \leq 3.00\text{ V}$
 - R: STM706P: $2.59\text{ V} \leq V_{RST} \leq 2.70\text{ V}$
- RST and $\overline{\text{RST}}$ outputs
- 200 ms (typ.) t_{rec}
- Watchdog timer - 1.6 s (typ.)
- Manual reset input ($\overline{\text{MR}}$)
- Power-fail comparator ($\text{PFI}/\overline{\text{PFO}}$)
- Low supply current - 40 μA (typ.)
- Guaranteed $\overline{\text{RST}}$ (RST) assertion down to $V_{CC} = 1.0\text{ V}$
- Operating temperature: $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (industrial grade)
- RoHS compliance
 - Lead-free components are compliant with the RoHS directive

Applications

- Computers
- Controllers
- Intelligent instruments

Table 1. Device summary

| | Watchdog input | Watchdog output ⁽¹⁾ | Active low $\overline{\text{RST}}$ ⁽¹⁾ | Active high RST ⁽¹⁾ | Manual reset input | Power-fail comparator |
|------------------------|----------------|--------------------------------|---|---|--------------------|-----------------------|
| STM706T/S/R | ✓ | ✓ | ✓ | | ✓ | ✓ |
| STM706P ⁽²⁾ | ✓ | ✓ | | ✓ | ✓ | ✓ |
| STM708T/S/R | | | ✓ | ✓ | ✓ | ✓ |

1. Push-pull output.

2. The STM706P device is identical to the STM706R device, except its reset output is active high.

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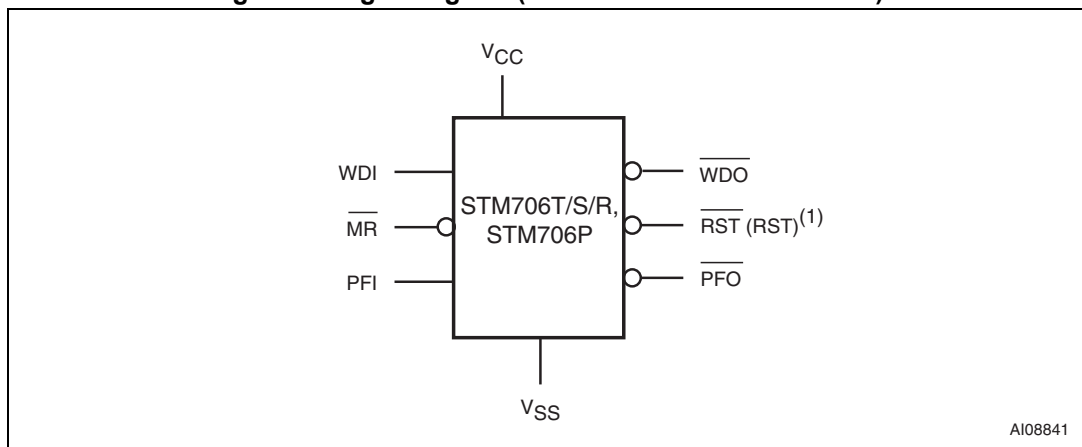
1 Description

The STM70x supervisors are self-contained devices which provide microprocessor supervisory functions. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the reset output (\overline{RST}) is forced low (or high in the case of RST).

These devices also offer a watchdog timer (except for STM708T/S/R) as well as a power-fail comparator to provide the system with an early warning of impending power failure.

The STM706P device is identical to the STM706R device, except its reset output is active high. These devices are available in a standard 8-pin SOIC package or a space-saving 8-pin TSSOP package.

Figure 1. Logic diagram (STM706T/S/R and STM706P)



1. For STM706P only.

Figure 2. Logic diagram (STM708T/S/R)

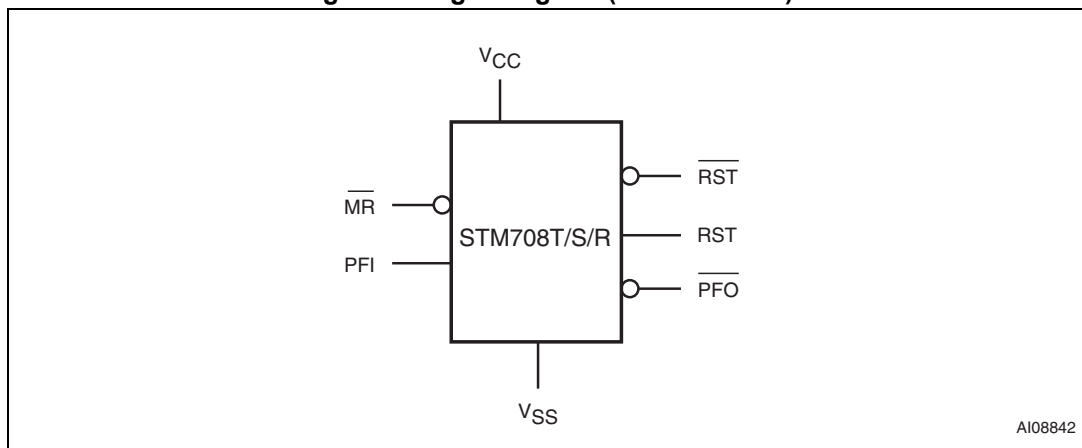
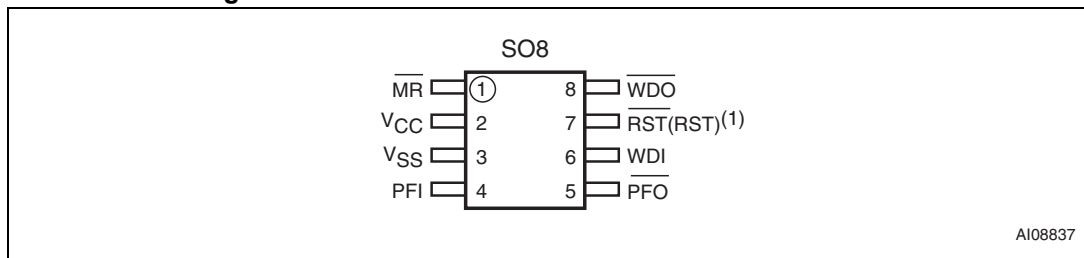


Table 2. Signal names

| Symbol | Name |
|--------------------|--------------------------|
| \overline{MR} | Push-button reset input |
| WDI | Watchdog input |
| \overline{WDO} | Watchdog output |
| \overline{RST} | Active low reset output |
| RST ⁽¹⁾ | Active high reset output |
| V _{CC} | Supply voltage |
| PFI | Power-fail input |
| \overline{PFO} | Power-fail output |
| V _{SS} | Ground |
| NC | No connect |

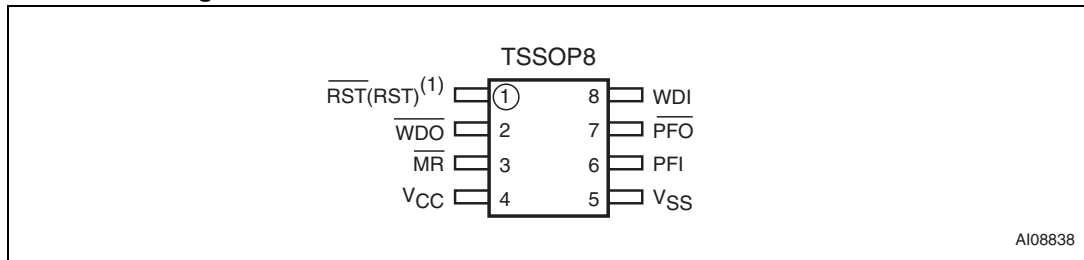
1. For STM706P and STM708T/S/R only.

Figure 3. STM706T/S/R and STM706P SO8 connections



1. For STM706P reset output is active high.

Figure 4. STM706T/S/R and STM706P TSSOP8 connections



1. For STM706P reset output is active high.

Figure 5. STM708T/S/R SO8 connections

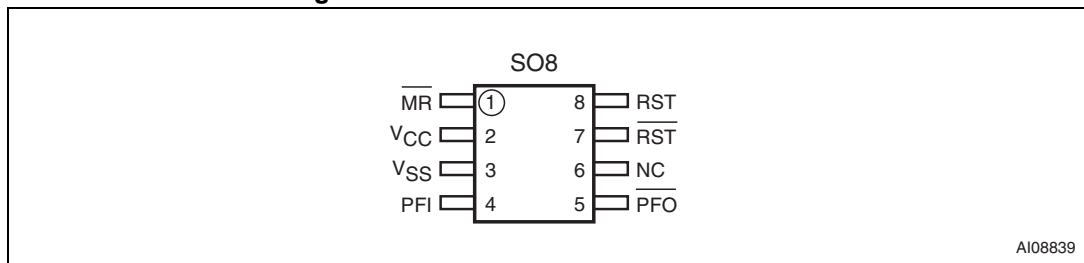
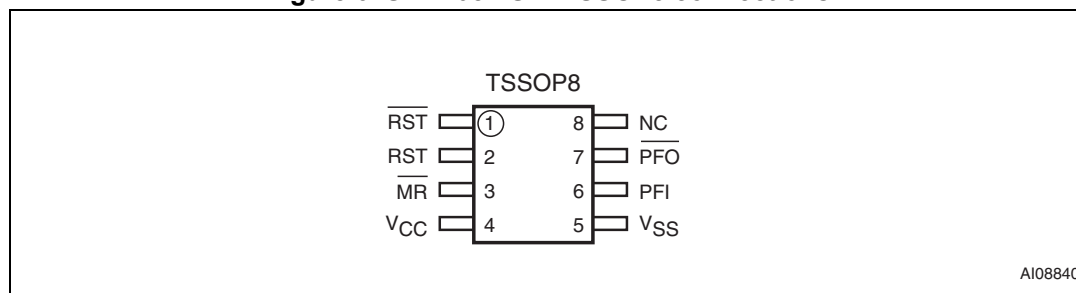


Figure 6. STM708T/S/R TSSOP8 connections



2 Pin descriptions

2.1 $\overline{\text{MR}}$

A logic low on $\overline{\text{MR}}$ asserts the reset output. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for t_{rec} after $\overline{\text{MR}}$ returns high. This active low input has an internal pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.

2.2 WDI

If WDI remains high or low for 1.6 s, the internal watchdog timer runs out and reset (or $\overline{\text{WDO}}$) is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge.

The watchdog function can be disabled by allowing the WDI pin to float. This feature is available for the “D” version only (see [Section 8: Part numbering](#)).

2.3 $\overline{\text{WDO}}$

$\overline{\text{WDO}}$ goes low when a transition does not occur on WDI within 1.6 s, and remains low until a transition occurs on WDI (indicating the watchdog interrupt has been serviced) or $\overline{\text{MR}}$ input is asserted (goes low). $\overline{\text{WDO}}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output, $\overline{\text{WDO}}$ goes high as soon as V_{CC} exceeds the reset threshold. Output type is push-pull.

Note: For those devices with a $\overline{\text{WDO}}$ output, a watchdog timeout will not trigger reset unless $\overline{\text{WDO}}$ is connected to $\overline{\text{MR}}$.

2.4 $\overline{\text{RST}}$

Pulses low for t_{rec} when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{\text{MR}}$ goes from low to high.

2.5 RST

Pulses high for t_{rec} when triggered, and stays high whenever V_{CC} is above the reset threshold or when $\overline{\text{MR}}$ is a logic high. It remains high for t_{rec} after either V_{CC} falls below the reset threshold, the watchdog triggers a reset, or $\overline{\text{MR}}$ goes from high to low.

2.6 PFI

When PFI is less than V_{PFI} , $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high. Connect to ground if unused.

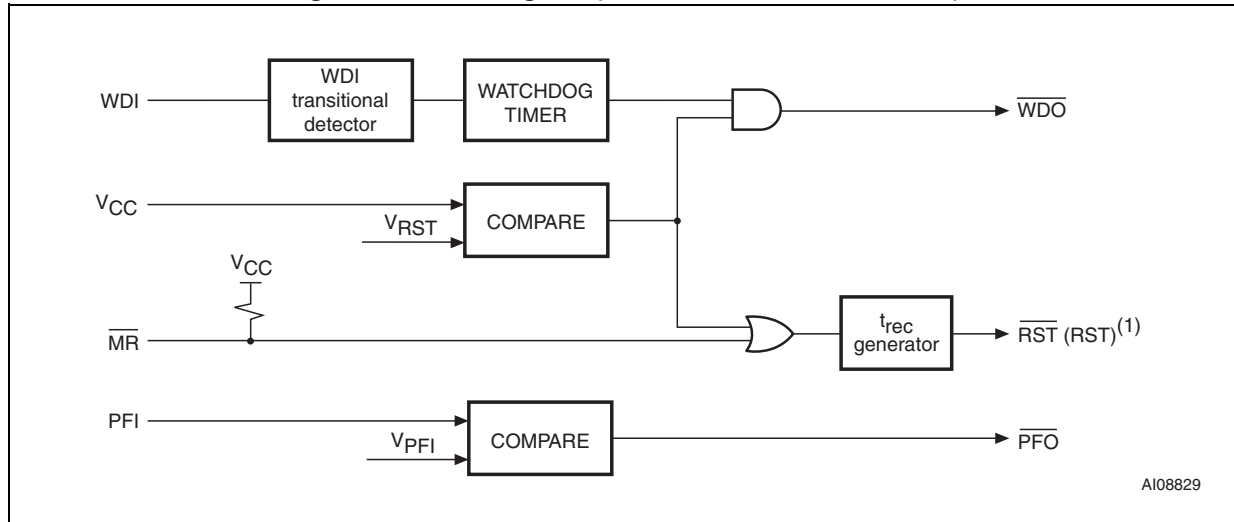
2.7 $\overline{\text{PFO}}$

When PFI is less than V_{PFI} , $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high. Output type is push-pull. $\overline{\text{PFO}}$ pin is not supposed to be forced low by a processor. MR input is gated off during the period $\overline{\text{PFO}}$ is forced low. Leave open if unused.

Table 3. Pin description

| Pin | | | | | | Name | Function |
|---------|--------|-------------|--------|-------------|--------|-------------------------|-------------------------------|
| STM706P | | STM706T/S/R | | STM708T/S/R | | | |
| SO8 | TSSOP8 | SO8 | TSSOP8 | SO8 | TSSOP8 | | |
| 1 | 3 | 1 | 3 | 1 | 3 | $\overline{\text{MR}}$ | Push-button reset input |
| 6 | 8 | 6 | 8 | — | — | WDI | Watchdog input |
| 8 | 2 | 8 | 2 | — | — | $\overline{\text{WDO}}$ | Watchdog output (push-pull) |
| — | — | 7 | 1 | 7 | 1 | $\overline{\text{RST}}$ | Active low reset output |
| 7 | 1 | — | — | 8 | 2 | RST | Active high reset output |
| 2 | 4 | 2 | 4 | 2 | 4 | V_{CC} | Supply voltage |
| 4 | 6 | 4 | 6 | 4 | 6 | PFI | Power-fail input |
| 5 | 7 | 5 | 7 | 5 | 7 | $\overline{\text{PFO}}$ | Power-fail output (push-pull) |
| 3 | 5 | 3 | 5 | 3 | 5 | V_{SS} | Ground |
| — | — | — | — | 6 | 8 | NC | No connect |

Figure 7. Block diagram (STM706T/S/R and STM706P)



1. For STM706P only

Figure 8. Block diagram (STM708T/S/R)

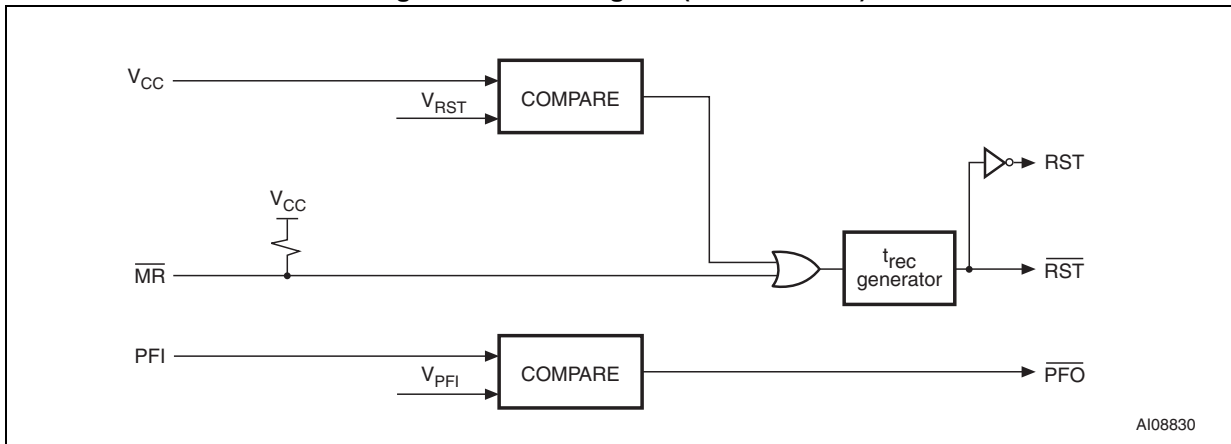
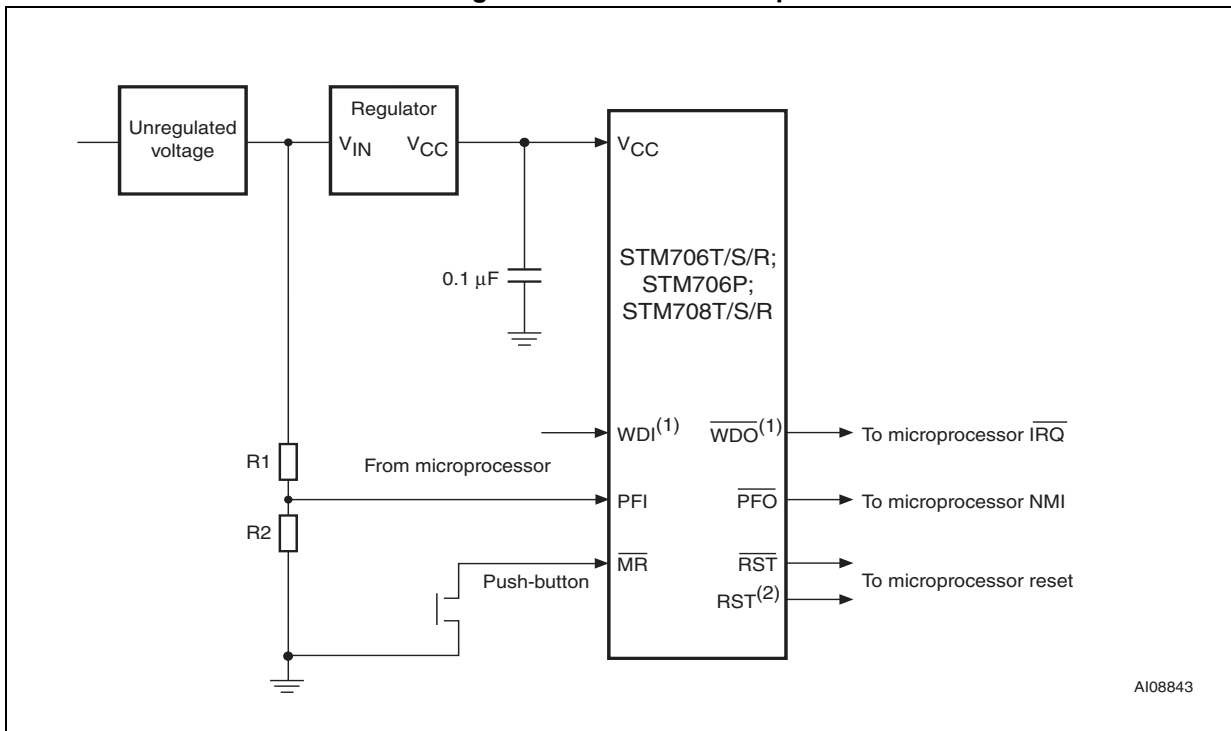


Figure 9. Hardware hookup



1. For STM706T/S/R and STM706P devices
2. For STM706P and STM708T/S/R devices

3 Operation

3.1 Reset output

The STM70x supervisor asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), a watchdog timeout occurs (if WDO is connected to MR), or when the push-button reset input (\overline{MR}) is taken low. \overline{RST} is guaranteed to be a logic low (logic high for STM706P and STM708T/S/R) for $V_{CC} < V_{RST}$ down to $V_{CC} = 1$ V for $T_A = 0$ °C to 85 °C.

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps \overline{RST} low for the reset timeout period, t_{rec} . After this interval \overline{RST} returns high.

If V_{CC} drops below the reset threshold, \overline{RST} goes low. Each time \overline{RST} is asserted, it stays low for at least the reset timeout period (t_{rec}). Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

3.2 Push-button reset input

A logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for t_{rec} (see [Figure 27](#)) after it returns high. The \overline{MR} input has an internal 40 k Ω pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain / collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual reset function; external debounce circuitry is not required. If \overline{MR} is driven from long cables or the device is used in a noisy environment, connect a 0.1 μ F capacitor from \overline{MR} to GND to provide additional noise immunity. \overline{MR} may float, or be tied to V_{CC} when not used.

3.3 Watchdog input (STM706T/S/R and STM706P)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the watchdog input (WDI) within t_{WDP} (1.6 s), the watchdog output pin (WDO) is asserted. The internal 1.6s timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high-to-low or low-to-high), which can detect pulses as short as 50 ns.

See [Figure 28](#) for STM706T/S/R and STM706P.

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting.

Note: The watchdog function may be disabled by floating WDI or tri-stating the driver connected to WDI. When tri-stated or disconnected, the maximum allowable leakage current is 10 μ A and the maximum allowable load capacitance is 200 pF.

3.4 Watchdog output (STM706T/S/R and STM706P)

When V_{CC} drops below the reset threshold, \overline{WDO} will go low even if the watchdog timer has not yet timed out. However, unlike the reset output, \overline{WDO} goes high as soon as V_{CC} exceeds the reset threshold. \overline{WDO} may be used to generate a reset pulse by connecting it to the MR input.

3.5 Power-fail input/output

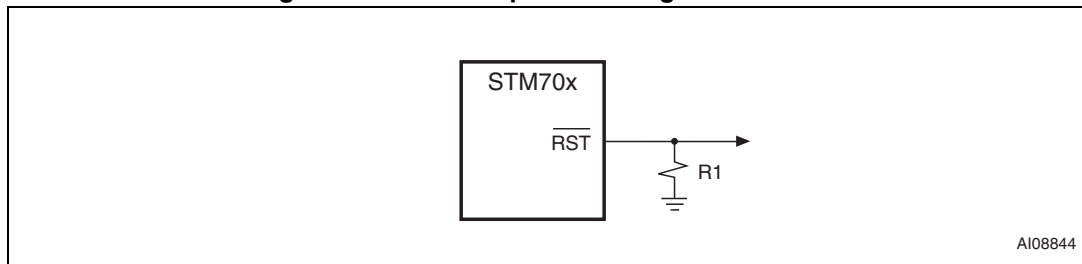
The power-fail input (PFI) is compared to an internal reference voltage (independent from the V_{RST} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the power-fail output (PFO) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see [Figure 9](#)) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the STM70x or the micro-processor drops below the minimum operating voltage.

If the comparator is unused, PFI should be connected to V_{SS} and \overline{PFO} left unconnected. \overline{PFO} may be connected to MR on the STM70x so that a low voltage on PFI will generate a reset output.

3.6 Ensuring a valid reset output down to $V_{CC} = 0$ V

When V_{CC} falls below 1 V, the state of the \overline{RST} output can no longer be guaranteed, and becomes essentially an open circuit. If a high value pulldown resistor is added to the \overline{RST} pin, the output will be held low during this condition. A resistor value of approximately 100 k Ω will be large enough to not load the output under operating conditions, but still sufficient to pull \overline{RST} to ground during this low voltage condition (see [Figure 10](#)).

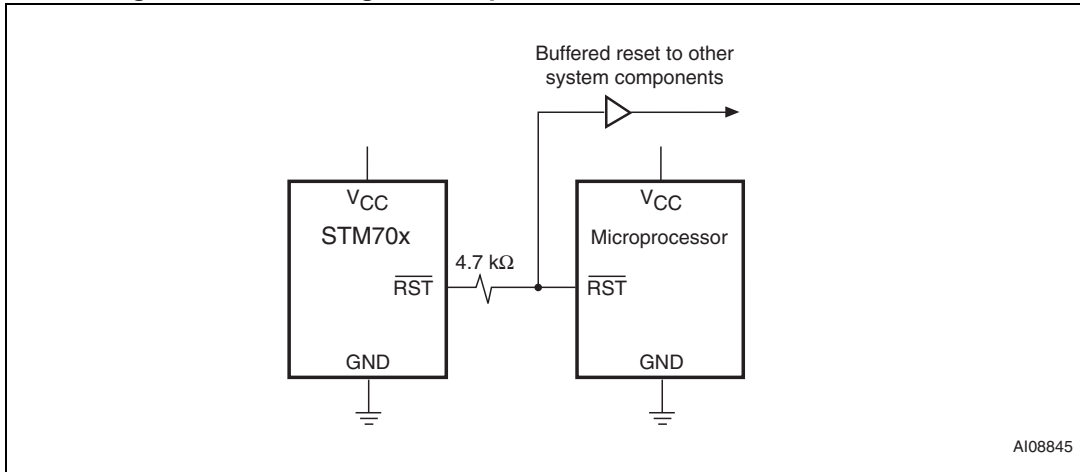
Figure 10. Reset output valid to ground circuit



3.7 Interfacing to microprocessors with bi-directional reset pins

Microprocessors with bi-directional reset pins can contend with the STM70x reset output. For example, if the reset output is driven high and the micro wants to pull it low, signal contention will result. To prevent this from occurring, connect a 4.7kΩ resistor between the reset output and the micro's reset I/O as in [Figure 11](#).

Figure 11. Interfacing to microprocessors with bi-directional reset I/O



4 Typical operating characteristics

Typical values are at $T_A = 25\text{ }^\circ\text{C}$.

Figure 12. Supply current vs. temperature (no load)

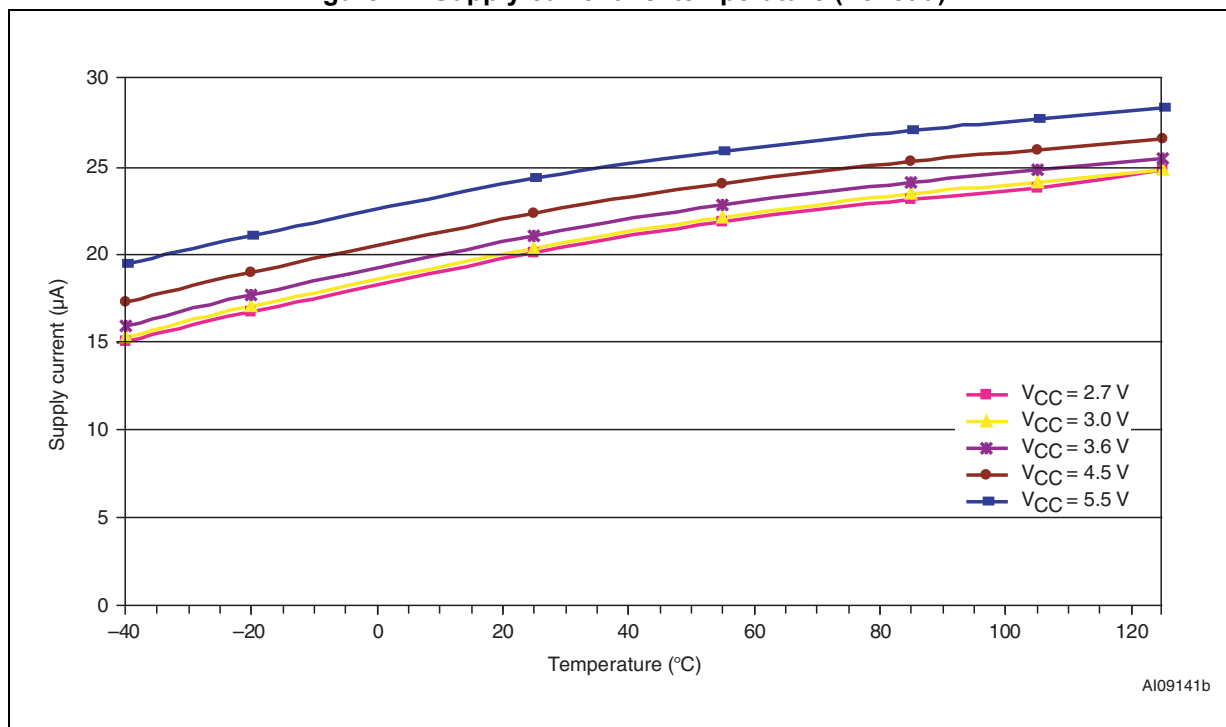


Figure 13. V_{PFI} threshold vs. temperature

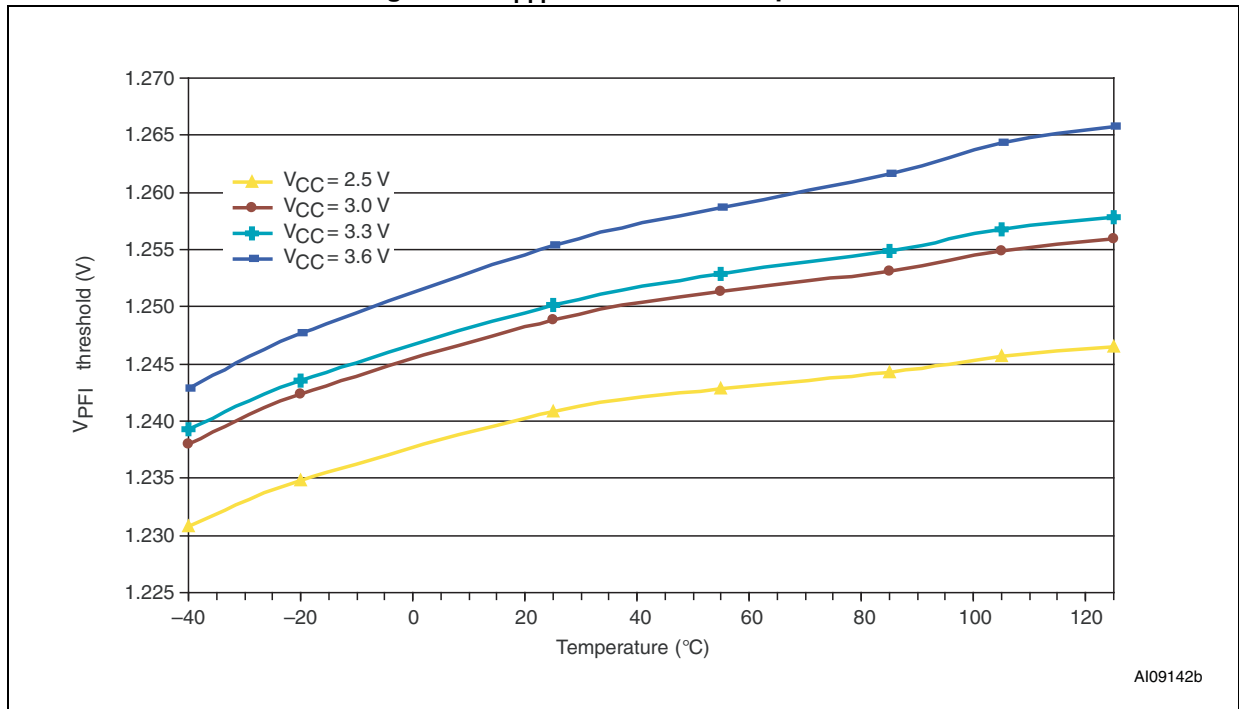


Figure 14. Reset comparator propagation delay vs. temperature

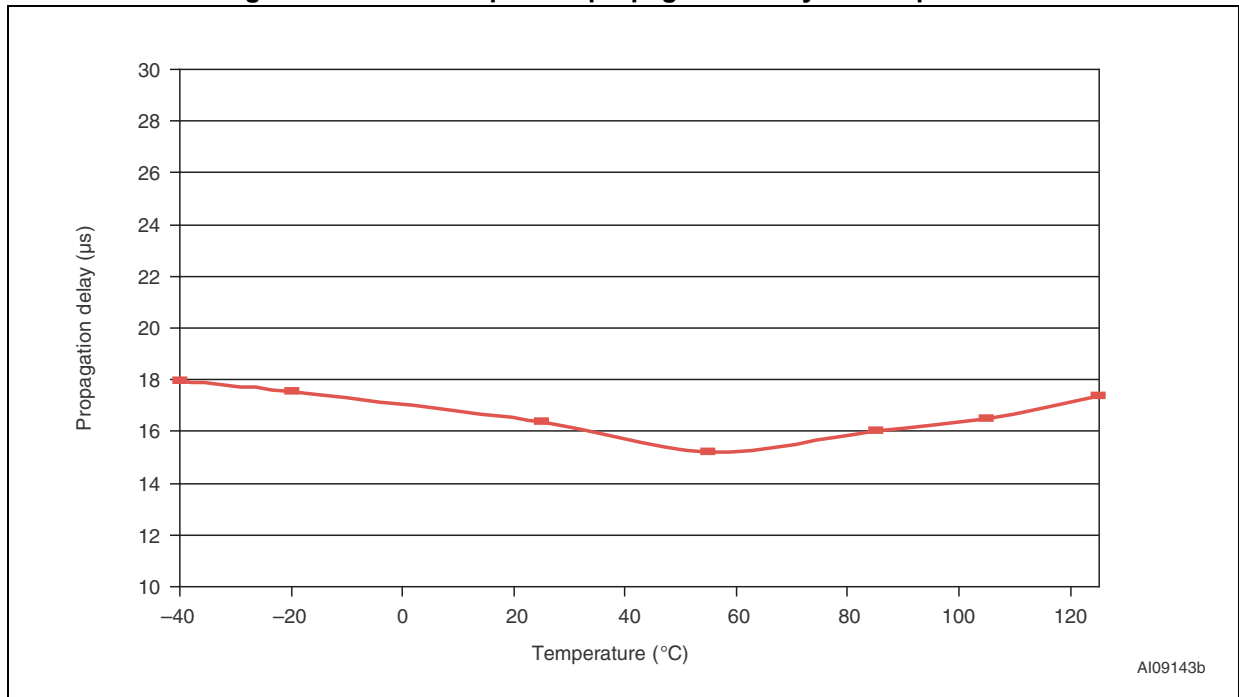


Figure 15. Power-up t_{rec} vs. temperature

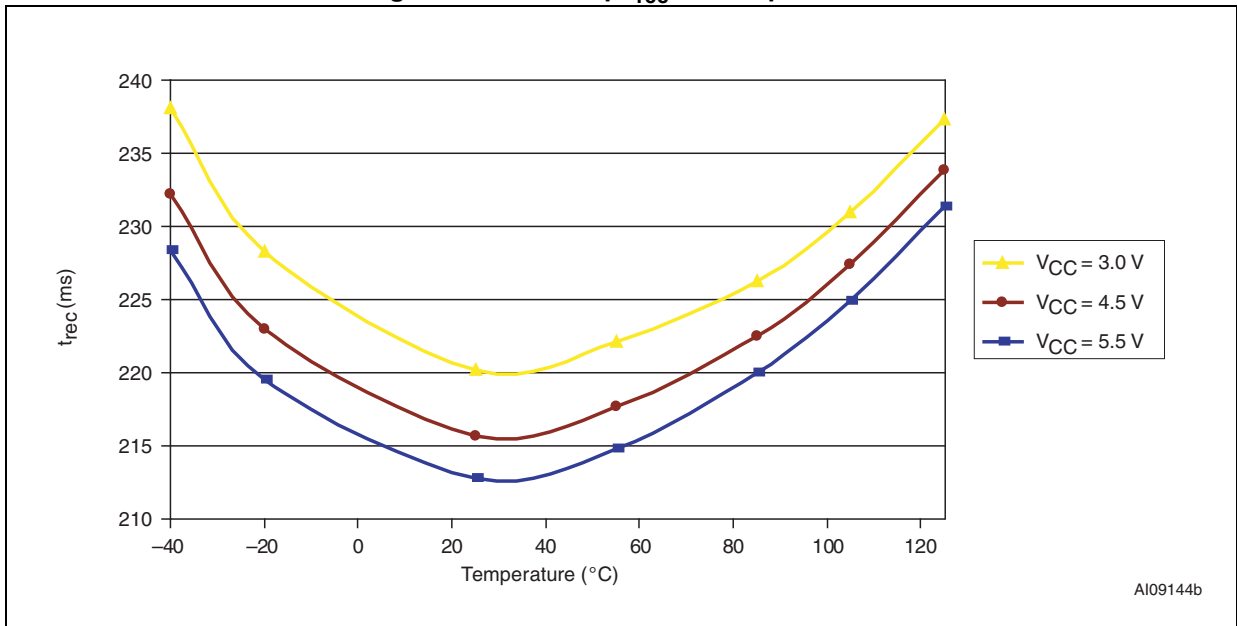


Figure 16. Normalized reset threshold vs. temperature

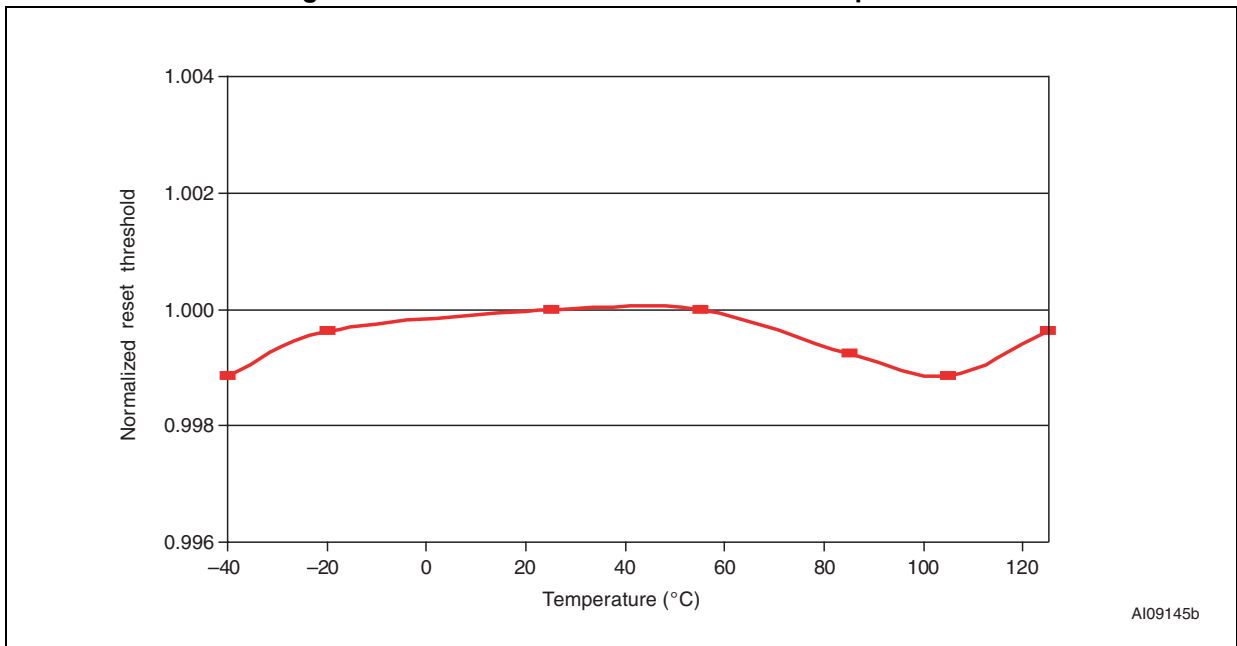


Figure 17. Watchdog timeout period vs. temperature

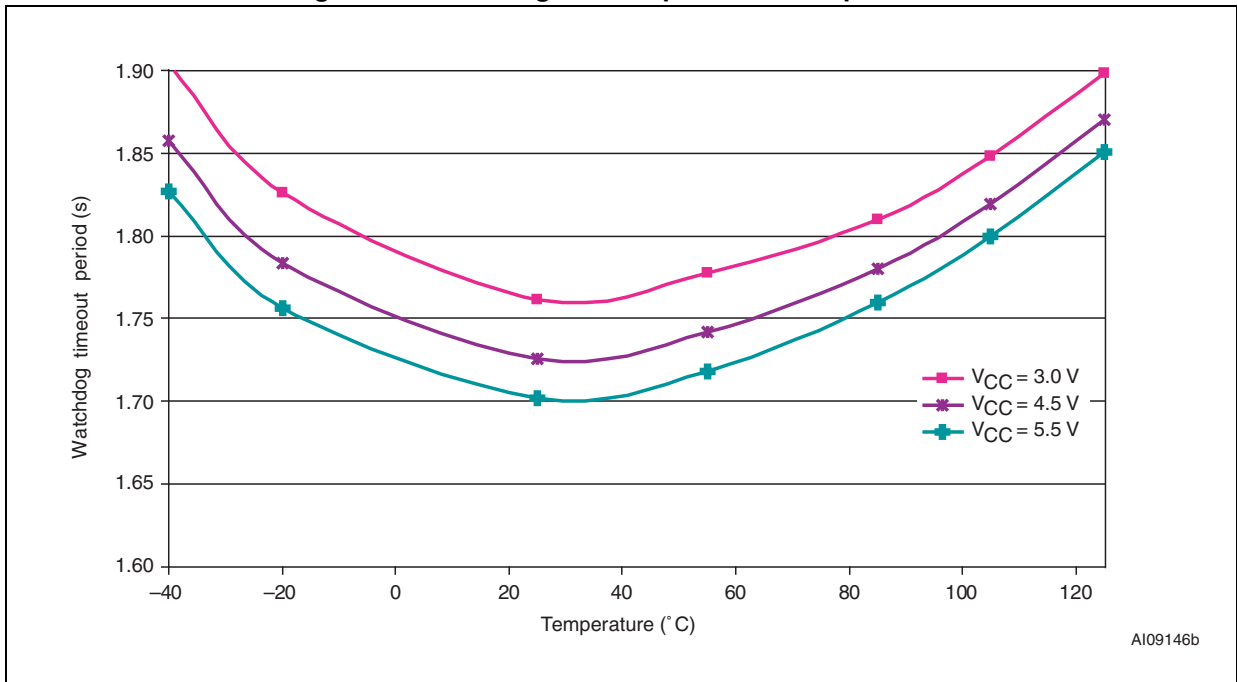


Figure 18. PFI to PFO propagation delay vs. temperature

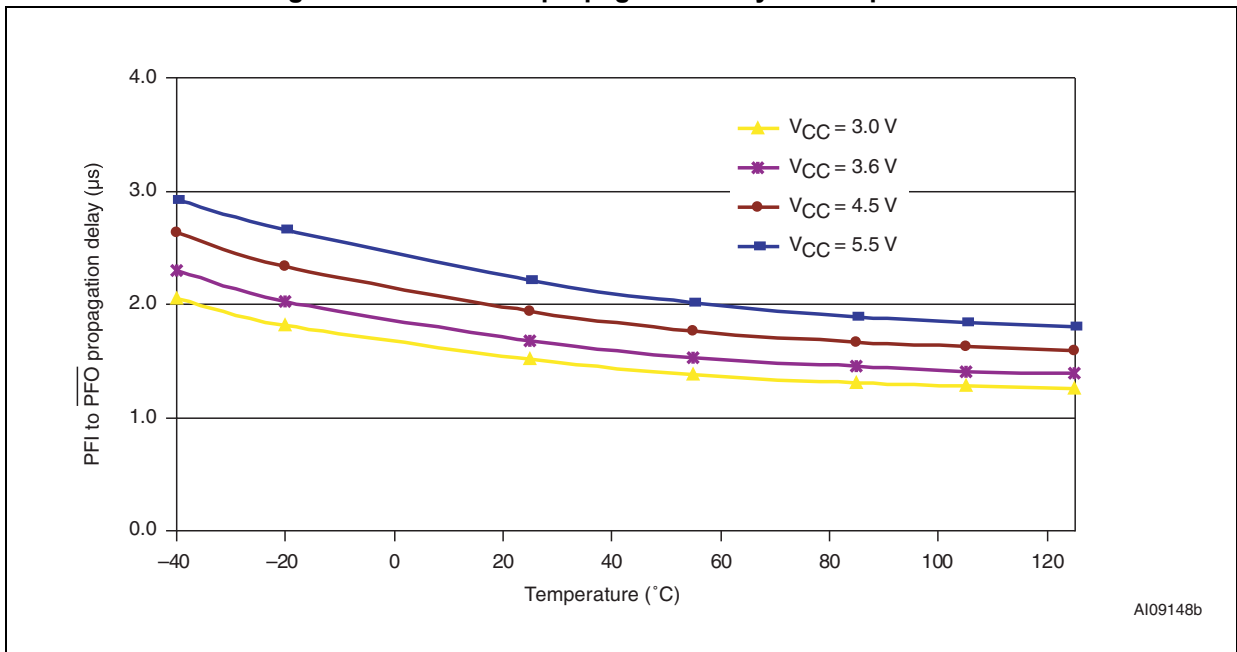


Figure 19. Output voltage vs. load current ($V_{CC} = 5\text{ V}$; $T_A = 25\text{ }^\circ\text{C}$)

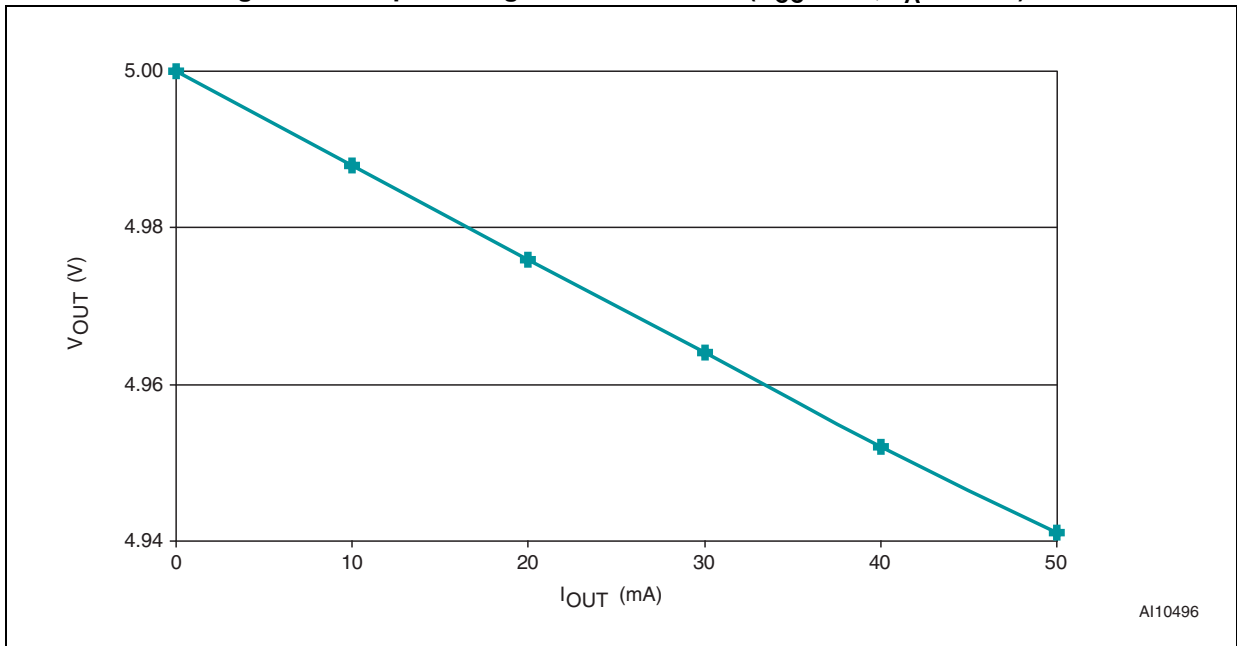


Figure 20. \overline{RST} output voltage vs. supply voltage

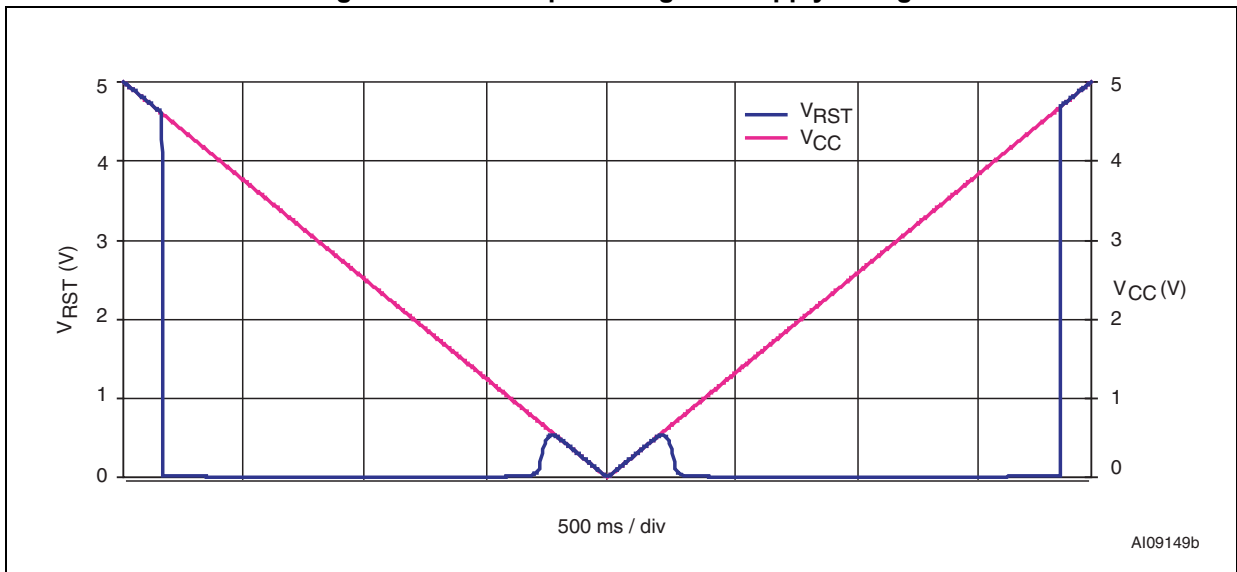


Figure 21. RST output voltage vs. supply voltage

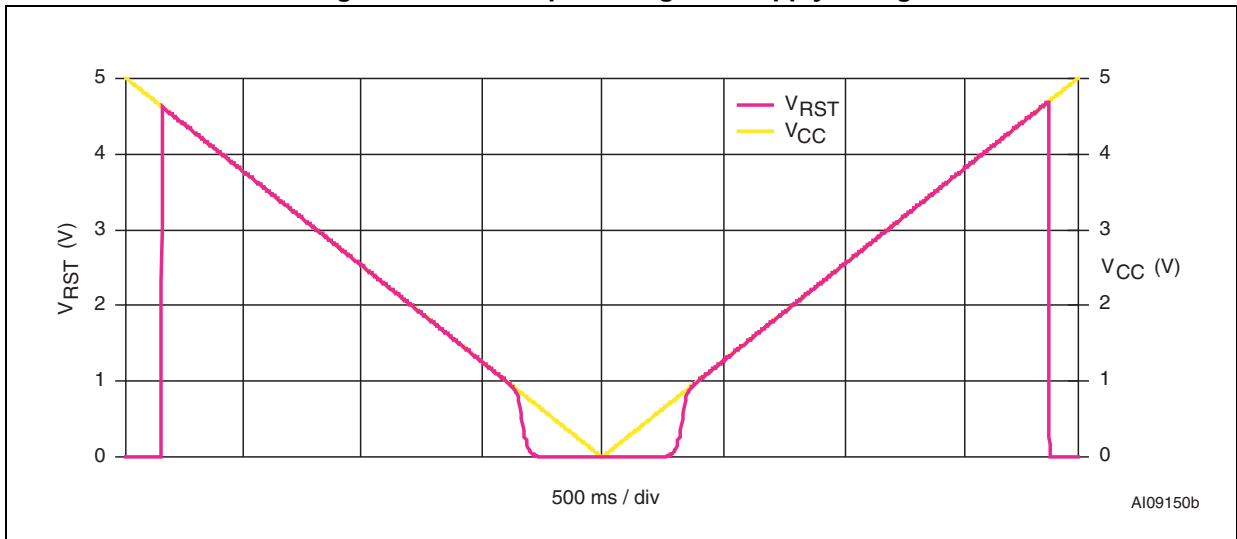


Figure 22. Power-fail comparator response time (assertion)

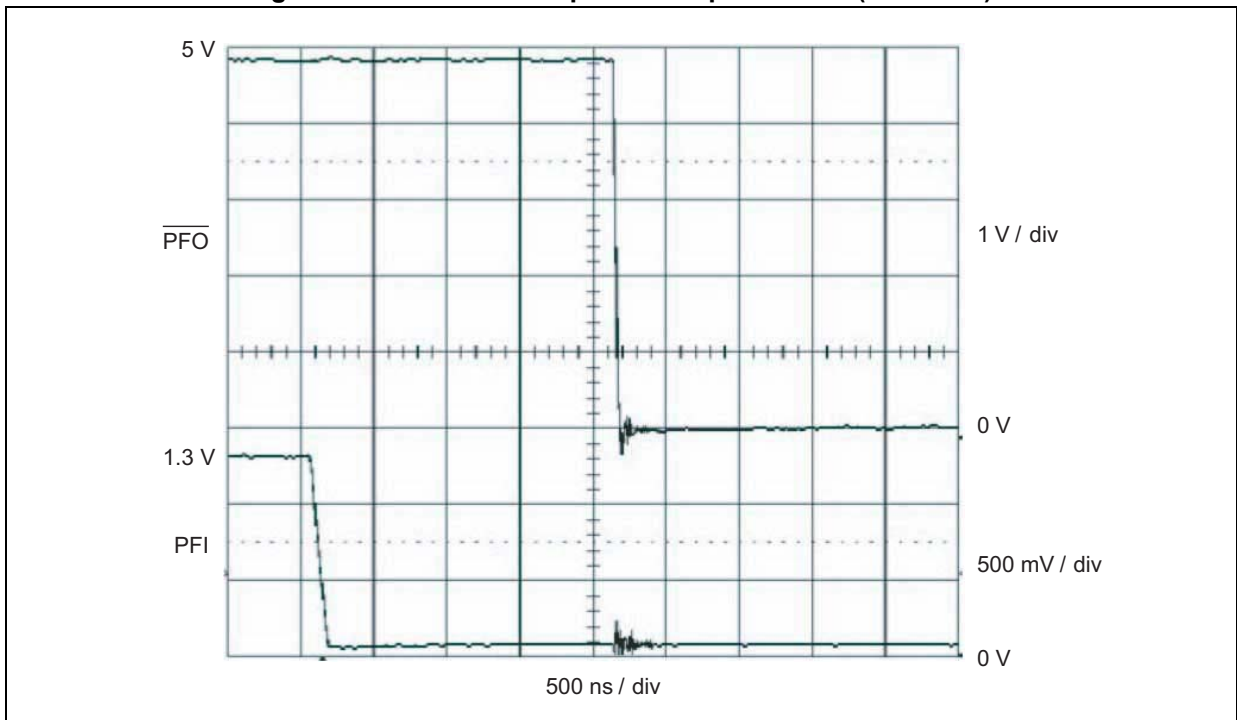


Figure 23. Power-fail comparator response time (de-assertion)

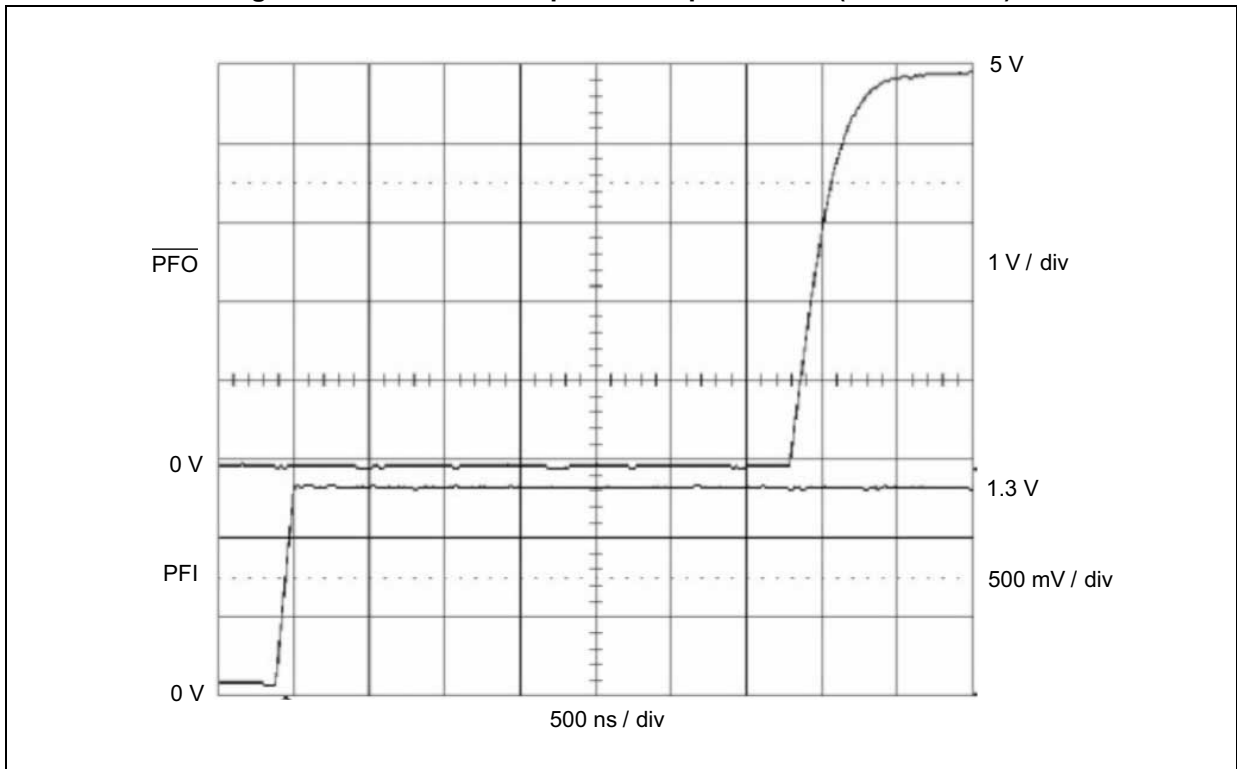
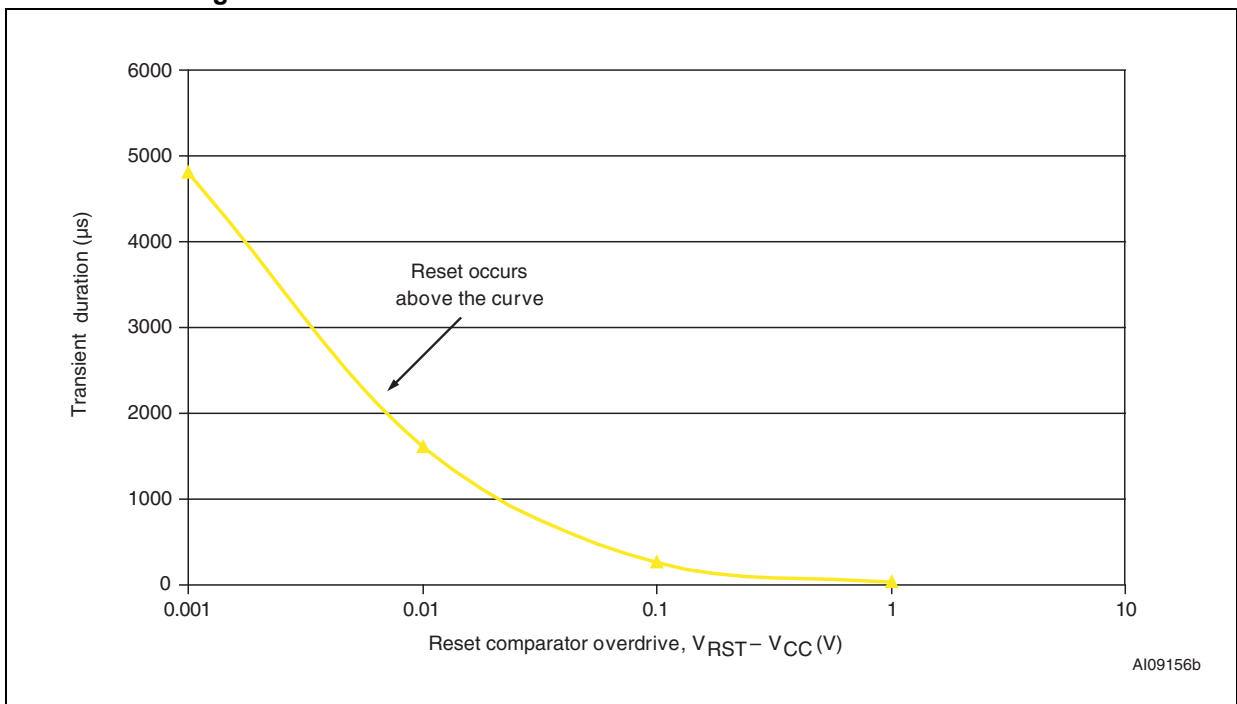


Figure 24. Maximum transient duration vs. reset threshold overdrive



5 Maximum ratings

Stressing the device above the rating listed in the [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Operating and AC measurement conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|--|------------------------|------|
| T_{STG} | Storage temperature (V_{CC} off) | -55 to 150 | °C |
| $T_{SLD}^{(1)}$ | Lead solder temperature for 10 seconds | 260 | °C |
| $V_{IO}^{(2)}$ | Input or output voltage | -0.3 to $V_{CC} + 0.3$ | V |
| V_{CC} | Supply voltage | -0.3 to 7.0 | V |
| I_O | Output current | 20 | mA |
| P_D | Power dissipation | 320 | mW |

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. Negative undershoot of -1.5 V for up to 10 ns or positive overshoot of $V_{CC} + 1.5$ V for up to 10 ns is allowable on the WDI and MR input pins.

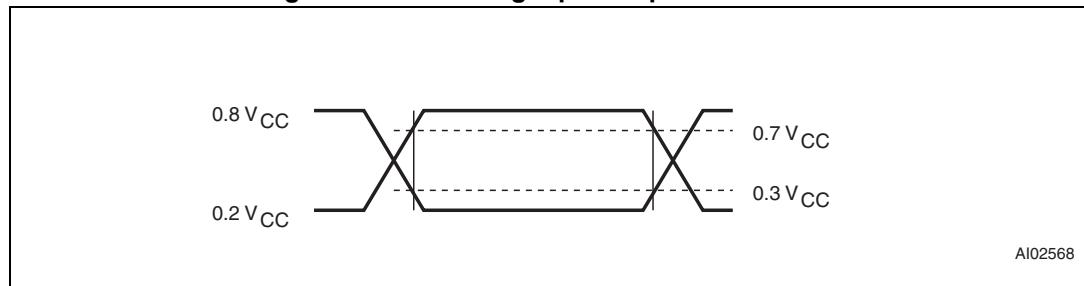
6 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in [Table 6: DC and AC characteristics](#) are derived from tests performed under the measurement conditions summarized in [Table 5: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

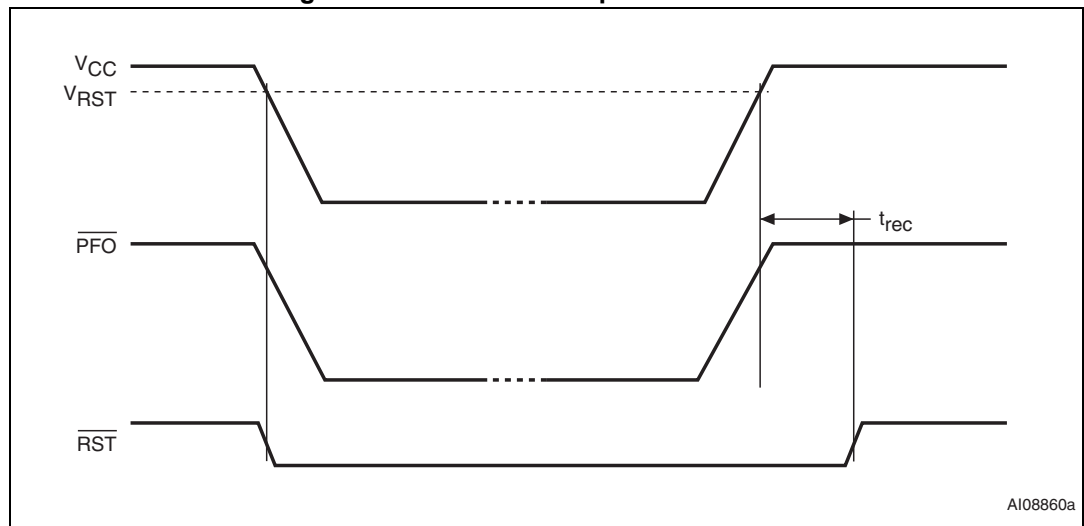
| Parameter | STM70x | Unit |
|---|----------------------------|------|
| V _{CC} supply voltage | 1.0 to 5.5 | V |
| Ambient operating temperature (T _A) | -40 to 85 | °C |
| Input rise and fall times | ≤ 5 | ns |
| Input pulse voltages | 0.2 to 0.8 V _{CC} | V |
| Input and output timing ref. voltages | 0.3 to 0.7 V _{CC} | V |

Figure 25. AC testing input/output waveforms



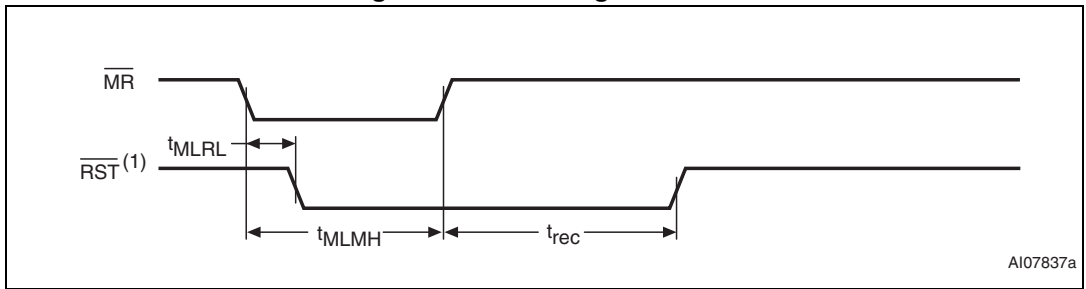
AI02568

Figure 26. Power-fail comparator waveform



AI08860a

Figure 27. $\overline{\text{MR}}$ timing waveform



1. RST for STM706P and STM708T/S/R.

Figure 28. Watchdog timing (STM706T/S/R and STM706P)

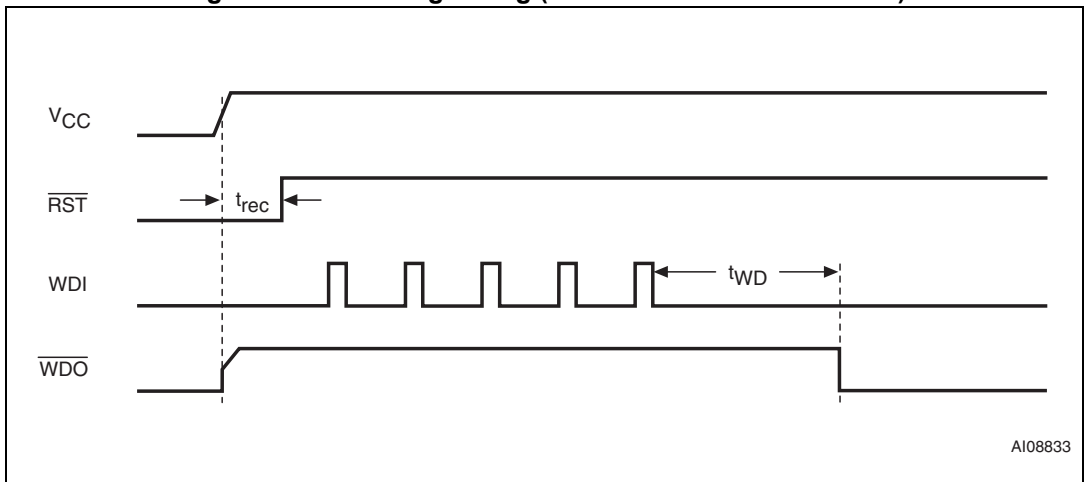


Table 6. DC and AC characteristics

| Symbol | Description | Test condition ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|------------------------------|--|--|--------------------|------|--------------|---------|
| V_{CC} | Operating voltage | | 1.2 ⁽²⁾ | | 5.5 | V |
| I_{CC} | V_{CC} supply current | $V_{CC} < 3.6$ V | | 35 | 50 | μ A |
| | | $V_{CC} < 5.5$ V | | 40 | 60 | μ A |
| I_{LI} | Input leakage current (WDI) | 0 V < V_{IN} < V_{CC} | -1 | | +1 | μ A |
| | Input leakage current (WDI) with watchdog disable feature ("D" version) | 0 V < V_{IN} < V_{CC} | -110 | | 110 | μ A |
| | Input leakage current (PFI) | 0 V < V_{IN} < V_{CC} | -25 | 2 | +25 | nA |
| | Input leakage current (MR) | V_{RST} (max.) < $V_{CC} < 3.6$ V | 25 | 80 | 250 | μ A |
| 4.5 V < $V_{CC} < 5.5$ V | | 75 | 125 | 300 | μ A | |
| V_{IH} | Input high voltage (\overline{MR}) | 4.5 V < $V_{CC} < 5.5$ V | 2.0 | | | V |
| | | V_{RST} (max.) < $V_{CC} < 3.6$ V | $0.7 V_{CC}$ | | | V |
| V_{IH} | Input high voltage (WDI) | V_{RST} (max.) < $V_{CC} < 5.5$ V | $0.7 V_{CC}$ | | | V |
| V_{IL} | Input low voltage (\overline{MR}) | 4.5 V < $V_{CC} < 5.5$ V | | | 0.8 | V |
| | | V_{RST} (max.) < $V_{CC} < 3.6$ V | | | 0.6 | V |
| V_{IL} | Input low voltage (WDI) | V_{RST} (max.) < $V_{CC} < 5.5$ V | | | $0.3 V_{CC}$ | V |
| V_{OL} | Output low voltage (\overline{PFO} , \overline{RST} , \overline{RST} , \overline{WDO}) | $V_{CC} = V_{RST}$ (max.), $I_{SINK} = 3.2$ mA | | | 0.3 | V |
| V_{OL} | Output low voltage (\overline{RST}) | $I_{SINK} = 50$ μ A, $V_{CC} = 1.0$ V, $T_A = 0$ °C to 85 °C | | | 0.3 | V |
| | | $I_{SINK} = 100$ μ A, $V_{CC} = 1.2$ V | | | 0.3 | V |
| V_{OH} | Output high voltage (\overline{RST} , \overline{RST} , \overline{WDO}) | $I_{SOURCE} = 1$ mA, $V_{CC} = V_{RST}$ (max.) | 2.4 | | | V |
| | | $I_{SOURCE} = 75$ μ A, $V_{CC} = V_{RST}$ (max.) | $0.8 V_{CC}$ | | | V |
| Power-fail comparator | | | | | | |
| V_{PFI} | PFI input threshold | PFI falling (STM70xP/R, $V_{CC} = 3.0$ V; STM70xS/T, $V_{CC} = 3.3$ V) | 1.20 | 1.25 | 1.30 | V |
| t_{PFD} | PFI to \overline{PFO} propagation delay | | | 2 | | μ s |

Table 6. DC and AC characteristics (continued)

| Symbol | Description | Test condition ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|---|--|---|------|------|------|------|
| Reset thresholds | | | | | | |
| V_{RST} | Reset threshold ⁽³⁾ | STM706P/70xR | 2.55 | 2.63 | 2.70 | V |
| | | STM70xS | 2.85 | 2.93 | 3.00 | V |
| | | STM70xT | 3.00 | 3.08 | 3.15 | V |
| | Reset threshold hysteresis | | | 20 | | mV |
| t_{rec} | \overline{RST} pulse width | Blank (see Table 9) | 140 | 200 | 280 | ms |
| | | A ⁽⁴⁾ (see Table 9) | 160 | 200 | 280 | |
| Push-button reset input | | | | | | |
| t_{MLMH} (or t_{MR}) | \overline{MR} pulse width | $V_{RST} (max.) < V_{CC} < 3.6 V$ | 500 | | | ns |
| | | $4.5 V < V_{CC} < 5.5 V$ | 150 | | | ns |
| t_{MLRL} (or t_{MRD}) | \overline{MR} to \overline{RST} output delay | $V_{RST} (max.) < V_{CC} < 3.6 V$ | | | 750 | ns |
| | | $4.5 V < V_{CC} < 5.5 V$ | | | 250 | ns |
| Watchdog timer (STM706T/S/R and STM706P) | | | | | | |
| t_{WD} | Watchdog timeout period | STM706P/70xR, $V_{CC} = 3.0 V$ | 1.12 | 1.60 | 2.24 | s |
| | | STM70xS/70XT, $V_{CC} = 3.3 V$ | | | | |
| | WDI pulse width | $4.5 V < V_{CC} < 5.5 V$ | 50 | | | ns |
| | | $V_{RST} (max.) < V_{CC} < 3.6 V$ | 100 | | | ns |

1. Valid for ambient operating temperature: $T_A = -40$ to 85 °C; $V_{CC} = V_{RST} (max.)$ to $5.5 V$ (except where noted).

2. $V_{CC} (min) = 1.0 V$ for $T_A = 0$ °C to $+85$ °C.

3. For V_{CC} falling.

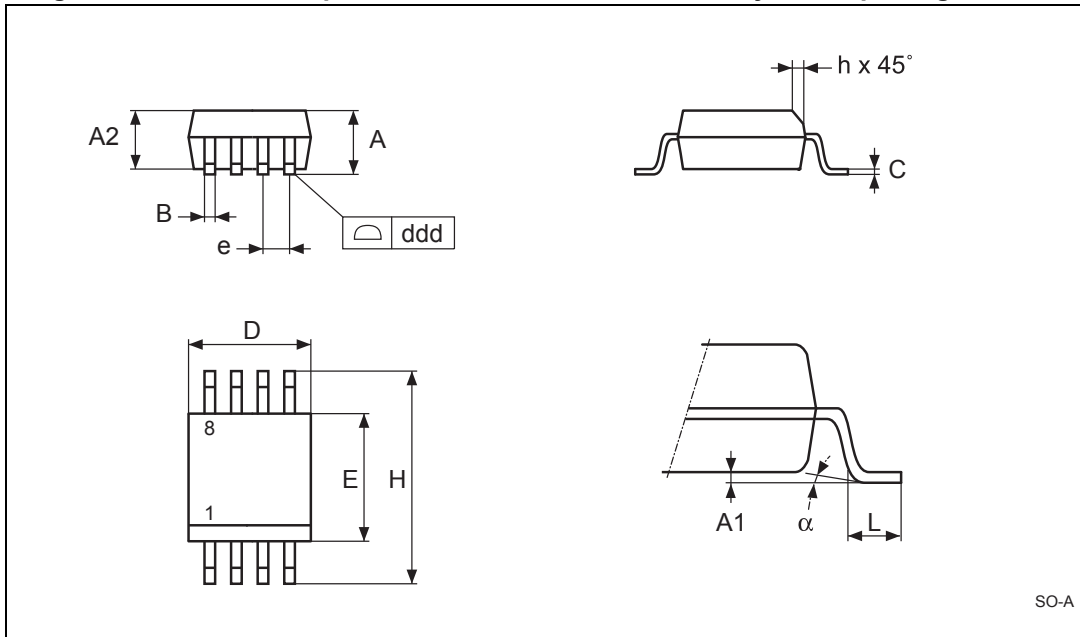
4. STM706P/STM70xR device, $V_{CC} = 3 V$; STM706xS/STM70xT device, $V_{CC} = 3.3 V$.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 SO8 package information

Figure 29. SO8 - 8-lead plastic small outline, 150 mils body width, package outline



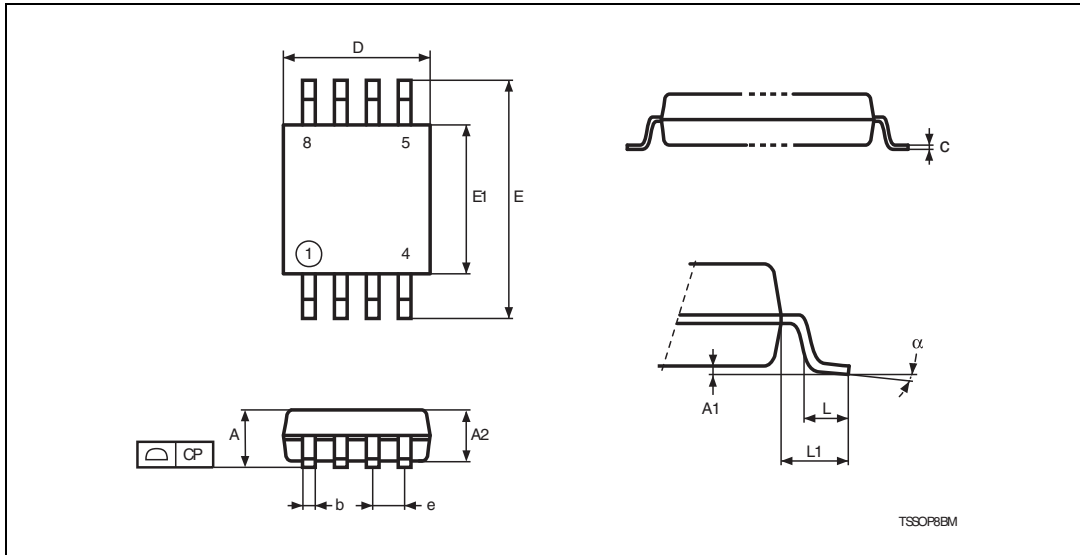
Note: Drawing is not to scale.

Table 7. SO8 - 8-lead plastic small outline, 150 mils body width, mechanical data

| Symbol | Dimensions | | | | | |
|--------|------------|------|------|--------|-------|-------|
| | mm | | | inches | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | — | 1.35 | 1.75 | — | 0.053 | 0.069 |
| A1 | — | 0.10 | 0.25 | — | 0.004 | 0.010 |
| B | — | 0.33 | 0.51 | — | 0.013 | 0.020 |
| C | — | 0.19 | 0.25 | — | 0.007 | 0.010 |
| D | — | 4.80 | 5.00 | — | 0.189 | 0.197 |
| ddd | — | — | 0.10 | — | — | 0.004 |
| E | — | 3.80 | 4.00 | — | 0.150 | 0.157 |
| e | 1.27 | — | — | 0.050 | — | — |
| H | — | 5.80 | 6.20 | — | 0.228 | 0.244 |
| h | — | 0.25 | 0.50 | — | 0.010 | 0.020 |
| L | — | 0.40 | 0.90 | — | 0.016 | 0.035 |
| α | — | 0° | 8° | — | 0° | 8° |
| N | 8 | 8 | | | | |

7.2 TSSOP8 3x3 (DS) package information

Figure 30. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, package outline



Note: Drawing is not to scale.

Table 8. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, mechanical data

| Symbol | Dimensions | | | | | |
|--------|------------|------|------|--------|-------|-------|
| | mm | | | inches | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | — | — | 1.10 | — | — | 0.043 |
| A1 | — | 0.05 | 0.15 | — | 0.002 | 0.006 |
| A2 | 0.85 | 0.75 | 0.95 | 0.034 | 0.030 | 0.037 |
| b | — | 0.25 | 0.40 | — | 0.010 | 0.016 |
| c | — | 0.13 | 0.23 | — | 0.005 | 0.009 |
| CP | — | — | 0.10 | — | — | 0.004 |
| D | 3.00 | 2.90 | 3.10 | 0.118 | 0.114 | 0.122 |
| e | 0.65 | — | — | 0.026 | — | — |
| E | 4.90 | 4.65 | 5.15 | 0.193 | 0.183 | 0.203 |
| E1 | 3.00 | 2.90 | 3.10 | 0.118 | 0.114 | 0.122 |
| L | 0.55 | 0.40 | 0.70 | 0.022 | 0.016 | 0.030 |
| L1 | 0.95 | — | — | 0.037 | — | — |
| α | — | 0° | 6° | — | 0° | 6° |
| N | 8 | 8 | | | | |

8 Part numbering

Table 9. Ordering information scheme

| Example: | STM706 | T | D | M | 6 | F |
|--------------------------------|---|---|---|---|---|---|
| Device type | STM706 STM708 | | | | | |
| Reset threshold voltage | T: $3.00\text{ V} \leq V_{RST} \leq 3.15\text{ V}$ S: $2.88\text{ V} \leq V_{RST} \leq 3.00\text{ V}$ R: STM706P: $2.59\text{ V} \leq V_{RST} \leq 2.70\text{ V}$ | | | | | |
| Watchdog disable | Blank = not activated D = activated | | | | | |
| RST pulse width | Blank = 140 to 280 ms A ⁽¹⁾ = 160 to 280 ms | | | | | |
| Package | M = SO8 DS ⁽²⁾ = TSSOP8 | | | | | |
| Temperature range | 6 = -40 to 85 °C | | | | | |
| Shipping method | F = ECOPACK® packages, tape and reel | | | | | |

1. Available in SO8 (M) package only
2. Contact local ST sales office for availability

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 10. Marking description

| Part number | Reset threshold | Package | Topside marking |
|-------------|-----------------|---------|-----------------|
| STM706P | 2.63 V | SO8 | 706P |
| | | TSSOP8 | |
| STM706T | 3.08 V | SO8 | 706T |
| | | TSSOP8 | |
| STM706S | 2.93 V | SO8 | 706S |
| | | TSSOP8 | |
| STM706R | 2.63 V | SO8 | 706R |
| | | TSSOP8 | |
| STM706RD | 2.63 V | SO8 | 706RD |
| | | TSSOP8 | |
| STM708T | 3.08 V | SO8 | 708T |
| | | TSSOP8 | |
| STM708S | 2.93 V | SO8 | 708S |
| | | TSSOP8 | |
| STM708R | 2.63 V | SO8 | 708R |
| | | TSSOP8 | |

9 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| Oct-2003 | 1 | Initial release. |
| 12-Dec-2003 | 2 | Reformatted; update characteristics (<i>Figure 2, 3, 8 to 10, 27 to 29; Table 6 to 9</i>). |
| 16-Jan-2004 | 2.1 | Add <i>Typical operating characteristics (Figure 13, to 19, 21, to 25)</i> . |
| 09-Apr-2004 | 3 | Reformatted; update characteristics (<i>Figure 15, 19, 21, 22, 25; Table 8</i>). |
| 25-May-2004 | 4 | Update characteristics (<i>Table 3, Table 6</i>). |
| 02-Jul-2004 | 5 | Datasheet promoted; waveform corrected (<i>Table 27</i>). |
| 21-Sep-2004 | 6 | Clarify root part numbers; (<i>Figure 2, to 10, 29; Table 1, 3, 6, 9</i>). |
| 25-Feb-2005 | 7 | Update typical characteristics (<i>Figure 13 to 25</i>). |
| 02-Nov-2009 | 8 | Updated <i>Table 1, Table 3, Table 4, Table 6, Table 9, Section 2.3, Section 2.7, text in Section 7</i> ; reformatted document. |
| 30-Apr-2010 | 9 | Updated <i>Table 4</i> , corrected typo in <i>Table 2, Section 2.3, Section 3, Section 5 and Section 6, Figure 17, Table 7 and Table 8</i> . |
| 06-Aug-2010 | 10 | Updated <i>Features, Section 4: Typical operating characteristics; Table 9</i> . |
| 06-Sep-2011 | 11 | Updated <i>Section 2.7, Section 5 and Disclaimer</i> , minor typo modifications throughout the document. |
| 21-Aug-2012 | 12 | Added <i>Applications</i> , updated <i>Section 2.2 and Section 2.3</i> , added note to <i>Section 3.3</i> , added cross-references in <i>Section 5 and Section 6</i> , minor text corrections throughout document. |
| 15-Dec-2015 | 13 | Updated layout of cover page and <i>Section 7: Package information</i> . Added information about the watchdog disable function to <i>Section 2.2: WDI, Table 6, Table 9, and Table 10</i> . <i>Table 9</i> : removed the "E" option (tubes) from shipping method |

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