



**THE DATASHEET OF
74ALVC74PW,118**



74ALVC74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 4 — 16 August 2017

Product data sheet

1 General description

The 74ALVC74 is a dual positive edge triggered, D-type flip-flop. It has individual data (nD) inputs, clock (nCP) inputs, set ($n\overline{SD}$) and ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2 Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
 - JESD8-7 (1.65 to 1.95 V)
 - JESD8-5 (2.3 to 2.7 V)
 - JESD8B/JESD36 (2.7 to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
 - HBM JESD22-A114-A exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC74D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC74PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC74BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm	SOT762-1

4 Functional diagram

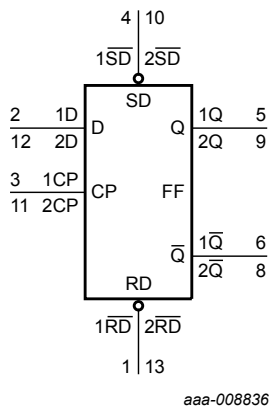


Figure 1. Logic symbol

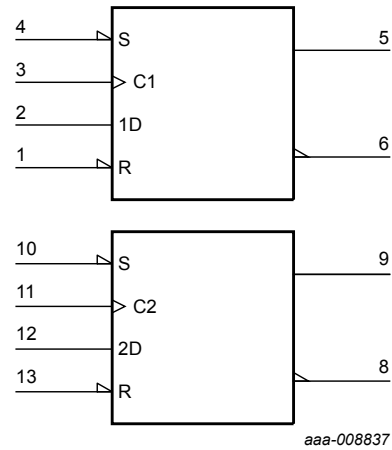


Figure 2. IEC logic symbol

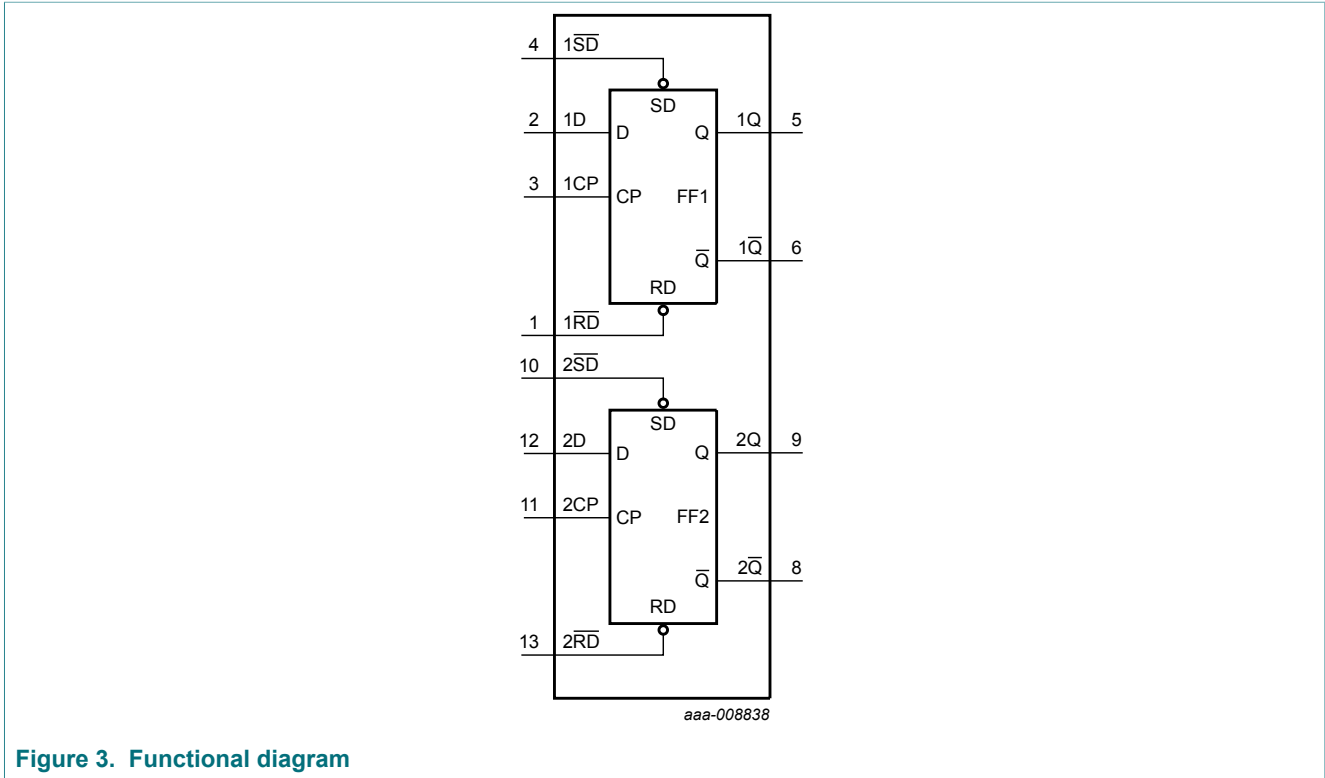


Figure 3. Functional diagram

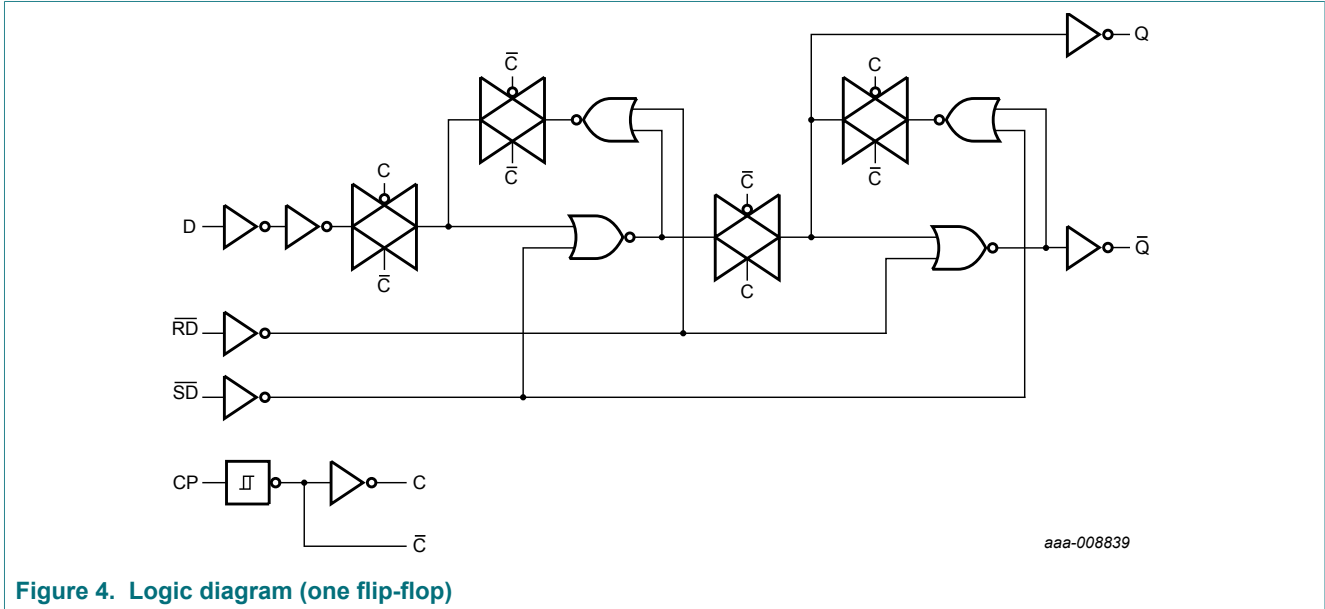
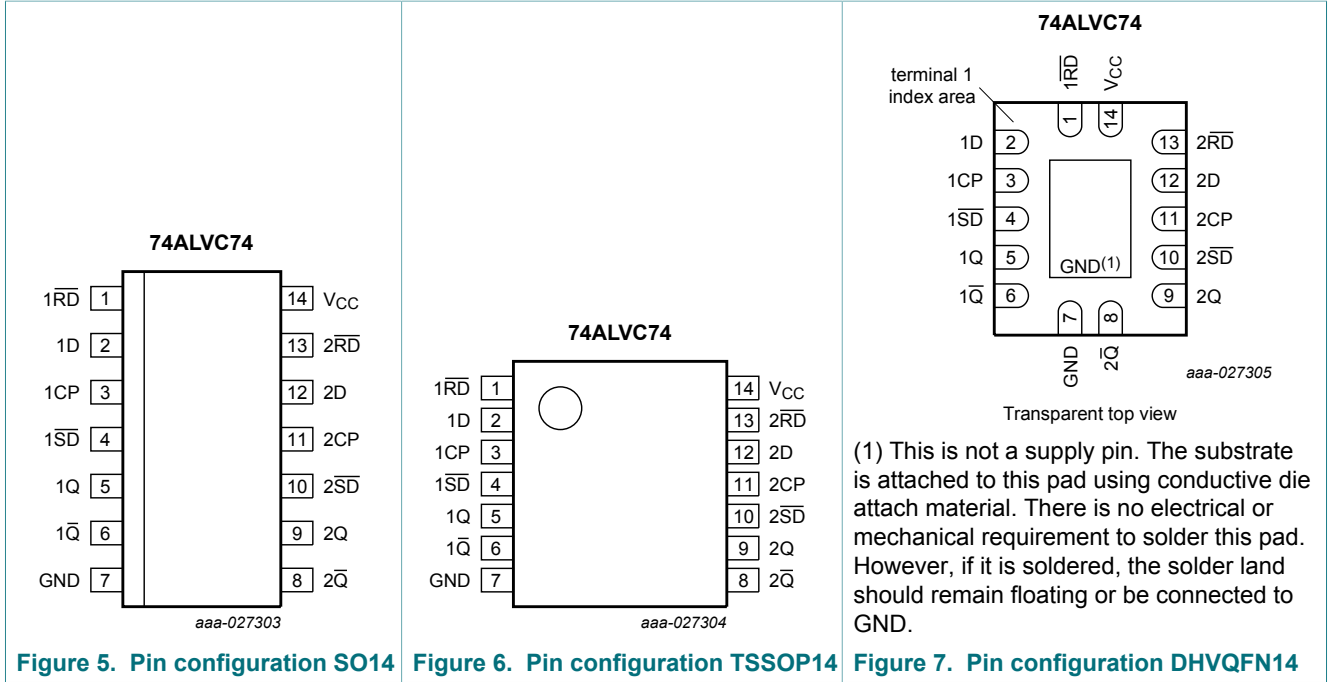


Figure 4. Logic diagram (one flip-flop)

5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1R \bar{D}	1	asynchronous reset-direct input (active-LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH), edge-triggered
1S \bar{D}	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop output
1Q $\bar{}$	6	complement flip-flop output
GND	7	ground (0 V)
2Q $\bar{}$	8	complement flip-flop output
2Q	9	true flip-flop output
2S \bar{D}	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered
2D	12	data input
2R \bar{D}	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6 Functional description

Table 3. Function table ^[1]

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ	nQ _{n+1}	nQ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 nQ_{n+1} = state after the next LOW-to-HIGH CP transition

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[1] -0.5	+4.6	V
V _O	output voltage		^[1] -0.5	V _{CC} + 0.5	V
		Power-down mode	^[1] ^[2] -0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	^[3] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.
 [3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
 For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	$V_{CC} = 1.65$ to 3.6 V	0	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65$ V to 3.6 V; $I_O = -100$ μ A	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 1.65$ V; $I_O = -6$ mA	1.25	1.51	-	V
		$V_{CC} = 2.3$ V; $I_O = -12$ mA	1.8	2.10	-	V
		$V_{CC} = 2.3$ V; $I_O = -18$ mA	1.7	2.01	-	V
		$V_{CC} = 2.7$ V; $I_O = -12$ mA	2.2	2.53	-	V
		$V_{CC} = 3.0$ V; $I_O = -18$ mA	2.4	2.76	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65$ V to 3.6 V; $I_O = 100$ μ A	-	-	0.2	V
		$V_{CC} = 1.65$ V; $I_O = 6$ mA	-	0.11	0.3	V
		$V_{CC} = 2.3$ V; $I_O = 12$ mA	-	0.17	0.4	V
		$V_{CC} = 2.3$ V; $I_O = 18$ mA	-	0.25	0.6	V
		$V_{CC} = 2.7$ V; $I_O = 12$ mA	-	0.16	0.4	V
		$V_{CC} = 3.0$ V; $I_O = 18$ mA	-	0.23	0.4	V
	$V_{CC} = 3.0$ V; $I_O = 24$ mA	-	0.30	0.55	V	

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_I	input leakage current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	$V_{CC} = \text{GND}$; V_I or $V_O = 3.6\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.2	10	μA
ΔI_{CC}	additional supply current	$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	750	μA
C_I	input capacitance		-	3.5	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$.

10 Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit	
t_{pd}	propagation delay	nCP to nQ, n \bar{Q} ; see Figure 8 ^[2]					
		$V_{CC} = 1.65\text{ to } 1.95\text{ V}$	1.0	3.7	6.2	ns	
		$V_{CC} = 2.3\text{ to } 2.7\text{ V}$	1.0	2.6	4.2	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	2.8	4.2	ns	
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.7	3.8	ns	
		n $\bar{S}\bar{D}$ to nQ, n \bar{Q} ; see Figure 9					
		$V_{CC} = 1.65\text{ to } 1.95\text{ V}$	1.0	3.4	5.4	ns	
		$V_{CC} = 2.3\text{ to } 2.7\text{ V}$	1.0	2.4	3.8	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	3.2	4.2	ns	
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.3	3.5	ns	
		n $\bar{R}\bar{D}$ to nQ, n \bar{Q} ; see Figure 9					
		$V_{CC} = 1.65\text{ to } 1.95\text{ V}$	1.0	3.5	5.4	ns	
		$V_{CC} = 2.3\text{ to } 2.7\text{ V}$	1.0	2.5	3.8	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	3.1	4.3	ns	
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.3	3.5	ns	

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit	
t _w	pulse width	nCP; HIGH or LOW; see Figure 8					
		V _{CC} = 1.65 to 1.95 V	2.5	0.9	-	ns	
		V _{CC} = 2.3 to 2.7 V	2.5	0.6	-	ns	
		V _{CC} = 2.7 V	2.5	1.3	-	ns	
		V _{CC} = 3.0 V to 3.6 V	2.5	1.3	-	ns	
		nSD or nRD; LOW; see Figure 9					
		V _{CC} = 1.65 to 1.95 V	2.5	0.9	-	ns	
		V _{CC} = 2.3 to 2.7 V	2.5	0.9	-	ns	
t _{rec}	recovery time	nRD to nCP; see Figure 9					
		V _{CC} = 1.65 to 1.95 V	0.7	-0.2	-	ns	
		V _{CC} = 2.3 to 2.7 V	0.7	-0.1	-	ns	
		V _{CC} = 2.7 V	0.7	-0.1	-	ns	
t _{su}	set-up time	nD to nCP; see Figure 8					
		V _{CC} = 1.65 to 1.95 V	1.2	0.6	-	ns	
		V _{CC} = 2.3 to 2.7 V	1.2	0.8	-	ns	
		V _{CC} = 2.7 V	0.9	0.5	-	ns	
t _h	hold time	nD to nCP; see Figure 8					
		V _{CC} = 1.65 to 1.95 V	0.6	-0.4	-	ns	
		V _{CC} = 2.3 to 2.7 V	0.6	-0.3	-	ns	
		V _{CC} = 2.7 V	0.7	-0.4	-	ns	
f _{max}	maximum frequency	nCP; see Figure 8					
		V _{CC} = 1.65 to 1.95 V	150	275	-	MHz	
		V _{CC} = 2.3 to 2.7 V	200	325	-	MHz	
		V _{CC} = 2.7 V	250	375	-	MHz	
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3]	-	35	-	pF	

[1] Typical values are measured at T_{amb} = 25 °C.

Typical values are measured at V_{CC} = 1.8 V for V_{CC} = 1.65 V to 1.95 V.

Typical values are measured at V_{CC} = 2.5 V for V_{CC} = 2.3 V to 2.7 V.

Typical values are measured at V_{CC} = 3.3 V for V_{CC} = 3.0 V to 3.6 V

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

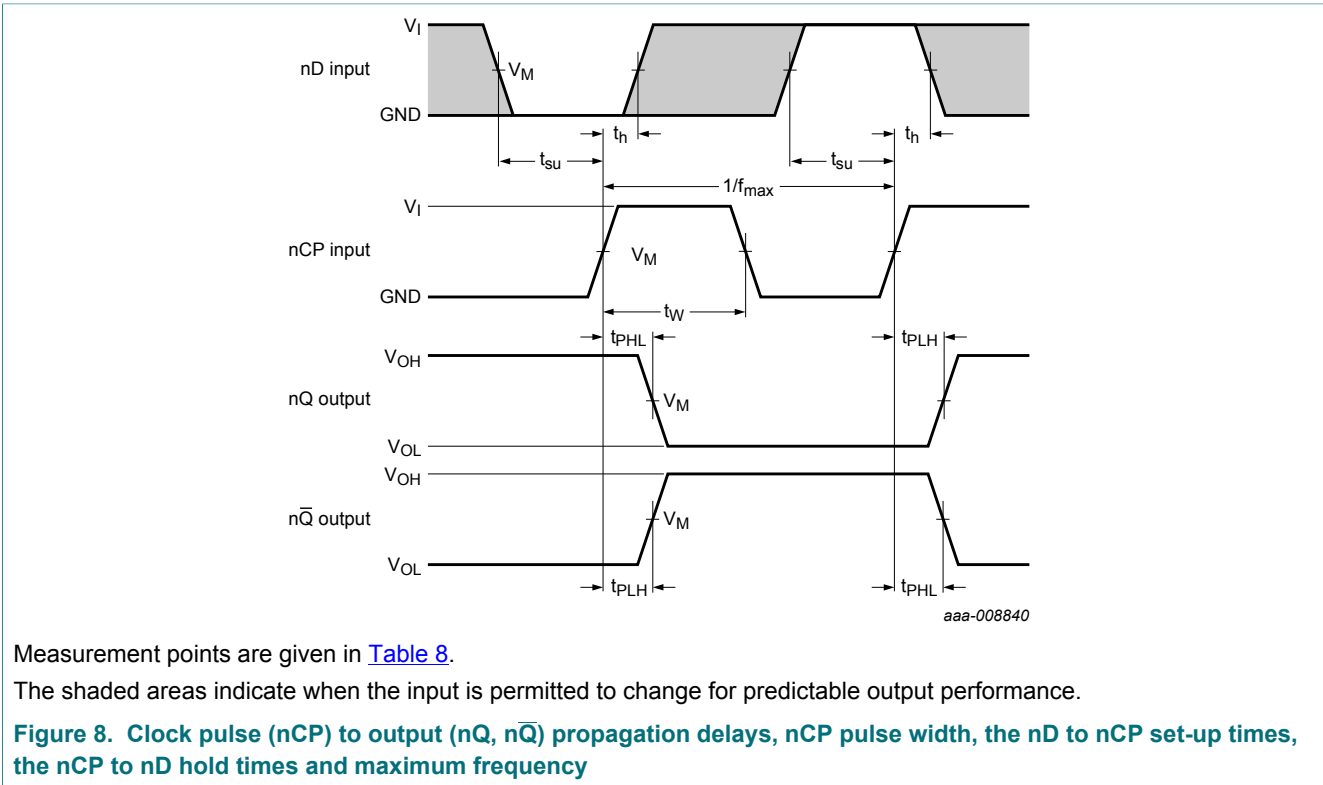
[3] C_{PD} is used to determine the dynamic power dissipation P_D = C_{PD} × V_{CC}² × f_i × N + Σ (C_L × V_{CC}² × f_o), where:

P_D in μW

f_i = input frequency in MHz;

f_o = output frequency in MHz;
 N = total load switching outputs
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

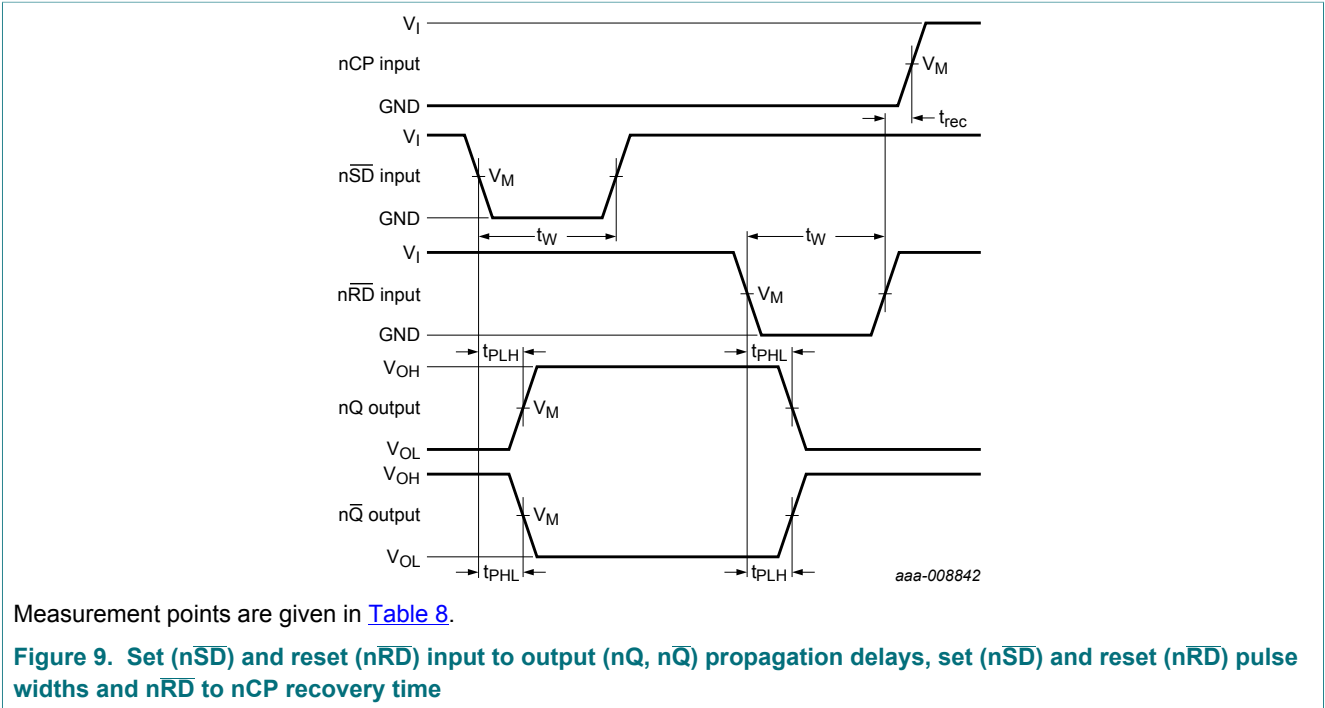
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 8. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width, the nD to nCP set-up times, the nCP to nD hold times and maximum frequency



Measurement points are given in [Table 8](#).

Figure 9. Set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ , $n\overline{Q}$) propagation delays, set ($n\overline{SD}$) and reset ($n\overline{RD}$) pulse widths and $n\overline{RD}$ to nCP recovery time

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.65 V to 1.95 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V

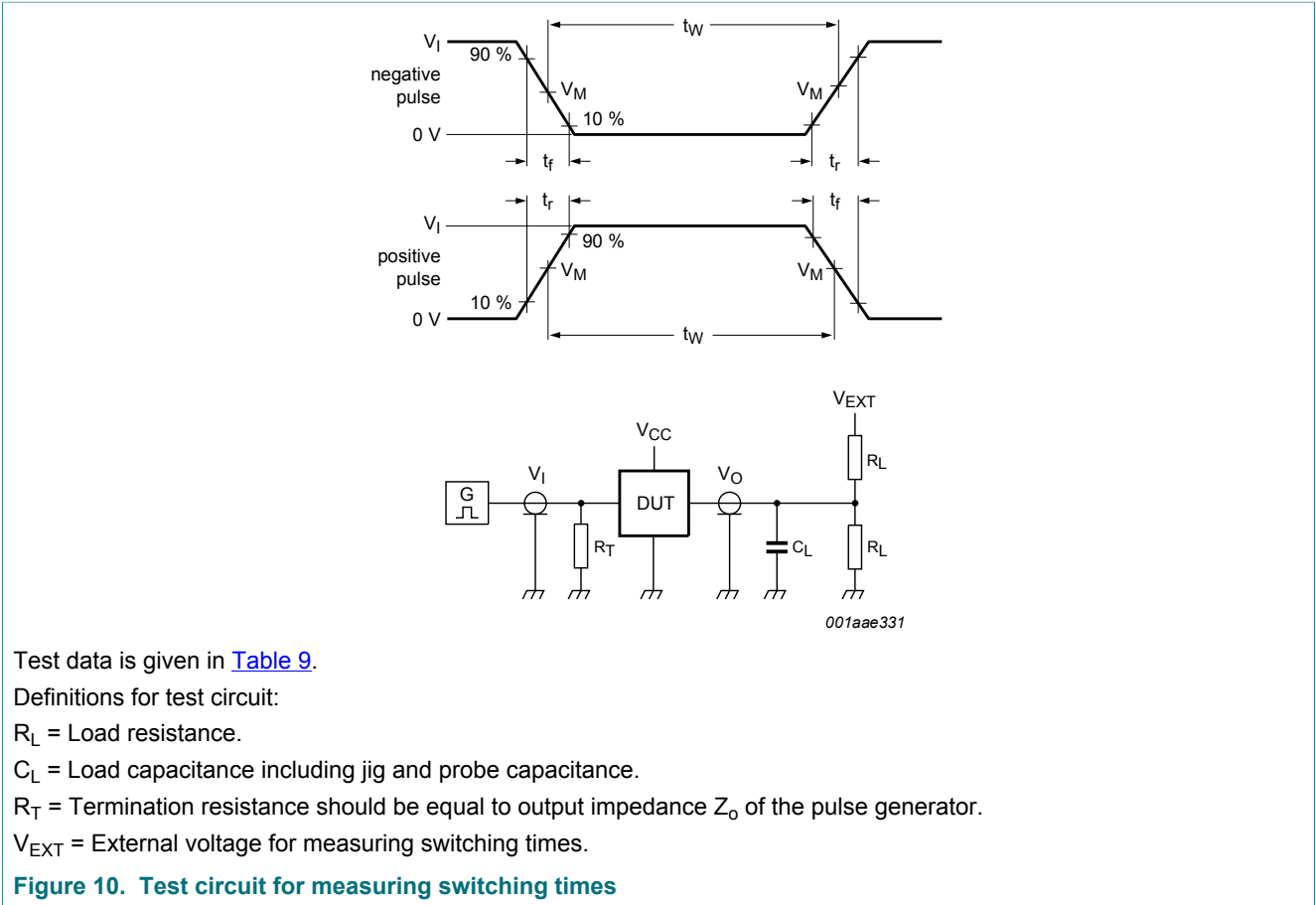


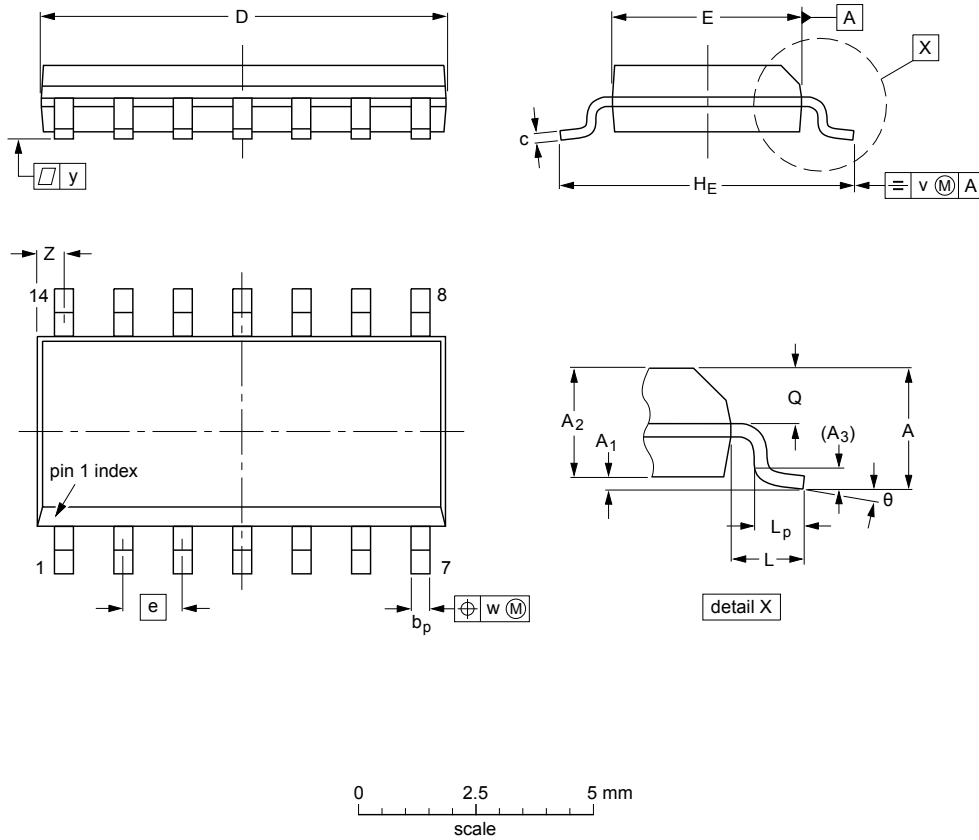
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

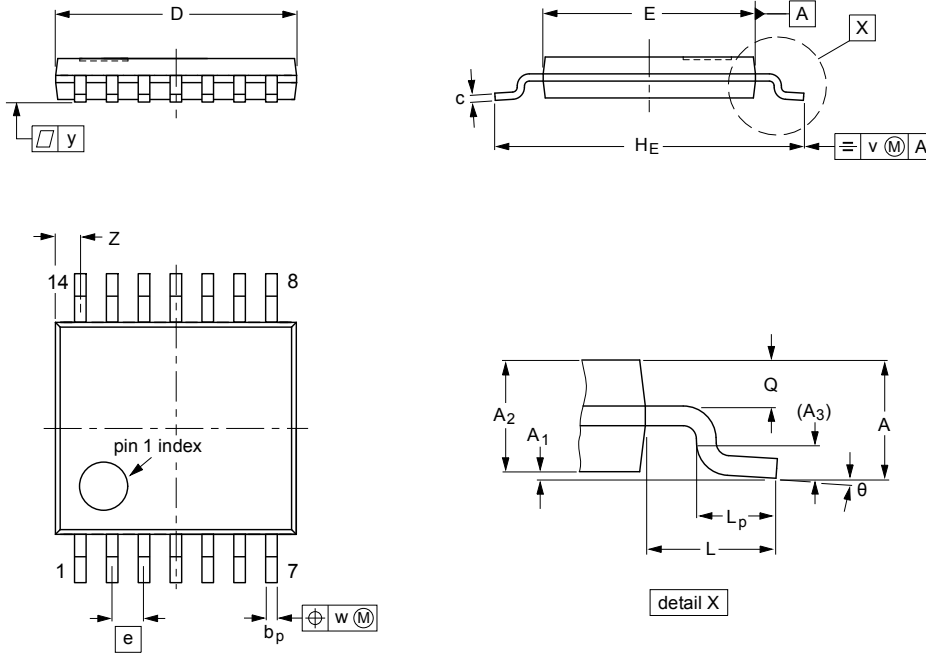
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

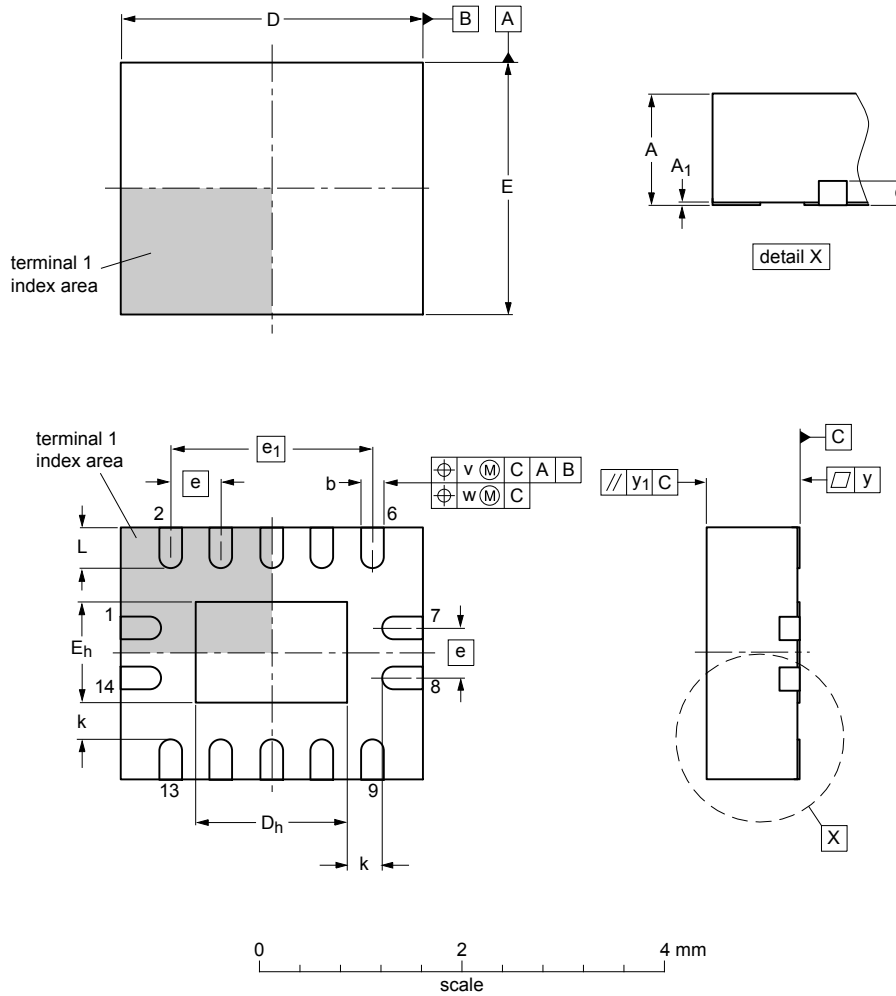
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Figure 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom	0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2	0.4	0.1	0.05	0.05	0.1	
	min	0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po


Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Figure 13. Package outline SOT762-1 (DHVQFN14)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC74 v.4	20170816	Product data sheet	-	74ALVC74 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVC74 v.3	20030526	Product specification	-	74ALVC74 v.2
74ALVC74 v.2	20030124	Product specification	-	74ALVC74 v.1
74ALVC74 v.1	20021115	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Dual D-type flip-flop with set and reset; positive-edge trigger

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