



**THE DATASHEET OF  
SKY13396-397LF**



**DATA SHEET**

# SKY13396-397LF: 0.4 to 3.0 GHz DPDT Switch

## Applications

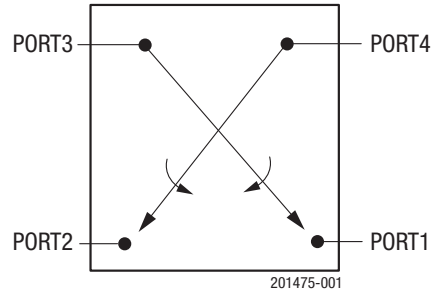
- Simultaneous voice and LTE systems
- Diversity antenna switching

## Features

- Single control voltage input
- Broadband frequency range: 0.4 to 3.0 GHz
- Low insertion loss: 0.5 dB @ 2.2 GHz
- No DC blocking capacitors required
- Positive control voltage range: 1.35 to 3.1 V
- GSM power handling
- Small QFN (12-pin, 2 x 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



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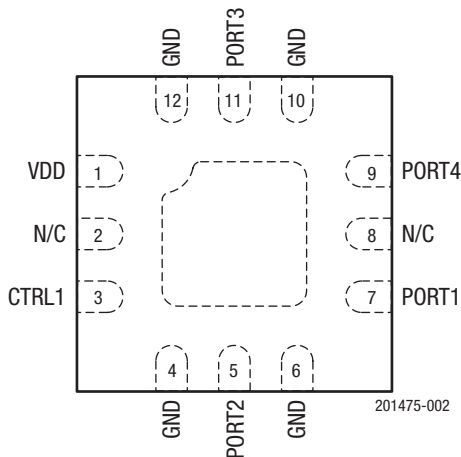
**Figure 1. SKY13396-397LF Block Diagram**

## Description

The SKY13396-397LF is a state-of-the-art CMOS, Silicon-On-Insulator (SOI) double-pole, double-throw (DPDT) switch. The switch provides high-linearity performance, low insertion loss, and high isolation.

Switching is controlled by one voltage input (CTRL1). Depending on the logic voltage level applied to this pin, the PORT1 and PORT2 pins connect to one of the two other RF port pins (PORT3 or PORT4) through a low insertion loss path, while maintaining a high isolation path to the alternate port. No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied externally.

The SKY13396-397LF DPDT switch is provided in a compact Quad Flat No-Lead (QFN) 2 x 2 mm package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



**Figure 2. SKY13396-397LF Pinout (Top View)**

**Table 1. SKY13396-397LF Signal Descriptions<sup>1</sup>**

Pin	Name	Description	Pin	Name	Description
1	VDD	DC power supply	7	PORT1	RF port 1
2	N/C	No connection. Pin may be grounded.	8	N/C	No connection. Pin may be grounded.
3	CTRL1	DC control voltage 1. See Table 4.	9	PORT4	RF Port 4
4	GND	Ground. Internally grounded.	10	GND	Ground. Internally grounded.
5	PORT2	RF port 2	11	PORT3	RF port 3
6	GND	Ground. Internally grounded.	12	GND	Ground. Internally grounded.

<sup>1</sup> Exposed pad must be properly grounded using a low impedance path.

**Table 2. SKY13396-397LF Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V <sub>DD</sub>		5.5	V
Control voltage	V <sub>CTL</sub>		3.3	V
Input power	P <sub>IN</sub>		+39	dBm
Storage temperature	T <sub>STG</sub>	-40	+125	°C
Operating temperature	T <sub>OP</sub>	-30	+90	°C
Electrostatic discharge: Human Body Model (HBM), Class 1B	ESD		500	V

<sup>1</sup> Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

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**ESD HANDLING:** *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

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## Functional Description

The SKY13396-397LF DPDT switch can be used to connect either RF port 1 or RF port 2 to either RF port 3 or RF port 4 by applying the proper bias to the control pin, CTRL1. When Port 1 is connected to Port 4 using a low loss path, Port 2 is connected to Port 3 also with a low loss path. When Port 1 is connected to Port 3 using low loss path, Port 2 is connected to Port 4 also with a low loss path.

The DPDT switch is designed to maximize the isolation between ports to minimize coupling between RF paths.

## Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13396-397LF are provided in Table 2. Electrical specifications are provided in Table 3.

The state of the SKY13396-397LF is determined by the logic provided in Table 4.

**Table 3. SKY13396-397LF Electrical Specifications<sup>1</sup>**

(V<sub>DD</sub> = 2.5 V, V<sub>CTL</sub> = 0 V and +1.8 V, T<sub>OP</sub> = +25 °C, P<sub>IN</sub> = 0 dBm, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>RF Specifications</b>						
Insertion loss	IL	PORT1/PORT2 to PORT3/PORT4:				
		0.4 to 1.0 GHz		0.4	0.45	dB
		1.0 to 2.2 GHz		0.5	0.55	dB
		2.5 to 2.7 GHz		0.6	0.7	dB
Isolation	Iso	PORT1/PORT2 to PORT3/PORT4, PORT1 to PORT2, PORT3 to PORT4:				
		0.4 to 1.0 GHz	23	25		dB
		1.0 to 2.2 GHz	18	20		dB
		2.5 to 2.7 GHz	15	17		dB
Return loss	IS11I	PORT1/PORT2 to PORT3/PORT4, 0.4 to 3.0 GHz	17	20		dB
Third order input intercept point	IIP3	P <sub>IN</sub> = +20 dBm/tone, Δf = 1 MHz, 0.7 to 3.0 GHz		63		dB
2 <sup>nd</sup> harmonic	2fo	P <sub>IN</sub> = +25 dBm, 0.7 to 3.0 GHz		-70	-55	dBm
Band 13 2 <sup>nd</sup> harmonic	2fo_B13	f = 786.5 MHz, P <sub>IN</sub> = +25 dBm		-89	-81	dBm
3 <sup>rd</sup> harmonic	3fo	P <sub>IN</sub> = +25 dBm, 0.7 to 3.0 GHz		-63	-55	dBm
Band 17 3 <sup>rd</sup> harmonic	3fo_B17	f = 710 MHz, P <sub>IN</sub> = +25 dBm		-89	-81	dBm
<b>GSM harmonics:</b>						
Low band	2fo	fo = 824 to 915 MHz, P <sub>IN</sub> = +35 dBm, 50 Ω		-65	-55	dBm
	3fo	fo = 824 to 915 MHz, P <sub>IN</sub> = +35 dBm, 50 Ω		-55	-50	dBm
	2fo	fo = 824 to 915 MHz, P <sub>IN</sub> = +35 dBm, 5:1 VSWR, all phases		-59	-50	dBm
	3fo	fo = 824 to 915 MHz, P <sub>IN</sub> = +35 dBm, 5:1 VSWR, all phases		-47	-38	dBm
High band	2fo	fo = 1710 to 1910 MHz, P <sub>IN</sub> = +33 dBm, 50 Ω		-55	-45	dBm
	3fo	fo = 1710 to 1910 MHz, P <sub>IN</sub> = +33 dBm, 50 Ω		-55	-40	dBm
	2fo	fo = 1710 to 1910 MHz, P <sub>IN</sub> = +33 dBm, 5:1 VSWR, all phases		-45	-40	dBm
	3fo	fo = 1710 to 1910 MHz, P <sub>IN</sub> = +33 dBm, 5:1 VSWR, all phases		-47	-38	dBm
Second order intermodulation distortion	IMD2	f1 > 800 MHz @ +20 dBm, f2 > 2.5 GHz @ -15 dBm		-105	-100	dBm
Third order intermodulation distortion	IMD3	f1 > 800 MHz @ +20 dBm, f2 > 2.5 GHz @ -15 dBm		-104	-95	dBm
Switching speed		50% V1/V2 to 90/10% RF		3	5	μs
		90/10% RF or 10/90% RF		3	5	μs
<b>DC Specifications</b>						
Control voltage:						
High	V <sub>CTL_H</sub>		1.35	2.70	3.10	V
Low	V <sub>CTL_L</sub>		-0.20	0	+0.45	V
Supply voltage	V <sub>DD</sub>		2.5		4.8	V
Supply current	I <sub>DD</sub>			35	65	μA
Control current	I <sub>CC</sub>			5	10	μA

<sup>1</sup> Performance is guaranteed only under the conditions listed in this table.

**Table 4. SKY13396-397LF Truth Table<sup>1</sup>**

CTRL1	State
1	PORT3 to PORT1, PORT4 to PORT2
0	PORT3 to PORT2, PORT4 to PORT1

<sup>1</sup> 1 = 1.35 to 3.1 V

0 = -0.20 to +0.45 V

Any state other than described in this table places the switch into an undefined state.

### Evaluation Board Description

The SKY13396-397LF Evaluation Board is used to test the performance of the SKY13396-397LF DPDT Switch.

An Evaluation Board schematic diagram is provided in Figure 3. An assembly drawing for the Evaluation Board is shown in Figure 4.

### Package Dimensions

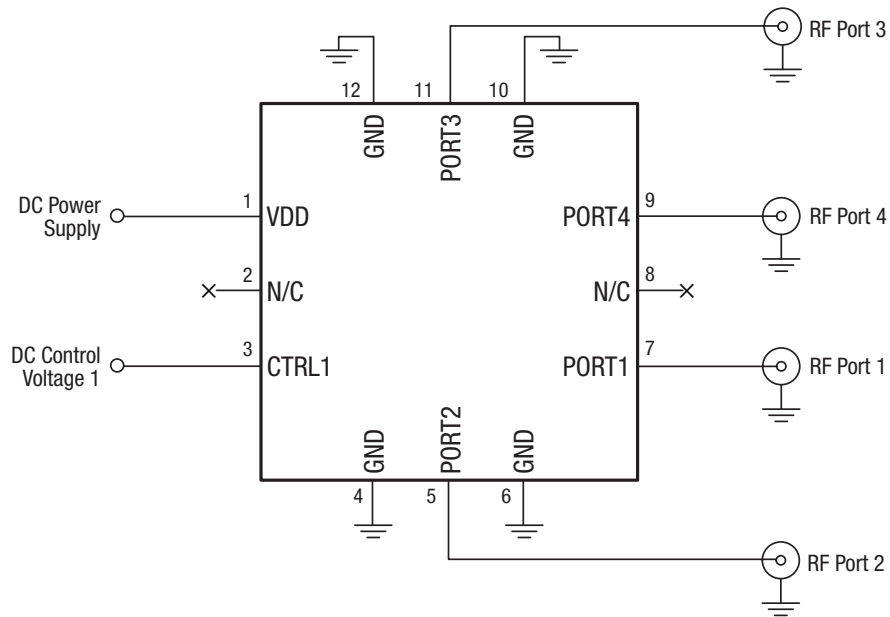
The PCB layout footprint for the SKY13396-397LF is provided in Figure 5. Typical part markings are shown in Figure 6. Package dimensions are shown in Figure 7, and tape and reel dimensions are provided in Figure 8.

### Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13396-397LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



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**Figure 3. SKY13396-397LF Evaluation Board Schematic**

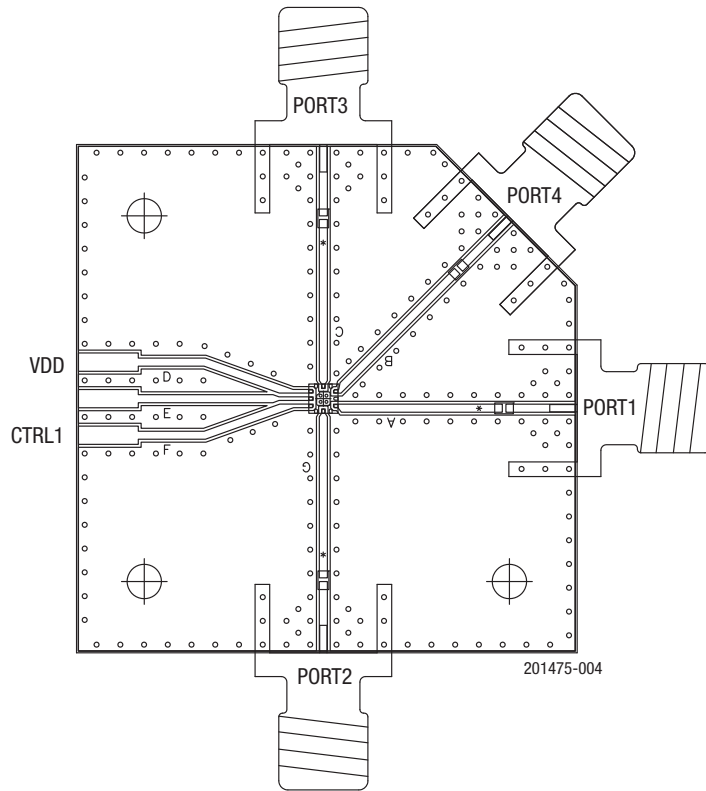
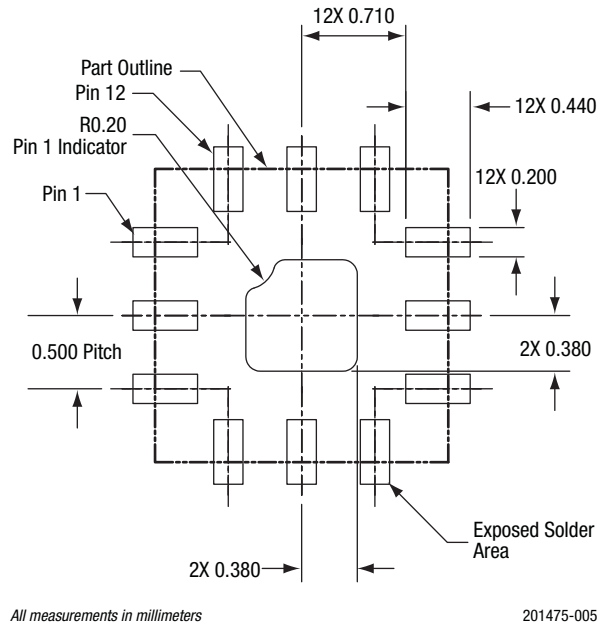


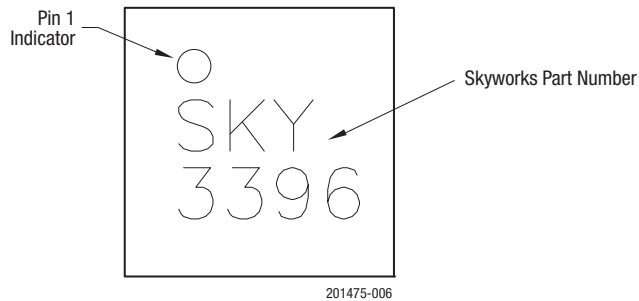
Figure 4. SKY13396-397LF Evaluation Board Assembly Diagram



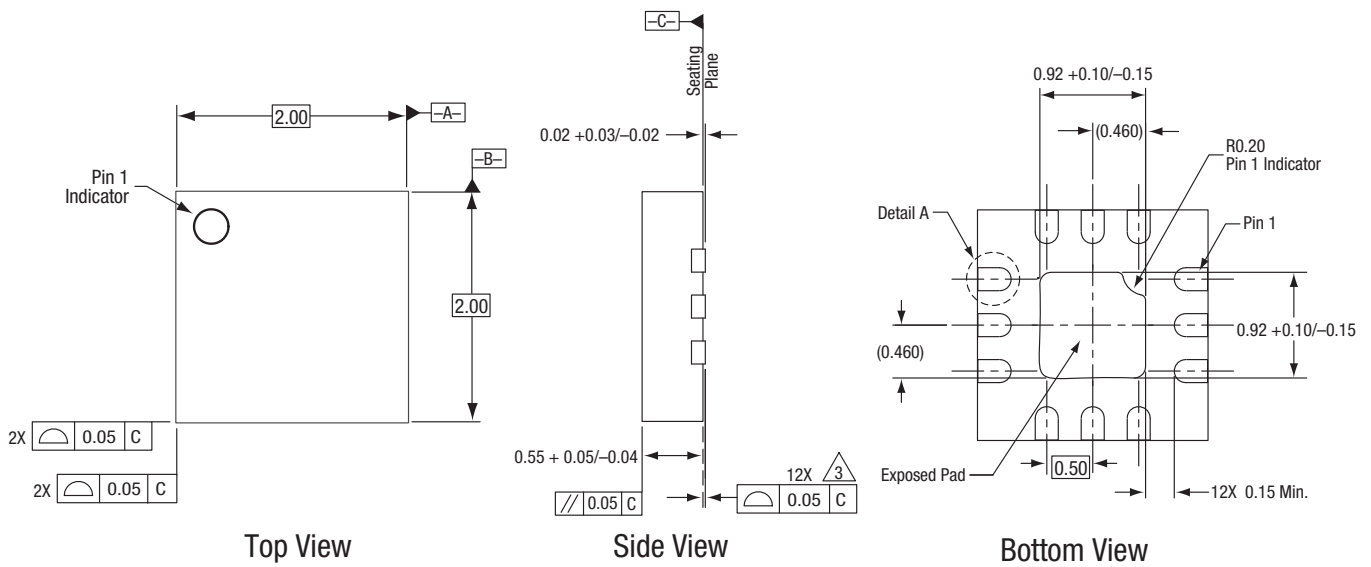
All measurements in millimeters

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Figure 5. SKY13396-397LF PCB Layout Footprint (Top View)

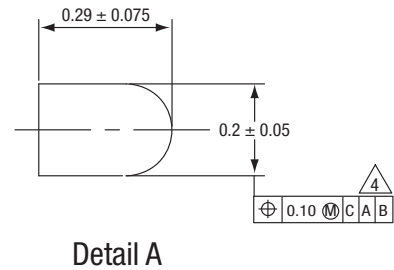


**Figure 6. Typical Part Markings (Top View)**



**Notes:**

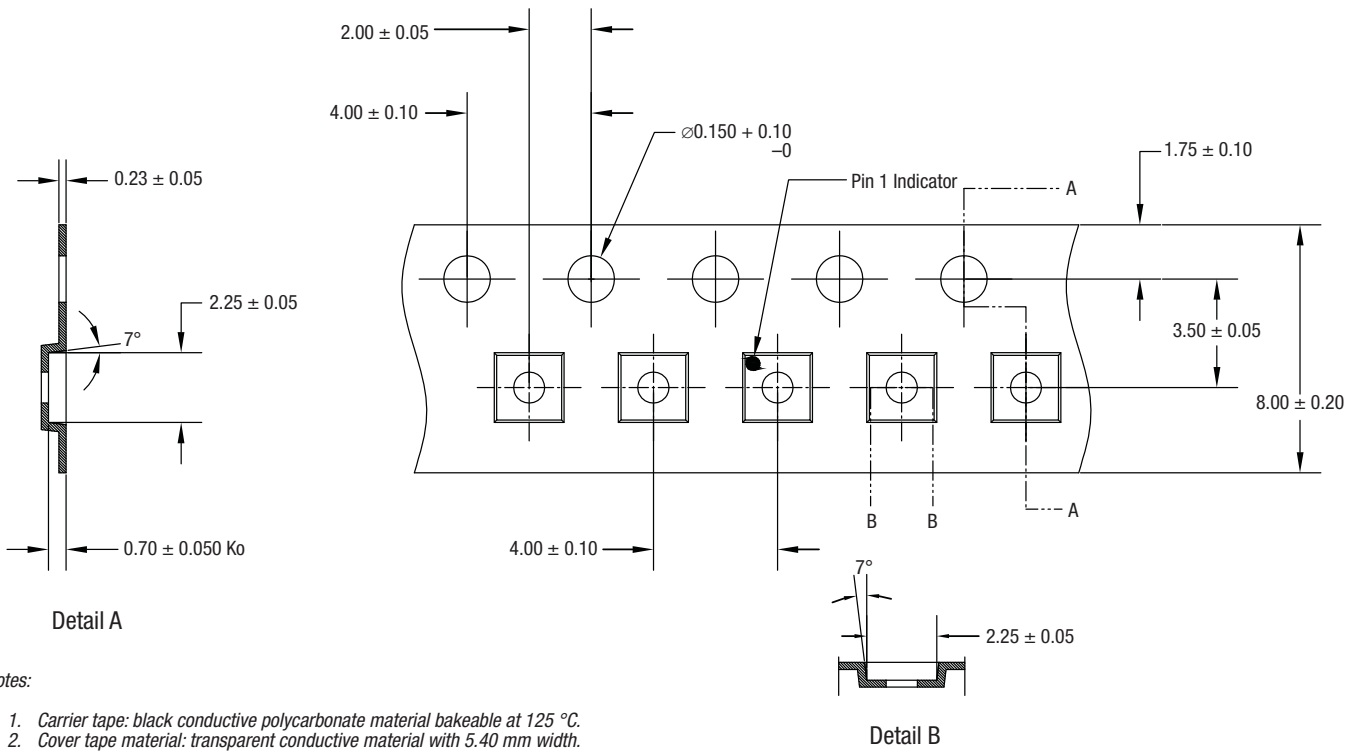
1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
3. Coplanarity applies to the terminals and all other bottom surface metallization.
4. Dimension applies to metallized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.



**Detail A**

201475-007

**Figure 7. SKY13396-397LF Package Dimensions**



Notes:

1. Carrier tape: black conductive polycarbonate material bakeable at 125 °C.
2. Cover tape material: transparent conductive material with 5.40 mm width.
3. ESD-surface resistivity must meet all ESD requirements of Skyworks specified on GP01-D232.
4. All dimensions are in millimeters.

201475-008

**Figure 8. SKY13396-397LF Tape and Reel Dimensions**

## Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13396-397LF: DPDT Switch	SKY13396-397LF	SKY13396-397LF-EVB

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