



**THE DATASHEET OF  
IR2117SPBF**



## IR2117(S)/IR2118(S) & (PbF)

### SINGLE CHANNEL DRIVER

#### Features

- Floating channel designed for bootstrap operation Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input (IR2117) or out of phase with input (IR2118)
- Also available LEAD-FREE

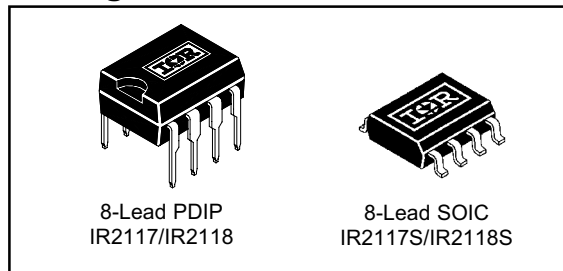
#### Description

The IR2117/IR2118(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 600 volts.

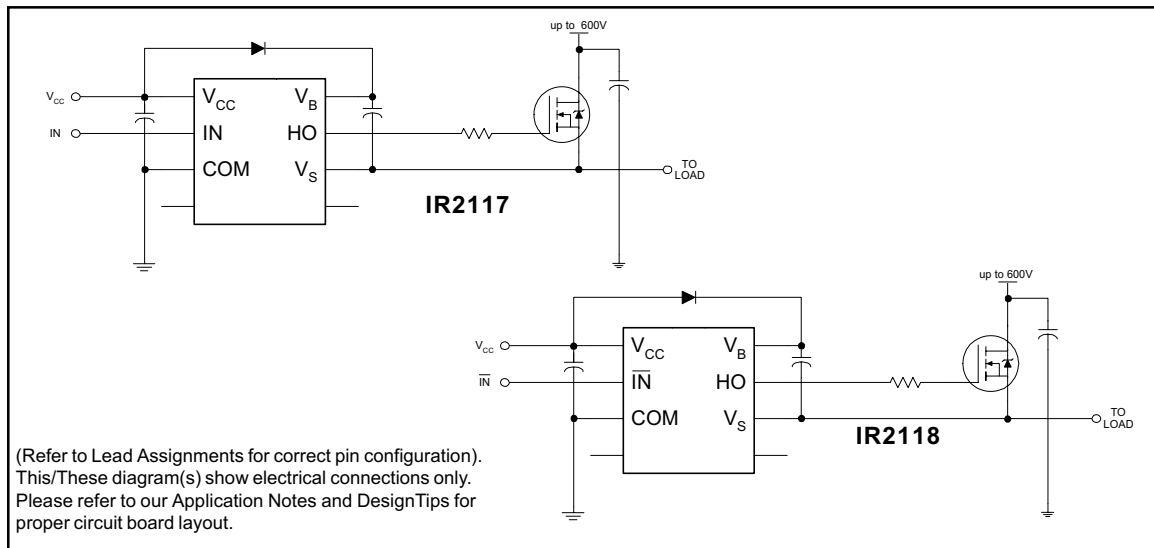
#### Product Summary

$V_{\text{OFFSET}}$	600V max.
$I_{\text{O}+/-}$	200 mA / 420 mA
$V_{\text{OUT}}$	10 - 20V
$t_{\text{on/off}}$ (typ.)	125 & 105 ns

#### Packages



#### Typical Connection



# IR2117(S)/IR2118(S) & (PbF)

International  
IR Rectifier

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 5 through 8.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating supply voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Logic supply voltage	-0.3	25		
V <sub>IN</sub>	Logic input voltage	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Logic supply voltage	10	20	
V <sub>IN</sub>	Logic input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	125	200	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	105	180		$V_S = 600V$
$t_r$	Turn-on rise time	—	80	130		
$t_f$	Turn-off fall time	—	40	65		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

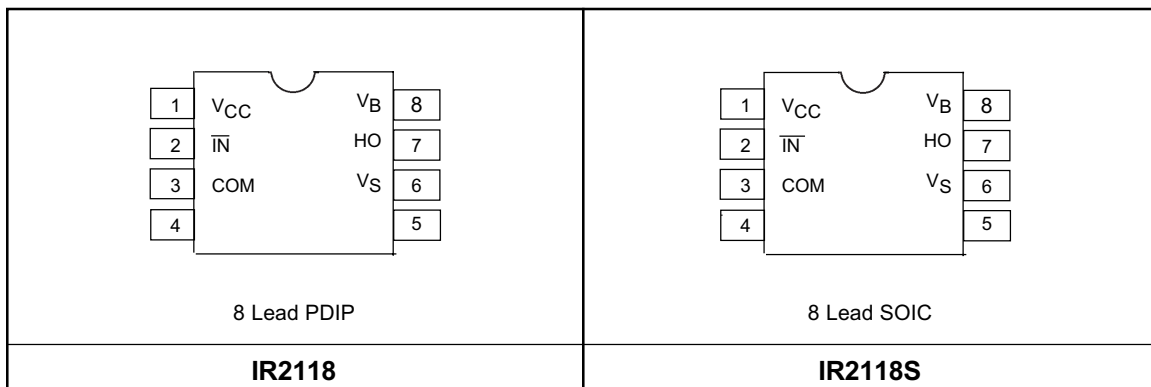
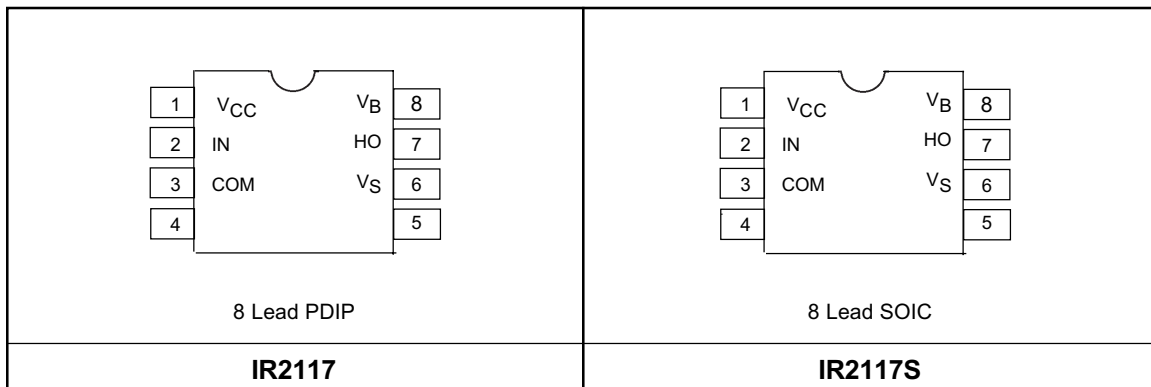
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	input voltage - logic "1" (IR2117) logic "0" (IR2118)	9.5	—	—	V	
$V_{IL}$	Input voltage - logic "0" (IR2117) logic "1" (IR2118)	—	—	6.0		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low level output voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	50	240		$V_{IN} = 0V$ or $V_{CC}$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	70	340		$V_{IN} = 0V$ or $V_{CC}$
$I_{IN+}$	Logic "1" input bias current (IR2117)	—	20	40		$V_{IN} = V_{CC}$
	(IR2118)					$V_{IN} = 0V$
$I_{IN-}$	Logic "0" input bias current (IR2117)	—	—	1.0		$V_{IN} = 0V$
	(IR2118)				$V_{IN} = V_{CC}$	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	7.6	8.6	9.6	V	
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.2	8.2	9.2		
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.6	8.6	9.6		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.2	8.2	9.2		
$I_{O+}$	Output high short circuit pulsed current	200	250	—	mA	$V_O = 0V$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	420	500	—		$V_O = 15V$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10 \mu s$



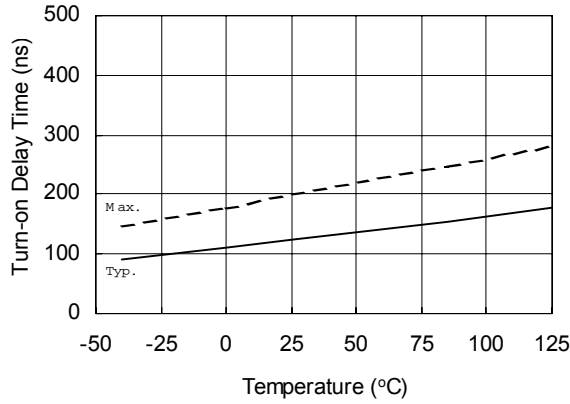
## Lead Definitions

Symbol	Description
V <sub>CC</sub>	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2117)
$\overline{\text{IN}}$	Logic input for gate driver output (HO), out of phase with HO (IR2118)
COM	Logic ground
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return

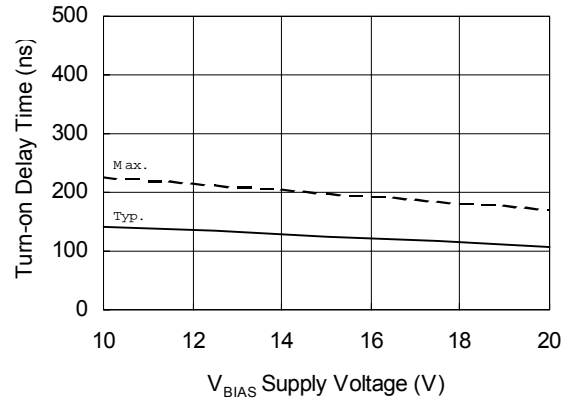
## Lead Assignments



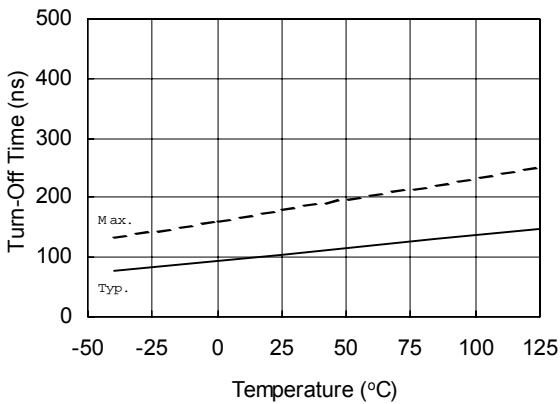




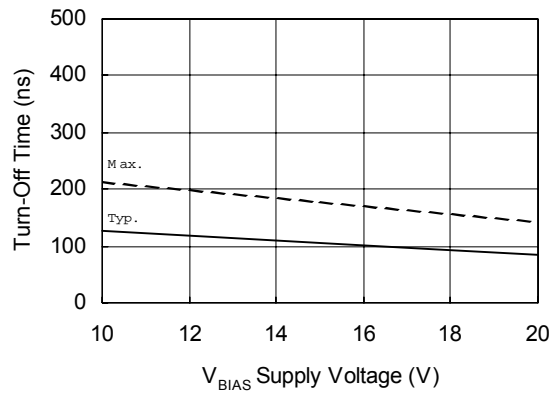
**Figure 4A. Turn-On Time vs. Temperature**



**Figure 4B. Turn-On Time vs. Supply Voltage**

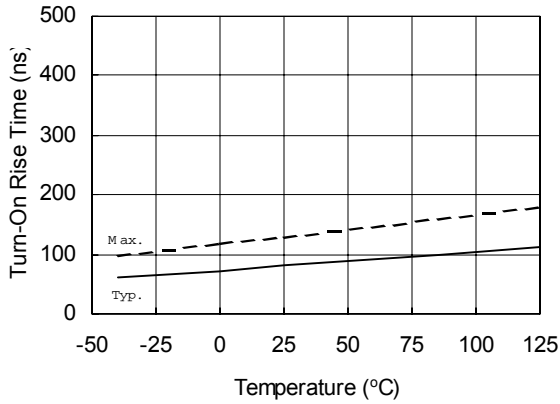


**Figure 5A. Turn-Off Time vs. Temperature**

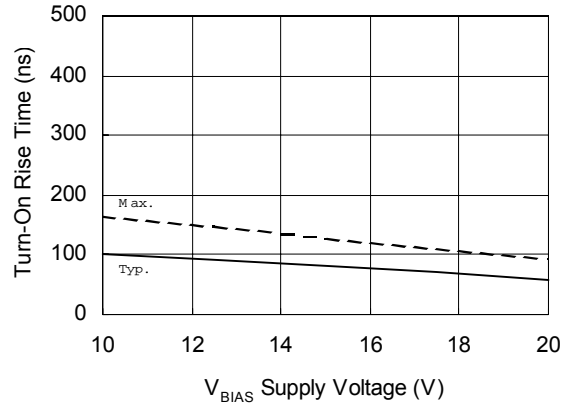


**Figure 5B. Turn-Off Time vs. Supply Voltage**

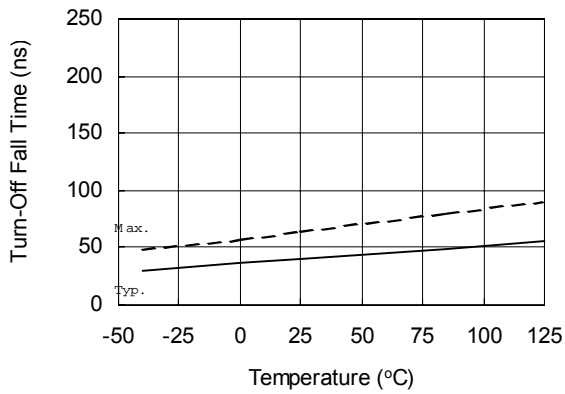
# IR2117(S)/IR2118(S) & (PbF)



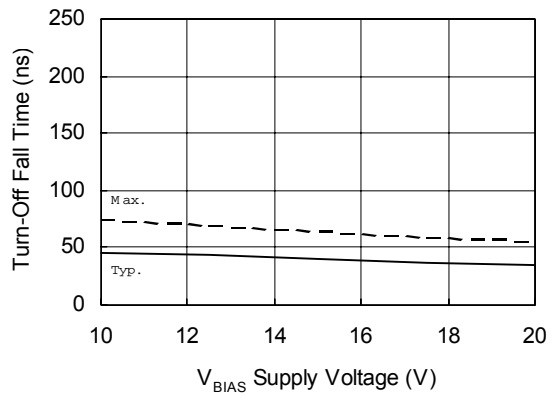
**Figure 6A. Turn-On Rise Time vs. Temperature**



**Figure 6B. Turn-On Rise Time vs. Supply Voltage**

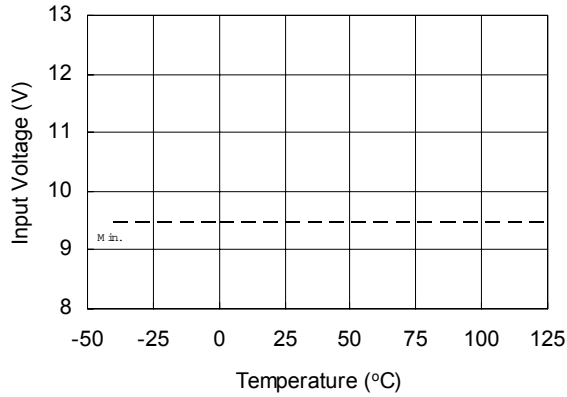


**Figure 7A. Turn-Off Fall Time vs. Temperature**

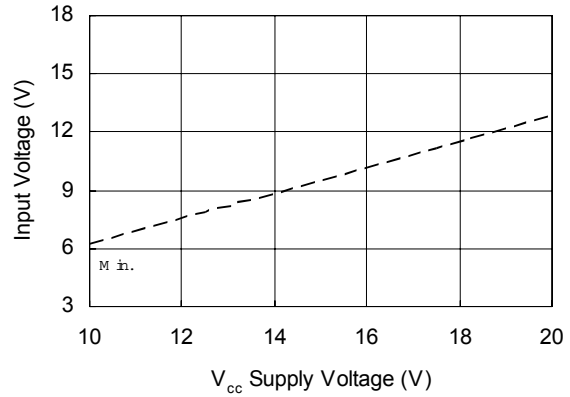


**Figure 7B. Turn-Off Fall Time vs. Supply Voltage**

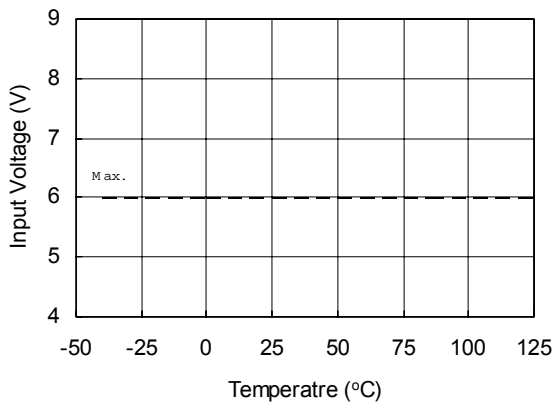
# IR2117(S)/IR2118(S) & (PbF)



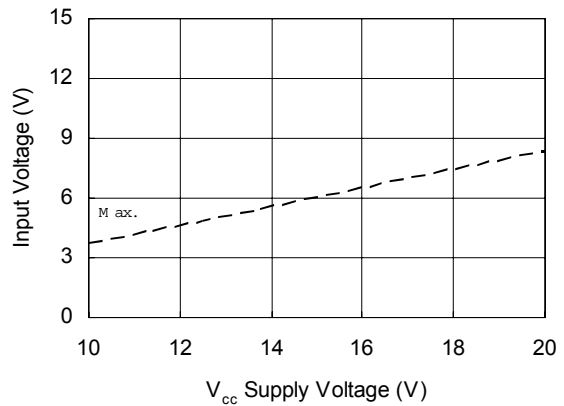
**Figure 8A. Logic "1" (IR2118 "0") Input Voltage vs. Temperature**



**Figure 8B. Logic "1" (IR2118 "0") Input Voltage vs. Supply Voltage**

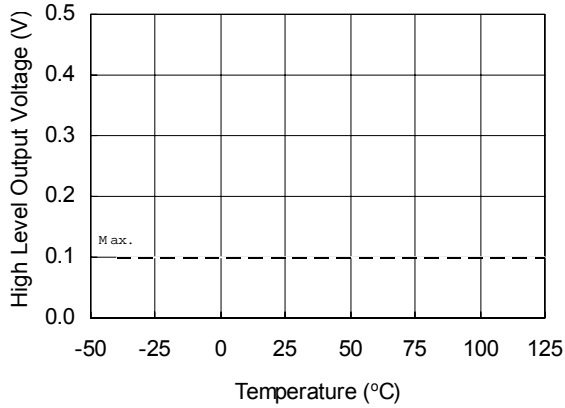


**Figure 9A. Logic "0" (IR2118 "1") Input Voltage vs. Temperature**

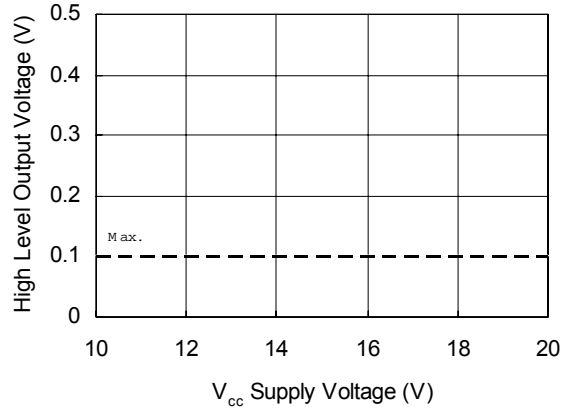


**Figure 9B. Logic "0" (IR2118 "1") Input Voltage vs. Supply Voltage**

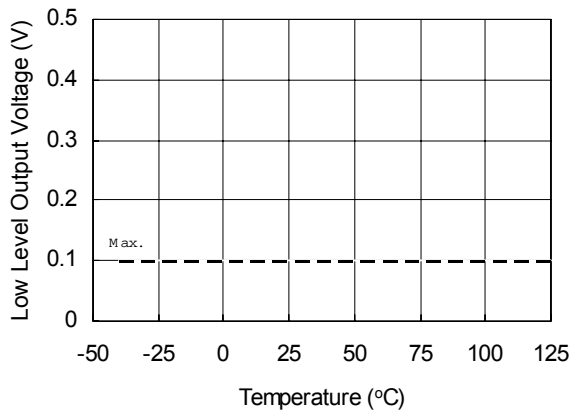
# IR2117(S)/IR2118(S) & (PbF)



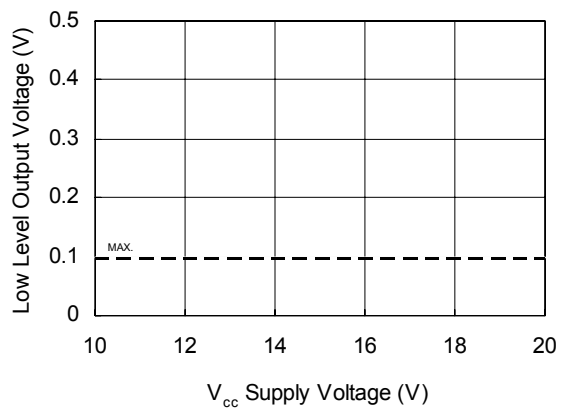
**Figure 10A. High Level Output vs. Temperature**



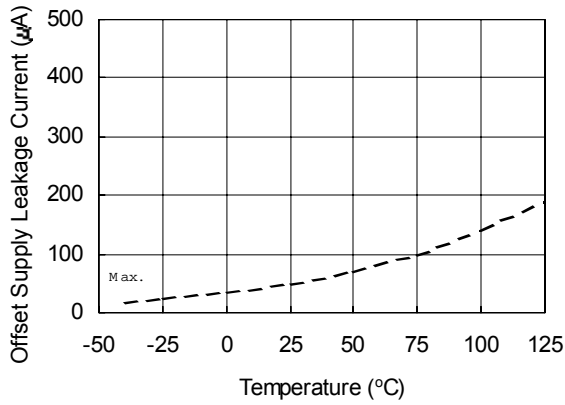
**Figure 10B. High Level Output vs. Supply Voltage**



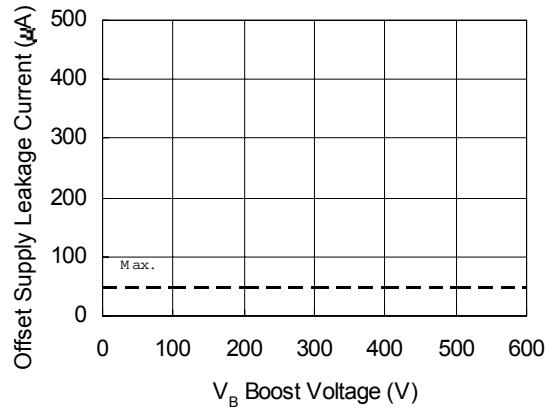
**Figure 11A. Low Level Output vs. Temperature**



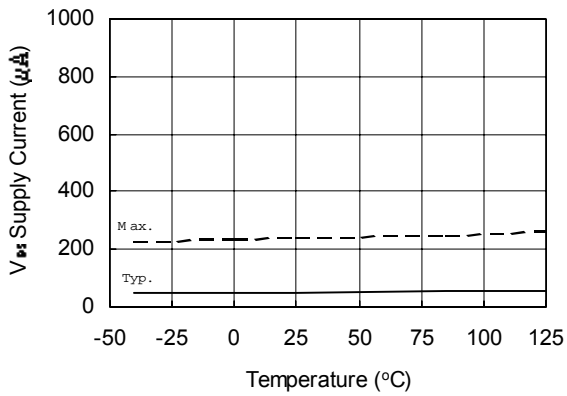
**Figure 11B. Low Level Output vs. Supply Voltage**



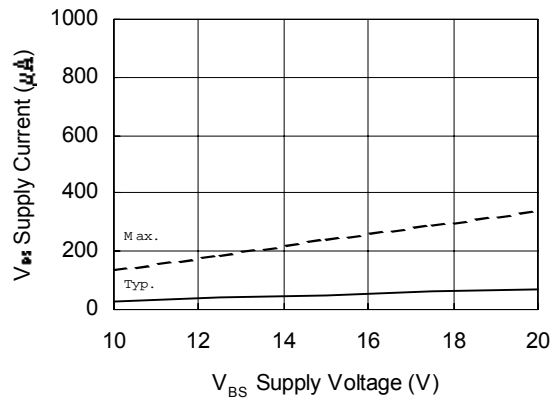
**Figure 12A. Offset Supply Leakage Current vs. Temperature**



**Figure 12B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage**

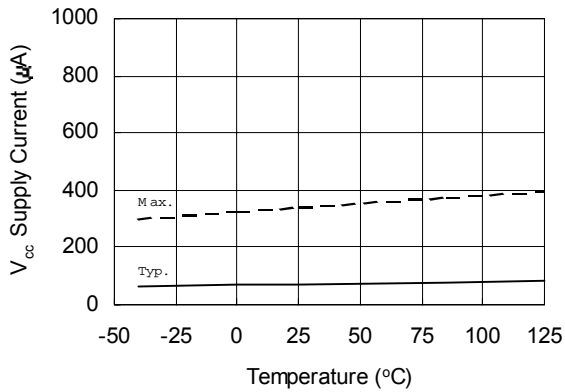


**Figure 13A. V<sub>BS</sub> Supply Current vs. Temperature**

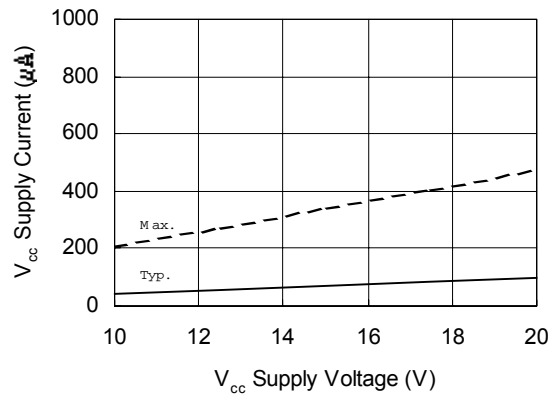


**Figure 13B. V<sub>BS</sub> Supply Current vs. Supply Voltage**

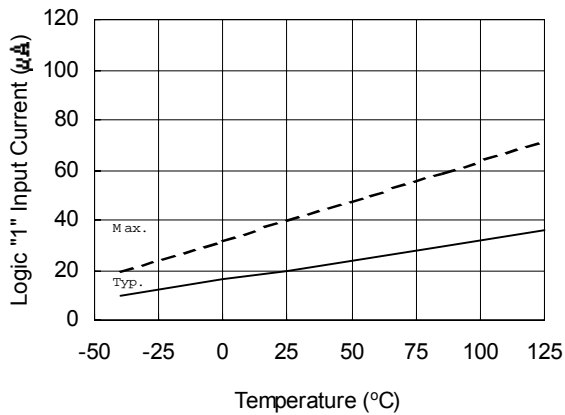
# IR2117(S)/IR2118(S) & (PbF)



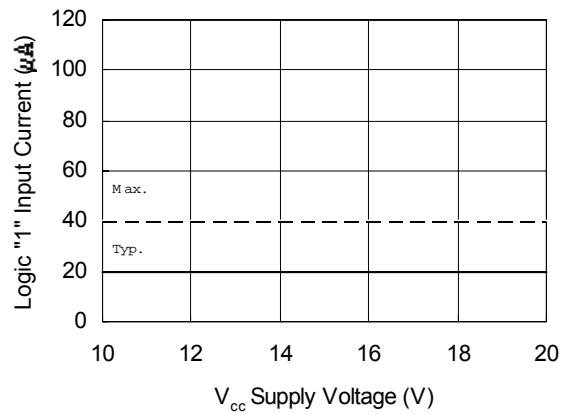
**Figure 14A. V<sub>cc</sub> Supply Current vs. Temperature**



**Figure 14B. V<sub>cc</sub> Supply Current vs. Supply Voltage**

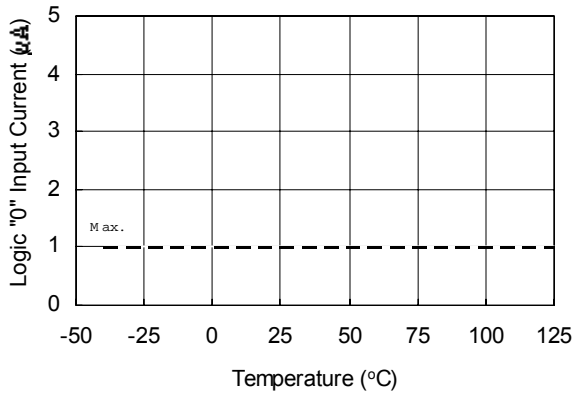


**Figure 15A. Logic "1" (2118 "0") Input Current vs. Temperature**

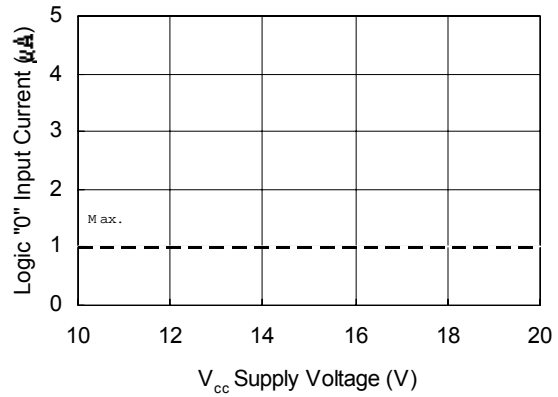


**Figure 15B. Logic "1" (2118 "0") Input Current vs. Supply Voltage**

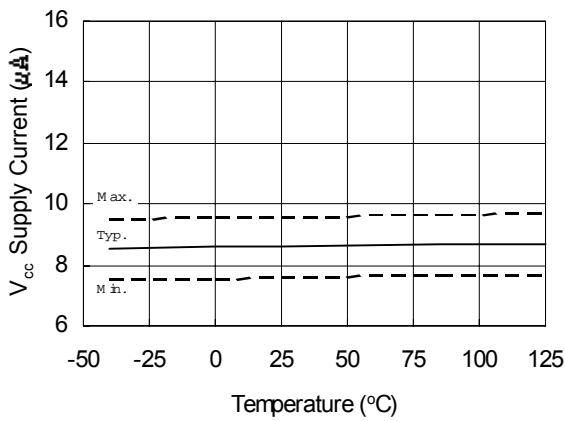
# IR2117(S)/IR2118(S) & (PbF)



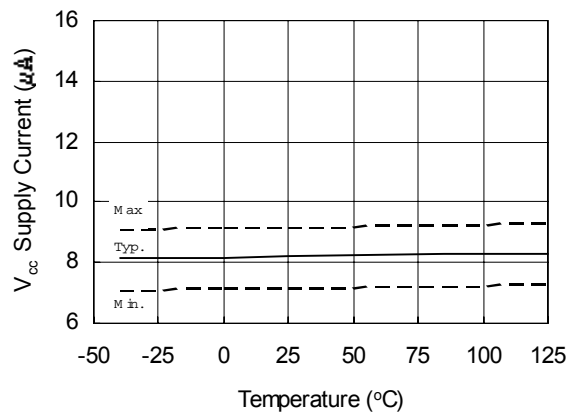
**Figure 16A. Logic "0" (2118"1") Input Current vs. Temperature**



**Figure 16B. Logic "0" (2118"1") Input Current vs. Supply Voltage**

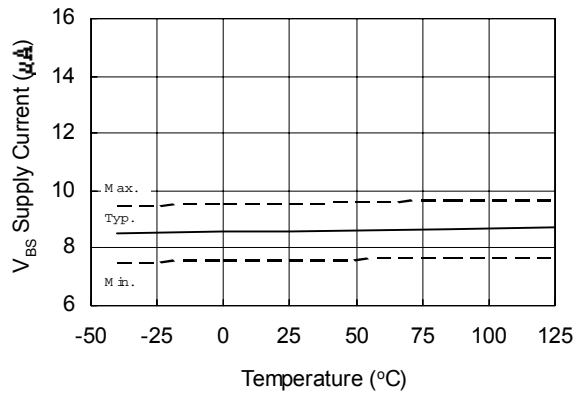


**Figure 17A. V<sub>cc</sub> Undervoltage Threshold (+) vs. Temperature**

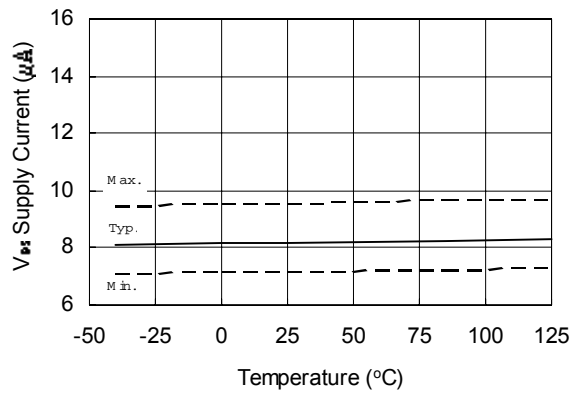


**Figure 18A. V<sub>cc</sub> Undervoltage Threshold (-) vs. Temperature**

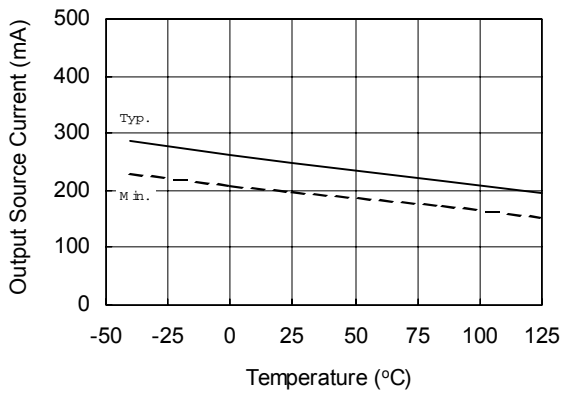
# IR2117(S)/IR2118(S) & (PbF)



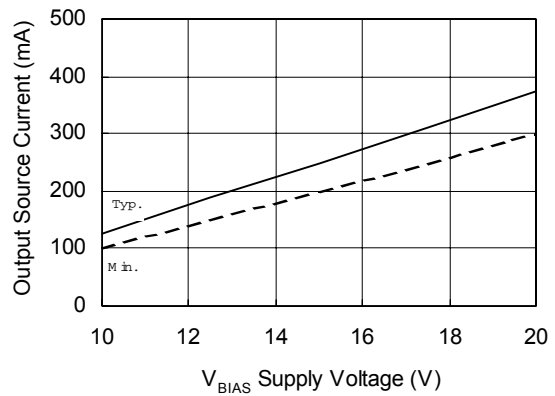
**Figure 19A.  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**



**Figure 20A.  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**

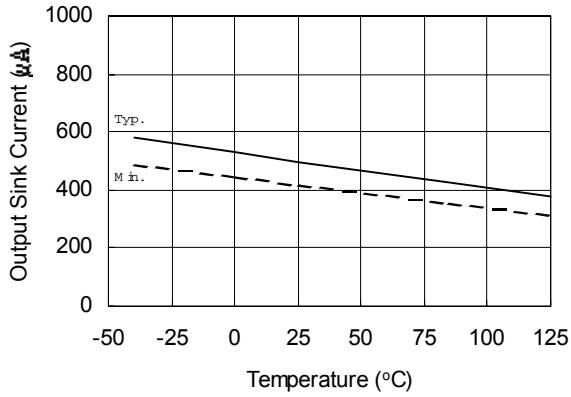


**Figure 21A. Output Source Current vs. Temperature**

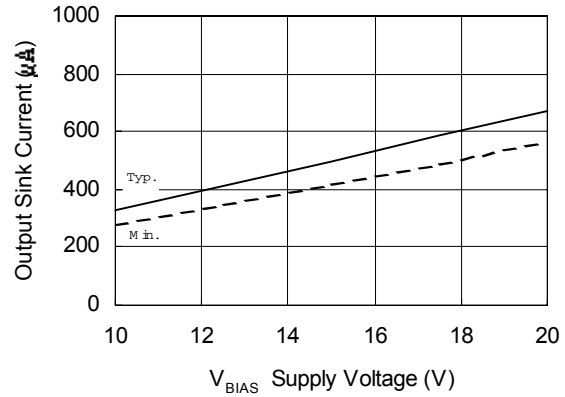


**Figure 21B. Output Source Current vs. Supply Voltage**

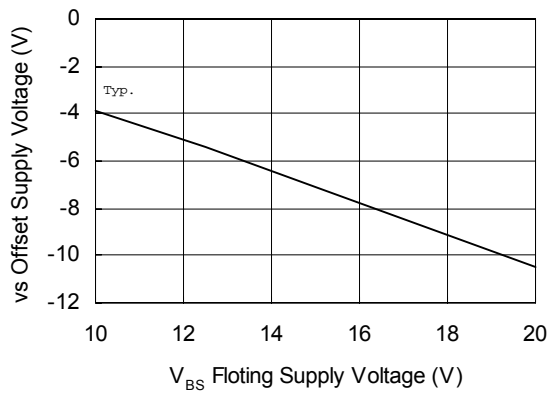
# IR2117(S)/IR2118(S) & (PbF)



**Figure 22A. Output Sink Current vs. Temperature**

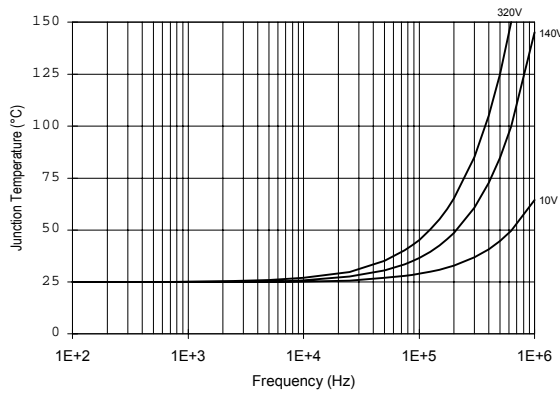


**Figure 22B. Output Sink Current vs. Supply Voltage**

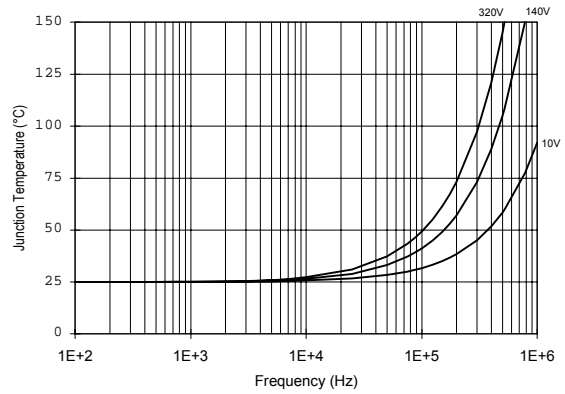


**Figure 23B. Maximum VS Negative Offset vs. Supply Voltage**

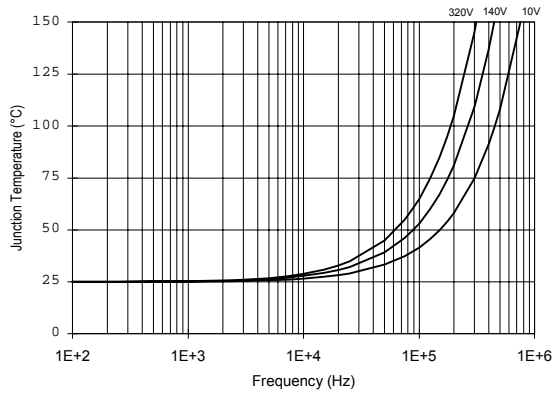
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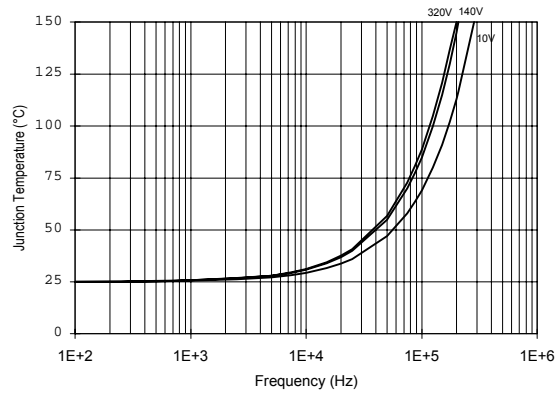
**Figure 24. IR2117/IR2118  $T_J$  vs. Frequency (IRFBC20)**  
 $R_{GATE} = 33\Omega$ ,  $V_{CC} = 15V$



**Figure 25. IR2117/IR2118  $T_J$  vs. Frequency (IRFBC30)**  
 $R_{GATE} = 22\Omega$ ,  $V_{CC} = 15V$



**Figure 26. IR2117/IR2118  $T_J$  vs. Frequency (IRFBC40)**  
 $R_{GATE} = 15\Omega$ ,  $V_{CC} = 15V$



**Figure 27. IR2117/IR2118  $T_J$  vs. Frequency (IRFPE50)**  
 $R_{GATE} = 10\Omega$ ,  $V_{CC} = 15V$

# IR2117(S)/IR2118(S) & (PbF)

## Case outlines

Technical drawing of an 8-Lead PDIP package. The top view shows dimensions: 10.92 [.430] and 8.84 [.348] for the body width, and 7.11 [.280] and 6.10 [.240] for the lead width. Lead pitch is 1.27 [.050]. Lead height is 5.33 [.210] MAX. Lead diameter is 0.558 [.022] and 0.356 [.014]. Lead length is 7.62 [.300]. Lead angle is 8X 0° - 15°. Lead thickness is 0.381 [.015] and 0.204 [.008]. Datum A is at the top edge, datum B is at the lead centerline, and datum C is at the lead base. Tolerances are shown in brackets.

NOTES:  
 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].  
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.  
 ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.  
 ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

01-6014  
01-3003 01 (MS-001AB)

**8-Lead PDIP**

Technical drawing of an 8-Lead SOIC package. The top view shows dimensions: 6.46 [.255] for the body width, 8X 0.72 [.028] for the lead width, and 8X 1.78 [.070] for the lead pitch. Lead height is 0.10 [.004]. Lead length is 8X L. Lead angle is 8X 45°. Lead thickness is 0.381 [.015] and 0.204 [.008]. Datum A is at the top edge, datum B is at the lead centerline, and datum C is at the lead base. Tolerances are shown in brackets.

FOOTPRINT

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:  
 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.  
 2. CONTROLLING DIMENSION: MILLIMETER  
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].  
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.  
 ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.15 [.006].  
 ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.25 [.010].  
 ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

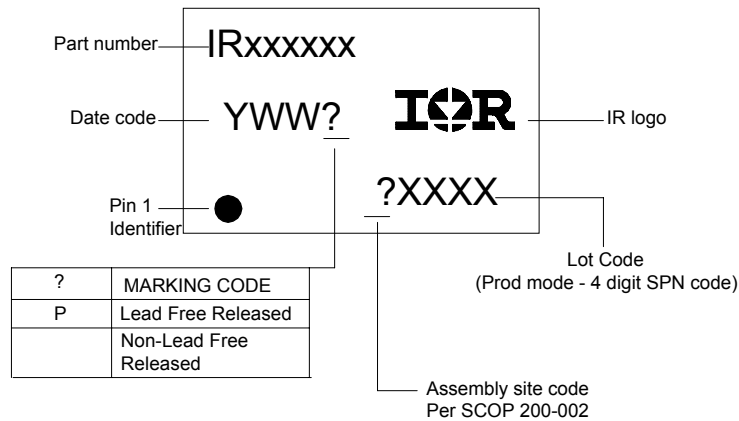
01-6027

**8-Lead SOIC**

# IR2117(S)/IR2118(S) & (PbF)

International  
**IR** Rectifier

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

8-Lead PDIP IR2117 order IR2117  
 8-Lead PDIP IR2118 order IR2118  
 8-Lead SOIC IR2117S order IR2117S  
 8-Lead SOIC IR2118S order IR2118S

### Leadfree Part

8-Lead PDIP IR2117 order IR2117PbF  
 8-Lead PDIP IR2118 order IR2118PbF  
 8-Lead SOIC IR2117S order IR2117SPbF  
 8-Lead SOIC IR2118S order IR2118SPbF

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105  
**This product has been qualified per industrial level**  
 Data and specifications subject to change without notice. 5/14/2007

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

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 [Infineon Technologies](#) Information

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