THE DATASHEET OF

EL5202IYZ-T13

Data Sheet | January 17, 2008 | FN7331.8

400MHz Slew Enhanced VFAs

The EL5x02 and EL5x03 families represent high-speed VFAs based on a CFA amplifier architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. With slew rates of 3500V/µs, this family of devices enables the use of voltage feedback amplifiers in a space where the only alternative has been current feedback amplifiers. This family will also be available in single, dual, and triple versions, with 200MHz, 400MHz, and 750MHz versions. These are all available in single, dual, and triple versions.

Both families operate on single 5V or ±5V supplies from minimum supply current. EL5x02 also features an output enable function, which can be used to put the output in to a high-impedance mode. This enables the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

Typical applications for these families will include cable driving, filtering, A/D and D/A buffering, multiplexing and summing within video, communications, and instrumentation designs.

Features

- Operates off 3V, 5V, or ±5V applications
- Power-down to 0µA (EL5x02)
- -3dB bandwidth = 400MHz
- ±0.1dB bandwidth = 50MHz
- Low supply current = 5mA
- Slew rate = 3500V/µs
- Low offset voltage = 5mV max
- Output current = 140mA
- A_{VOL} = 2000
- Differential gain/phase = 0.01%/0.01°
- Pb-free available (RoHS compliant)

Applications

- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Ordering Information

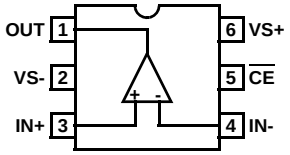
PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL5102IS	5102IS	8 Ld SOIC (150 mil)	MDP0027
EL5102IS-T7*	5102IS	8 Ld SOIC (150 mil)	MDP0027
EL5102IS-T13*	5102IS	8 Ld SOIC (150 mil)	MDP0027
EL5102ISZ (Note)	5102ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5102ISZ-T7* (Note)	5102ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5102ISZ-T13* (Note)	5102ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5102IW-T7*	q	6 Ld SOT-23	MDP0038
EL5102IW-T7A*	q	6 Ld SOT-23	MDP0038
EL5102IWZ-T7* (Note)	BBSA	6 Ld SOT-23 (Pb-free)	MDP0038
EL5102IWZ-T7A* (Note)	BBSA	6 Ld SOT-23 (Pb-free)	MDP0038
EL5103IC	B	5 Ld SC-70	P5.049
EL5103IC-T7*	B	5 Ld SC-70	P5.049
EL5103IC-T7A*	B	5 Ld SC-70	P5.049
EL5103IW-T7*	g	5 Ld SOT-23	MDP0038
EL5103IW-T7A*	g	5 Ld SOT-23	MDP0038
EL5103IWZ-T7*	BBTA	5 Ld SOT-23 (Pb-free)	MDP0038
EL5103IWZ-T7A*	BBTA	5 Ld SOT-23 (Pb-free)	MDP0038
EL5202IY	BRAAA	10 Ld MSOP (3.0mm)	MDP0043
EL5202IY-T7*	BRAAA	10 Ld MSOP (3.0mm)	MDP0043
EL5202IY-T13*	BRAAA	10 Ld MSOP (3.0mm)	MDP0043
EL5202IYZ (Note)	BAAAD	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5202IYZ-T7* (Note)	BAAAD	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5202IYZ-T13* (Note)	BAAAD	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5203IS	5203IS	8 Ld SOIC (150 mil)	MDP0027
EL5203IS-T7*	5203IS	8 Ld SOIC (150 mil)	MDP0027
EL5203IS-T13*	5203IS	8 Ld SOIC (150 mil)	MDP0027
EL5203ISZ (Note)	5203ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5203ISZ-T7* (Note)	5203ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5203ISZ-T13* (Note)	5203ISZ	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5203IY	BSAAA	8 Ld MSOP (3.0mm)	MDP0043
EL5203IY-T7*	BSAAA	8 Ld MSOP (3.0mm)	MDP0043
EL5203IY-T13*	BSAAA	8 Ld MSOP (3.0mm)	MDP0043
EL5203IYZ (Note)	BAAAE	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5203IYZ-T7* (Note)	BAAAE	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5203IYZ-T13* (Note)	BAAAE	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5302IU	5302IU	16 Ld QSOP (150 mil)	MDP0040
EL5302IU-T7*	5302IU	16 Ld QSOP (150 mil)	MDP0040
EL5302IU-T13*	5302IU	16 Ld QSOP (150 mil)	MDP0040
EL5302IUZ (Note)	5302IUZ	16 Ld QSOP (150 mil) (Pb-free)	MDP0040
EL5302IUZ-T7* (Note)	5302IUZ	16 Ld QSOP (150 mil) (Pb-free)	MDP0040
EL5302IUZ-T13* (Note)	5302IUZ	16 Ld QSOP (150 mil) (Pb-free)	MDP0040

* Please refer to TB347 for details on reel specifications.

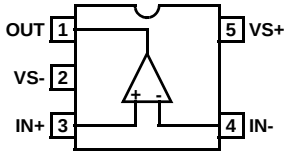
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

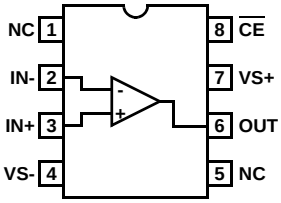
EL5102
(6 LD SOT-23)
TOP VIEW



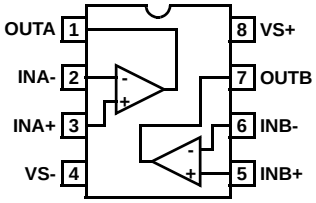
EL5103
(5 LD SOT-23)
TOP VIEW



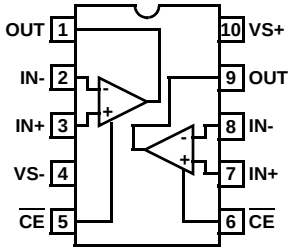
EL5102
(8 LD SOIC)
TOP VIEW



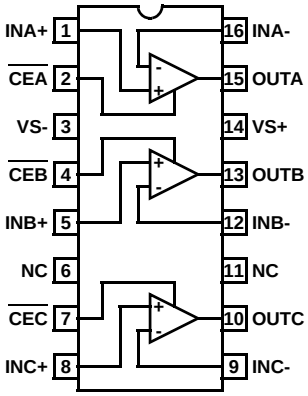
EL5203
(8 LD SOIC, MSOP)
TOP VIEW



EL5202
(10 LD MSOP)
TOP VIEW



EL5302
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and GND 13.2V
Maximum Supply Slewrate between V_S+ and V_S- 1V/µs
Input Voltage . . . . . .$\pm V_S$
Differential Input Voltage . . . . . .±4V
Maximum Continuous Output Current 80mA
Maximum Current into I_N+, I_N-, $\overline{CE}$ . . . . . ±5mA

Thermal Information

Power Dissipation . . . . . See Curves
Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature Range . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = +25°C, R_L = 500Ω, V_{ENABLE} = +5V, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage	EL5102, EL5103, EL5202, EL5203		1	5	mV
		EL5302		2	8	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		10		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-12	2	12	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-8	1	8	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		50		nA/°C
PSRR	Power Supply Rejection Ratio	V_S = ±4.75V to ±5.25V	-70	-80		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = -3V to 3.0V	-60	-80		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3	±3.3	3	V
R_{IN}	Input Resistance	Common mode	200	400		kΩ
C_{IN}	Input Capacitance	SO package		1		pF
$I_{S,ON}$	Supply Current - Enabled Per Amplifier		4.6	5.2	5.8	mA
$I_{S,OFF}$	Supply Current - Shut-down Per Amplifier	V_S+	+1	+9	+25	µA
		V_S-	-25	-13	-1	µA
AVOL	Open Loop Gain	V_{OUT} = ±2.5V, R_L = 1kΩ to GND	58	66		dB
		V_{OUT} = ±2.5V, R_L = 150Ω to GND		60		dB
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to GND	±3.5	±3.9		V
		R_L = 150Ω to GND	±3.4	±3.7		V
I_{OUT}	Output Current	A_V = 1, R_L = 10Ω to 0V	±80	±150		mA
$V_{\overline{CE}}$-ON	$\overline{CE}$ Pin Voltage for Power-up		(V_S+) -5		(V_S+) -3	V
$V_{\overline{CE}}$-OFF	$\overline{CE}$ Pin Voltage for Shut-down		(V_S+) -1		V_S+	V
I_{EN}-ON	Pin Current - Enabled	$\overline{CE}$ = 0V	-1	0	+1	µA
I_{EN}-OFF	Pin Current - Disabled	$\overline{CE}$ = +5V	1	14	25	µA

Closed Loop AC Electrical Specifications

$V_S+ = +5V$, $V_S- = -5V$, $T_A = +25°C$, $V_{ENABLE} = +5V$, $A_V = +1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND Pin, Unless Otherwise Specified. (Note 1)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth (V_{OUT} = 400mV_{P-P})	$A_V = 1$, $R_F = 0\Omega$		400		MHz
SR	Slew Rate	$A_V = +2$, $R_L = 100\Omega$, V_{OUT} = -3V to +3V	1100	2200	5000	V/µs
		$R_L = 500\Omega$, V_{OUT} = -3V to +3V		4000		V/µs
t_R,t_F	Rise Time, Fall Time	±0.1V step		2.8		ns
OS	Overshoot	±0.1V step		10		%
t_S	0.1% Settling Time	$V_S = ±5V$, $R_L = 500\Omega$, $A_V = 1$, $V_{OUT} = ±3V$		20		ns
dG	Differential Gain (Note 2)	$A_V = 2$, $R_F = 1k\Omega$		0.01		%
dP	Differential Phase (Note 2)	$A_V = 2$, $R_F = 1k\Omega$		0.01		°
e_N	Input Noise Voltage	f = 10kHz		12		nV/$\sqrt{Hz}$
i_N	Input Noise Current	f = 10kHz		11		pA/$\sqrt{Hz}$
t_{DIS}	Disable Time (Note 3)			50		ns
t_{EN}	Enable Time (Note 3)			25		ns

NOTES:

1. All AC tests are performed on a “warmed up” part, except slew rate, which is pulse tested.
2. Standard NTSC signal = 286mV_{P-P}, f = 3.58MHz, as V_{IN} is swept from 0.6V to 1.314V.R_L is DC coupled.
3. Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.

Typical Performance Curves

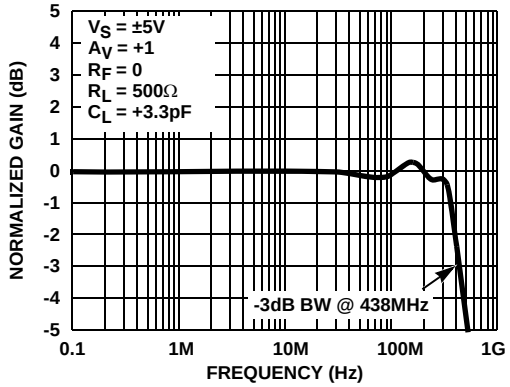


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

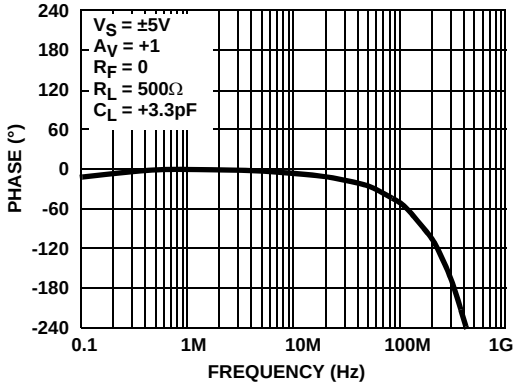


FIGURE 2. PHASE vs FREQUENCY

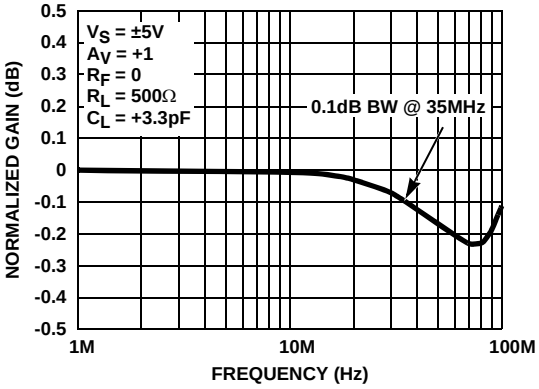


FIGURE 3. 0.1dB BANDWIDTH

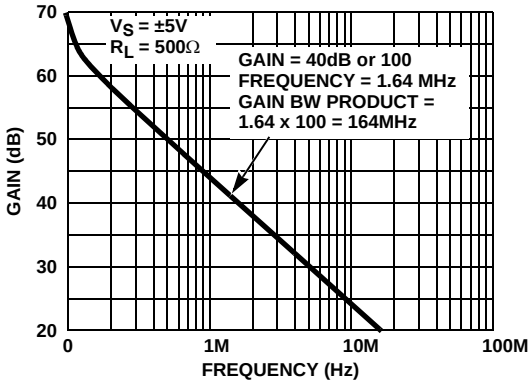


FIGURE 4. GAIN BANDWIDTH PRODUCT

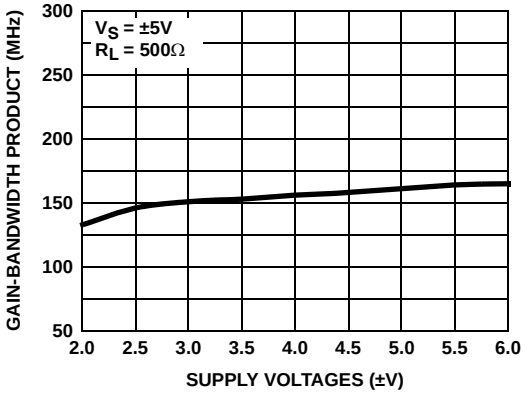


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

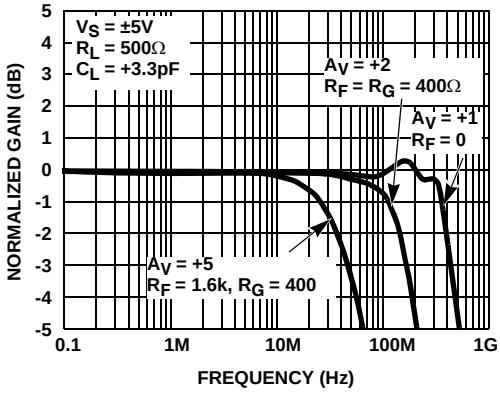


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS +A_V

Typical Performance Curves (Continued)

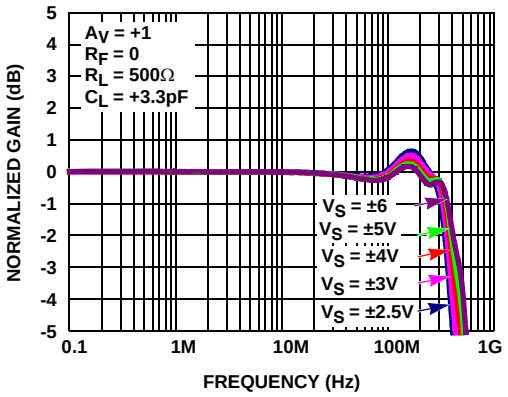


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS ±V_S

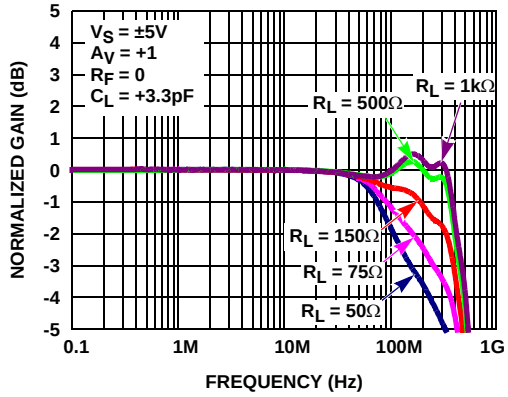


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +1)

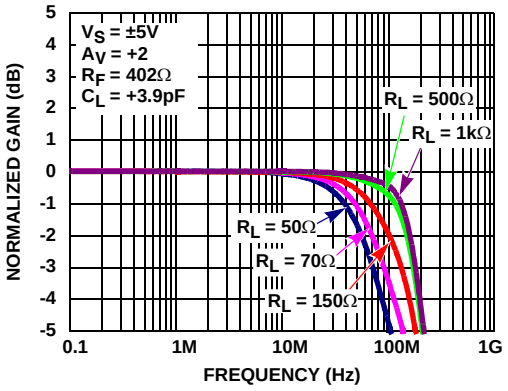


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +2)

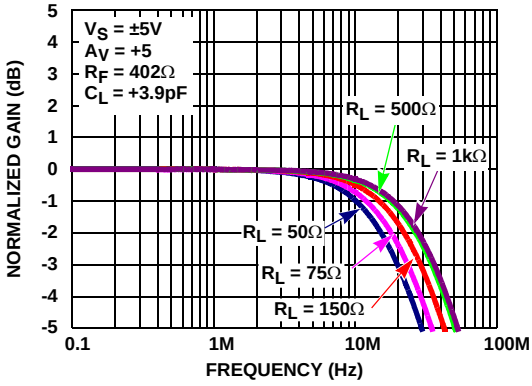


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +5)

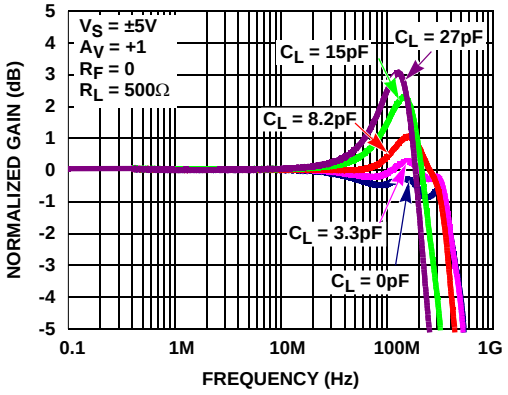


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +1)

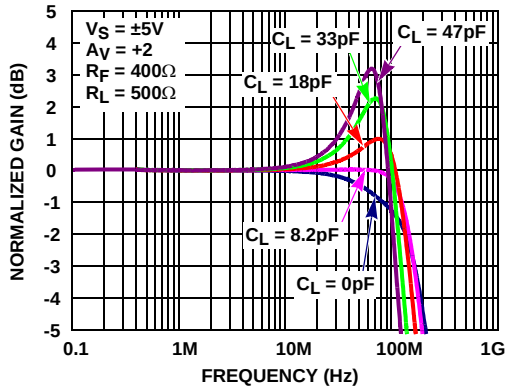


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +2)

Typical Performance Curves (Continued)

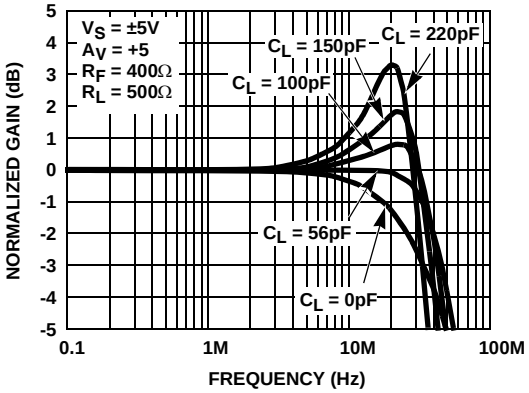


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +5)

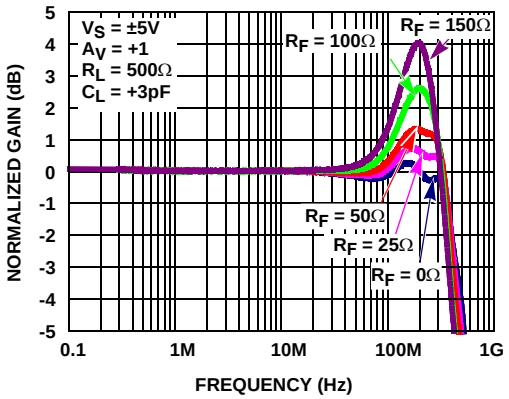


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +1)

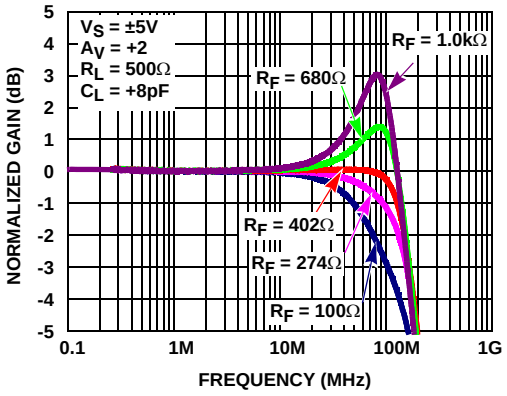


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +2)

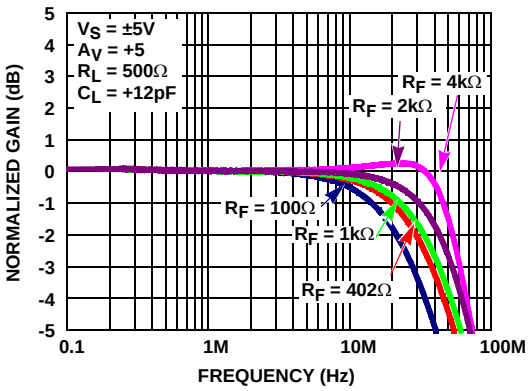


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +5)

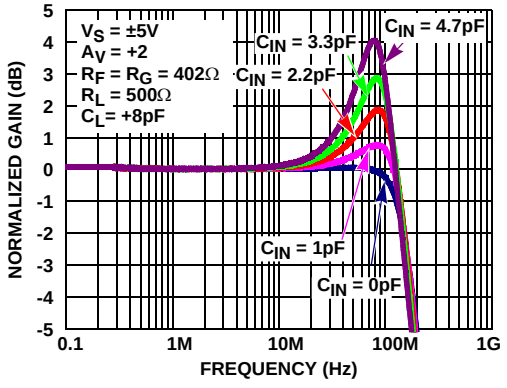


FIGURE 17. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +2)

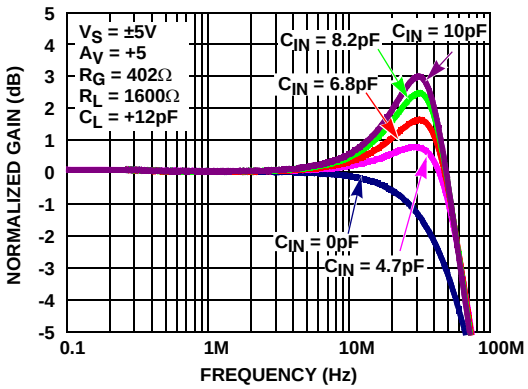


FIGURE 18. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +5)

Typical Performance Curves (Continued)

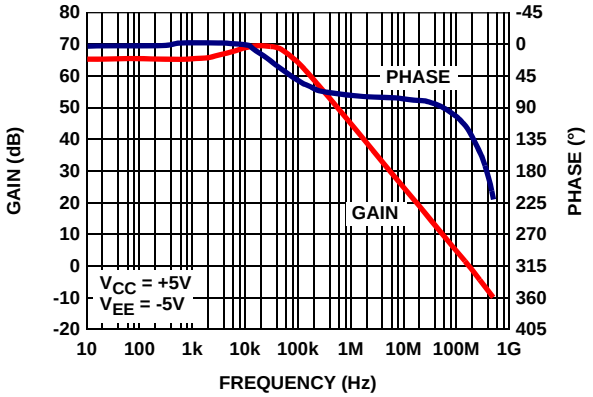


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

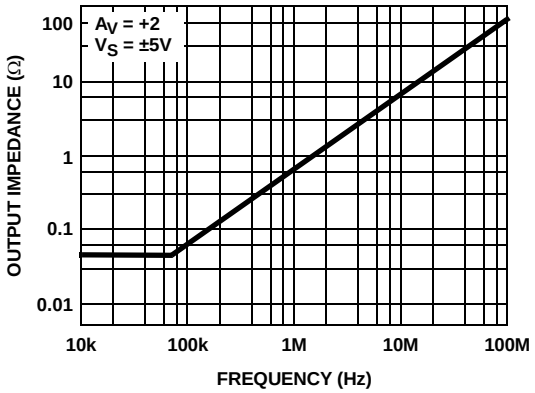


FIGURE 20. OUTPUT IMPEDANCE/PHASE vs FREQUENCY

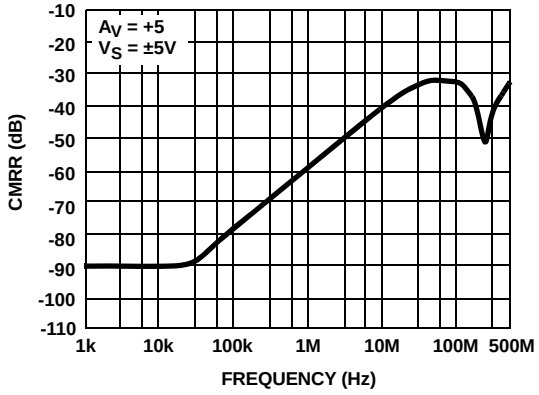


FIGURE 21. CMRR vs FREQUENCY

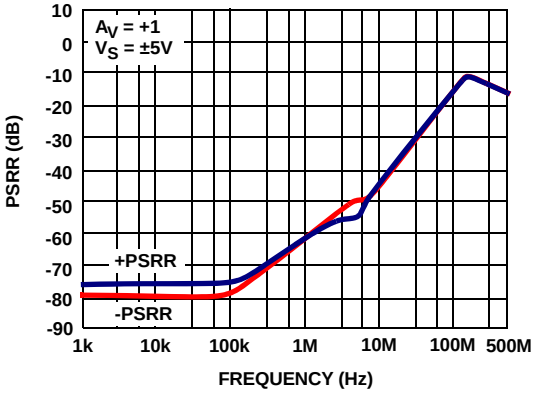


FIGURE 22. PSRR vs FREQUENCY

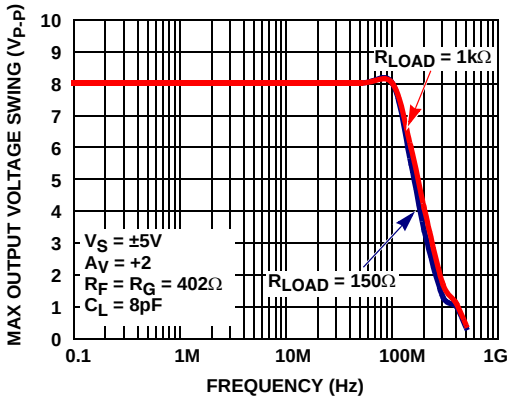


FIGURE 23. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

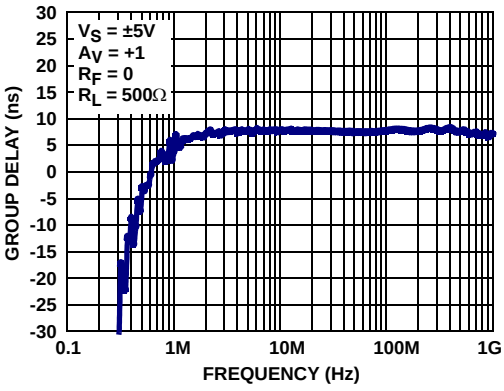


FIGURE 24. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

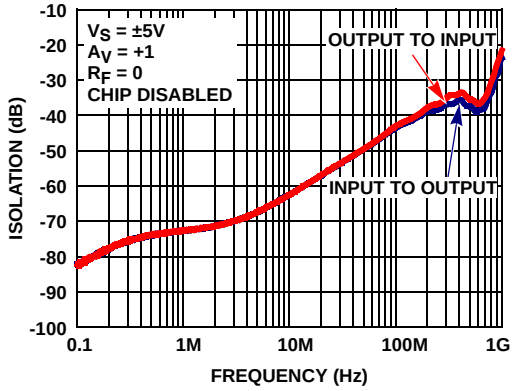


FIGURE 25. INPUT AND OUTPUT ISOLATION

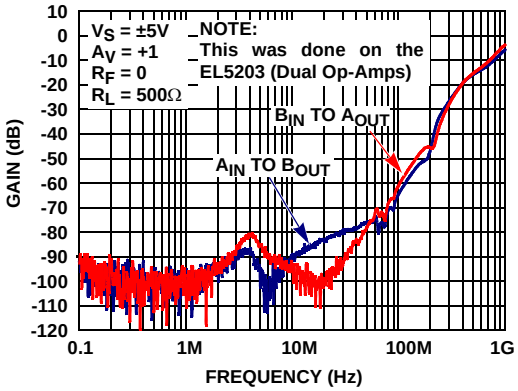


FIGURE 26. CHANNEL-TO-CHANNEL ISOLATION

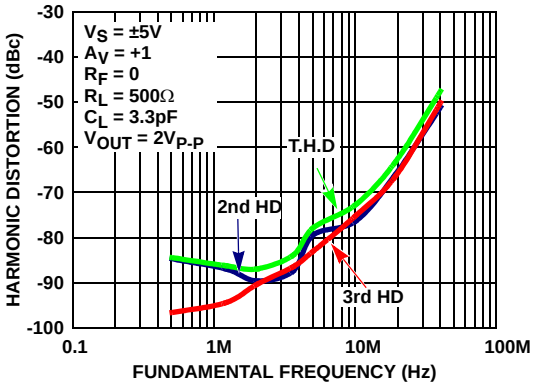


FIGURE 27. HARMONIC DISTORTION vs FREQUENCY

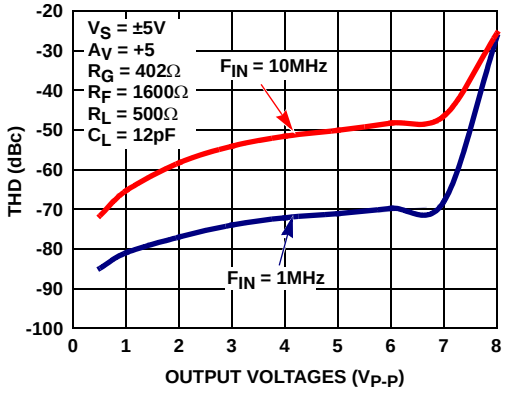


FIGURE 28. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

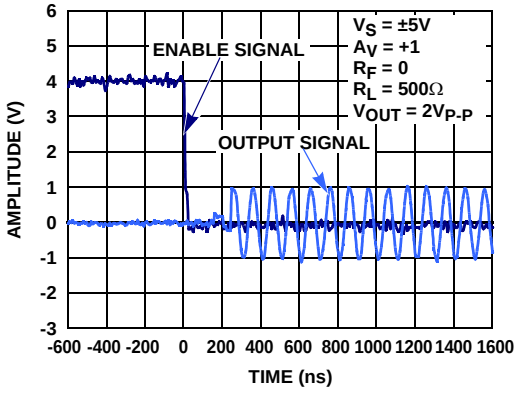


FIGURE 29. TURN-ON TIME

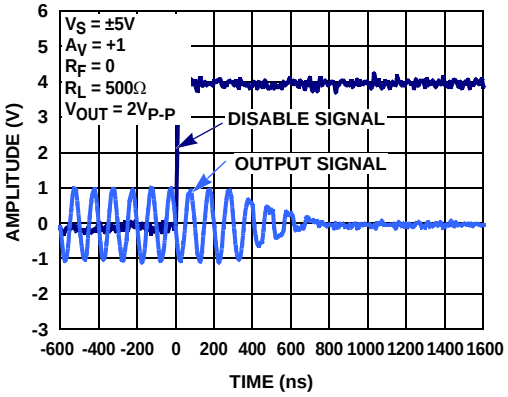


FIGURE 30. TURN-OFF TIME

Typical Performance Curves (Continued)

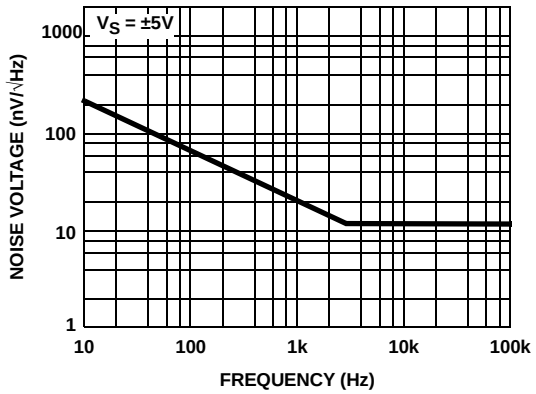


FIGURE 31. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

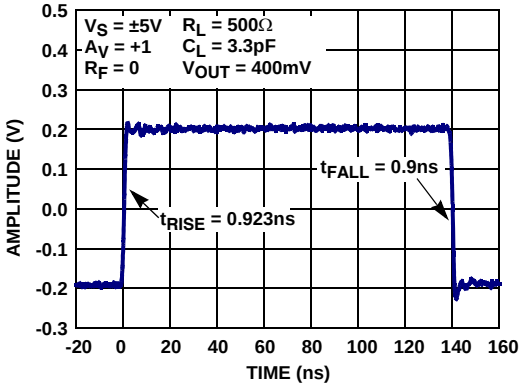


FIGURE 32. SMALL SIGNAL STEP RESPONSE RISE AND FALL TIME

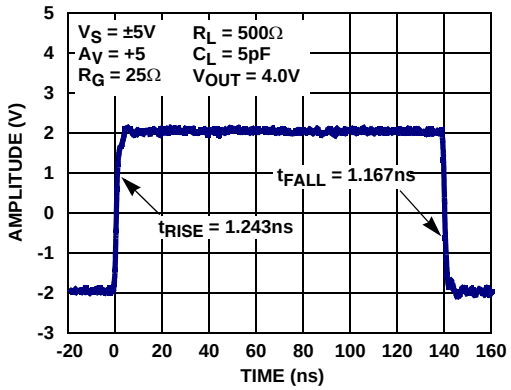


FIGURE 33. LARGE SIGNAL STEP RESPONSE RISE AND FALL TIME

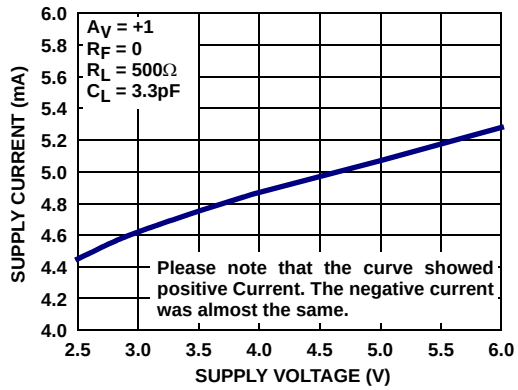


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

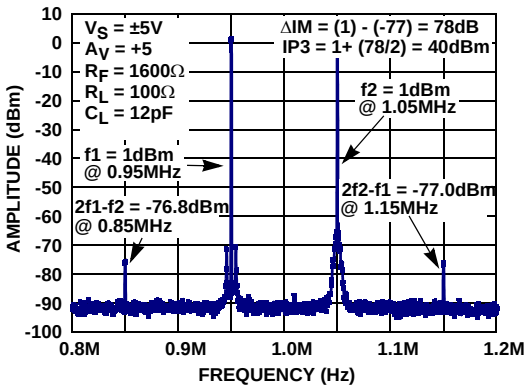


FIGURE 35. THIRD ORDER IMD INTERCEPT (IP3)

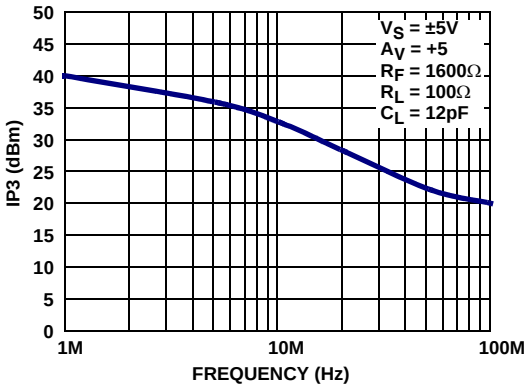


FIGURE 36. THIRD ORDER IMD INTERCEPT vs FREQUENCY

Typical Performance Curves (Continued)

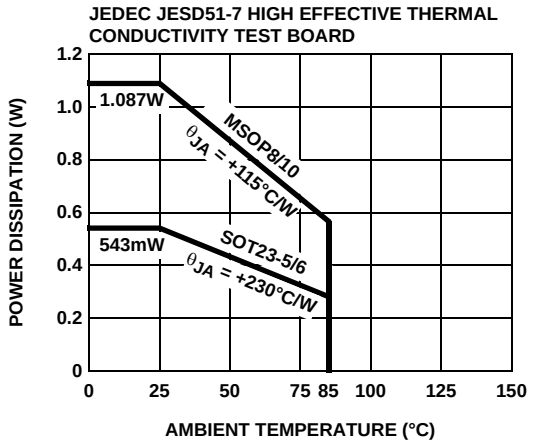


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

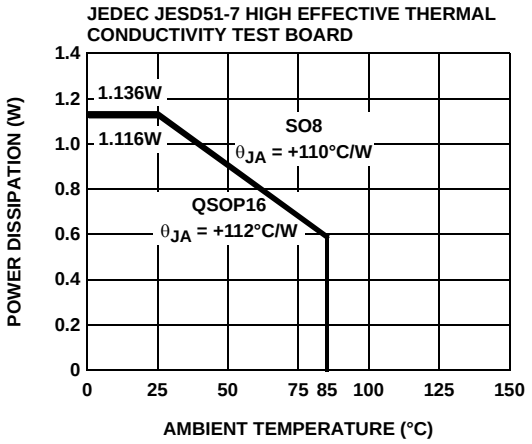


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

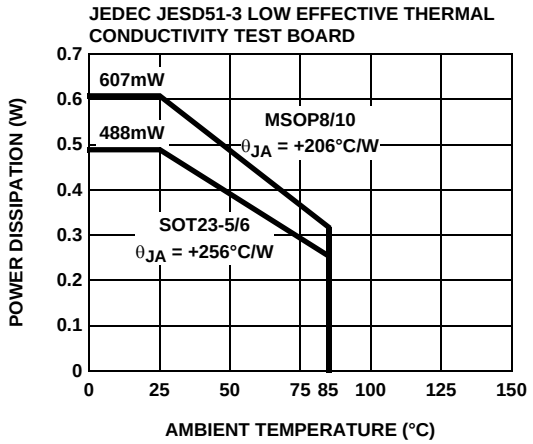


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

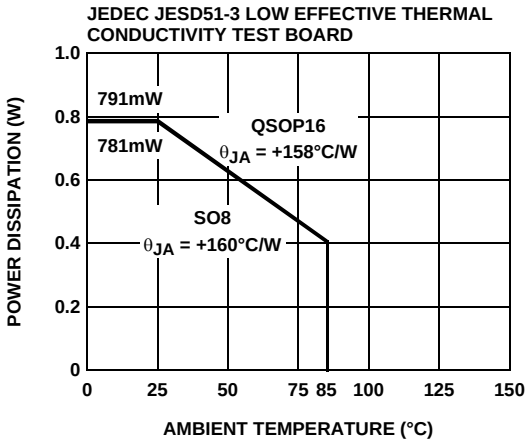
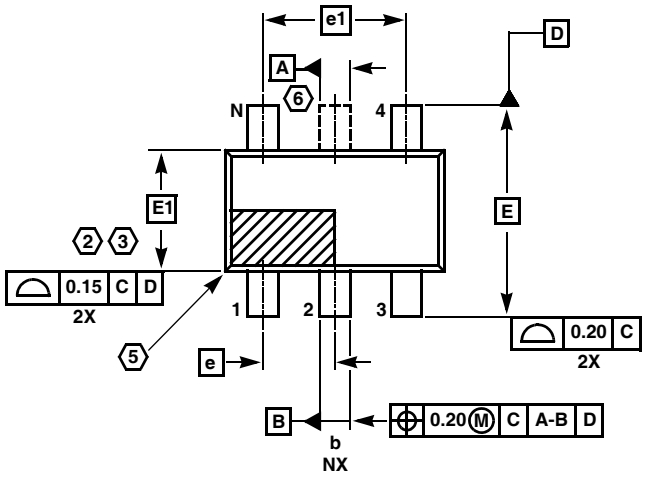
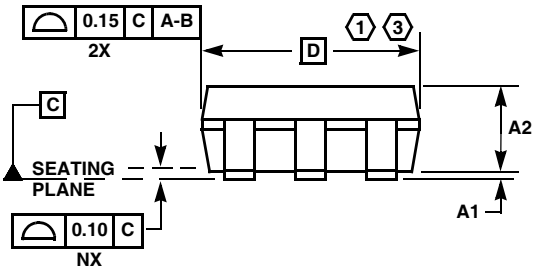
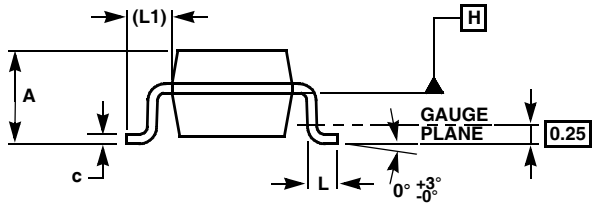


FIGURE 40. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

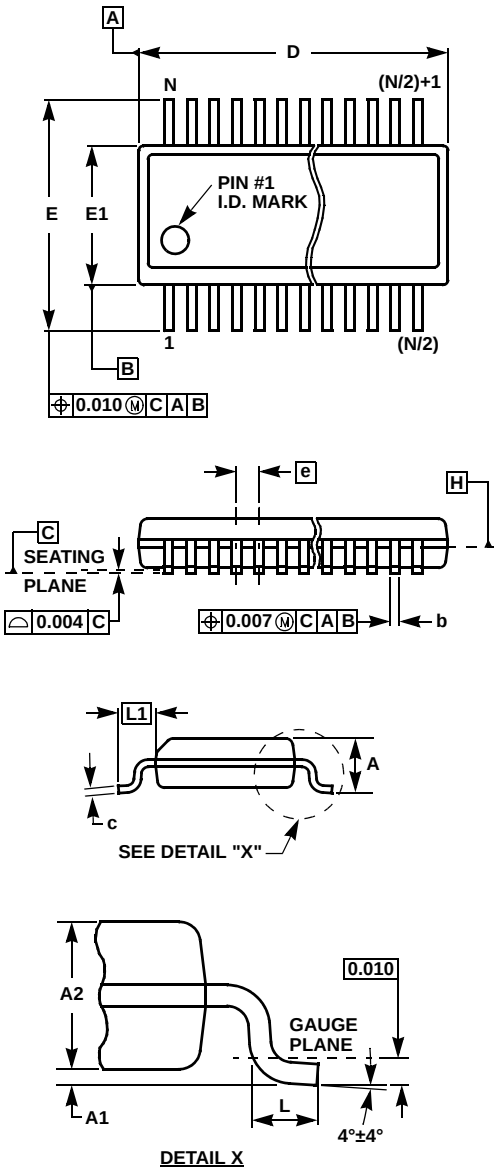
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

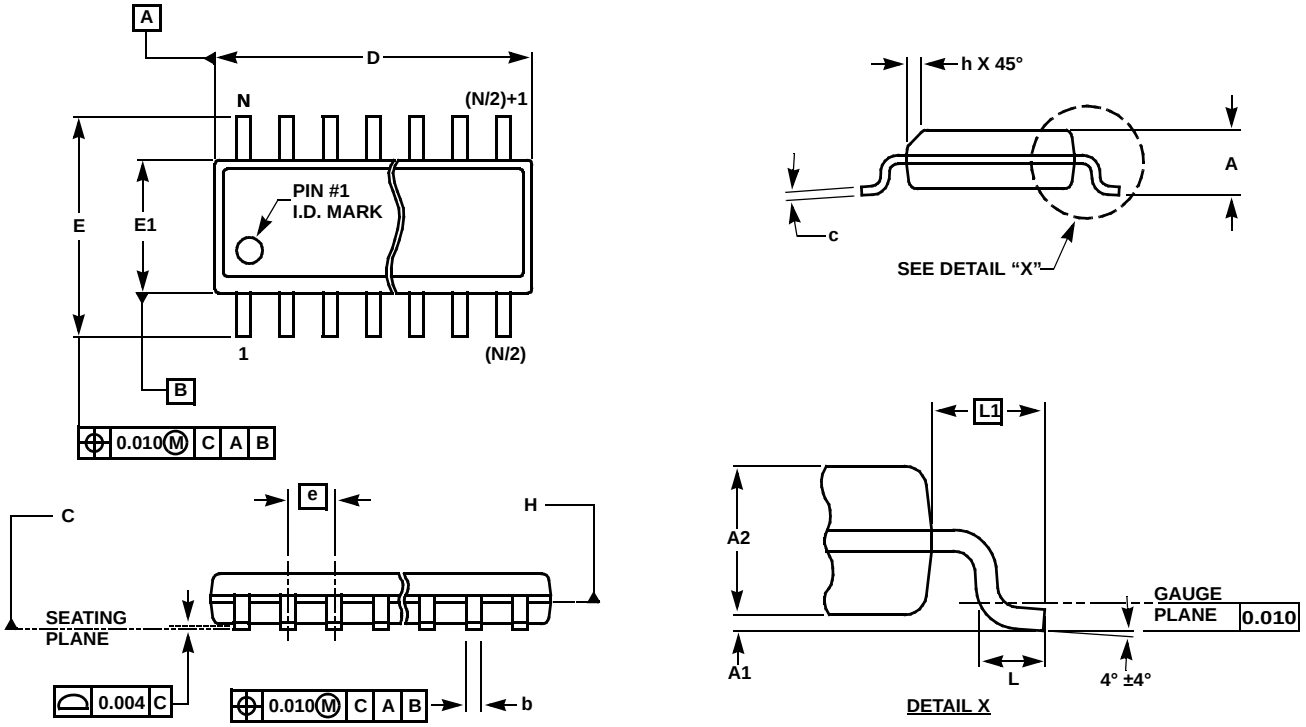
SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

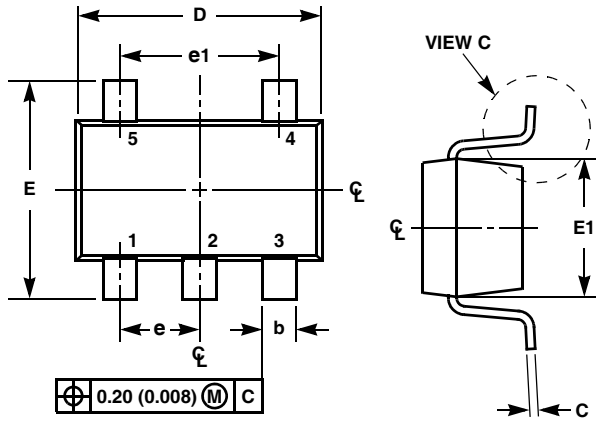
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

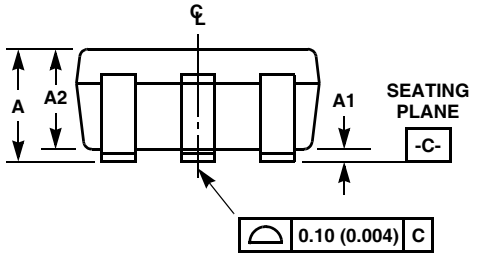
Rev. M 2/07

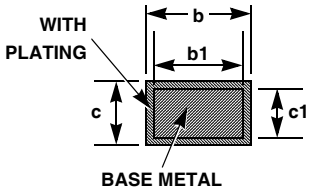
NOTES:

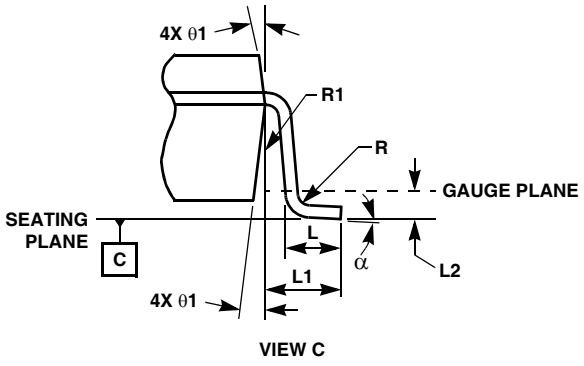
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

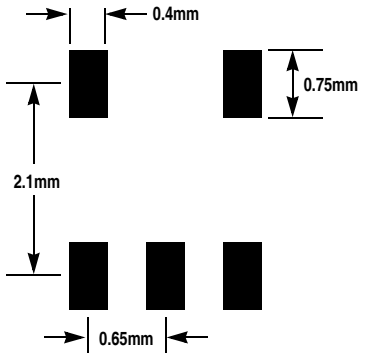
Small Outline Transistor Plastic Packages (SC70-5)











TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

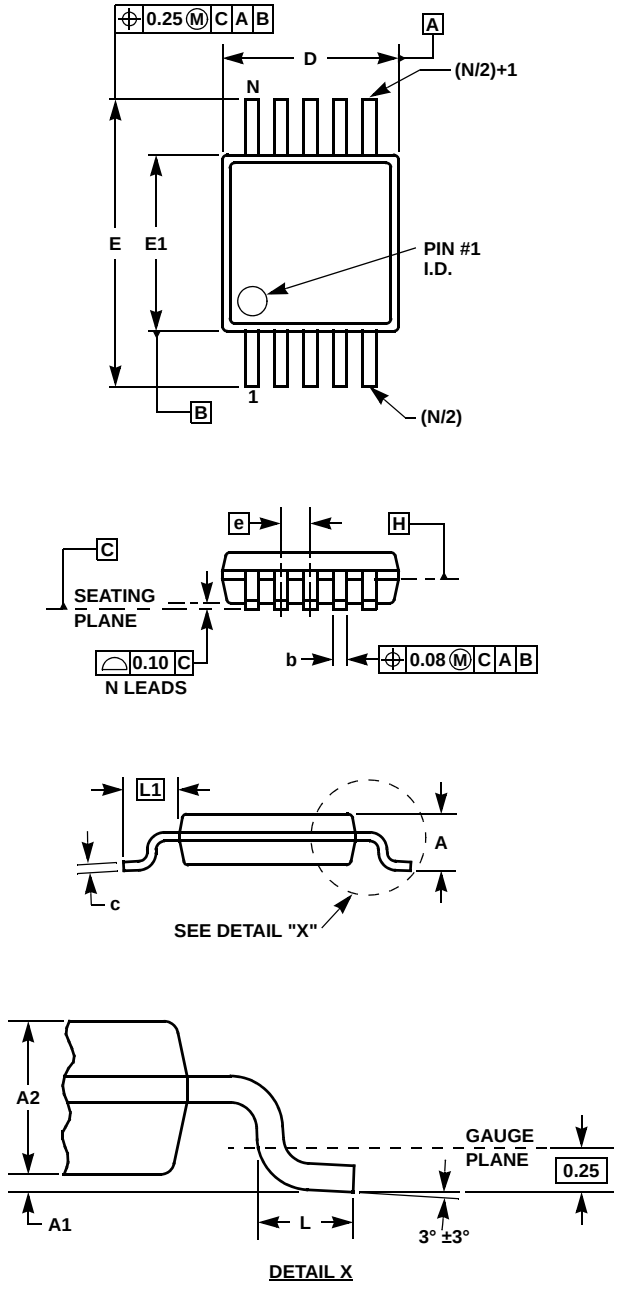
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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