THE DATASHEET OF

A8502KLPTR-T

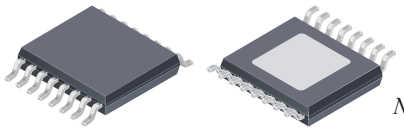
Wide Input Voltage Range, High Efficiency Fault Tolerant LED Driver

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Wide input voltage range of 5 to 40 V for start/stop, cold crank and load dump requirements
- Fully integrated LED current sinks and boost converter with 60 V DMOS
- Sync function to synchronize boost converter switching frequency up to 2.3 MHz, allowing operation above the AM band
- Excellent input voltage transient response
- Single resistor primary OVP minimizes V_{OUT} leakage
- Internal secondary OVP for redundant protection
- LED current of 120 mA per channel
- Drives up to 12 series LEDs in 2 parallel strings
- 0.7% to 0.8% LED to LED matching accuracy
- PWM and analog dimming inputs
- 5000:1 PWM dimming at 200 Hz
- Provides driver for optional external PMOS input disconnect switch
- Extensive protection against:
  - Shorted boost switch or inductor
  - Shorted FSET or ISET resistor
  - Shorted output
  - Open or shorted LED pin
  - Open boost Schottky
  - Overtemperature (OTP)

PACKAGE:

16-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

The A8502 is a multi-output white LED driver for small-size LCD backlighting. It integrates a current-mode boost converter with internal power switch and two current sinks. The boost converter can drive up to 24 LEDs, 12 LEDs per string, at 120 mA. The LED sinks can be paralleled together to achieve even higher LED currents, up to 240 mA. The A8502 can operate with a single power supply, from 5 to 40 V, which allows the part to withstand load dump conditions encountered in automotive systems.

If required, the A8502 can drive an external P-FET to disconnect the input supply from the system in the event of a fault. The A8502 provides protection against output short and overvoltage, open or shorted diode, open or shorted LED pin, shorted boost switch or inductor, shorted FSET or ISET resistor, and IC overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects the internal current switch against high current overloads.

The A8502 has a synchronization pin that allows its switching frequencies to be synchronized in the range of 260 kHz to 2.3 MHz. The high switching frequency allows the A8502 to operate above the AM radio band.

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APPLICATIONS:

LCD backlighting or LED lighting for:

- Automotive infotainment
- Automotive cluster
- Automotive center stack

Typical Application Circuit

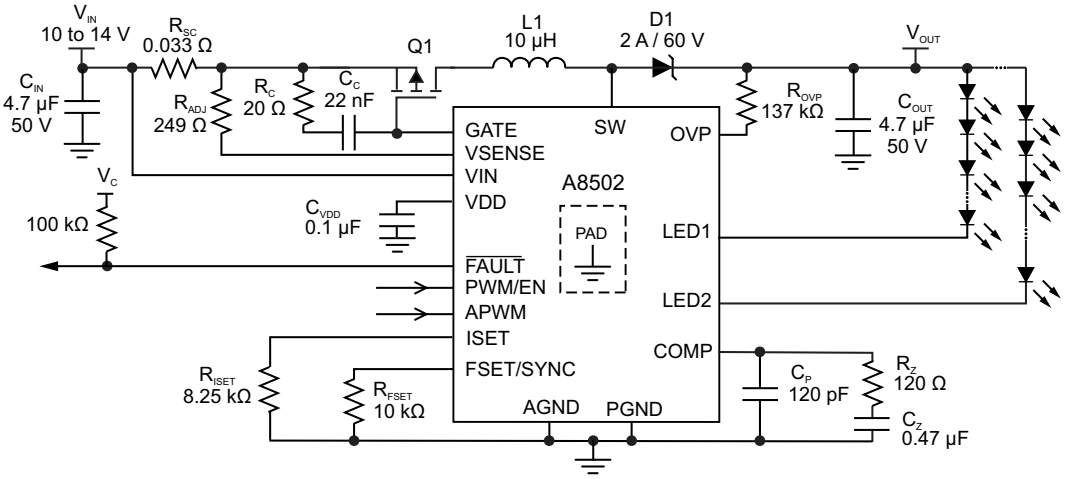


Figure 1: Application with VIN to ground short protection, using optional P-MOSFET sensing

DESCRIPTION (continued)

The A8502 is provided in a 16-pin TSSOP package (suffix LP) with an exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin lead frame plating.

SELECTION GUIDE

Part Number	Packing*
A8502KLPTR-T	4000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pins			–0.3 to 55	V
OVP Pin			–0.3 to 60	V
VIN, VSENSE, GATE Pins		VSENSE and GATE pins should not exceed V_{IN} by more than 0.4 V	–0.3 to 40	V
SW Pin		Continuous	–0.6 to 62	V
		t < 50 ns	–1.0	V
$\overline{\text{FAULT}}$ Pin			-0.3 to 40	V
ISET, FSET, APWM, COMP Pins			–0.3 to 5.5	V
All Other Pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

*Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

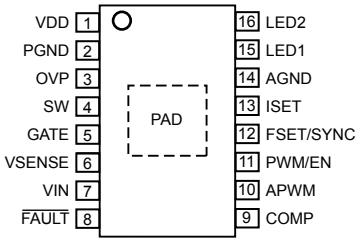
Table of Contents

Thermal Characteristics: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer PCB, 3 in.^{2}	48.5	°C/W
		On 4-layer PCB based on JEDEC standard	34	°C/W

*Additional thermal information available on the Allegro website

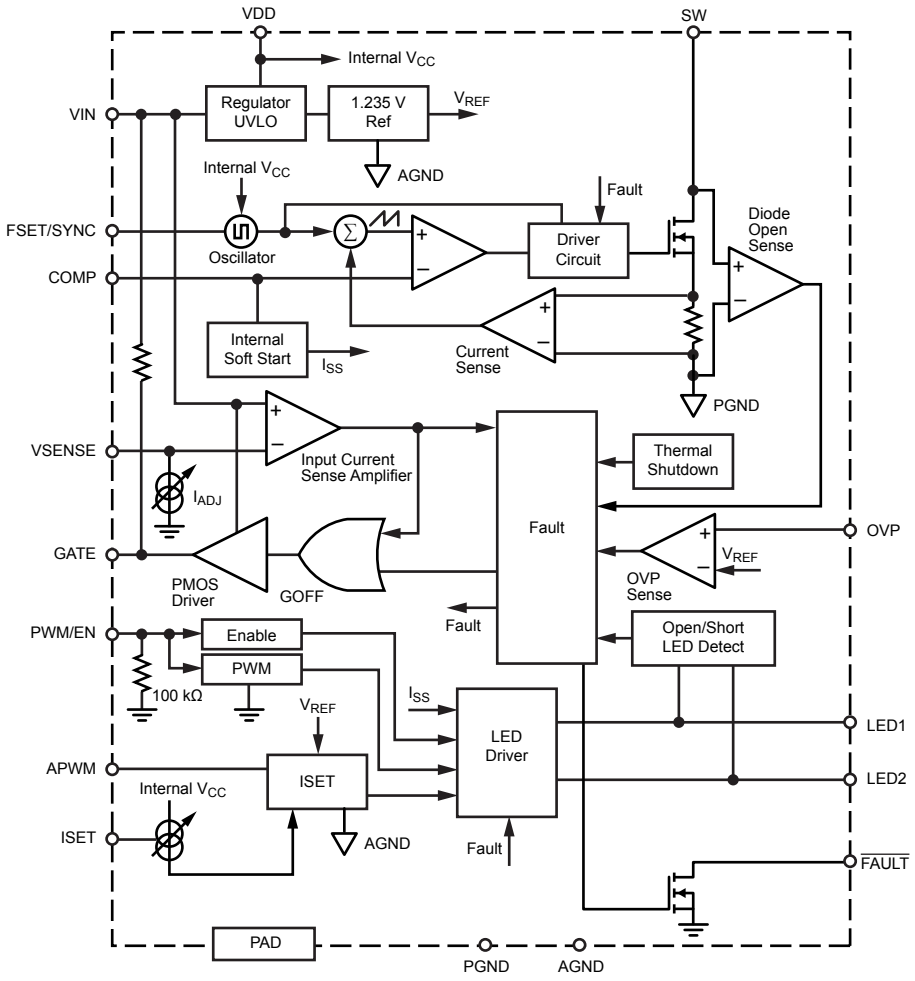
Pinout Diagram



Terminal List Table

Number	Name	Function
1	VDD	Output of internal LDO; connect a 0.1 µF decoupling capacitor between this pin and ground.
2	PGND	Power ground for internal DMOS device.
3	OVP	Overvoltage Condition (OVP) sense; connect the R_{OVP} resistor from V_{OUT} to this pin to adjust the overvoltage protection.
4	SW	The drain of the internal DMOS switch of the boost converter.
5	GATE	Output gate driver pin for external P-channel FET control.
6	VSENSE	Connect this pin to the negative sense side of the current sense resistor R_{SC}. The threshold voltage is measured as $V_{IN} - V_{SENSE}$. There is also a fixed current sink to allow for trip threshold adjustment.
7	VIN	Input power to the A8502 as well as the positive input used for current sense resistor.
8	$\overline{\text{FAULT}}$	Indicates a fault condition. Connect a 100 kΩ resistor between this pin and the required logic level voltage. The pin is an open drain type configuration that will be pulled low when a fault occurs.
9	COMP	Output of the error amplifier and compensation node. Connect a series R_Z-C_Z network from this pin to ground for control loop compensation.
10	APWM	Analog trimming option for dimming. Applying a digital PWM signal to this pin adjusts the internal I_{SET} current.
11	PWM/EN	PWM dimming pin, used to control the LED intensity by using pulse width modulation. Also used to enable the A8502.
12	FSET/SYNC	Frequency/synchronization pin. A resistor R_{FSET} from this pin to ground sets the switching frequency. This pin can also be used to synchronize two or more A8502s in the system. The maximum synchronization frequency is 2.3 MHz.
13	ISET	Connect the R_{ISET} resistor between this pin and ground to set the 100% LED current.
14	AGND	LED signal ground.
15	LED1	Connect the cathode of the LED string to this pin.
16	LED2	Connect the cathode of the LED sring to this pin.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad.

Functional Block Diagram



ELECTRICAL CHARACTERISTICS [1][2]: Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over full operating temperature range with $T_A = T_J$ = –40°C to 125°C, unless otherwise stated

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range [3]	V_{IN}		•	5	–	40	V
UVLO Start Threshold	$V_{UVLOrise}$	V_{IN} rising	•	–	–	4.35	V
UVLO Stop Threshold	$V_{UVLOfall}$	V_{IN} falling	•	–	–	3.90	V
UVLO Hysteresis [2]	$V_{UVLOHYS}$			300	450	600	mV
INPUT CURRENTS							
Input Quiescent Current	I_Q	PWM/EN = V_{IH}; SW = 2 MHz, no load	•	–	5.5	10	mA
Input Sleep Supply Current	I_{QSLEEP}	V_{IN} = 16 V, $V_{PWMEN} = V_{FSETSYNC}$ = 0 V	•	–	2.0	10.0	µA
INPUT LOGIC LEVELS (PWM/EN AND APWM)							
Input Logic Level-Low	V_{IL}	V_{IN} throughout operating input voltage range	•	–	–	400	mV
Input Logic Level-High	V_{IH}	V_{IN} throughout operating input voltage range	•	1.5	–	–	V
PWM/EN Pin Open Drain Pull-Down Resistor	R_{PWMEN}	PWM/EN = 5 V		60	100	140	kΩ
APWM Pull-Down Resistor	R_{APWM}	PWM/EN = V_{IH}		60	100	140	kΩ
APWM							
APWM Frequency [2]	f_{APWM}	V_{IH} = 2 V, V_{IL} = 0 V	•	20	–	1000	kHz
ERROR AMPLIFIER							
Open Loop Voltage Gain	A_{VOL}			44	48	52	dB
Transconductance	g_m	ΔI_{COMP} = ±10 µA		750	990	1220	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–350	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	350	–	µA
COMP Pin Pull-down Resistance	R_{COMP}	$\overline{FAULT}$ = 0		–	2000	–	Ω
OVERVOLTAGE PROTECTION							
Overvoltage Threshold	$V_{OVP(th)}$	OVP connected to V_{OUT}	•	7.7	8.1	8.5	V
OVP Sense Current	I_{OVPH}		•	188	199	210	µA
OVP Leakage Current	I_{OVPLKG}	R_{OVP} = 40.2 kΩ, V_{IN} = 16 V, PWM/EN = V_{IL}	•	–	0.1	1	µA
Secondary Overvoltage Protection	$V_{OVP(sec)}$		•	53	55	58	V
BOOST SWITCH							
Switch On-Resistance	R_{SW}	I_{SW} = 0.750 A, V_{IN} = 16 V	•	75	300	600	mΩ
Switch Leakage Current	I_{SWLKG}	V_{SW} = 16 V, PWM/EN = V_{IL}	•	–	0.1	1	µA
Switch Current Limit	$I_{SW(LIM)}$		•	3.0	3.5	4.2	A
Secondary Switch Current Limit [2]	$I_{SW(LIM2)}$	Higher than $I_{SW(LIM)}$(max) for all conditions, device latches when detected		–	7.00	–	A
Soft Start Boost Current Limit	$I_{SWSS(LIM)}$	Initial soft start current for boost switch		–	700	–	mA
Minimum Switch On-Time	$t_{SWONTIME}$		•	60	85	111	ns
Minimum Switch Off-Time	$t_{SWOFFTIME}$		•	30	47	68	ns

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ELECTRICAL CHARACTERISTICS [1][2] (continued): Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over full operating temperature range with $T_A = T_J$ = –40°C to 125°C, unless otherwise stated

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 10 kΩ	•	1.8	2	2.2	MHz
		R_{FSET} = 20 kΩ	•	0.9	1	1.1	MHz
		R_{FSET} = 35.6 kΩ		520	580	640	kHz
		R_{FSET} = 105 kΩ	•	178	200	222	kHz
FSET/SYNC Pin Voltage	V_{FSET}	R_{FSET} = 10 kΩ		–	1.00	–	V
FSET Frequency Range	f_{FSET}		•	200	–	2500	kHz
SYNCHRONIZATION							
Synchronized Switching Frequency	f_{SWSYNC}		•	260	–	2300	kHz
Synchronization Input Minimum Off-Time	$t_{PWSYNCOFF}$		•	150	–	–	ns
Synchronization Input Minimum On-Time	$t_{PWSYNCON}$		•	150	–	–	ns
SYNC Input Logic Voltage	$V_{SYNC(H)}$	FSET/SYNC pin, high level	•	2.0	–	–	V
	$V_{SYNC(L)}$	FSET/SYNC pin, low level	•	–	–	0.4	V
LED CURRENT SINKS							
LEDx Accuracy	Err_{LED}	I_{SET} = 120 µA	•	–	–	2	%
LEDx Matching	ΔLEDx	I_{SET} = 120 µA	•	–	–	1	%
LEDx Regulation Voltage	V_{LED}	$V_{LED1} = V_{LED2}$, I_{SET} = 120 µA	•	620	720	820	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 120 µA	•	960	980	1000	A/A
ISET Pin Voltage	V_{ISET}			0.988	1.003	1.018	V
Allowable ISET Current	I_{SET}		•	40	–	120	µA
V_{LED} Short Detect	V_{LEDSC}	While LED sinks are in regulation, sensed from LEDx pin to ground	•	4.6	5.1	5.6	V
Soft Start LEDx Current	I_{LEDSS}	Current through each enabled LEDx pin during soft start		–	3.2	–	mA
Maximum PWM Dimming Until Off-Time [2]	t_{PWML}	Measured while PWM/EN = low, during dimming control and internal references are powered-on (exceeding t_{PWML} results in shutdown)		–	32,750	–	f_{SW} cycles
Minimum PWM On-Time	t_{PWMH}	First cycle when powering-up device	•	–	0.75	2	µs
PWM High to LED-On Delay	$t_{dPWM(on)}$	Time between PWM enable and LED current reaching 90% of maximum	•	–	0.5	1	µs
PWM Low to LED-Off Delay	$t_{dPWM(off)}$	Time between PWM enable going low and LED current reaching 10% of maximum	•	–	360	500	ns

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ELECTRICAL CHARACTERISTICS [1][2] (continued): Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over full operating temperature range with $T_A = T_J$ = –40°C to 125°C, unless otherwise stated

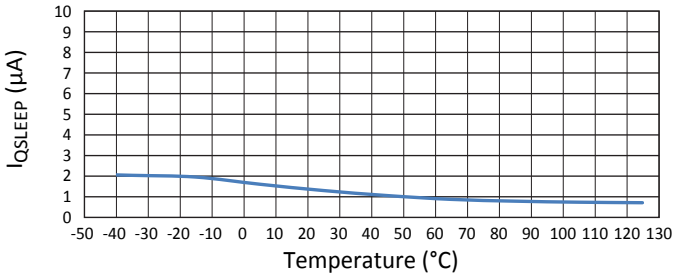
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
GATE PIN							
GATE Pin Sink Current	I_{GSINK}	$V_{GS} = V_{IN}$		–	−104	–	µA
Gate Fault Shutdown Greater Than 2× Current [2]	$t_{GFAULT2}$			–	–	3	µs
Gate Fault Shutdown Greater Than 1–2× Current	$t_{GFAULT1}$			–	10,000	–	f_{SW} cycles
Gate Voltage	V_{GS}	Gate to source voltage measured when gate is on		–	–6.7	–	V
VSENSE PIN							
VSENSE Pin Sink Current	I_{ADJ}		•	18.8	20.3	21.8	µA
VSENSE Trip Point	$V_{SENSEtrip1}$	Measured between VIN and VSENSE, R_{ADJ} = 0 Ω	•	94	104	114	mV
VSENSE 2× Trip [2]	$V_{SENSEtrip2}$	2× $V_{SENSEtrip}$, instantaneous shutdown, R_{ADJ} = 0 Ω		–	180	–	mV
$\overline{\text{FAULT}}$ PIN							
$\overline{\text{FAULT}}$ Pull-Down Voltage	V_{FAULT}	I_{FAULT} = 1 mA	•	–	–	0.5	V
$\overline{\text{FAULT}}$ Pin Leakage Current	$I_{FAULTLKG}$	V_{FAULT} = 5 V		–	–	1	µA
THERMAL PROTECTION (TSD)							
Thermal Shutdown Threshold [2]	T_{SD}	Temperature rising		–	165	–	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Minimum V_{IN} = 5 V is only required at startup. After startup is completed, the IC is able to function down to V_{IN} = 4 V.

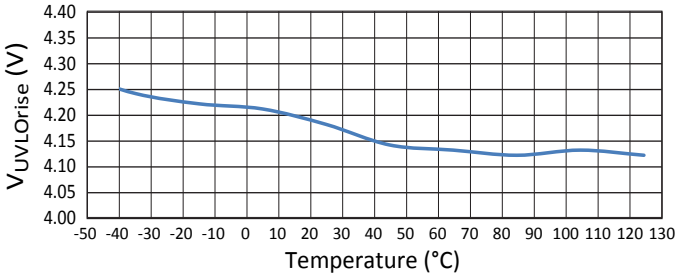
CHARACTERISTIC PERFORMANCE

$T_A = T_J$

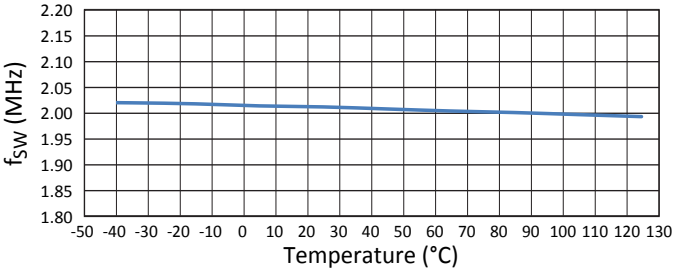
VIN Input Sleep Mode Current versus Ambient Temperature



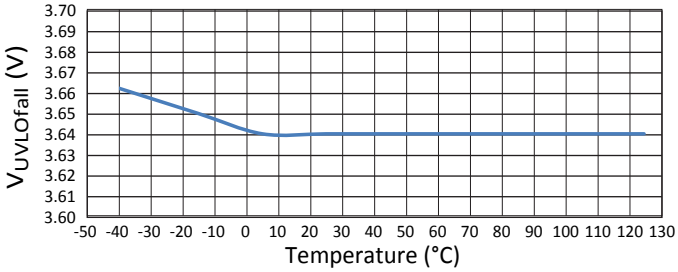
VIN UVLO Start Threshold Voltage versus Ambient Temperature



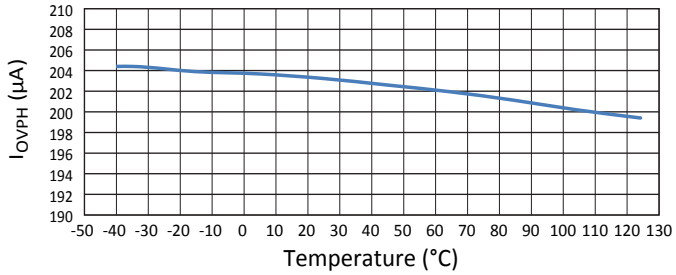
Switching Frequency versus Ambient Temperature



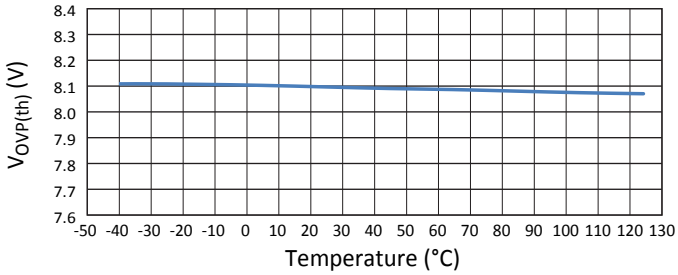
VIN UVLO Stop Threshold Voltage versus Ambient Temperature



OVP Pin Sense Current versus Ambient Temperature

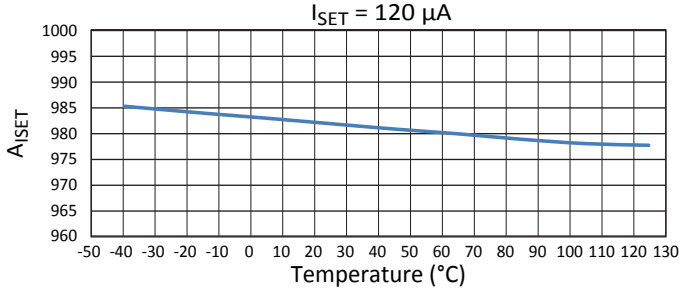


OVP Pin Overvoltage Threshold versus Ambient Temperature

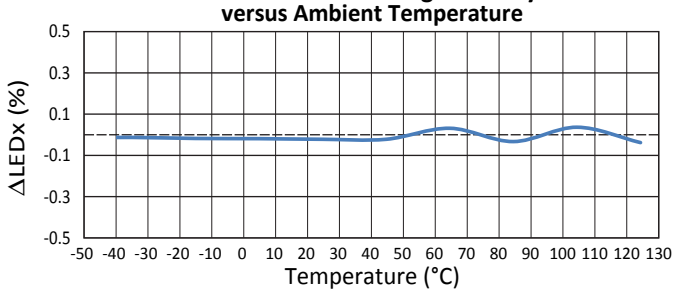


ISET to LED Current Gain versus Ambient Temperature

I_{SET} = 120 µA

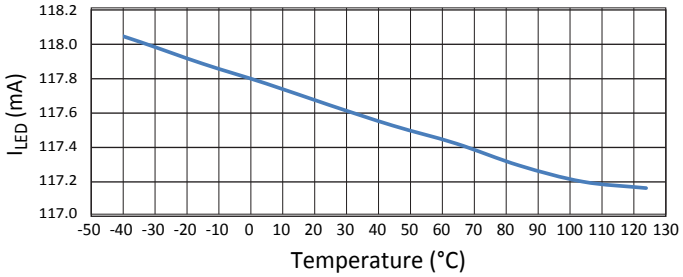


LED to LED Matching Accuracy versus Ambient Temperature

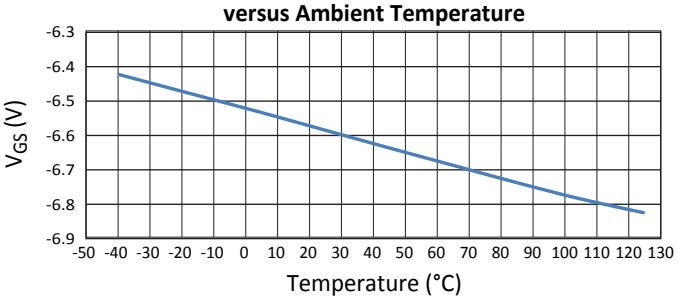


LED Current versus Ambient Temperature

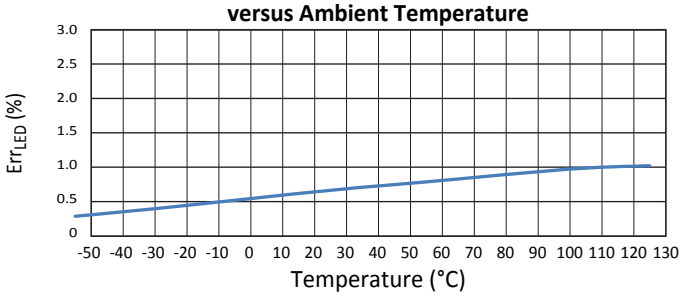
I_{SET} = 120 µA



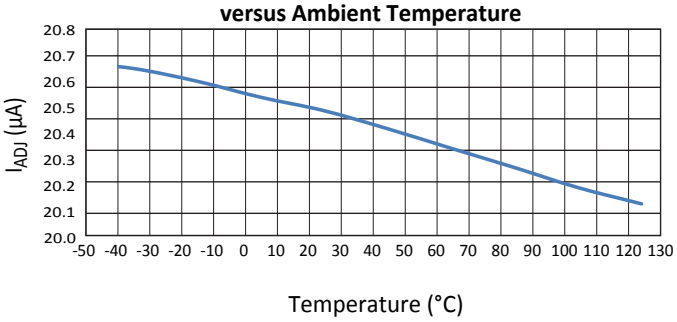
Input Disconnect Switch Gate to Source Voltage versus Ambient Temperature

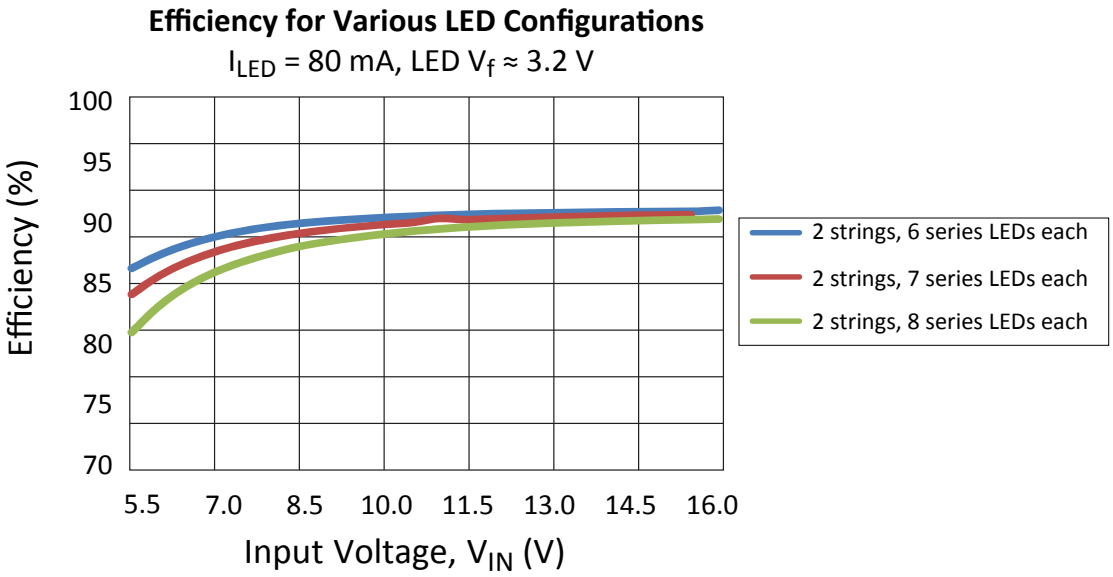


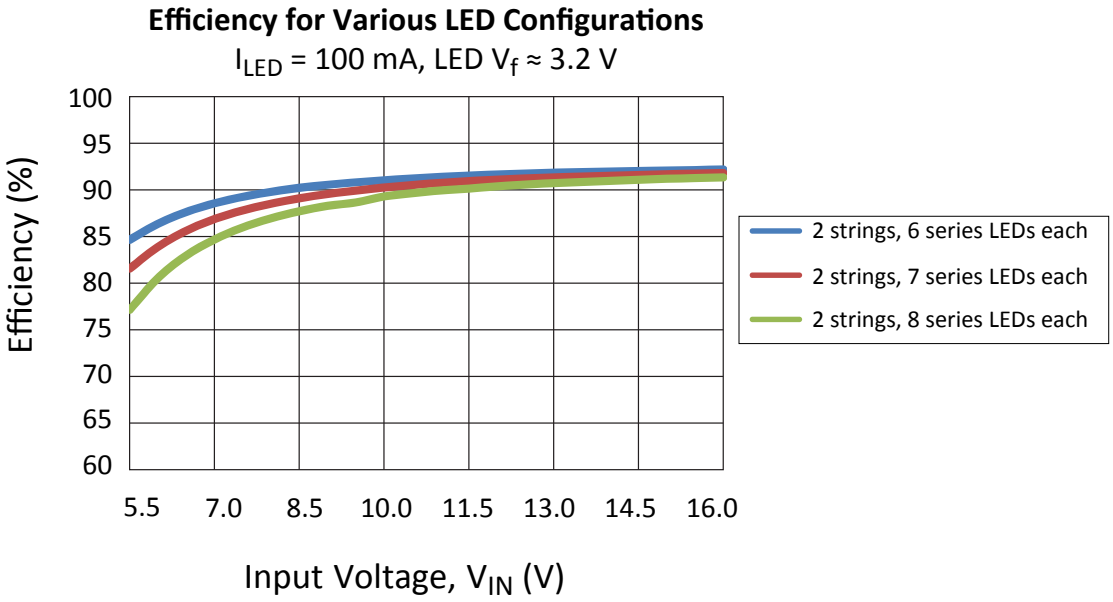
LED Current Setpoint Accuracy versus Ambient Temperature



VSENSE Pin Sink Current versus Ambient Temperature




Efficiency for Various LED Configurations
I_{LED} = 80 mA, LED V_f ≈ 3.2 V
Efficiency (%)
100
95
90
85
80
75
70
5.5
7.0
8.5
10.0
11.5
13.0
14.5
16.0
Input Voltage, V_{IN} (V)
2 strings, 6 series LEDs each
2 strings, 7 series LEDs each
2 strings, 8 series LEDs each


Efficiency for Various LED Configurations
I_{LED} = 100 mA, LED V_f ≈ 3.2 V
Efficiency (%)
100
95
90
85
80
75
70
65
60
5.5
7.0
8.5
10.0
11.5
13.0
14.5
16.0
Input Voltage, V_{IN} (V)
2 strings, 6 series LEDs each
2 strings, 7 series LEDs each
2 strings, 8 series LEDs each

FUNCTIONAL DESCRIPTION

The A8502 incorporates a current-mode boost controller with internal DMOS switch, and two LED current sinks. It can be used to drive two LED strings of up to 12 white LEDs in series, with current up to 120 mA per string. For optimal efficiency, the output of the boost stage is adaptively adjusted to the minimum voltage required to power both LED strings. This is expressed by the following equation:

$$V_{OUT} = \max (V_{LED1}, V_{LED2}) + V_{REG} \quad (1)$$

where

V_{LEDx} is the voltage drop across LED strings 1 and 2, and

V_{REG} is the regulation voltage of the LED current sinks (typically 0.72 V at the maximum LED current).

Enabling the IC

The IC turns on when a logic high signal is applied on the PWM/EN pin with a minimum duration of t_{PWMH} for the first clock cycle, and the input voltage present on the VIN pin is greater than the 4.35 V necessary to clear the UVLO ($V_{UVLOrise}$) threshold. The power-up sequence is shown in Figure 2. Before the LEDs are enabled, the A8502 driver goes through a system check to determine if there are any possible fault conditions that might prevent the system from functioning correctly. Also, if the FSET/SYNC pin is pulled low, the IC will not power-up. More information on the FSET/SYNC pin can be found in the Sync section of this datasheet.

Powering up: LED pin short-to-ground check

The VIN pin has a UVLO function that prevents the A8502 from powering-up until the UVLO threshold is reached. After the VIN pin goes above UVLO, and a high signal is present on the PWM/EN pin, the IC proceeds to power-up. As shown in Figure 3, at this point the A8502 enables the disconnect switch and checks if any LEDx pins are shorted to ground and/or are not used.

The LED detect phase starts when the GATE voltage of the disconnect switch is equal to $V_{IN} - 4.5$ V. After the voltage threshold on the LEDx pins exceeds 120 mV, a delay of between 3000 and 4000 clock cycles is used to determine the status of the pins. Thus, the LED detection duration varies with the switching

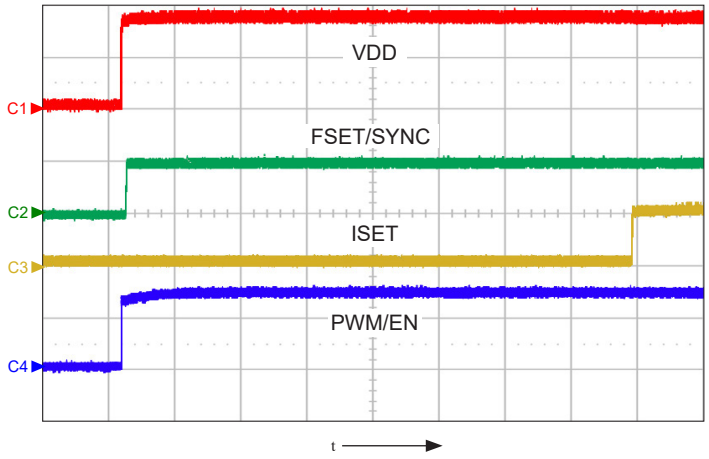


Figure 2: Power-up diagram; shows VDD (ch1, 2 V/div.), FSET/SYNC (ch2, 1 V/div.), ISET (ch3, 1 V/div.), and PWM/EN (ch4, 2 V/div.) pins, time = 200 µs/div.

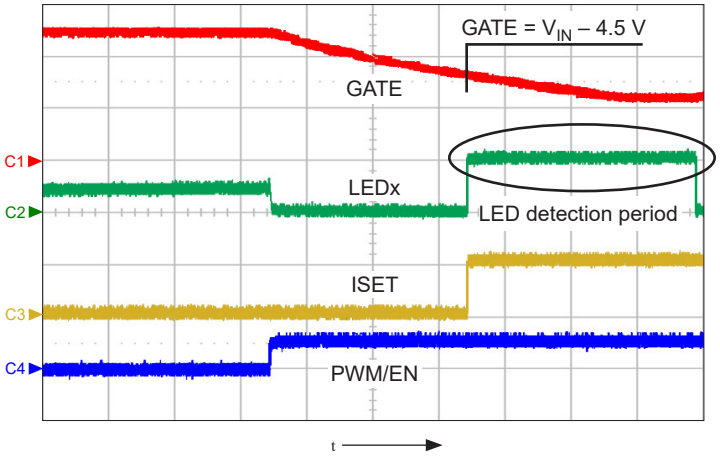


Figure 3: Power-up diagram; shows the relationship of an LEDx pin with respect to the gate voltage of the disconnect switch (if used) during the LED detect phase, as well as the duration of the LED detect phase for a switching frequency of 2 MHz; shows GATE (ch1, 5 V/div.), LED (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and PWM/EN (ch4, 5 V/div.) pins, time = 500 µs/div.

frequency, as shown in the following table:

Switching Frequency (MHz)	Detection Time (ms)
2	1.5 to 2
1	3 to 4
0.800	3.75 to 5
0.600	5 to 6.7

The LED pin detection voltage thresholds are as follows:

LED Pin Voltage	LED Pin Status	Action
<70 mV	Short-to-ground	Power-up is halted
150 mV	Not used	LED removed from operation
325 mV	LED pin in use	None

All unused pins should be connected with a 1.54 kΩ resistor to ground, as shown in Figure 5. The unused pin, with the pull-down resistor, will be taken out of regulation at this point and will not contribute to the boost regulation loop.

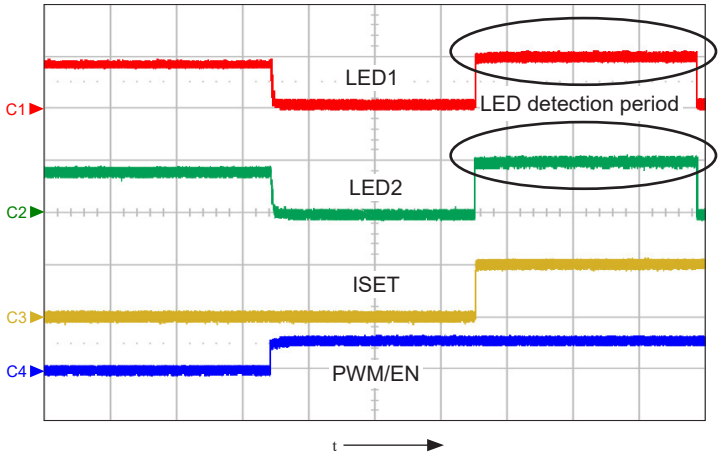


Figure 4A: An LED detect occurring when both LED pins are selected to be used; shows LED1 (ch1, 500 mV/div.), LED2 (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and PWM/EN (ch4, 5 V/div.) pins, time = 500 µs/div.

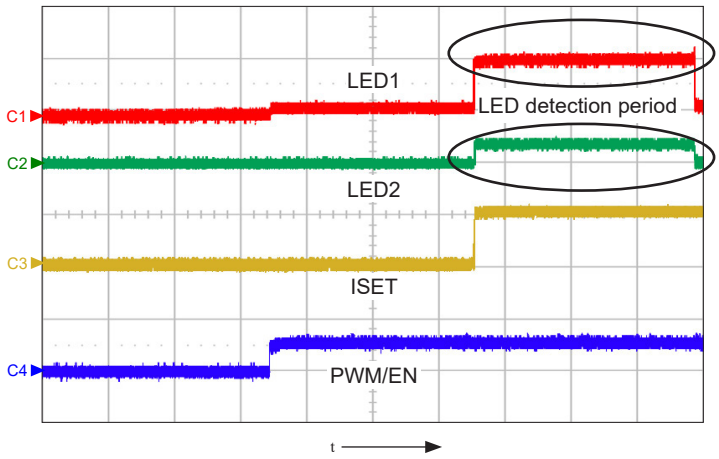


Figure 4B: Example with LED2 pin not being used; the detect voltage is about 150 mV; shows LED1 (ch1, 500 mV/div.), LED2 (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and PWM/EN (ch4, 5 V/div.) pins, time = 500 µs/div.

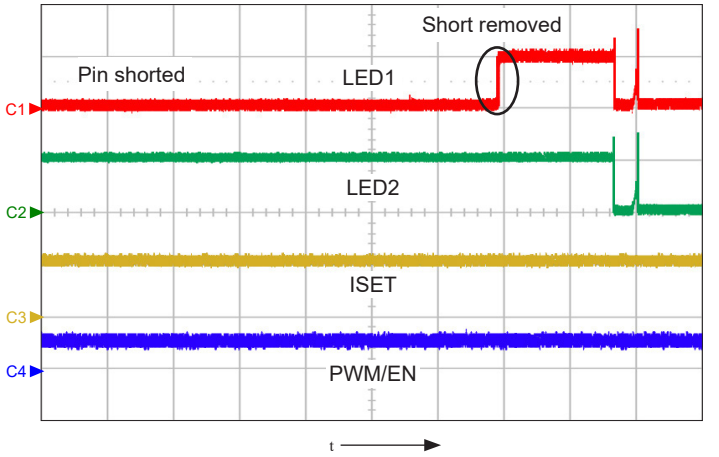


Figure 4C: Example with one LED shorted to ground. The IC will not proceed with power-up until the shorted LED pin is released, at which point the LED is checked to see if it is being used; shows LED1 (ch1, 500 mV/div.), LED2 (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and PWM/EN (ch4, 5 V/div.) pins, time = 1 ms/div.

If a LEDx pin is shorted to ground the A8502 will not proceed with soft start until the short is removed from the LEDx pin. This prevents the A8502 from powering-up and putting an uncontrolled amount of current through the LEDs.

Soft start function

During soft start the LEDx pins are set to sink (I_{LEDSS}) and the boost switch current is reduced to the $I_{SWSS(LIM)}$ level to limit the inrush current generated by charging the output capacitors. When the converter senses that there is enough voltage on the LEDx pins the converter proceeds to increase the LED current to the preset regulation current and the boost switch current limit is switched to the $I_{SW(LIM)}$ level to allow the A8502 to deliver the necessary output power to the LEDs. This is shown in Figure 6.

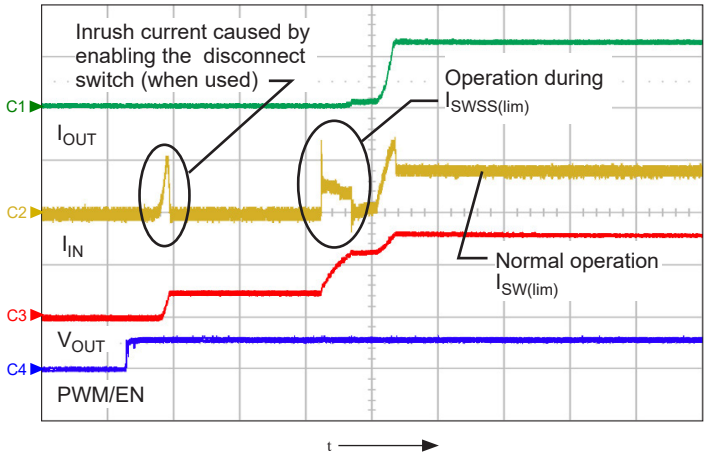


Figure 6: Startup diagram showing the input current, output voltage, and output current; shows I_{OUT} (ch1, 200 mA/div.), I_{IN} (ch2, 1 A/div.), V_{OUT} (ch3, 20 V/div.), and PWM/EN (ch4, 5 V/div.), time = 1 ms/div.

Frequency selection

The switching frequency on the boost regulator is set by the resistor connected to the FSET/SYNC pin. The switching frequency can be can be anywhere from 200 kHz to 2.3 MHz. Figure 7 shows the typical switching frequency for different resistor values. The relationship between FSET resistance and the typical switching frequency is given as:

$$f_{SW} = \frac{k}{(R_{FSET} + R_{INT})}$$

where f_{SW} is in MHz, R_{FSET} is in kΩ, k = 20.9, and R_{INT} = 0.6 kΩ (internal resistance of FSET pin).

In case during operation a fault occurs that will increase the switching frequency, the FSET/SYNC pin is clamped to a maximum switching frequency of no more than 3.5 MHz. If the FSET/SYNC pin is shorted to GND the part will shut down. For more details see the Fault Mode table later in this datasheet.

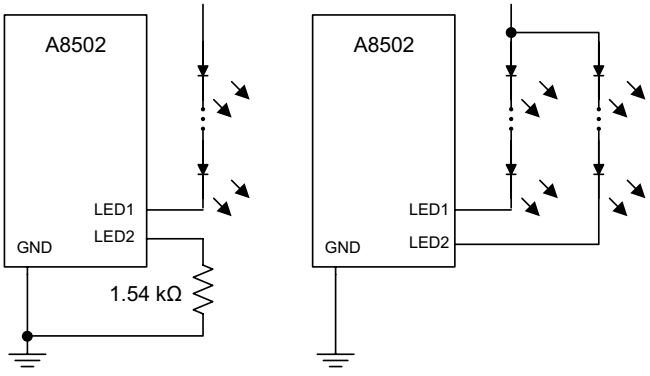


Figure 5: Channel select setup: (left) using only channel LED1, (right) using both channels.

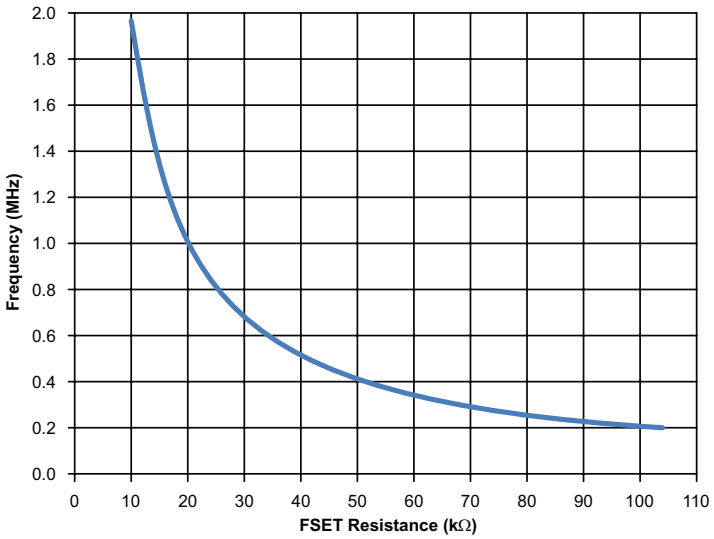


Figure 7: Typical Switching Frequency versus value of R_{FSET} resistor.

Sync

The A8502 can also be synchronized using an external clock on the FSET/SYNC pin. Figure 8 shows the correspondence of a sync signal and the FSET/SYNC pin, and Figure 9 shows the result when a sync signal is detected: the LED current does not show any variation while the frequency changeover occurs. At power-up if the FSET/SYNC pin is held low, the IC will not power-up. Only when the FSET/SYNC pin is tri-stated to allow the pin to rise, to about 1 V, or when a synchronization clock is detected, will the A8502 try to power-up.

The basic requirement of the sync signal is 150 ns minimum on-time and 150 ns minimum off time, as indicated by the specifications for $t_{PWSYNCON}$ and $t_{PWSYNCOFF}$. Figure 10 shows the timing for a synchronization clock into the A8502 at 2.2 MHz. Thus any pulse with a duty cycle of 33% to 66% at 2.2 MHz can be used to synchronize the IC.

The SYNC pulse duty cycle ranges for selected switching frequencies are:

SYNC Pulse Frequency (MHz)	Duty Cycle Range (%)
2.2	33 to 66
2	30 to 70
1	15 to 85
0.800	12 to 88
0.600	9 to 91

If during operation a sync clock is lost, the IC will revert to the preset switching frequency that is set by the resistor R_{FSET}. During this period the IC will stop switching for a maximum period of about 7 µs to allow the sync detection circuitry to switch over to the externally preset switching frequency.

If the clock is held low for more than 7 µs, the A8502 will shut

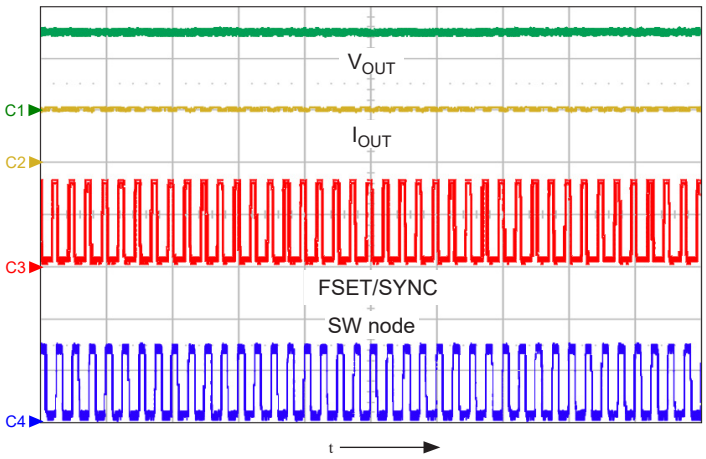


Figure 8: Diagram showing a synchronized FSET/SYNC pin and switch node; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 200 mA/div.), FSET/SYNC (ch3, 2 V/div.), and SW node (ch4, 20 V/div.), time = 2 µs/div.

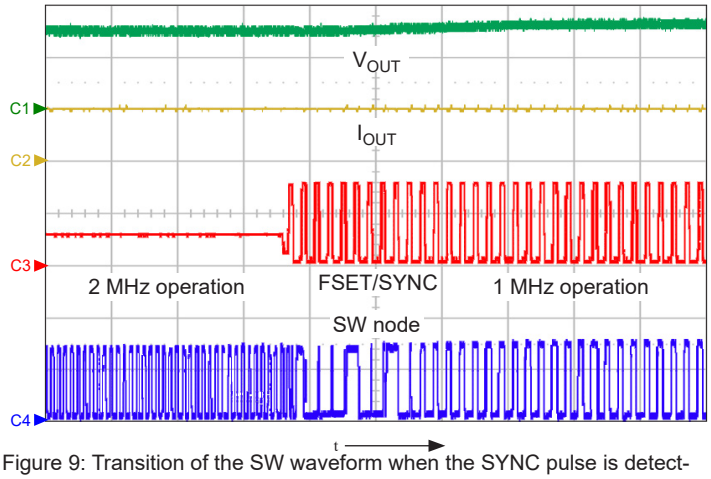


Figure 9: Transition of the SW waveform when the SYNC pulse is detected. The A8502 switching at 2 MHz, applied SYNC pulse at 1 MHz; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 200 mA/div.), FSET/SYNC (ch3, 2 V/div.), and SW node (ch4, 20 V/div.), time = 5 µs/div.

down. In this shutdown mode the IC will stop switching, the input disconnect switch is open, and the LEDs will stop sinking current. To shutdown the IC into low power mode, the user must disable the IC using the PWM pin, by keeping the pin low for a period of 32,750 clock cycles. If the FSET/SYNC pin is released at any time after 7 µs, the A8502 will proceed to soft start.

To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown in Figure 11 can be used. When the external SYNC signal goes low, the A8502 will continue to operate normally at the switching frequency set by RFSET. No FAULT flag is generated.

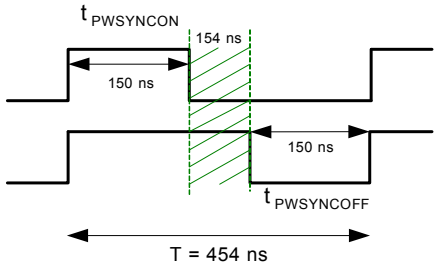


Figure 10: SYNC pulse on and off time requirements.

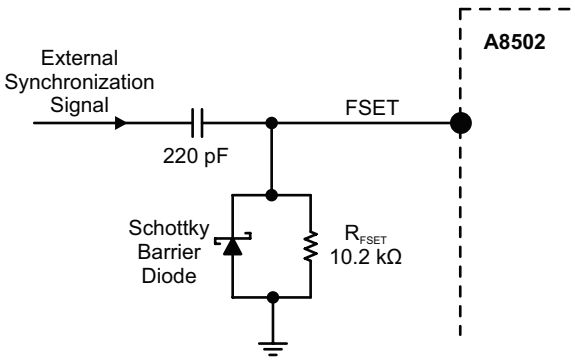


Figure 11: Countermeasure to prevent external sync signal stuck-at-low fault

If it is necessary to switch over between internal oscillator and external sync during operation, ensure the transition takes place at least 500 ns after the previous PWM = H rising edge. Alternatively, execute the switchover during PWM = L only. This restriction does not apply if PWM dimming is not being used.

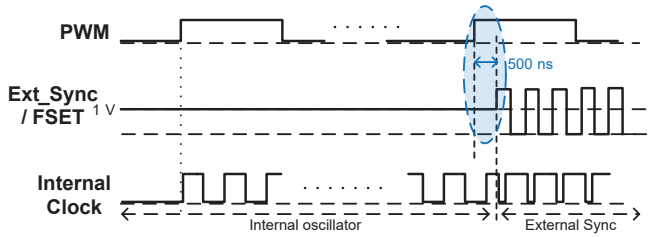


Figure 12: Avoid switching over between Internal Oscillator and External Sync in highlighted region

LED current setting and LED dimming

The maximum LED current can be up to 120 mA per channel, and is set through the ISET pin. To set the I_{LED} current, connect a resistor, R_{ISET}, between this pin and ground, according to the following formula:

$$R_{ISET} = (1.003 \times 980) / I_{LED} \quad (2)$$

where I_{LED} is in A and R_{ISET} is in Ω. This sets the maximum current through the LEDs, referred to as the *100% current*. Standard R_{ISET} values, at gain equals 980, are as follows:

Standard Closest R_{ISET} Resistor Value (kΩ)	LED current per LED, I_{LED} (mA)
8.25	120
9.76	100
12.1	80
15.0	65

PWM dimming

The LED current can be reduced from the 100% current level by PWM dimming using the PWM/EN pin. When the PWM/EN pin is pulled high, the A8502 turns on and all enabled LEDs sink 100% current. When PWM/EN is pulled low, the boost converter and LED sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active. The typical PWM dimming frequencies fall between 200 Hz and 1 kHz. Figure 13A to Figure 13D provide examples of PWM switching behavior.

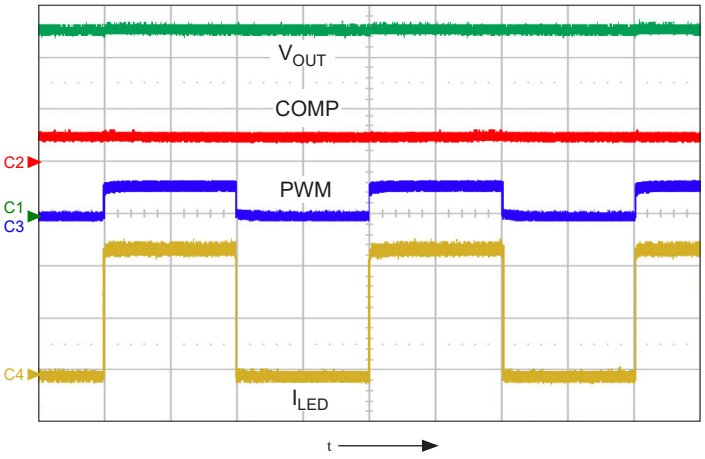


Figure 13A: Typical PWM diagram showing V_{OUT}, I_{LED}, and COMP pin as well as the PWM signal. PWM dimming frequency is 500 Hz at 50% duty cycle; shows V_{OUT} (ch1, 10 V/div.), COMP (ch2, 2 V/div.), PWM (ch3, 5 V/div.), and I_{LED} (ch4, 50 mA/div.), time = 500 µs/div.

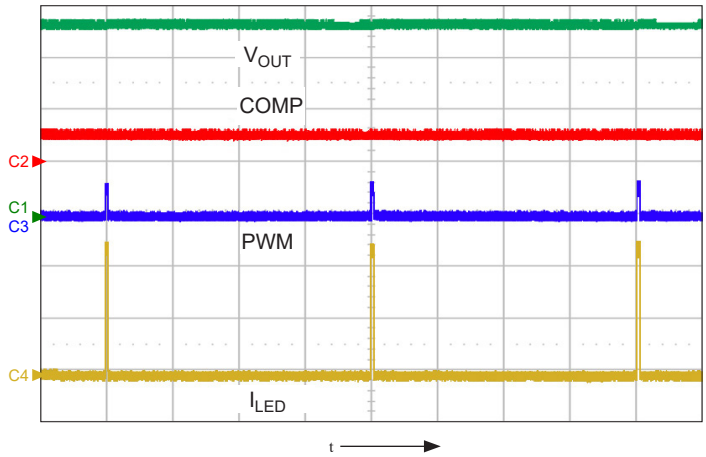


Figure 13B: Typical PWM diagram showing V_{OUT}, I_{LED}, and COMP pin as well as the PWM signal. PWM dimming frequency is 500 Hz at 1% duty cycle ; shows V_{OUT} (ch1, 10 V/div.), COMP (ch2, 2 V/div.), PWM (ch3, 5 V/div.), and I_{LED} (ch4, 50 mA/div.), time = 500 µs/div.

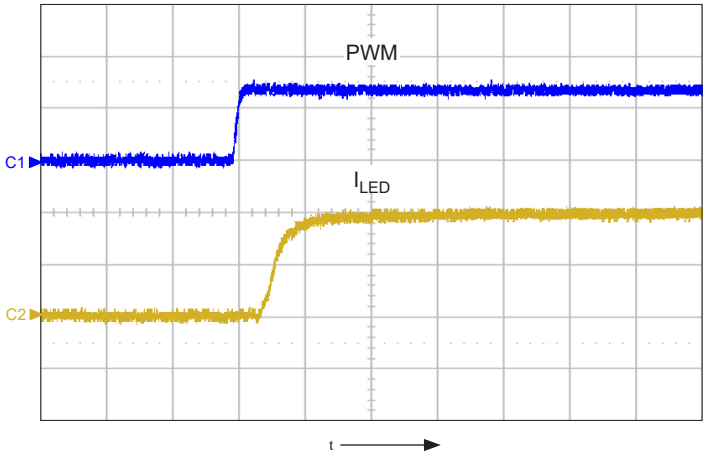


Figure 13C: Delay from rising edge of PWM signal to LED current; shows PWM (ch1, 2 V/div.), and I_{LED} (ch2, 50 mA/div.), time = 200 ns/div.

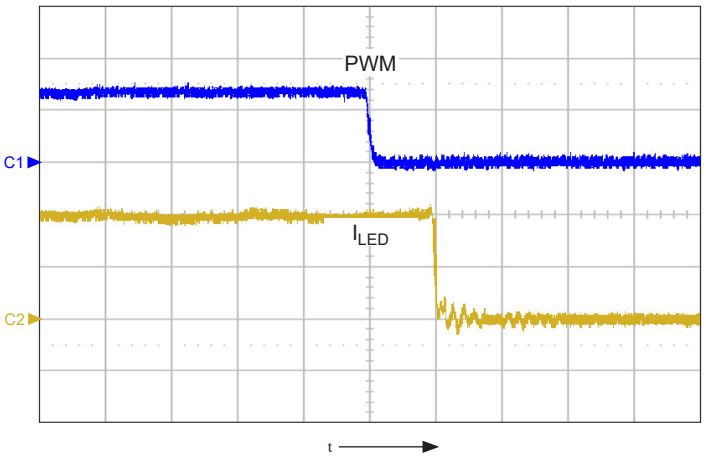


Figure 13D: Delay from falling edge of PWM signal to LED current turn off; shows PWM (ch1, 2 V/div.), and I_{LED} (ch2, 50 mA/div.), time = 200 ns/div.

Another important feature of the A8502 is the PWM signal to LED current delay. This delay is typically less than 500 ns, which allows greater accuracy at low PWM dimming duty cycles, as shown in Figure 14.

APWM pin

The APWM pin is used in conjunction with the ISET pin (see Figure 15). This is a digital signal pin that internally adjusts the ISET current. When this pin is not used it should be tied to ground.

The typical input signal frequency is between 20 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current that is delivered to the LEDs (Figure 16).

To use this pin for a trim function, the user should set the maximum output current to a value higher than the required current by at least 5%. The LED I_{SET} current is then trimmed down to the appropriate value. Another consideration that also is important is the limitation of the user APWM signal duty cycle. In some cases it might be preferable to set the maximum I_{SET} current to be 25% to 50% higher, thus allowing the APWM signal to have duty cycles that are between 25% and 50%.

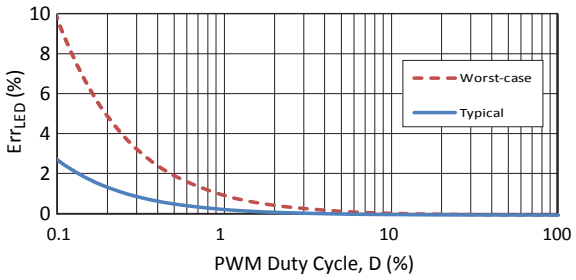


Figure 14: Percentage Error of the LED current versus PWM duty cycle (at 200 Hz PWM frequency).

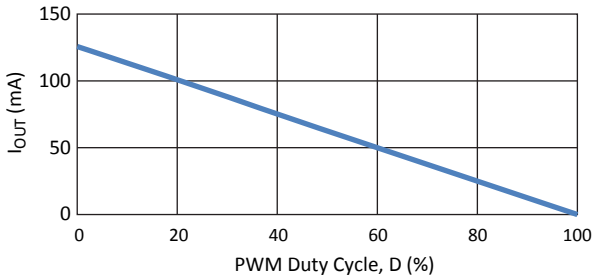


Figure 16: Output current versus duty cycle; 200 kHz APWM signal.

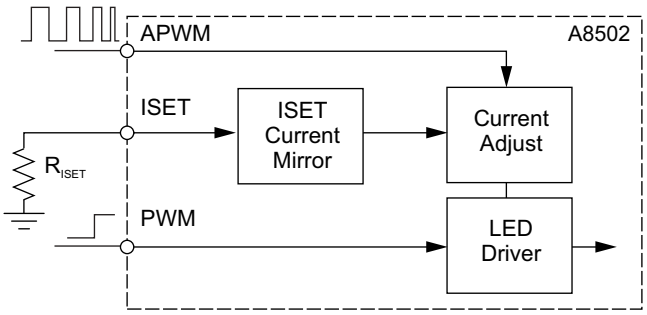


Figure 15: Simplified block diagram of the APWM and ISET circuit.

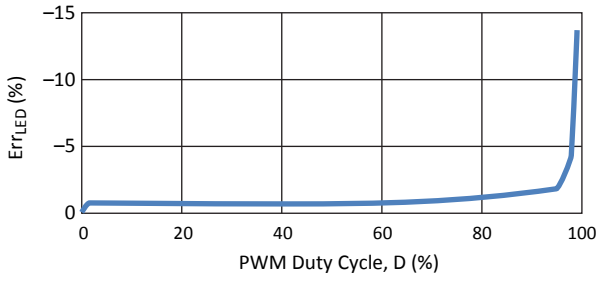


Figure 17: Percentage Error of the LED current versus PWM duty cycle; 200 kHz APWM signal.

As an example, a system that delivers a full LED current of 120 mA per LED would deliver 90 mA of current per LED when an APWM signal is applied with a duty cycle of 25% (Figure 18 and Figure 19).

Although the APWM dimming function has a wide frequency range, if this function is used strictly as an analog dimming function it is recommended to use frequency ranges between 50 and 500 kHz for best accuracy. The frequency range must be considered only if the user is not using this function as a closed loop trim function. Another limitation is that the propagation delay between this APWM signal and I_{OUT} takes several milliseconds to change the actual LED current. This effect is shown in Figure 18, Figure 19, and Figure 20.

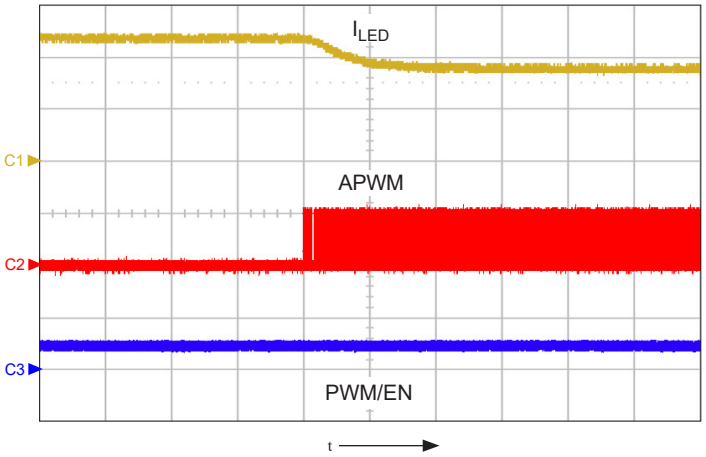


Figure 18: Diagram showing the transition of LED current from 120 mA to 90 mA, when a 25% duty cycle signal is applied to the APWM pin; PWM = 1; shows I_{LED} (ch1, 50 mA/div.), APWM (ch2, 5 V/div.), and PWM/EN (ch3, 5 V/div.), time = 500 µs/div.

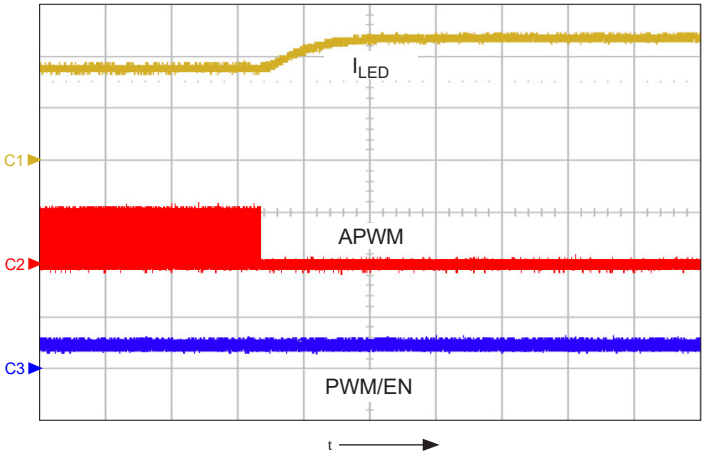


Figure 19: Diagram showing the transition of LED current from 90 mA to 120 mA, when a 25% duty cycle signal is removed from the APWM pin. PWM = 1; shows I_{LED} (ch1, 50 mA/div.), APWM (ch2, 5 V/div.), and PWM/EN (ch3, 5 V/div.), time = 500 µs/div.

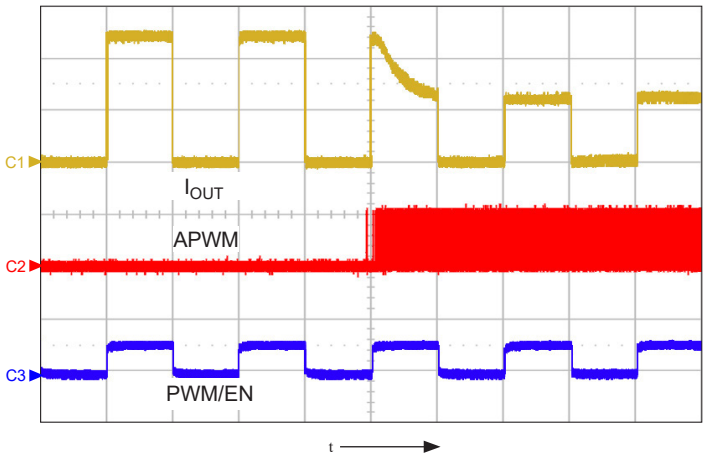


Figure 20: Transition of output current level when a 50% duty cycle signal is applied to the APWM pin, in conjunction with a 50% duty cycle PWM dimming being applied to the PWM pin; shows I_{OUT} (ch1, 100 mA/div.), APWM (ch2, 5 V/div.), and PWM/EN (ch3, 5 V/div.), time = 1 ms/div.

Analog dimming

The A8502 can also be dimmed by using an external DAC or another voltage source applied either directly to the ground side of the R_{ISET} resistor or through an external resistor to the ISET pin (see Figure 20). The limit of this type of dimming depends on the range of the ISET pin. In the case of the A8502 the limit is 40 to 125 µA.

• For a single resistor (panel A of Figure 21), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}} \quad (3)$$

where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

When the DAC voltage is 0 V the LED current will be at its maximum. To keep the internal gain amplifier stable, the user should not decrease the current through the R_{ISET} resistor to less than 40 µA

• For a dual-resistor configuration (panel B of Figure 21), the I_{SET} current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET}}{R_{ISET}} - \frac{V_{DAC} - V_{ISET}}{R_1} \quad (4)$$

The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the R_{ISET} resistor:

- V_{DAC} = 1.003 V; the output is strictly controlled by R_{ISET}
- V_{DAC} > 1.003 V; the LED current is reduced
- V_{DAC} < 1.003 V; the LED current is increased

LED short detect

Both LEDx pins are capable of handling the maximum V_{OUT} that the converter can deliver, thus providing protection from the LEDx pin to V_{OUT} in the event of a connector short.

An LEDx pin that has a voltage exceeding V_{LEDSC} will be removed from operation (see Figure 22). This is to prevent the IC from dissipating too much power by having a large voltage present on an LEDx pin.

While the IC is being PWM-dimmed, the IC rechecks the disabled LED every time the PWM signal goes high, to prevent false tripping of an LED short event. This also allows some self-correction if an intermittent LED pin short to V_{OUT} is present.

Overvoltage protection

The A8502 has overvoltage protection (OVP) and open Schottky diode (D1 in Figure 1) protection. The OVP protection has a

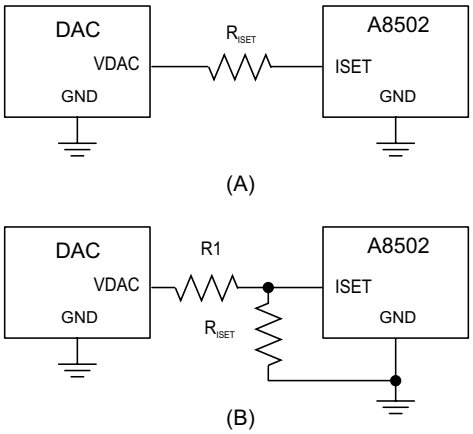


Figure 21: Simplified diagrams of voltage control of I_{LED}: typical applications using a DAC to control I_{LED} using a single resistor (upper), and dual resistors (lower).

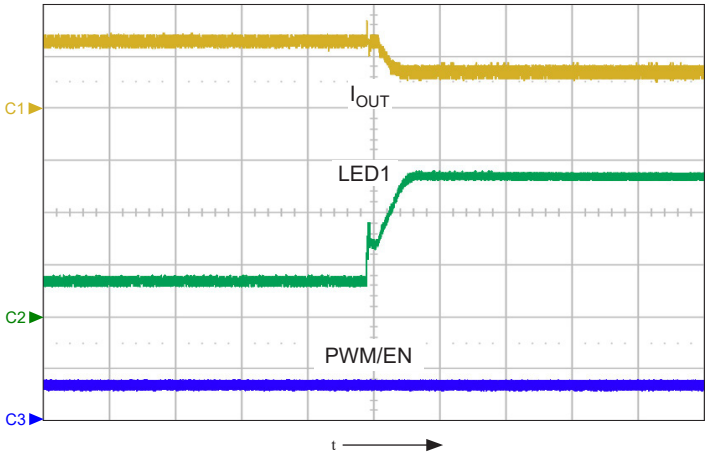


Figure 22: Example of the disabling of an LED string when the LED pin voltage is increased above 4.6 V; shows I_{OUT} (ch1, 200 mA/div.), LED1 (ch2, 5 V/div.), and PWM/EN (ch3, 5 V/div.), time = 10 µs/div.

default level of 8.1 V and can be increased up to 53 V by connecting resistor R_{OVP} between the OVP pin and V_{OUT}. When the current into the OVP pin exceeds 199 µA (typical), the OVP comparator goes low and the boost stops switching.

The following equation can be used to determine the resistance for setting the OVP level:

$$R_{OVP} = (V_{OUTovp} - V_{OVP(th)}) / I_{OVPH} \quad (5)$$

where:

V_{OUTovp} is the target overvoltage level,

R_{OVP} is the value of the external resistor, in Ω,

$V_{OVP(th)}$ is the pin OVP trip point found in the Electrical Characteristics table, and

I_{OVPH} is the current into the OVP pin.

There are several possibilities for why an OVP condition would be encountered during operation, the two most common being: a disconnected output, and an open LED string. Examples of these are provided in Figure 23 and Figure 24.

Figure 23 illustrates when the output of the A8502 is disconnected from load during normal operation. The output voltage instantly increases up to OVP voltage level and then the boost stops switching to prevent damage to the IC. If the output is drained off, eventually the boost might start switching for a short duration until the OVP threshold is hit again.

Figure 24 displays a typical OVP event caused by an open LED string. After the OVP condition is detected, the boost stops switching, and the open LED string is removed from operation. Afterwards V_{OUT} is allowed to fall, and eventually the boost will resume switching and the A8502 will resume normal operation.

A8502 also has built-in secondary overvoltage protection to protect the internal switch in the event of an open diode condition. Open Schottky diode detection is implemented by detecting overvoltage on the SW pin of the device. If voltage on the SW

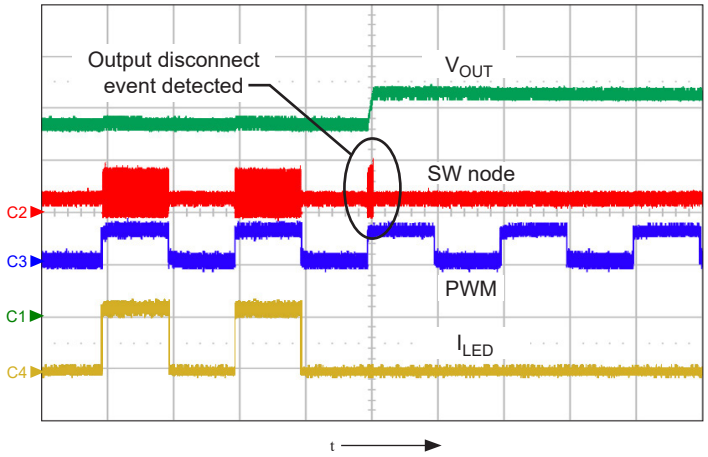


Figure 23: OVP protection in an output disconnect event; shows V_{OUT} (ch1, 10 V/div.), SW node (ch2, 50 V/div.), PWM (ch3, 5 V/div.), and I_{LED} (ch4, 200 mA/div.), time = 1 ms/div.

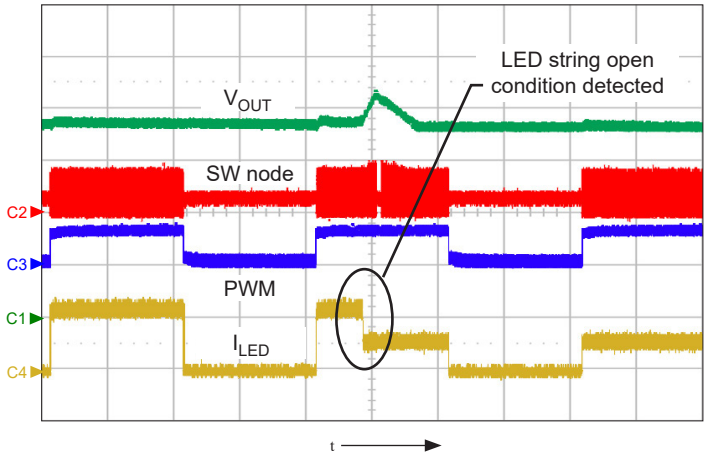


Figure 24: OVP protection in an open LED string event; shows V_{OUT} (ch1, 10 V/div.), SW node (ch2, 50 V/div.), PWM (ch3, 5 V/div.), and I_{LED} (ch4, 200 mA/div.), time = 500 µs/div.

pin exceeds the device safe operating voltage rating, the A8502 disables and remains latched. To clear this fault, the IC must be shut down either by using the PWM/EN signal or by going below the UVLO threshold on the VIN pin. Figure 25 illustrates this. As soon as the switch node voltage (SW) exceeds 60 V, the IC shuts down. Due to small delays in the detection circuit, as well as there being no load present, the switch node voltage will rise above the trip point voltage.

Figure 26 illustrates when the A8502 is being enabled during an open diode condition. The IC goes through all of its initial LED detection and then tries to enable the boost, at which point the open diode is detected.

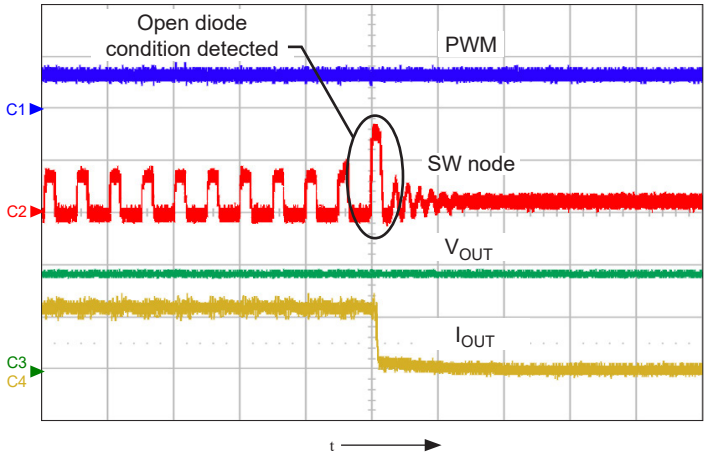


Figure 25: OVP protection in an open Schottky diode event, while the IC is in normal operation; shows PWM (ch1, 5 V/div.), SW node (ch2, 50 V/div.), V_{OUT} (ch3, 20 V/div.), and I_{OUT} (ch4, 200 mA/div.), time = 1 µs/div.

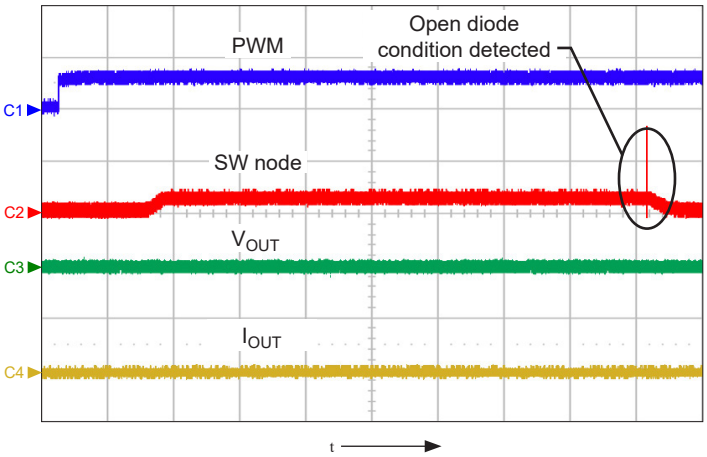


Figure 26: OVP protection when the IC is enabled during an open diode condition; shows PWM (ch1, 5 V/div.), SW node (ch2, 50 V/div.), V_{OUT} (ch3, 10 V/div.), and I_{OUT} (ch4, 200 mA/div.), time = 500 µs/div.

Boost switch overcurrent protection

The boost switch is protected with cycle-by-cycle current limiting set at a minimum of 3.0 A. There is also a secondary current limit that is sensed on the boost switch. When detected this current limit immediately shuts down the A8502. The level of this current limit is set above the cycle-by-cycle current limit to protect the switch from destructive currents when the boost inductor is shorted. Various boost switch overcurrent conditions are shown in Figure 27, Figure 28, and Figure 29.

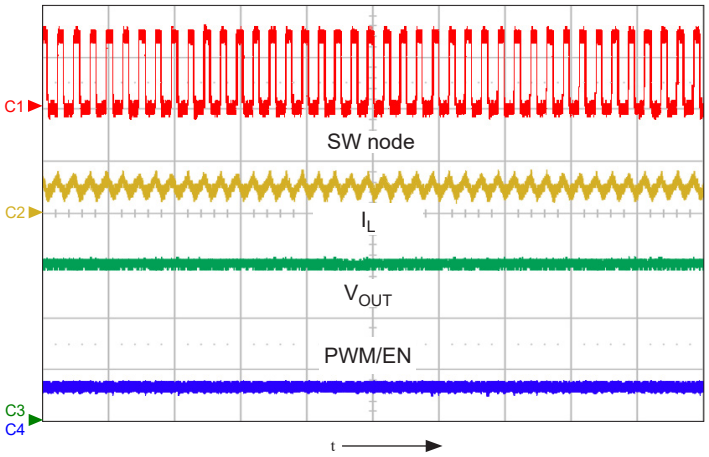


Figure 27: Normal operation of the switch node (SW); inductor current (I_L) and output voltage (V_{OUT}) for 9 series LEDs in each of 2 strings configuration; shows SW node (ch1, 20 V/div.), inductor current, I_L (ch2, 1 A/div.), V_{OUT} (ch3, 10 V/div.), and PWM/EN (ch4, 5 V/div.), time = 2 µs/div.

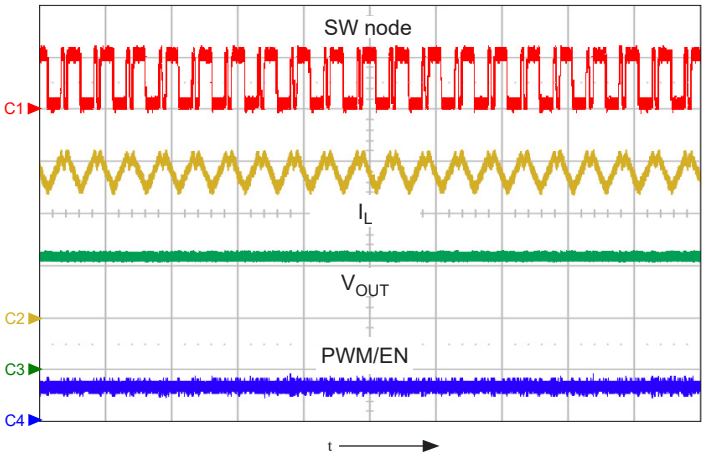


Figure 28: Cycle-by-cycle current limiting; inductor current (yellow trace, I_L), note reduction in output voltage as compared to normal operation with the same configuration (Figure 24); shows SW node (ch1, 20 V/div.), inductor current, I_L (ch2, 1 A/div.), V_{OUT} (ch3, 10 V/div.), and PWM/EN (ch4, 5 V/div.), time = 2 µs/div.

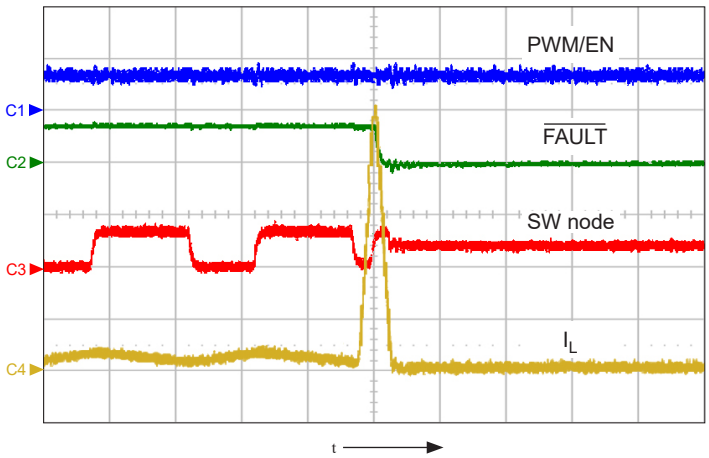


Figure 29: Secondary boost switch current limit; when this limit is hit, the A8502 immediately shuts down; shows PWM/EN (ch1, 5 V/div.), $\overline{FAULT}$ (ch2, 5 V/div.), SW node (ch3, 50 V/div.), and inductor current, I_L (ch4, 2 A/div.), time = 100 ns/div.

Input overcurrent protection and disconnect switch

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition. The external circuit implementing the disconnect is shown in Figure 30. If the input disconnect switch is not used, the VSENSE pin must be tied to VIN and the GATE pin must be left open.

When selecting the external PMOS, check for the following parameters:

- Drain-source breakdown voltage $V_{(BR)DSS} > -40$ V
- Gate threshold voltage (make sure it is fully conducting at V_{GS} = -4 V, and cut-off at –1 V)
- $R_{DS(on)}$: Make sure the on-resistance is rated at V_{GS} = -4.5 V or similar, not at -10 V; derate it for higher temperature

The input disconnect switch has two modes of operation:

• **1X mode** When the input current is between one and two times the preset current limit value, the disconnect switch enters a constant-current mode for a maximum duration of 10,000 cycles or 5 ms at 2 MHz. During this time, the Fault flag is set immediately and the disconnect switch goes into a linear mode of operation, in which the input current will be limited to a value approximate to the 1X current trip point level (Figure 31). If the fault corrects itself before the expiration of the timer, the Fault flag will be removed and normal operation will resume.

The user can also during this time decide whether to shut down the A8502. To immediately shut down the device, pull the FSET/SYNC pin low for more than 7 µs. After the FSET/SYNC pin has been low for a period longer than 7 µs, the IC will stop switching, the input disconnect switch will open, and the LEDx pins will stop sinking current. The A8502 can be powered-down into low power mode. To do so, disable the IC by keeping the PWM/EN pin low for a period of 32,750 clock cycles. To keep the discon-

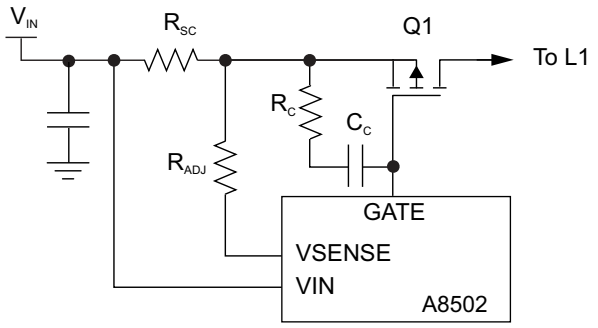


Figure 30: Typical circuit showing the implementation of the input disconnect feature.

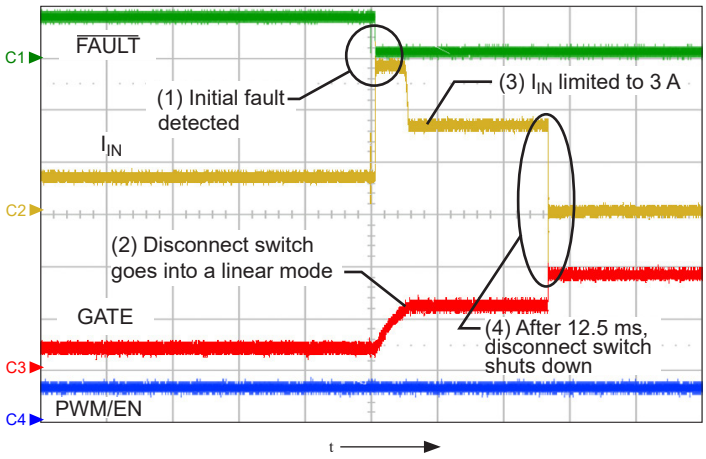


Figure 31: Showing typical wave forms for a 3-A, 1X current limit under a fault condition; shows f_{SW} = 800 kHz, $\overline{\text{FAULT}}$ (ch1, 5 V/div.), I_{IN} (ch2, 2 A/div.), GATE (ch3, 5 V/div.), and PWM/EN (ch4, 5 V/div.), time = 5 ms/div.

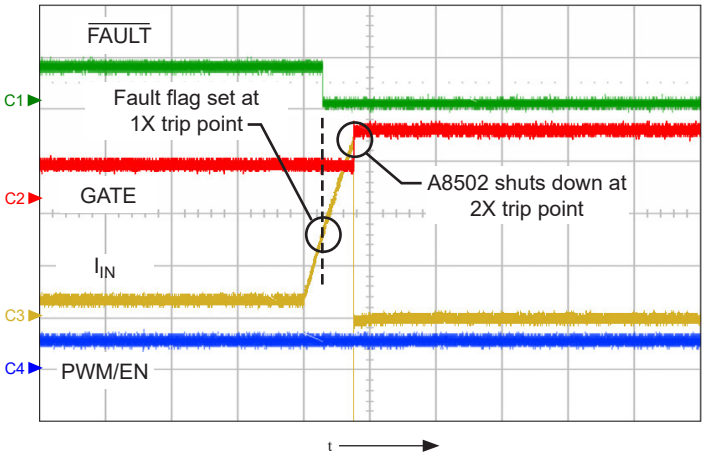


Figure 32: 2X mode, secondary overcurrent fault condition. I_{IN} is the input current through the switch. The Fault flag is set at the 1X current limit, and when the 2X current limit is reached the A8502 disables the gate of the disconnect switch (GATE); shows $\overline{\text{FAULT}}$ (ch1, 5 V/div.), GATE (ch2, 10 V/div.), I_{IN} (ch3, 2 A/div.), and PWM/EN (ch4, 5 V/div.), time = 5 µs/div.

nect switch stable while the disconnect switch is in 1X mode, use a 22 nF capacitor for C_C and a 20 Ω resistor for R_C.

• **2X current limit** If the input current level goes above 2X of the preset current limit threshold, the A8502 will shut down in less than 3 µs regardless of user input (Figure 32). This is a latched condition. The Fault flag is also set to indicate a fault. This feature is meant to prevent catastrophic failure in the system due to inductor short to ground, switch pin short to ground, or output short to ground.

Setting the current sense resistor

The typical threshold for the current sense circuit is 104 mV, when R_{ADJ} is 0 Ω. This voltage can be trimmed by the R_{ADJ} resistor. The typical 1X trip point should be set at about 3 A, which coincides with the cycle-by-cycle current limit minimum threshold.

For example, given 3 A of input current, and the calculated maximum value of the sense resistor, R_{SC} = 0.033 Ω.

The R_{SC} chosen is 0.03 Ω, a standard.

Also:

$$R_{ADJ} = (V_{SENSETRIP} - V_{ADJ}) / I_{ADJ} \quad (6)$$

The trip point voltage is calculated as:

$$V_{ADJ} = 3.0\ A \times 0.03\ \Omega = 0.090\ V$$

$$R_{ADJ} = (0.104 - 0.09\ V) / (20.3\ \mu A) = 731\ \Omega$$

Input UVLO

When V_{IN} and V_{SENSE} rise above the $V_{UVLOrise}$ threshold, the A8502 is enabled. A8502 is disabled when V_{IN} falls below the $V_{UVLOfall}$ threshold for more than 50 µs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply. When V_{IN} falls below 4.35 V, the IC will shut down (see Figure 33).

VDD

The VDD pin provides regulated bias supply for internal circuits. Connect the capacitor C_{VDD} with a value of 0.1 µF or greater to this pin. The internal LDO can deliver no more than 2 mA of current with a typical V_{DD} of about 3.5 V, enabling this pin to serve as the pull-up voltage for the $\overline{FAULT}$ pin.

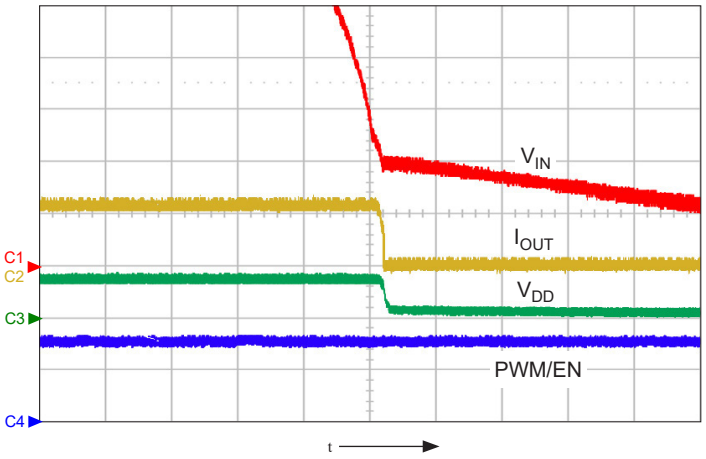


Figure 33: Shutdown showing a falling input voltage (V_{IN}); shows V_{IN} (ch1, 2 V/div.), I_{OUT} (ch2, 200 mA/div.), V_{DD} (ch3, 5 V/div.), and PWM/EN (ch4, 2 V/div.), time = 5 ms/div.

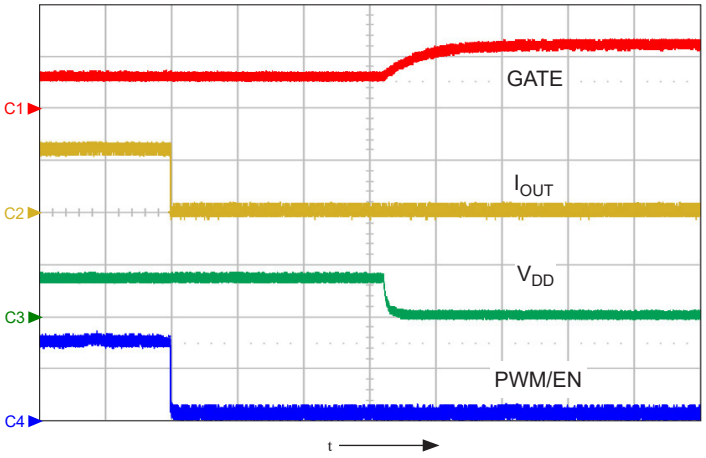


Figure 34: Shutdown using the enable function, showing the 16 ms delay between the PWM/EN signal and when the VDD and GATE of the disconnect switch turns off; shows GATE (ch1, 10 V/div.), I_{OUT} (ch2, 200 mA/div.), V_{DD} (ch3, 5 V/div.), and PWM/EN (ch4, 2 V/div.), time = 5 ms/div.

Shutdown

If the PWM/EN pin is pulled low for more than t_{PWML} (32,750 clock cycles), the device enters shutdown mode and clears all internal fault registers. As an example, at a 2 MHz clock frequency, it will take approximately 16.3 ms to shut down the IC into the low power mode (Figure 34). When the A8502 is shut down, the IC will disable all current sources and wait until the PWM/EN signal goes high to re-enable the IC. If faster shut down is required, the FSET/SYNC pin can be used.

Fault protection during operation

The A8502 constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the Fault Mode table.

The possible fault conditions that the device can detect are: Open LED pin, LED pin shorted to ground, shorted inductor, V_{OUT} short to ground, SW pin shorted to ground, ISET pin shorted to ground, and input disconnect switch source shorted to ground.

Note the following:

- Some of the protection features might not be active during startup, to prevent false triggering of fault conditions.
- Some of these faults will not be protected if the input disconnect switch is not being used. An example of this is V_{OUT} short to ground.

Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	Sink Driver
Primary switch overcurrent protection (cycle-by-cycle current limit)	Auto-restart	Always	No	This fault condition is triggered by the cycle-by-cycle current limit, $I_{SW(LIM)}$.	Off for a single cycle	On	On
Secondary switch current limit	Latched	Always	Yes	When the current through the boost switch exceeds secondary current SW limit ($I_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers, and boost. The Fault flag is set. To re-enable the device, the PWM/EN pin must be pulled low for 32,750 clock cycles.	Off	Off	Off
Input disconnect current limit	Latched	Always	Yes	The device is immediately shut off if the voltage across the input sense resistor is 2X the preset current value. The Fault flag is set. If the input current limit is between 1X and 2X, the Fault flag is set but the IC will continue to operate normally for $t_{GFAULT1}$ or until it is shut down. To re-enable the device the PWM/EN pin must be pulled low for 32,750 clock cycles.	Off	Off	Off
Secondary OVP	Latched	Always	Yes	Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(SEC)}$ is reached. This fault latches the IC. The input disconnect switch is disabled as well as the LED drivers, and the Fault flag is set. To re-enable the part the PWM pin must be pulled low for 32,750 clock cycles.	Off	Off	Off

Continued on the next page…

Fault Mode Table (continued)

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	Sink driver
LED Pin Short Protection	Auto-restart	Startup	No	This fault prevents the device from starting-up if either of the LEDx pins are shorted. The device stops soft-start from starting while either of the LEDx pins are determined to be shorted. After the short is removed, soft-start is allowed to start.	Off	On	Off
LED Pin open	Auto-restart	Normal Operation	No	When an LEDx pin is open the device will determine which LED pin is open by increasing the output voltage until OVP is reached. Any LED string not in regulation will be turned off. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	On	On	Off for open pins. On for all others.
ISET Short Protection	Auto-restart	Always	No	This fault occurs when the ISET current goes above 150% of the maximum current. The boost will stop switching, the disconnect switch will turn off, and the IC will disable the LED sinks until the fault is removed. When the fault is removed the IC will try to to regulate to the preset LED current.	Off	On	Off
FSET/SYNC Short Protection	Auto-restart	Always	Yes	Fault occurs when the FSET/SYNC current goes above 150% of maximum current, about 180 µA. The boost will stop switching, the disconnect switch will turn off, and the IC will disable the LED sinks until the fault is removed. When the fault is removed the IC will try to restart with soft-start.	Off	Off	Off
Overvoltage Protection	Auto-restart	Always	No	Fault occurs when OVP pin exceeds $V_{OVP(th)}$ threshold. The A8502 will immediately stop switching to try to reduce the output voltage. If the output voltage decreases then the A8502 will restart switching to regulate the output voltage.	Stop during OVP event.	On	On
LED Short Protection	Auto-restart	Always	No	Fault occurs when the LED pin voltage exceeds V_{LEDSC}. When the LED short protection is detected the LED string that is above the threshold will be removed from operation.	On	On	Off for shorted pins. On for all others.
Overtemperature Protection	Auto-restart	Always	No	Fault occurs when the die temperature exceeds the overtemperature threshold, 165°C.	Off	Off	Off
VIN UVLO	Auto-restart	Always	No	Fault occurs when V_{IN} drops below V_{UVLO}, 3.90 V maximum. This fault resets all latched faults.	Off	Off	Off

APPLICATION INFORMATION

Design Example for Boost Configuration

This section provides a method for selecting component values when designing an application using the A8502. The resulting design is diagrammed in Figure 35.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 10 to 14 V
- Quantity of LED channels, $\#_{CHANNELS}$: 2
- Quantity of series LEDs per channel, $\#_{SERIESLEDS}$: 10
- LED current per channel, I_{LED}: 120 mA
- LED V_f at 120 mA: 3.2 V
- f_{SW}: 2 MHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% duty cycle

Procedure: The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence.

Step 1: Connect LEDs to pins LED1 and LED2.

Step 2: Determining the LED current setting resistor R_{ISET}:

$$R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED} \quad (7)$$
$$= (1.003\ (V) \times 980) / 120\ (mA) = 8.19\ k\Omega$$

Choose a 8.25 kΩ resistor.

Step 3: Determining the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter.

Step 3a: The first step is determining the maximum voltage based on the LED requirements. The regulation voltage, V_{LED}, of the A8502 is 720 mV. A constant term, 2 V, is added to give margin to the design due to noise and output voltage ripple.

$$V_{OUT(OVP)} = \#_{SERIESLEDS} \times V_f + V_{LED} + 2\ (V) \quad (8)$$
$$= 10 \times 3.2\ (V) + 0.720\ (V) + 2\ (V)$$
$$= 34.72\ V$$

Then the OVP resistor is:

$$R_{OVP} = (V_{OUT(OVP)} - V_{OVP(th)}) / I_{OVPH} \quad (9)$$
$$= (34.72\ V - 8.1\ V) / 199\ \mu A = 133.77\ k\Omega$$

where both I_{OVPH} and $V_{OVP(th)}$ are taken from the Electrical Characteristics table.

Chose a value of resistor that is higher value than the calculated R_{OVP}. In this case a value of 137 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor:

$$V_{OUT(OVP)} = 137\ (k\Omega) \times 199\ (\mu A) + 8.1\ (V) = 35.36\ V$$

Step 3b: At this point a quick check must be done to determine if the conversion ratio is acceptable for the selected frequency.

$$D_{maxofboost} = 1 - t_{SWOFFTIME} \times f_{SW} \quad (10)$$
$$= 1 - 68\ (ns) \times 2\ (MHz) = 86.4\%$$

where the minimum off-time ($t_{SWOFFTIME}$) is found in the Electrical Characteristics table.

The Theoretical Maximum V_{OUT} is then calculated as:

$$V_{OUT}(max) = \frac{V_{IN}(min)}{1 - D_{maxofboost}} - V_d \quad (11)$$
$$= \frac{10\ (V)}{1 - 0.864} - 0.4\ (V) = 73.13\ V$$

where V_d is the diode forward voltage.

The Theoretical Maximum V_{OUT} value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, the switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirements.

Step 4: Selecting the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system must operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determining the duty cycle, calculated as follows:

$$D(\text{max}) = 1 - \frac{V_{IN}(\text{min})}{V_{OUT(OVP)} + V_d} \quad (12)$$

$$= 1 - \frac{10\ (\text{V})}{35.36\ (\text{V}) + 0.4\ (\text{V})} = 72.04\%$$

Step 4b: Determining the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor. First, the maximum input current, given:

$$I_{OUT} = \#_{CHANNELS} \times I_{LED} \quad (13)$$

$$= 2 \times 0.120\ (\text{A}) = 0.240\ \text{A}$$

then:

$$I_{IN}(\text{max}) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\text{min}) \times \eta} \quad (14)$$

$$= \frac{35.36\ (\text{V}) \times 240\ (\text{mA})}{10\ (\text{V}) \times 0.90} = 0.94\ \text{A}$$

where η is efficiency.

Next, calculate minimum input current, as follows:

$$I_{IN}(\text{min}) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\text{max}) \times \eta} \quad (15)$$

$$= \frac{35.36\ (\text{V}) \times 240\ (\text{mA})}{14\ (\text{V}) \times 0.90} = 0.67\ \text{A}$$

A good approximation of efficiency, η, can be taken from the efficiency curves located in the datasheet. A value of 90% is a good starting approximation.

Step 4c: Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor must be set such that the ½ inductor ripple current is not greater than the average minimum input current. As a first pass assume I_{ripple} to be 40% of the maximum inductor current:

$$\Delta I_L = I_{IN}(\text{max}) \times I_{ripple} \quad (16)$$

$$= 0.94\ (\text{A}) \times 0.40 = 0.376\ \text{A}$$

then:

$$L = \frac{V_{IN}(\text{min})}{\Delta I_L \times f_{SW}} \times D(\text{max}) \quad (17)$$

$$= \frac{10\ (\text{V})}{0.376\ (\text{A}) \times 2\ (\text{MHz})} \times 0.72 = 9.57\ \mu\text{H}$$

Step 4d: Double-check to make sure the ½ current ripple is less than $I_{IN}(\text{min})$:

$$I_{IN}(\text{min}) > {}^1/_2\ \Delta I_L \quad (18)$$

$$0.67\ \text{A} > 0.19\ \text{A}$$

A good inductor value to use would be 10 µH.

Step 4e: This step is used to verify that there is sufficient slope compensation for the inductor chosen. The slope compensation value is determined by the following formula:

$$\text{Slope Compensation} = \frac{3.6 \times f_{SW}}{2 \times 10^6} = 3.6\ \text{A}/\mu\text{s} \quad (19)$$

Next insert the inductor value used in the design:

$$\Delta I_{Lused} = \frac{V_{IN}(\text{min}) \times D(\text{max})}{L_{used} \times f_{SW}} \quad (20)$$

$$= \frac{10\ (\text{V}) \times 0.72}{10\ (\mu\text{H}) \times 2.0\ (\text{MHz})} = 0.36\ \text{A}$$

Calculate the minimum required slope:

$$\text{Required Slope (min)} = \frac{\Delta I_{Lused} \times 1 \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D(\text{max}))} \quad (21)$$

$$= \frac{0.36\ (\text{A}) \times 1 \times 10^{-6}}{\frac{1}{2.0\ (\text{MHz})} \times (1 - 0.72)} = 2.57\ \text{A}/\mu\text{s}$$

If the minimum required slope is greater than the calculated slope compensation, the inductor value must be increased.

Note: The slope compensation value is in A/µs, and 1×10^{-6} is a constant multiplier.

Step 4f: Determining the inductor current rating. The inductor current rating must be greater than the $I_{IN}(\text{max})$ value plus half of the ripple current ΔI_L, calculated as follows:

$$L(\text{min}) = I_{IN}(\text{max}) + {}^1/_2\,\Delta I_{Lused} \quad (22)$$

$$= 0.94\ (\text{A}) + 0.36\ (\text{A}) / 2 = 1.12\ \text{A}$$

Step 5: Determining the resistor value for a particular switching frequency. Use the R_{FSET} values shown in Figure 7. For example, a 10 kΩ resistor will result in a 2 MHz switching frequency.

Step 6: Choosing the proper switching diode. The switching diode must be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are: current rating of the diode and reverse voltage rating.

The reverse voltage rating should be such that during operation condition, the voltage rating of the device is larger than the maximum output voltage. In this case it is $V_{OUT(OVP)}$.

The peak current through the diode is calculated as:

$$I_{dp} = I_{IN}(max) + {}^{1}/_{2}\,\Delta I_{Lused} \quad (23)$$
$$= 0.94\ (A) + 0.36\ (A) / 2 = 1.12\ A$$

The third major component in deciding the switching diode is the reverse current, I_R, characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding off of the output voltage, due to leakage currents. I_R can be a large contributor, especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA.

Step 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor are: PWM dimming frequency and PWM duty cycle. Another major contributor is leakage current, I_{LK}. This current is the combination of the OVP leakage current as well as the reverse current of the switching diode. In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically, the voltage variation on the output, V_{COUT}, during PWM dimming must be less than 250 mV, so that no audible hum can be heard. The capacitance can be calculated as follows:

$$C_{OUT} = I_{LK} \times \frac{1 - D(min)}{f_{PWM(dimming)} \times V_{COUT}} \quad (24)$$
$$= 200\ (\mu A) \times \frac{1 - 0.01}{200\ (Hz) \times 0.250\ (V)} = 3.96\ \mu F$$

A capacitor larger than 3.96 µF should be selected due to degradation of capacitance at high voltages on the capacitor. A ceramic 4.7 µF 50 V capacitor is a good choice to fulfill this requirement. Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

The rms current through the capacitor is given by:

$$I_{COUT}rms = I_{OUT} \sqrt{\frac{D(max) + \frac{\Delta I_{Lused}}{I_{IN}(max) \times 12}}{1 - D(max)}} \quad (25)$$
$$= 0.240\ (A) \sqrt{\frac{0.72 + \frac{0.36\ (A)}{0.94\ (A) \times 12}}{1 - 0.72}} = 0.39\ A$$

The output capacitor must have a current rating of at least 390 mA. The capacitor selected in this design was a 4.7 µF 50 V capacitor with a 3 A current rating.

Step 8: Selecting input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A good estimation rule is to set the input voltage ripple, ΔV_{IN}, to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (26)$$
$$= \frac{0.36\ (A)}{8 \times 2\ (MHz) \times 0.1\ (V)} = 0.23\ \mu F$$

The rms current through the capacitor is given by:

$$C_{IN}rms = \frac{I_{OUT} \times \frac{\Delta I_{Lused}}{I_{IN}(max)}}{(1 - D) \times \sqrt{12}} \quad (27)$$
$$= \frac{0.240\ (A) \times \frac{0.36\ (A)}{0.94\ (A)}}{(1 - 0.72) \times \sqrt{12}} = 0.095\ A$$

A good ceramic input capacitor with ratings of 2.2 µF 50 V or 4.7 µF 50 V will suffice for this application. Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

Step 9: Choosing the input disconnect switch components. Set the input disconnect 1X current limit to 3 A by choosing a sense resistor. The calculated maximum value of the sense resistor is:

$$R_{SC}(\text{max}) = V_{SENSEtrip} / 3.0\ (\text{A}) \quad (28)$$
$$= 0.104\ (\text{V}) / 3.0\ (\text{A}) = 0.035\ \Omega$$

The R_{SC} chosen is 0.033 Ω, a standard.

The trip point voltage must be:

$$V_{ADJ} = 3.0\ (\text{A}) \times 0.033\ (\Omega) = 0.099\ (\text{V}), \text{ therefore}$$
$$R_{ADJ} = (V_{SENSEtrip} - V_{ADJ}) / I_{ADJ}\ (\text{typ}) \quad (29)$$
$$= (0.104\ (\text{V}) - 0.099\ (\text{V})) / 20.3\ (\mu\text{A}) = 246.31\ \Omega$$

A value of 249 Ω was chosen for this design.

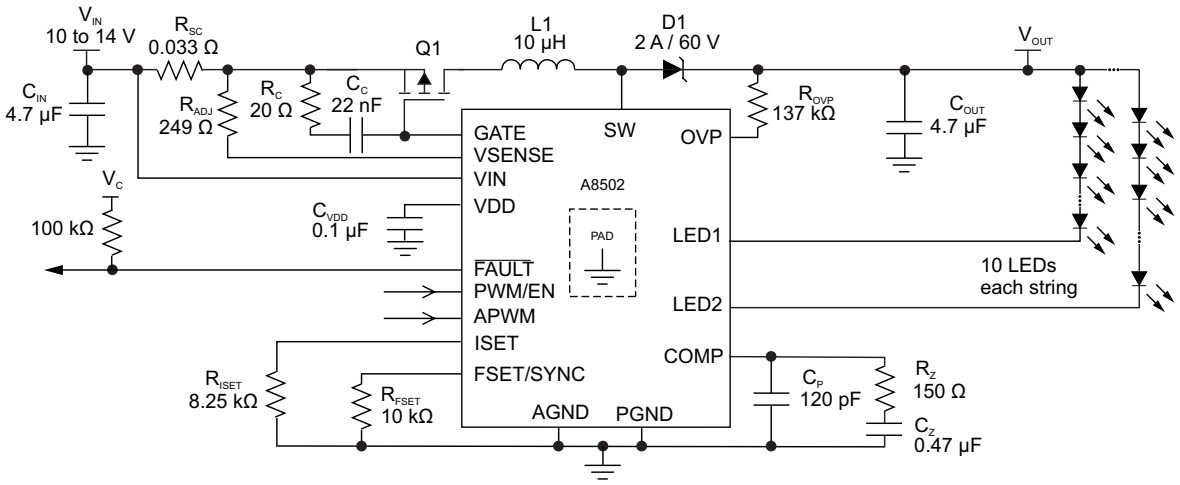


Figure 35: The schematic diagram showing calculated values from the design example above.

Design Example for SEPIC Configuration

This section provides a method for selecting component values when designing an application using the A8502 in SEPIC (Single-Ended Primary-Inductor Converter) circuit. SEPIC topology has the advantage that it can generate a positive output voltage either higher or lower than the input voltage. The resulting design is diagrammed in Figure 36.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 6 to 14 V (V_{IN}(min): 5 V and V_{IN}(max): 16 V)
- Quantity of LED channels, $\#_{CHANNELS}$: 2
- Quantity of series LEDs per channel, $\#_{SERIESLEDS}$: 4
- LED current per channel, I_{LED}: 120 mA
- LED V_f at 120 mA: ≈ 3.3 V
- f_{SW}: 2 MHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% duty cycle

Procedure: The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence.

Step 1: Connect LEDs to pins LED1 and LED2. Note: if only one LED channel is needed, the unused LEDx pin should be pulled to ground using a 1.5 kΩ resistor. Alternatively, short the LED1 and LED2 pins together, and half the LED current, to 60 mA per channel.

Step 2: Determining the LED current setting resistor R_{ISET}:

$$R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED} \quad (30)$$
$$= (1.003\ (V) \times 980) / 120\ mA = 8.19\ k\Omega$$

Choose a 8.25 kΩ resistor 1% resistor (or 16.2 kΩ if I_{LED} is 60mA/channel).

Step 3: Determining the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter.

Step 3a: The first step is determining the maximum voltage based on the LED requirements. The regulation voltage, V_{LED}, of the A8502 is 720 mV. A constant term, 2 V, is added to give margin to the design due to noise and output voltage ripple.

$$V_{OUT(OVP)} = \#_{SERIESLEDS} \times V_f + V_{LED} + 2\ (V) \quad (31)$$
$$= 4 \times 3.2\ (V) + 0.720\ (V) + 2\ (V) = 15.9\ V$$

Then the OVP resistor is:

$$R_{OVP} = (V_{OUT(OVP)} - V_{OVP(th)}) / I_{OVPH} \quad (32)$$
$$= (15.9\ (V) - 8.1\ (V)) / 0.199\ (mA) = 39.196\ k\Omega$$

where both I_{OVPH} and $V_{OVP(th)}$ are taken from the Electrical Characteristics table.

In this case a value of 39.2 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor:

$$V_{OUT(OVP)} = 39.2\ (k\Omega) \times 0.199\ (mA) + 8.1\ (V) = 15.9\ V$$

Step 3b: At this point a quick check must be done to determine if the conversion ratio is acceptable for the selected frequency.

$$D_{max} = 1 - t_{SWOFFTIME} \times f_{SW} \quad (33)$$
$$= 1 - 68\ (ns) \times 2\ (MHz) = 86.4\%$$

where the minimum off-time ($t_{SWOFFTIME}$) is found in the Electrical Characteristics table.

The Theoretical Maximum V_{OUT} is then calculated as:

$$V_{OUT}(max) = V_{IN}(min) \times \frac{D_{max}}{1 - D_{max}} - V_d \quad (34)$$
$$= 5\ (V) \times \frac{0.86}{1 - 0.86} - 0.4\ (V) = 30.3\ V$$

where V_d is the diode forward voltage.

The Theoretical Maximum V_{OUT} value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, the switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirements.

Step 4: Selecting the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system must operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determining the duty cycle, calculated as follows:

$$D(\max) = \frac{V_{OUT(OVP)} + V_d}{V_{IN}(\min) + V_{OUT(OVP)} + V_d} \quad (35)$$

$$= \frac{15.9\ (V) + 0.4\ (V)}{5\ (V) + 15.9\ (V) + 0.4\ (V)} = 76.5\%$$

Step 4b: Determining the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor. First, the maximum input current, given:

$$I_{OUT} = \#_{CHANNELS} \times I_{LED} \quad (36)$$

$$= 2 \times 0.120\ (A) = 0.240\ A$$

then:

$$I_{IN}(\max) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\min) \times \eta} \quad (37)$$

$$= \frac{15.9\ (V) \times 0.24\ (A)}{5\ (V) \times 0.90} = 0.848\ A$$

where η is efficiency.

Next, calculate minimum input current, as follows:

$$I_{IN}(\min) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\max) \times \eta} \quad (38)$$

$$= \frac{15.9\ (V) \times 0.24\ (A)}{16\ (V) \times 0.90} = 0.265\ A$$

A good approximation of efficiency, η, can be taken from the efficiency curves located in the datasheet. A value of 90% is a good starting approximation.

Step 4c: Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor must be set such that the ½ inductor ripple current is not greater than the average minimum input current. As a first pass assume I_{ripple} to be 30% of the maximum inductor current:

$$\Delta I_L = I_{IN}(\max) \times I_{ripple} \quad (39)$$

$$= 0.848 \times 0.30 = 0.254\ A$$

then:

$$L = \frac{V_{IN}(\min)}{\Delta I_L \times f_{SW}} \times D(\max) \quad (40)$$

$$= \frac{5\ (V)}{0.254\ (A) \times 2\ (MHz)} \times 0.765 = 7.53\ \mu H$$

Step 4d: Double-check to make sure the ½ current ripple is less than $I_{IN}(\min)$:

$$I_{IN}(\min) > {}^1/_2\ \Delta I_L \quad (41)$$

$$0.265\ A > 0.127\ A$$

A good inductor value to use would be 10 µH.

Step 4e: Next insert the inductor value used in the design to determine the actual inductor ripple current:

$$\Delta I_{Lused} = \frac{V_{IN}(\min) \times D(\max)}{L_{used} \times f_{SW}} \quad (42)$$

$$= \frac{5\ (V) \times 0.765}{10\ (\mu H) \times 2.0\ (MHz)} = 0.191\ A$$

Step 4f: Determining the inductor current rating. The inductor current rating must be greater than the $I_{IN}(\max)$ value plus half of the ripple current ΔI_L, calculated as follows:

$$L(\min) = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} \quad (43)$$

$$= 0.848\ (A) + 0.096\ (A) = 0.944\ A$$

Step 5: Determining the resistor value for a particular switching frequency. Use the R_{FSET} values shown in Figure 7. For example, a 10 kΩ resistor will result in a 2 MHz switching frequency.

Step 6: Choosing the proper switching diode. The switching diode must be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are: current rating of the diode and reverse voltage rating.

The reverse breakdown voltage rating for the output diode in a SEPIC circuit should be:

$$V_{BD} > V_{OUT(OVP)}(\max) + V_{IN}(\max) \quad (44)$$
$$> 15.9\ (V) + 16\ (V) = 31.9\ V$$

because the maximum output voltage in this case is $V_{OUT(OVP)}$.

The peak current through the diode is calculated as:

$$I_{dp} = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} \quad (45)$$
$$= 0.848\ (A) + 0.096\ (A) = 0.944\ A$$

The third major component in deciding the switching diode is the reverse current, I_R , characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding off of the output voltage, due to leakage currents. I_R can be a large contributor, especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA. It is often advantageous to pick a diode with a much higher breakdown voltage, just to reduce the reverse current. Therefore for this example, pick a diode rated for a V_{BD} of 60 V, instead of just 40 V.

Step 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor are: PWM dimming frequency and PWM duty cycle. Another major contributor is leakage current, I_{LK}. This current is the combination of the OVP leakage current as well as the reverse current of the switching diode. In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically, the voltage variation on the output, V_{COUT}, during PWM dimming must be less than 250 mV, so that no audible hum can be heard. The capacitance can be calculated as follows:

$$C_{OUT} = I_{LK} \times \frac{1 - D(\min)}{f_{PWM(dimming)} \times V_{COUT}} \quad (46)$$
$$= 200\ (\mu A) \times \frac{1 - 0.01}{200\ (Hz) \times 0.250\ (V)} = 3.96\ \mu F$$

A capacitor larger than 3.96 µF should be selected due to degradation of capacitance at high voltages on the capacitor. Select a 4.7 µF capacitor for this application.

The rms current through the capacitor is given by:

$$I_{COUT}\text{rms} = I_{OUT} \sqrt{\frac{D(\max)}{1 - D(\max)}} \quad (47)$$
$$= 0.240\ (A) \sqrt{\frac{0.765}{1 - 0.765}} = 0.433\ A$$

The output capacitor must have a ripple current rating of at least 500 mA. The capacitor selected for this design is a 4.7 µF 50 V capacitor with a 1.5 A current rating.

Step 8: Selecting input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A estimation rule is to set the input voltage ripple, ΔV_{IN}, to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (48)$$
$$= \frac{0.191\ (A)}{8 \times 2\ (MHz) \times 0.05\ (V)} = 0.24\ \mu F$$

The rms current through the capacitor is given by:

$$C_{IN}\text{rms} = \frac{\Delta I_{Lused}}{\sqrt{12}} \quad (49)$$
$$= \frac{0.191\ (A)}{\sqrt{12}} = 0.055\ A$$

A good ceramic input capacitor with a rating of 2.2 µF 25 V will suffice for this application.

Step 9: Selecting coupling capacitor C_{SW}. The minimum capacitance of C_{SW} is related to the maximum voltage ripple allowed across it:

$$C_{SW} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_{SW} \times f_{SW}} = \frac{0.24\ (A) \times 0.765}{0.1\ (V) \times 2\ (MHz)} = 0.92\ \mu F \quad (50)$$

The rms current requirement of the coupling capacitor is given by:

$$I_{CSW}rms = I_{IN} \sqrt{\frac{1 - D(max)}{D(max)}} = 0.848\ (A) \sqrt{\frac{1 - 0.765}{0.765}} = 0.47\ A \quad (51)$$

The voltage rating of the coupling capacitor must be greater than $V_{IN}(max)$, or 16 V in this case. A ceramic capacitor rated for 2.2 µF 25V will suffice for this application.

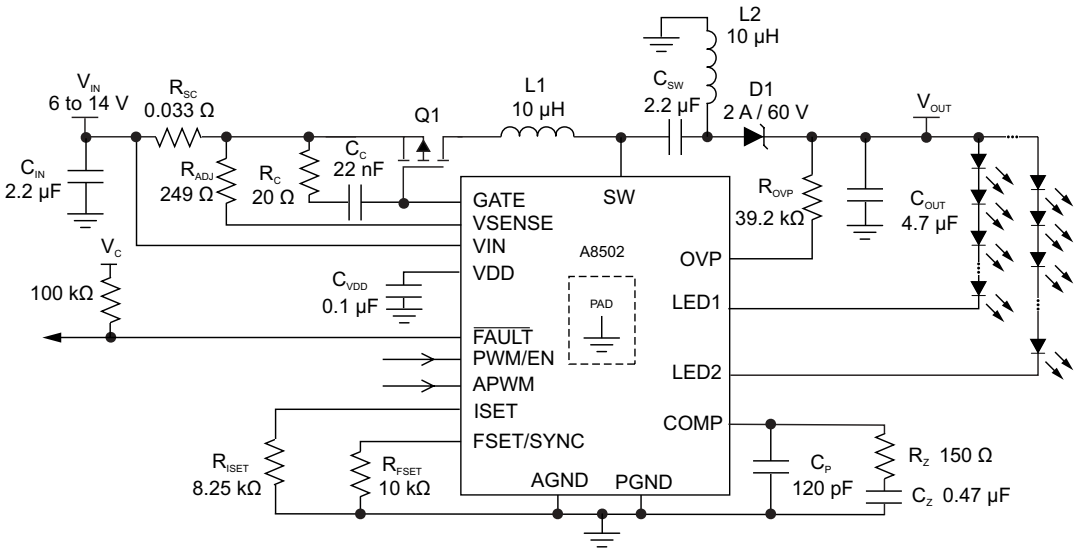
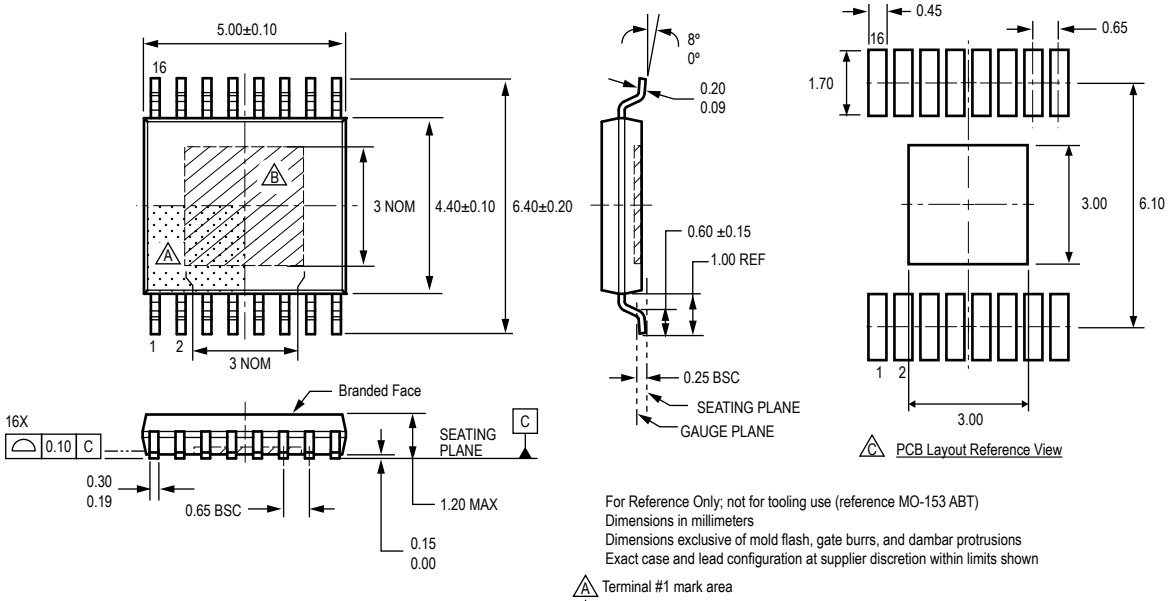


Figure 36: Typical application showing SEPIC configuration, designed according to the application example.

Package LP, 16-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Number	Date	Description
3	January 16, 2012	Update Features list and g_m
4	July 8, 2014	Updated FSET resistance and typical switching frequency
5	December 1, 2014	Updated specifications on EC table
6	October 1, 2015	Added Figure 11, and renumbered subsequent figures
7	February 27, 2017	Corrected SYNC Input Logic Voltage values on page 6
8	March 13, 2019	Updated Sync section (page 15)

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