THE DATASHEET OF

A5941GLKTR-T

A5941

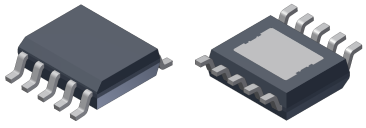
Three-Phase Sensorless Fan Driver

FEATURES AND BENEFITS

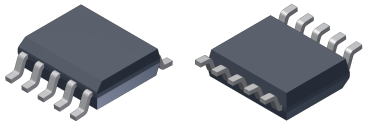
- AEC-Q100 qualified (K version)
- Quiet startup
- 180° sinusoidal drive for low audible noise
- High-efficiency control algorithm
- Sensorless operation
- Wide supply voltage range
- FG speed output
- Lock detection
- Overcurrent protection
- Soft start
- Short-circuit protection

PACKAGES:

10-Pin SOIC with Exposed Pad (suffix LK)



10-Pin SOIC (suffix LN)



Not to scale

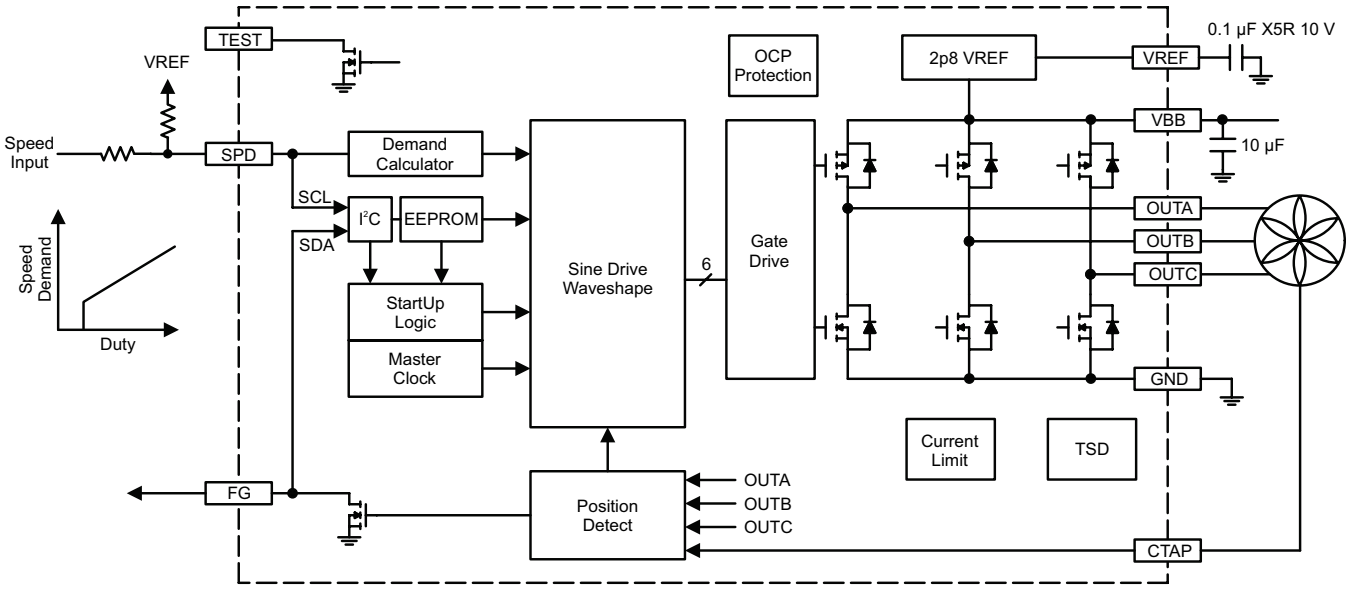
DESCRIPTION

The A5941 three-phase motor driver incorporates sinusoidal drive to minimize audible noise and vibration for medium-power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly start and gradually ramp up the motor to the desired speed. The voltage profile is set to a default value that will operate for a wide range of motor characteristics. EEPROM can be altered to customize the startup operation, if desired.

The motor speed is controlled by applying a duty-cycle command to the PWM input. The PWM input is allowed to operate over a wide frequency range. If desired, an analog voltage can be used to control motor speed, set via EEPROM adjustment.

The A5941 is available in a 10-pin SOIC (suffix LN), and a 10-pin SOIC with exposed pad (suffix LK). Both packages are Pb (lead) free, with 100% matte-tin leadframe plating.



Typical Application Diagram

SELECTION GUIDE

Part Number	Ambient Temperature Range	Package	Packing
A5941GLKTR-T	–40°C to 105°C	10-pin SOIC with exposed pad	3000 pieces per 13 in. reel
A5941GLNTR-T [1]	–40°C to 105°C	10-pin SOIC	3000 pieces per 13 in. reel
A5941KLKTR-T [2]	–40°C to 125°C	10-pin SOIC with exposed pad	3000 pieces per 13 in. reel

[1] Part variant A5941GLNTR-T is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status change date: April 1, 2024. Last-time buy date: July 31, 2024.

[2] Part variant A5941KLKTR-T is in production; however, it has been deemed Pre-End of Life. This variant is approaching end of life. Within a minimum of 6 months, this variant will enter its final, Last Time Buy, order phase. Date of status change: December 5, 2018.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS WITH RESPECT TO GND

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		18	V
Input Voltage Range	V_{IN}	SPD	–0.3 to 5.5	V
Logic Output Voltage	V_O	FG	18	V
Logic Output Current	I_O	FG	10	mA
Output Current	I_{OUT}	Internally limited	I_{OCLMAX}	A
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C
		Range K	–40 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LK package, 2-sided PCB 1 in.^{2} copper	35	°C/W
		LN package, single-sided PCB	130	°C/W

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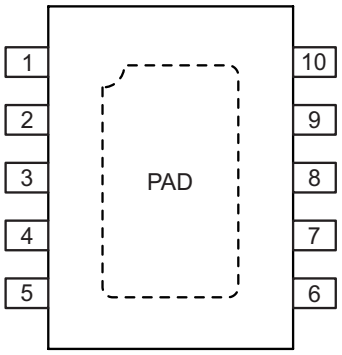
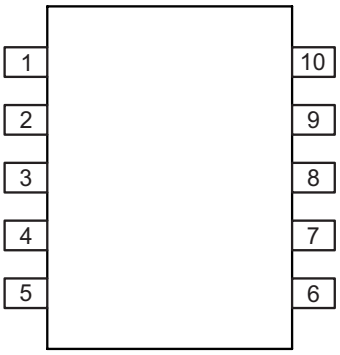
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LK, 10-Pin SOIC Pinout Diagram



Package LN, 10-Pin SOIC Pinout Diagram

Terminal List Table

Number	Name		Function
	LK	LN	
1	SPD	SPD	Speed input
2	FG	FG	Output speed signal
3	VBB	VBB	Input supply
4	OUTA	OUTA	Motor terminal
5	OUTB	OUTB	Motor terminal
6	GND	GND	Ground
7	OUTC	OUTC	Motor terminal
8	VREF	VREF	Analog output
9	TEST	TEST	Logic output
10	CTAP	CTAP	Analog input

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ELECTRICAL CHARACTERISTICS: G version valid at T_A = 25°C, V_{BB} = 4 to 18 V; K version valid at T_J = –40°C to 125°C, V_{BB} = 4 to 18 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Current	I_{BB}		–	7	9	mA
Total Driver On-Resistance (Sink + Source)	R_{DSON}	I_{OUT} = 1 A, T_J = 25°C, V_{BB} = 12 V	0.7	1	1.15	Ω
		I_{OUT} = 1 A, T_J = 25 C, V_{BB} = 4 V	–	1.3	–	Ω
		Source driver	–	650	800	mΩ
		Sink driver	–	350	450	mΩ
VREF Output Voltage	V_{REF}	I_{OUT} = 5 mA	2.75	2.85	2.95	V
SPD INPUT (VSP MODE)						
SPD On Threshold	V_{THON}		210	250	290	mV
SPD Off Threshold	V_{THOFF}		160	200	240	mV
SPD Maximum	V_{THMAX}		–	2.5	–	V
Resolution			–	4.89	–	mV
Accuracy			–	±6 LSB	–	–
SPD INPUT (PWM MODE)						
PWM On Threshold	DC_{ON}		–	10	–	%
PWM Off Threshold	DC_{OFF}		–	7.5	–	%
PWM Input Frequency Range	f_{PWM}		2.5	–	100	kHz
Motor PWM Frequency	f_{pwm}		23.2	24.4	25.6	kHz
VBB UVLO	V_{BBUVLO}	V_{BB} rising	–	3.85	3.98	V
VBB UVLO Hysteresis	V_{BBHYS}		150	300	450	mV
Lock Protection	t_{OFF}	Relative to target	–	±7	–	%
Overcurrent Limit	I_{OCL}		1.4	1.75	2.1	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
LOGIC/INPUT OUTPUT / I²C						
Input Current (SPD, FG)	I_{IN}	V_{IN} = 0 to 5.5 V	–5	<1	5	µA
Logic Input Voltage, Low Level	V_{IL}		0	–	0.8	V
Logic Input Voltage, High Level	V_{IH}		2	–	5.5	V
Logic Input Voltage Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage	V_{SAT}	I_{OUT} = 5 mA	–	–	0.3	V
FG Output Leakage Current	I_{FG}	V_{OUT} = 18 V, motor drive disabled	–	–	1	µA
SCL Clock Frequency	f_{CLK}		–	–	400	kHz
I²C TIMING						
Bus Free-Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	µs

*Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A5941 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan can be controlled by voltage mode (control of power supply amplitude), variable duty cycle PWM input, or via an adjustable analog input. Use of the PWM or analog input allows overall system cost savings by eliminating the requirement of an external variable power supply. Operation down to 4 V can be achieved to allow the IC to fit into legacy systems with voltage mode operation.

The SPD input (duty or analog voltage) is measured and converted to a 9-bit number. This 9-bit demand is applied to a PWM generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120° phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A BEMF detection window is opened on the phase A modulation profile to measure the rotor position to define the modulation timing. The control system maintains the window to a small level to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

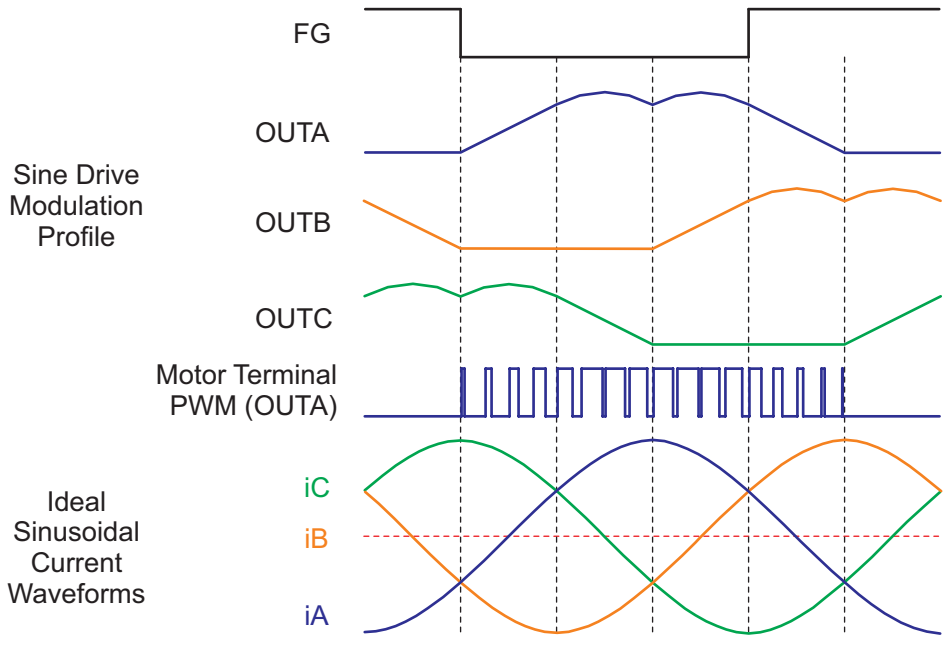

Figure 1: Sinusoidal PWM

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Speed Control Options

1. PWM Duty to SPD pin
2. Power Supply Modulation
3. Analog Voltage to SPD pin
4. Serial Port Command (I^2C)

DUTY CYCLE INPUT

A duty cycle measurement circuit converts the applied duty to a demand value (9-bit resolution) to control speed of the fan. The motor drive will be enabled if duty is larger than DC_{ON}. The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

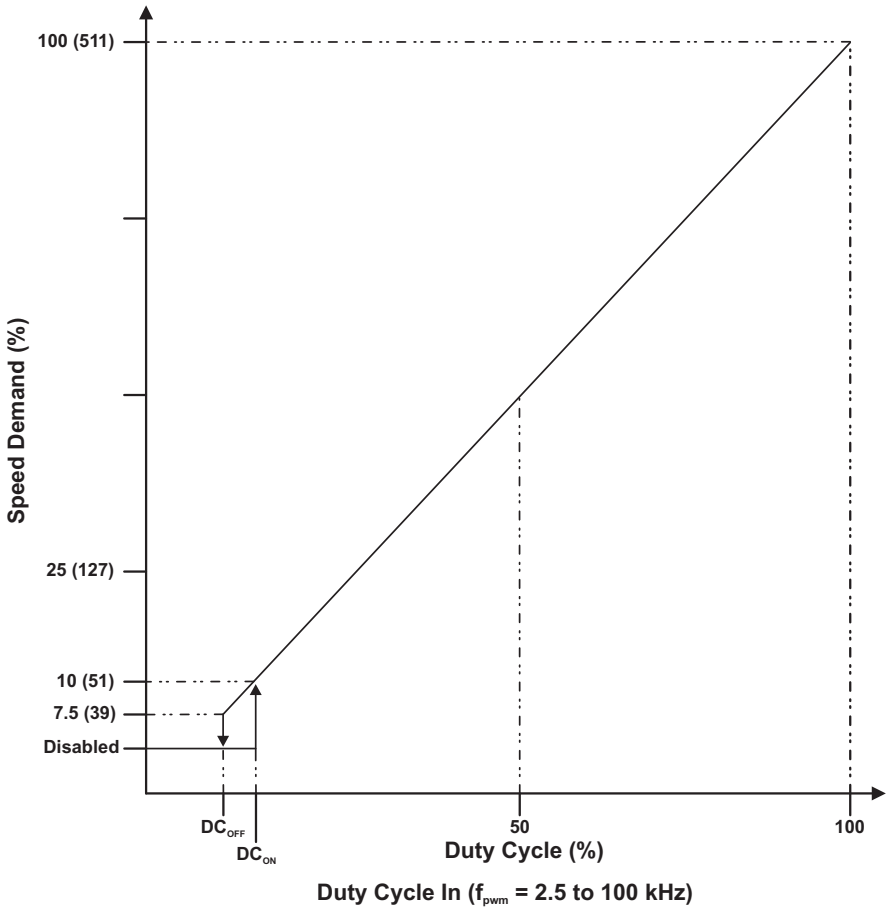

Figure 2: PWM Speed Input Characteristic

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POWER SUPPLY MODULATION

Speed can be controlled simply by varying the power supply voltage. Motor drive will be enabled and disabled at undervoltage rising and falling thresholds.

ANALOG INPUT

An internal analog-to-digital converter translates the input voltage to a demand value to control speed of the fan. The motor drive will be enabled if SPD is higher than V_{THON} and disabled if lower than V_{THOFF}.

Note: The default setting for A5941 is PWM duty input; EEPROM adjustment is required for use of analog voltage speed control mode.

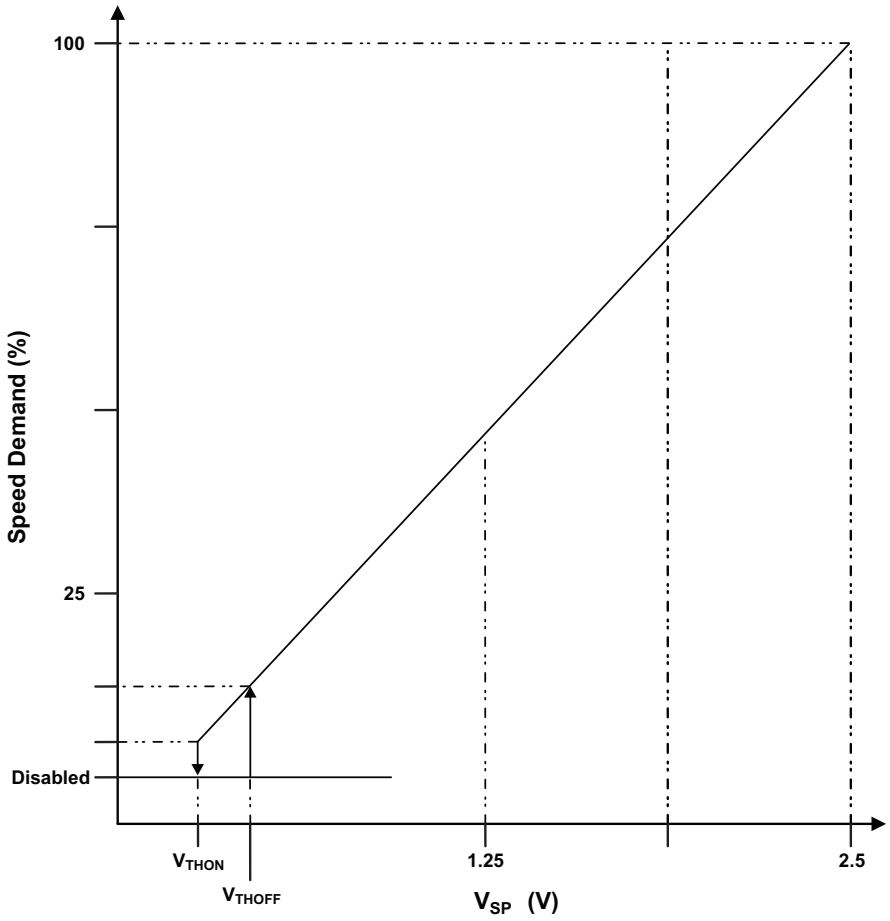

Figure 3: Analog Speed Input Characteristic

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Serial Port Control

An internal register can be used to program the speed directly with the I²C interface. Any code above 51(10%) will turn the A5941 on; any code below 39 (7.5%) will turn the A5941 off. To use serial port control, hold the SPD pin low during power up to prevent motor from starting with 100% demand. Write to the speed control register to set the desired speed demand.

Table 1: Speed Control – Register 165 (sets 9-bit speed demand)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	Speed Command = (0..511)									(LSB)

Lock Detect

Speed is monitored to determine if the rotor is locked. If a lock condition is detected, the IC will be disabled for t_{OFF} before an auto-restart is attempted. The default value for t_{OFF} is 5 seconds.

FG

An open drain output provides speed information to the system. For the default setting, FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

CTAP

The CTAP pin is the connection terminal for a motor common for Wye-connected motors. A virtual centertap is created internally if a motor common is not available or a delta-type motor is used. The CTAP pin should be left open if it is not used.

Current Limit

Load current is monitored on the low-side MOSFET. If the current has reached I_{OCL}, the source drivers will turn off for the remaining time of the PWM cycle.

Test

The TEST pin is a logic output that provides signals for production testing of the IC. This pin should be left open or pulled up to VREF with a 10 kΩ resistor in the application circuit.

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Quiet Startup

The A5941 controls startup in three stages, as represented in Figure 4:

1. Align/Hold – Moves motor to known starting position
2. Ramp up motor speed – Accelerate with modulation profile applied to motor windings in open loop (no position measurement)
3. Ramp to final value of external duty (or 100% for power supply speed control system). This occurs after switching to position sensing mode.

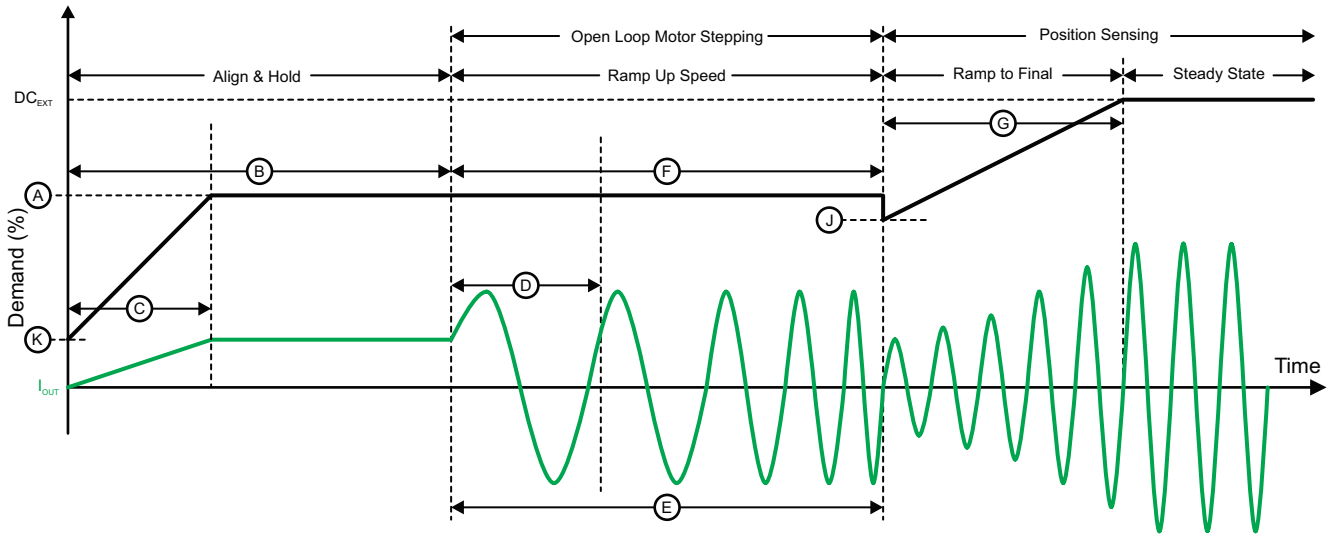

Figure 4: Applied Demand (Modulated Voltage) and Resultant I_{OUT} Typical Wave during Startup

Table 2: Parameter Notes

	Variable	Setting	Description
A	STRTDMD	25%	Demand level during open loop startup
B	ALIGNT	2 seconds	Total duration of alignment phase
C	ALIGNRMP	40%/second	Demand ramp rate during alignment
D	STRTF	0.25 Hz	Starting frequency
E	ACCEL	4 Hz/second	Acceleration rate
F	ACCELT	1.8 seconds	Total duration of acceleration phase
G	DMDRMP	15%/second	Demand ramp rate
J	DMDPOST	20%	Initial demand starting point after open loop mode
K	ALIGNINI	6%	Initial align demand level

Note: Duty cycle demand levels stated above (A, J, K) are for V_{BB} = 12 V. For lower power supply voltages, the demand level is compensated for by approximately 5%/V.

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Serial Port

The A5941 uses a standard fast mode I²C serial port format to program the EEPROM or to control the motor speed demand serially. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG pin will interfere with attempts at I²C communication. Disable the output with the SPD pin before trying to write a serial port command.

The 5941 7-bit slave address is 0x55 (1010101 binary).

I²C Timing Diagrams

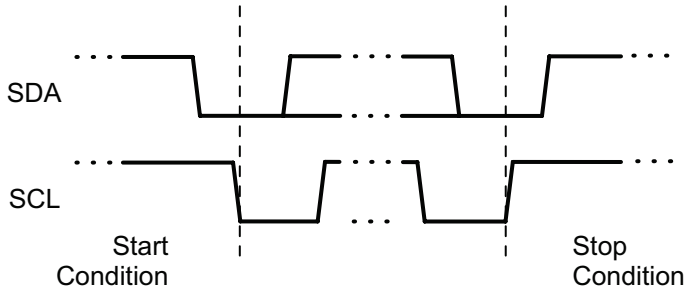

Figure 5: Start and Stop Conditions

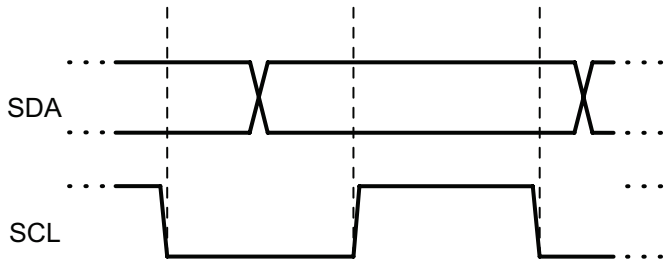

Figure 6: Clock and Data Bit Synchronization

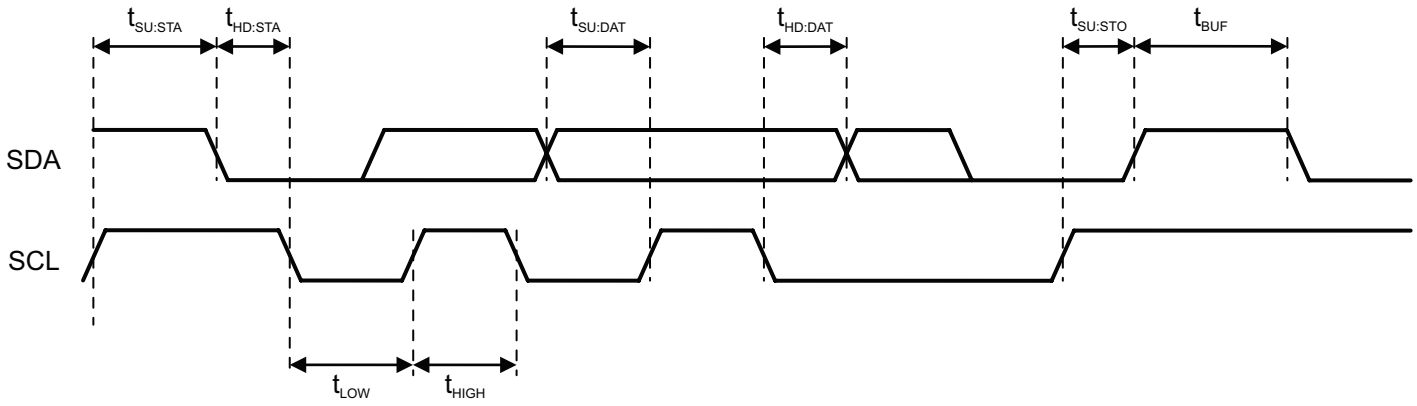

Figure 7: I²C-Compatible Timing Requirements

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Write Command

1. Start condition
2. 7-bit I²C slave address (device ID) 1010101, R/W bit = 0
3. Internal register address
4. 2 data bytes, MSB first
5. Stop condition

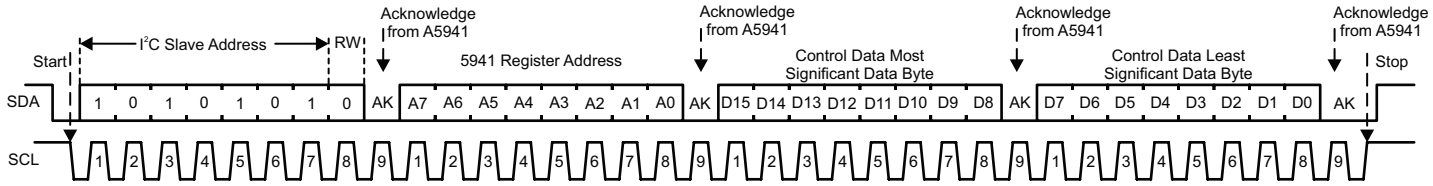

Figure 8: Write Command

Read Command

1. Start condition
2. 7-bit I²C slave address (device ID) 1010101, R/W bit = 0
3. Internal register address to be read
4. Stop condition
5. Start condition
6. 7-bit I²C slave address (device ID) 1010101, R/W bit = 1
7. Read 2 data bytes
8. Stop condition

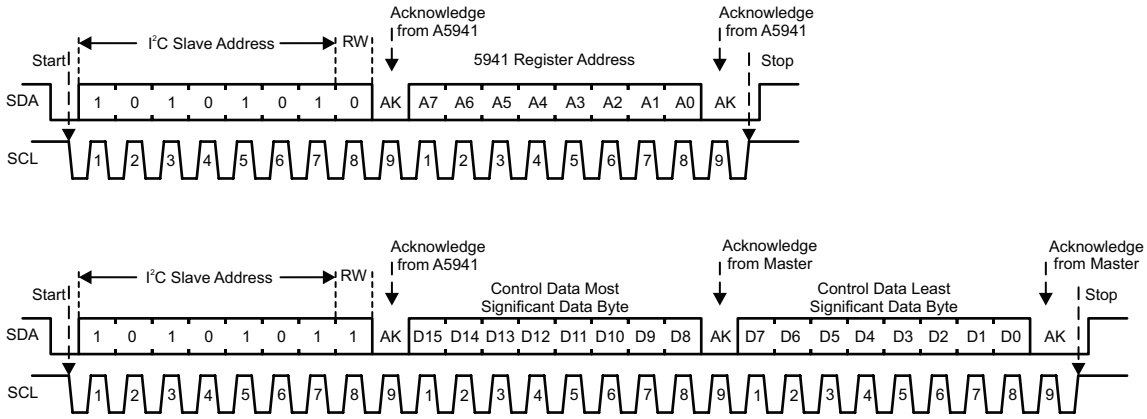

Figure 9: Read Command

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Programming EEPROM

The A5941 contains 20 words of 16-bit length. The EEPROM is controlled with the following I²C registers. Refer to application note for EEPROM definition.

Table 3: EEPROM Control – Register 161 (Used to control programming of EEPROM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM voltage required for writing or erasing
1	ER	Sets mode to erase
2	WR	Sets mode to write
15:3	n/a	Do not use; always set to zero during programming process

Table 4: EEPROM Control – Register 162 (Used to set the EEPROM address to be altered)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
4:0	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory controlled.
15:5	n/a	Do not use; always set to zero during programming process

Table 5: EEPROM Control – Register 163 (Used to set the EEPROM new data to be programmed)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed

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Upon power-up of the IC, the contents of the EEPROM are loaded into registers 0 to 19. To read the EEPROM contents, simply perform an I²C read command (see page 11) of a specific register. Each register must be read individually. Writing new data to the EEPROM is a two-step process. First the data is erased, and then new data is written. Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (0x0105)

1) Erase the Word

	I²C Write REGADDR[Data]	; comment
a.	162[5]	; set EEPROM address to erase
b.	163[0]	; set 0000 as Data In
c.	161[3]	; set control to Erase and trigger high-voltage pulse
d.	Wait 12 ms	; wait for pulse to end

2) Write the New Data

a.	162[5]	; set EEPROM address to write
b.	163[261]	; set Data In = 261
c.	161[5]	; set control to Write and trigger high-voltage pulse
d.	Wait 12 ms	; wait for pulse to end

Caution:

1. Do not power down IC during the two-step programming process.
2. It is recommended to readback data to confirm correct programming.
3. Do not program or erase EEPROM Address 0.

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APPLICATION INFORMATION

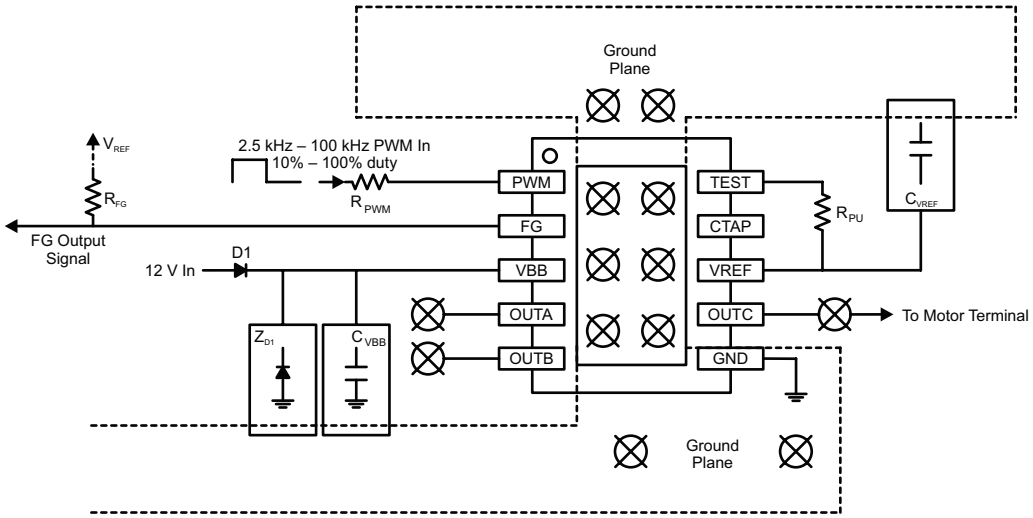

Figure 10: Typical Application Circuit

Table 6: Typical Application Components

Name	Suggested Value	Comment
C_{VREF}	0.1 µF / X5R / 10 V	Ceramic capacitor required
C_{VBB}	4.7 µF to 47 µF	Power supply stabilization – electrolytic or ceramic OK
R_{FG}	10 kΩ	Optional – pull-up resistor for speed feedback
D1	Not installed	May be required to isolate motor from system or for reverse polarity protection
ZD1	Not installed	Optional TVS to limit maximum V_{BB} due to transients from motor generation or power line. Suggested to clamp below 18 V (example: Fairchild SMBJ14A). Typically required if blocking diode D1 used.
R_{PWM}	1 kΩ	Optional – If SPD wired to connector – R_{PWM} will isolate IC pin from noise or overvoltage transients.

Layout Notes:

1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VREF} and C_{VBB} as close as possible to IC, connected to GND plane.

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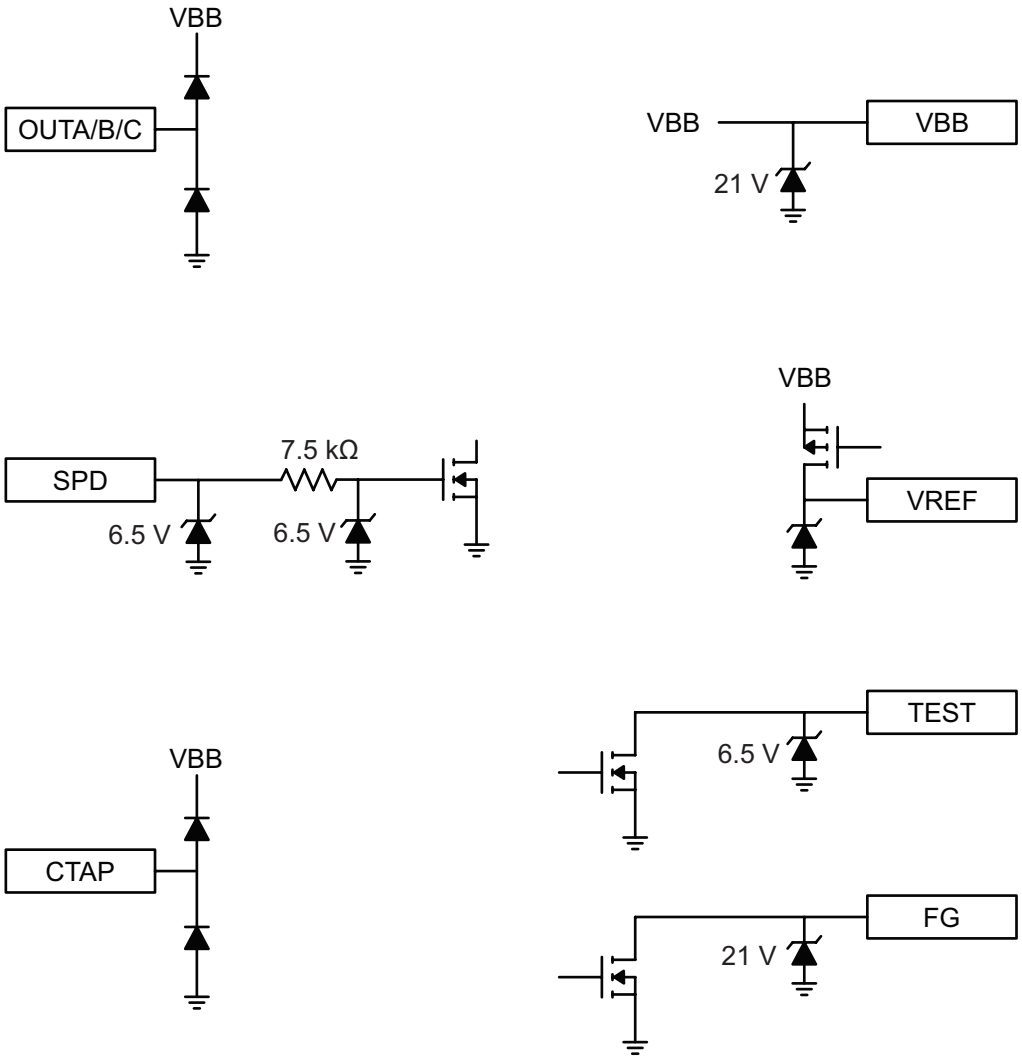

Figure 11: Pin Diagrams

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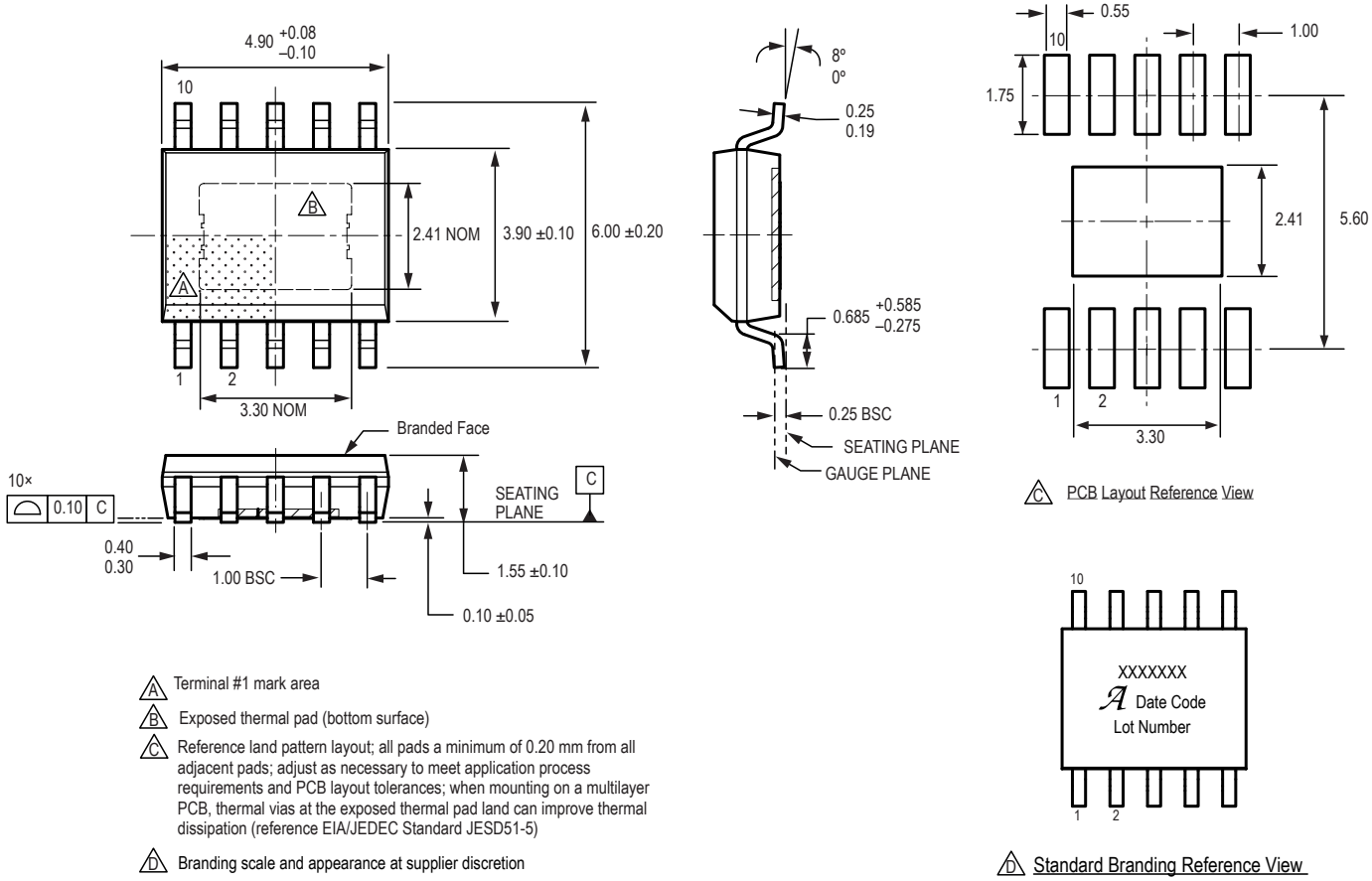
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000380, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2: Maximum 7 characters per line
Line 3: Maximum 5 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 12: Package LK, 10-Pin SOIC with Exposed Thermal Pad

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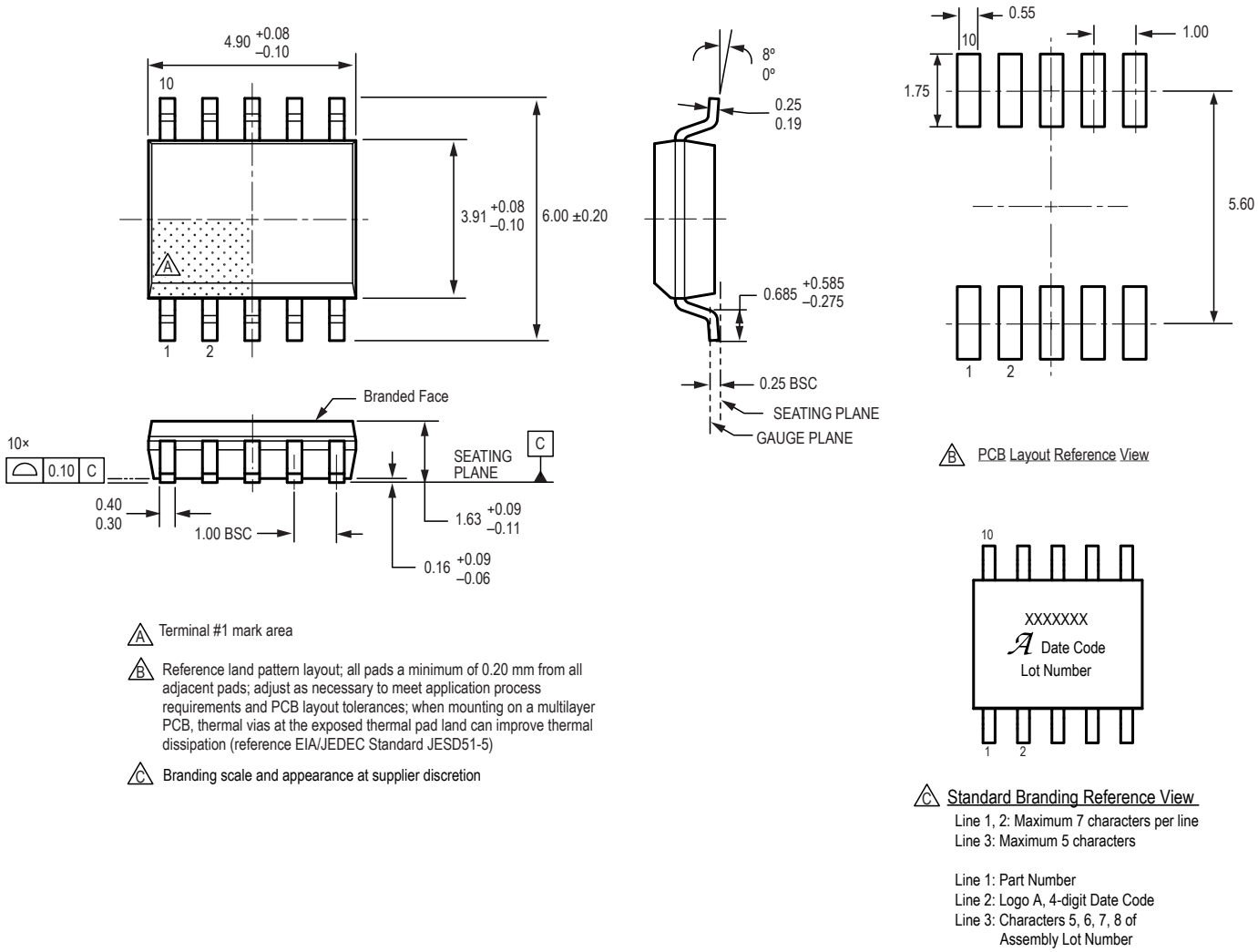
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

C Standard Branding Reference View
Line 1, 2: Maximum 7 characters per line
Line 3: Maximum 5 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 13: Package LN, 10-Pin SOIC

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	August 27, 2014	Initial Release
1	April 14, 2015	Added K version
2	March 30, 2016	Corrected LK package drawing dimension
3	May 18, 2016	Corrected Electrical Characteristics table K temperature reference; miscellaneous editorial changes
4	February 5, 2019	Product status changed to Pre-End-of-Life
5	April 1, 2019	Corrected product status
6	April 10, 2020	Updated LK package drawing and minor editorial updates
7	March 29, 2023	Updated LN package drawing
8	March 19, 2024	Part variant A5941GLNTR-T status changed to Last-Time Buy (page 2).

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