



THE DATASHEET OF PESD5V0U2BM,315





PESD5V0U2BM

Ultra low capacitance bidirectional double ESD protection array

15 October 2018

Product data sheet

1. General description

Ultra low capacitance bidirectional double ElectroStatic Discharge (ESD) protection diode array in a SOT883 (SC-101) leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect up to two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of up to two lines
- Ultra low diode capacitance: $C_d = 2.9$ pF
- Ultra low leakage current: $I_{RM} = 5$ nA
- ESD protection up to 10 kV
- IEC 61000-4-2; level 4 (ESD)
- AEC-Q101 qualified

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- SIM card protection
- High-speed data lines

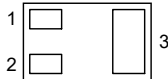
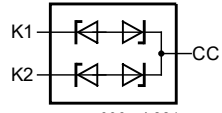
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	2.9	3.5	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view</p> <p>DFN1006-3 (SOT883)</p>	 <p>006aab331</p>
2	K2	cathode (diode 2)		
3	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U2BM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U2BM	GA

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1] [2]	-	10	kV
		HBM MIL-STD-883	[1] [2]	-	8	V

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 or 2 to pin 3.

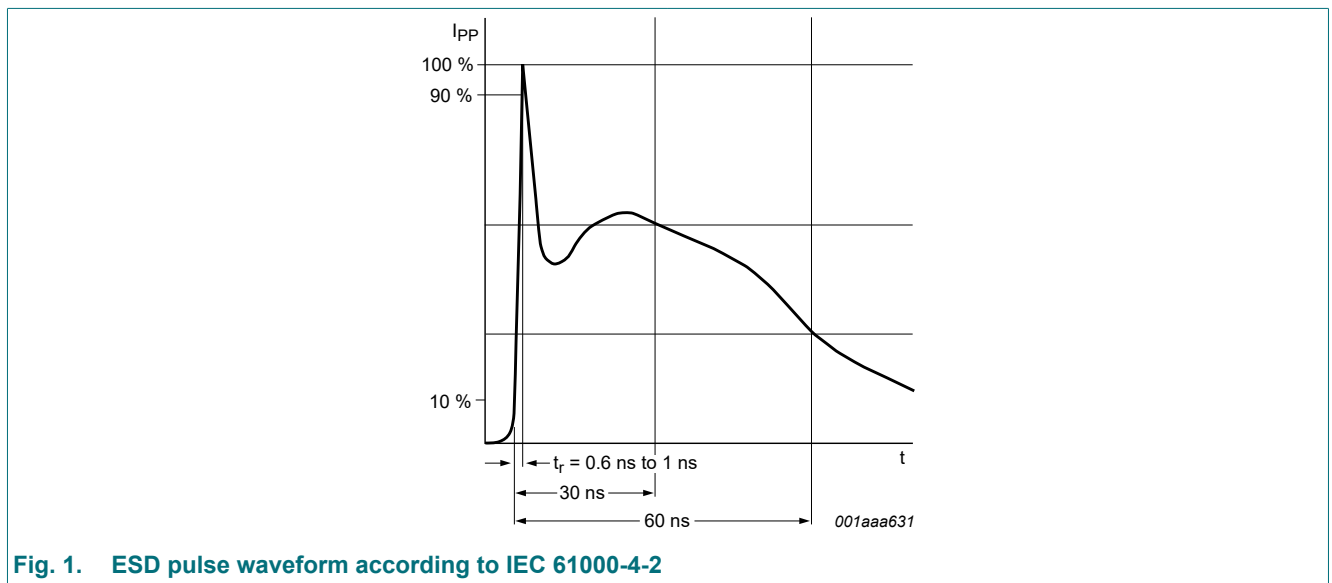
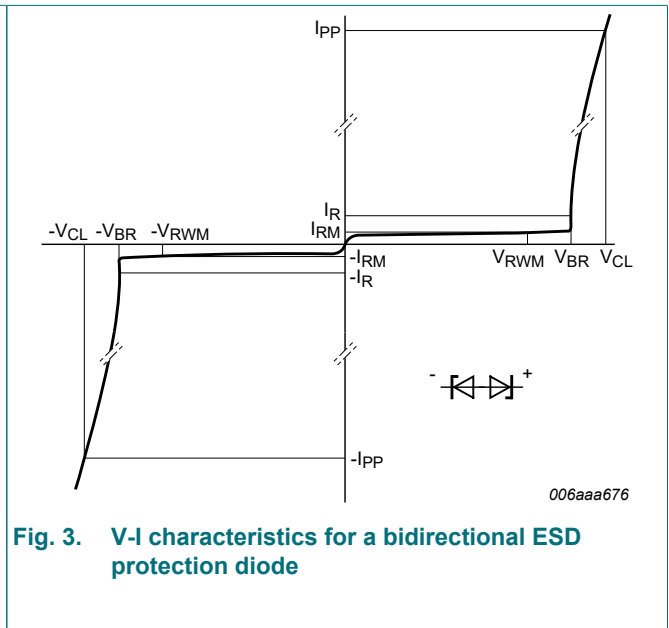
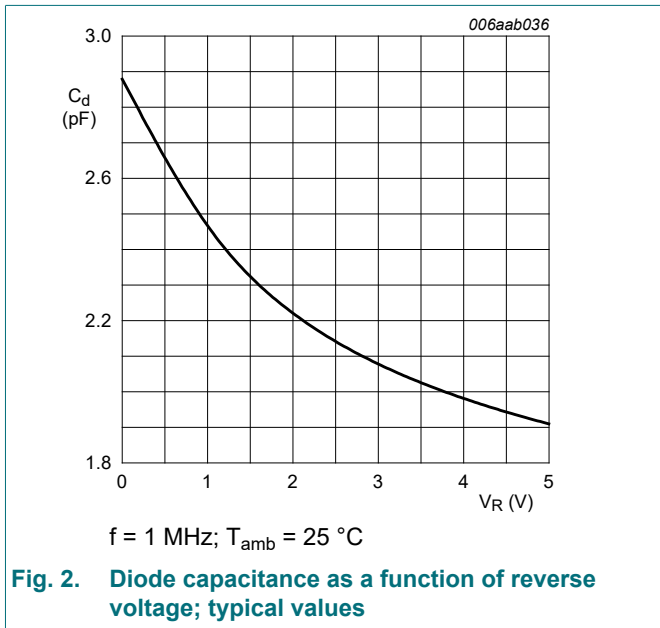


Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	5.5	6.5	9.5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	5	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2.9	3.5	pF
		$f = 1\text{ MHz}; V_R = 5\text{ V}$	-	1.9	-	pF
r_{dif}	differential resistance	$I_R = 1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	100	Ω



Ultra low capacitance bidirectional double ESD protection array

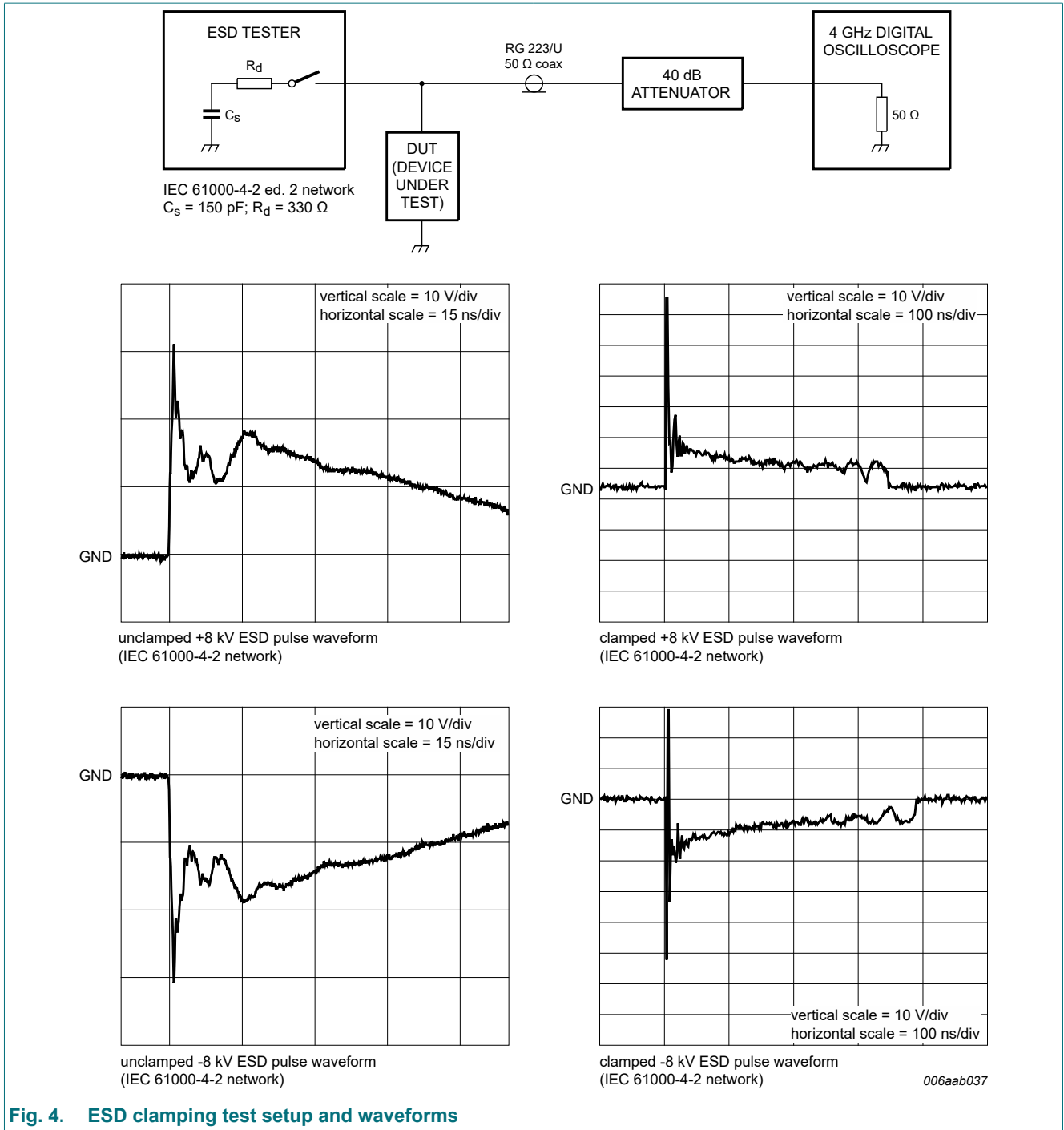


Fig. 4. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of up to two bidirectional data or signal lines from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

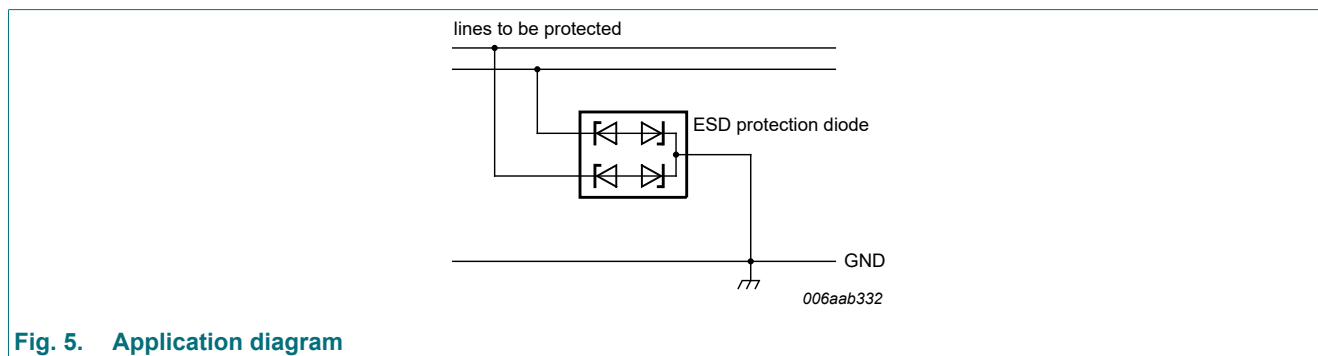


Fig. 5. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U2BM v.2	20181015	Product data sheet	-	PESD5V0U2BM v.1
Modifications:	<ul style="list-style-type: none">• Application information: updated• Legal texts have been adapted to the new company name where appropriate.• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.			
PESD5V0U2BM v.1	20080814	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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