THE DATASHEET OF

MB95F332KP-G-SH-SNE2

MB95F332H/F332K/F333H/F333K/F334H/F334K

F²MC-8FX MB95330H Series 8-bit Microcontrollers

MB95330H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  Main CR clock (1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz)
- Selectable subclock source
  Sub-OSC clock (32.768 kHz)
  External clock (32.768 kHz)
  Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

Timer

- 8/16-bit composite timer × 2 channels
- 8/16-bit PPG × 3 channels
- 16-bit PPG × 1 channel (can work independently or together with the multi-pulse generator)
- 16-bit reload timer × 1 channel (can work independently or together with the multi-pulse generator)
- Time-base timer × 1 channel
- Watch prescaler × 1 channel

UART/SIO × 1 channel

- Full duplex double buffer
- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer

I²C × 1 channel

- Built-in wake-up function

Multi-pulse generator (MPG) (for DC motor control) × 1 channel

- 16-bit reload timer × 1 channel
- 16-bit PPG timer × 1 channel
- Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)

LIN-UART

- Full duplex double buffer
- Capable of clock-synchronous serial data transfer and clock-asynchronous serial data transfer

External interrupt × 10 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/10-bit A/D converter × 8 channels

- 8-bit and 10-bit resolution can be chosen.

Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F332H/F333H/F334H (maximum no. of I/O ports: 28)
  General-purpose I/O ports (N-ch open drain): 3
  General-purpose I/O ports (CMOS I/O): 25
- MB95F332K/F333K/F334K (maximum no. of I/O ports: 29)
  General-purpose I/O ports (N-ch open drain): 4
  General-purpose I/O ports (CMOS I/O): 25

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer

Low-voltage detection reset circuit

- Built-in low-voltage detector

Clock supervisor counter

- Built-in clock supervisor counter function

Programmable port input voltage level

- CMOS input level / hysteresis input level

Dual operation Flash memory

- The erase/write operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

- Protects the content of the Flash memory

Contents

1. Product Line-up

Part number / Parameter	MB95F332H	MB95F333H	MB95F334H	MB95F332K	MB95F333K	MB95F334K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	1008 bytes	240 bytes	496 bytes	1008 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 µs (with machine clock = 16.25 MHz)					
General-purpose I/O	I/O ports (Max): 28 CMOS I/O: 25 N-ch open drain: 3			I/O ports (Max): 29 CMOS I/O: 25 N-ch open drain: 4		
Time-base timer	Interrupt cycle: 0.256 ms to 8.3 s (when external clock = 4 MHz)					
Hardware/software watchdog timer	Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	A wide range of communication speeds can be selected by a dedicated reload timer. Clock-synchronous serial data transfer and clock-asynchronous serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	8 channels					
	8-bit resolution and 10-bit resolution can be chosen.					
8/16-bit composite timer	2 channels					
	The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.					
External interrupt	10 channels					
	Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from different standby modes.					
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)					

(Continued)

(Continued)

Part number / Parameter	MB95F332H	MB95F333H	MB95F334H	MB95F332K	MB95F333K	MB95F334K
UART/SIO	1 channel					
	Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I^2C	1 channel					
	Master/slave transmission and receiving It has a bus error function, an arbitration function, a transmission direction detection function and a wake-up function. It also has functions of generating and detecting repeated START conditions.					
8/16-bit PPG	3 channels					
	Each channel of PPG can be used as two 8-bit PPG channels or a single 16-bit PPG channel. The counter operating clock can be selected from eight clock sources.					
16-bit PPG	PWM mode and one-shot mode are available to use. The counter operating clock can be selected from eight clock sources. It supports external trigger start. It can work independently or together with the multi-pulse generator.					
16-bit reload timer	Two clock modes and two counter operating modes are available to use. It can output square waveform. Count clock: it can be selected from internal clocks (seven types) and external clocks. Two counter operating modes: reload mode and one-shot mode It can work independently or together with the multi-pulse generator.					
Multi-pulse generator (for DC motor control)	16-bit PPG timer: 1 channel 16-bit reload timer operations: toggle output, one-shot output Event counter: 1 channel Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-32P-M30 DIP-32P-M06 LCC-32P-M19					

2. Packages and Corresponding Products

Part number / Package	MB95F332H	MB95F332K	MB95F333H	MB95F333K	MB95F334H	MB95F334K
FPT-32P-M30	O	O	O	O	O	O
DIP-32P-M06	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O

O: Available

3. Differences Among Products and Notes On Product Selection

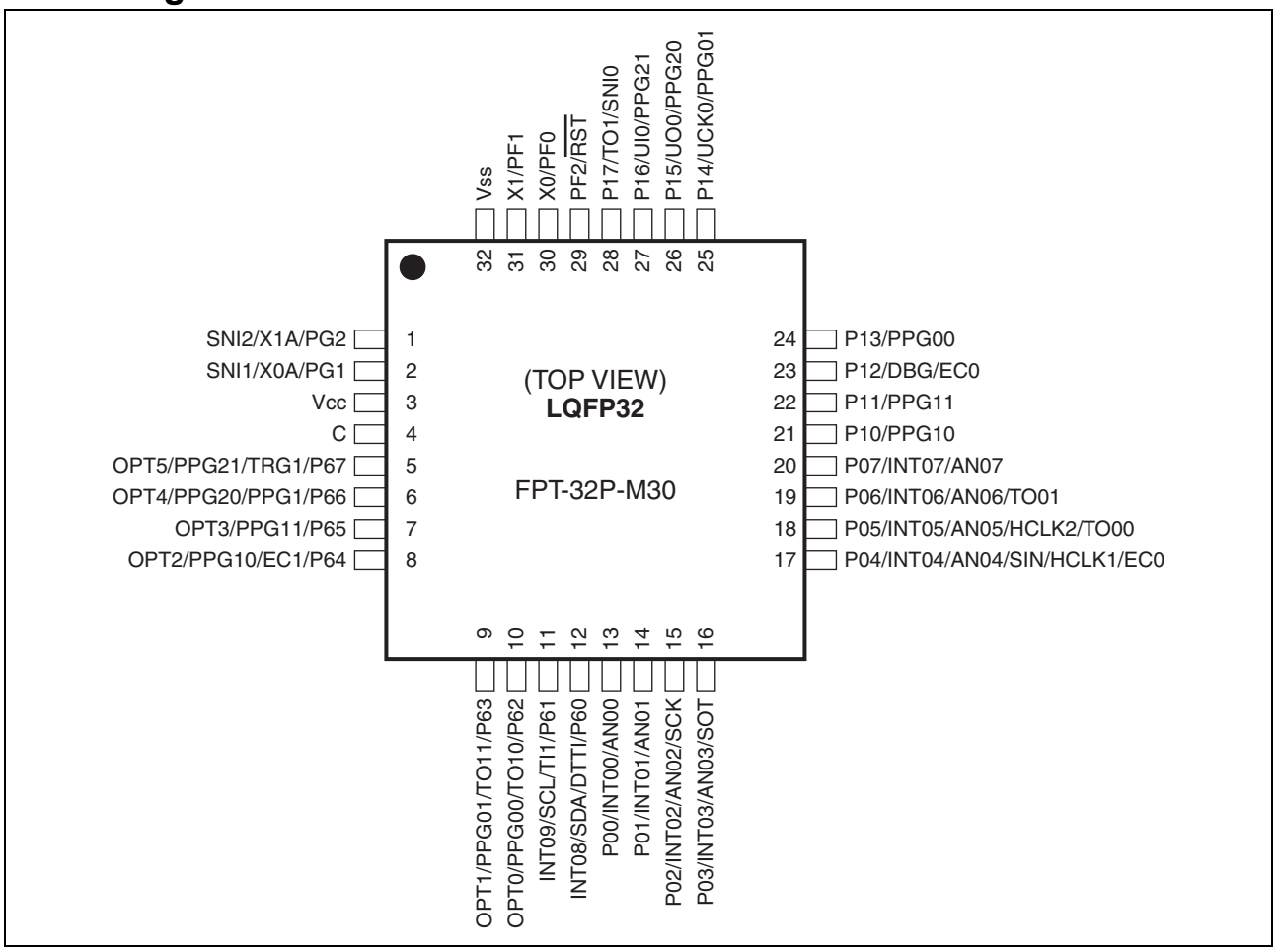
■ • Current consumption
When using the on-chip debug function, take account of the current consumption of flash erase/write.
For details of current consumption, see “Electrical Characteristics.

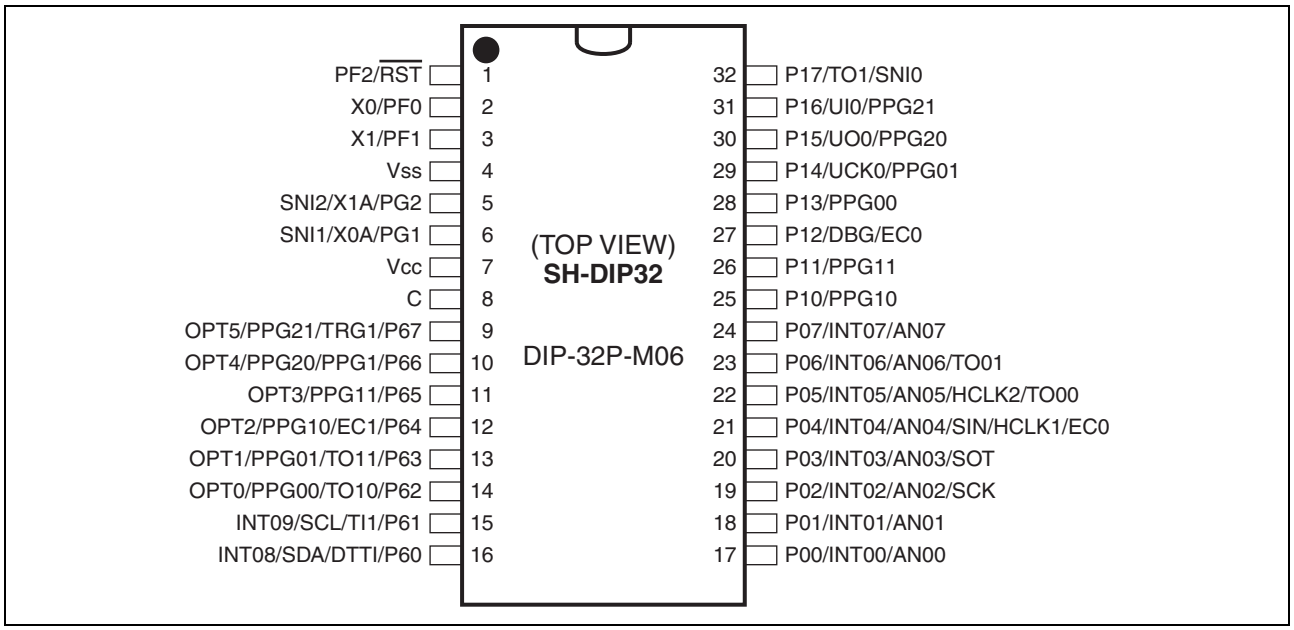
■ • Package
For details of information on each package, see “Packages and Corresponding Products” and “Package Dimension”.

■ • Operating voltage
The operating voltage varies, depending on whether the on-chip debug function is used or not.
For details of the operating voltage, see “Electrical Characteristics”.

■ • On-chip debug function
The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool.

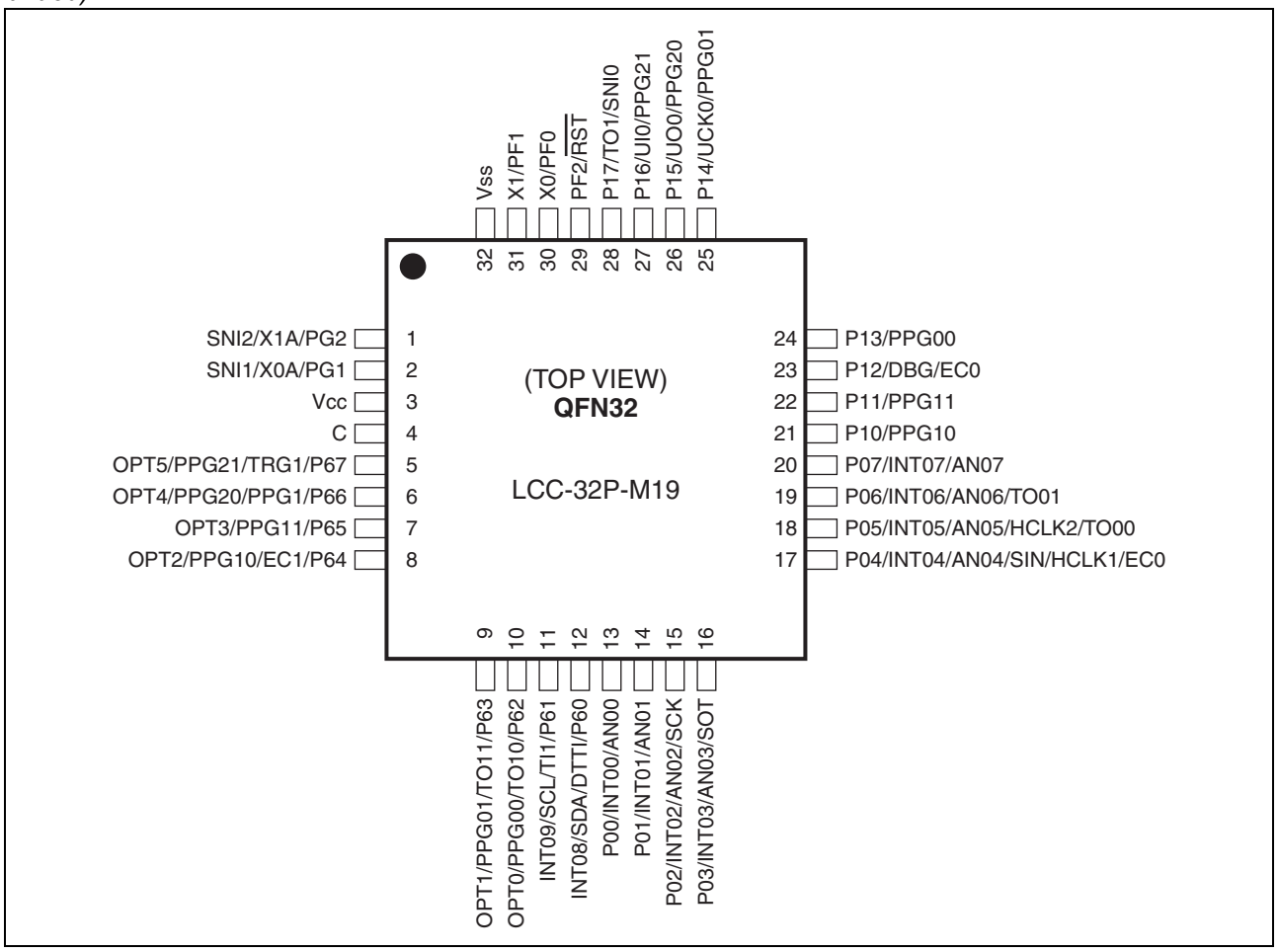
4. Pin Assignment





(Continued)

(Continued)


Vss
X1/PF1
X0/PF0
PF2/RST
P17/TO1/SNI0
P16/UI0/PPG21
P15/UO0/PPG20
P14/UCK0/PPG01
32
31
30
29
28
27
26
25
SNI2/X1A/PG2 1
SNI1/X0A/PG1 2
Vcc 3
C 4
OPT5/PPG21/TRG1/P67 5
OPT4/PPG20/PPG1/P66 6
OPT3/PPG11/P65 7
OPT2/PPG10/EC1/P64 8
(TOP VIEW)
QFN32
LCC-32P-M19
24 P13/PPG00
23 P12/DBG/EC0
22 P11/PPG11
21 P10/PPG10
20 P07/INT07/AN07
19 P06/INT06/AN06/TO01
18 P05/INT05/AN05/HCLK2/TO00
17 P04/INT04/AN04/SIN/HCLK1/EC0
9
10
11
12
13
14
15
16
OPT1/PPG01/TO11/P63
OPT0/PPG00/TO10/P62
INT09/SCL/TI1/P61
INT08/SDA/DTTI/P60
P00/INT00/AN00
P01/INT01/AN01
P02/INT02/AN02/SCK
P03/INT03/AN03/SOT

5. Pin Description

Pin no.		Pin name	I/O circuit type*4	Function
LQFP32*1 & QFN32*2	SH-DIP32*3			
1	5	PG2	C	General-purpose I/O port
		X1A		Subclock I/O oscillation pin
		SNI2		Trigger input pin for the position detection function of the MPG waveform sequencer
2	6	PG1	C	General-purpose I/O port
		X0A		Subclock input oscillation pin
		SNI1		Trigger input pin for the position detection function of the MPG waveform sequencer
3	7	V_{CC}	—	Power supply pin
4	8	C	—	Capacitor connection pin
5	9	P67	D	General-purpose I/O port High-current pin
		PPG21		8/16-bit PPG ch. 2 output pin
		TRG1		16-bit PPG ch. 1 trigger input pin
		OPT5		MPG waveform sequencer output pin
6	10	P66	D	General-purpose I/O port High-current pin
		PPG20		8/16-bit PPG ch. 2 output pin
		PPG1		16-bit PPG ch. 1 output pin
		OPT4		MPG waveform sequencer output pin
7	11	P65	D	General-purpose I/O port High-current pin
		PPG11		8/16-bit PPG ch. 1 output pin
		OPT3		MPG waveform sequencer output pin
8	12	P64	D	General-purpose I/O port High-current pin
		EC1		8/16-bit composite timer ch. 1 clock input pin
		PPG10		8/16-bit PPG ch. 1 output pin
		OPT2		MPG waveform sequencer output pin
9	13	P63	D	General-purpose I/O port High-current pin
		TO11		8/16-bit composite timer ch. 1 output pin
		PPG01		8/16-bit PPG ch. 0 output pin
		OPT1		MPG waveform sequencer output pin

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function
LQFP32*1 & QFN32*2	SH-DIP32*3			
10	14	P62	D	General-purpose I/O port High-current pin
		TO10		8/16-bit composite timer ch. 1 output pin
		PPG00		8/16-bit PPG ch. 0 output pin
		OPT0		MPG waveform sequencer output pin
11	15	P61	I	General-purpose I/O port
		INT09		External interrupt input pin
		SCL		I^2C clock I/O pin
		TI1		16-bit reload timer ch. 1 input pin
12	16	P60	I	General-purpose I/O port
		INT08		External interrupt input pin
		SDA		I^2C data I/O pin
		DTTI		MPG waveform sequencer input pin
13	17	P00	E	General-purpose I/O port
		INT00		External interrupt input pin
		AN00		A/D converter analog input pin
14	18	P01	E	General-purpose I/O port
		INT01		External interrupt input pin
		AN01		A/D converter analog input pin
15	19	P02	E	General-purpose I/O port
		INT02		External interrupt input pin
		AN02		A/D converter analog input pin
		SCK		LIN-UART clock I/O pin
16	20	P03	E	General-purpose I/O port
		INT03		External interrupt input pin
		AN03		A/D converter analog input pin
		SOT		LIN-UART data output pin
17	21	P04	F	General-purpose I/O port
		INT04		External interrupt input pin
		AN04		A/D converter analog input pin
		SIN		LIN-UART data input pin
		HCLK1		External clock input pin
		EC0		8/16-bit composite timer ch. 0 clock input pin

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function
LQFP32*1 & QFN32*2	SH-DIP32*3			
18	22	P05	E	General-purpose I/O port
		INT05		External interrupt input pin
		AN05		A/D converter analog input pin
		HCLK2		External clock input pin
		TO00		8/16-bit composite timer ch. 0 output pin
19	23	P06	E	General-purpose I/O port
		INT06		External interrupt input pin
		AN06		A/D converter analog input pin
		TO01		8/16-bit composite timer ch. 0 output pin
20	24	P07	E	General-purpose I/O port
		INT07		External interrupt input pin
		AN07		A/D converter analog input pin
21	25	P10	G	General-purpose I/O port
		PPG10		8/16-bit PPG ch. 1 output pin
22	26	P11	G	General-purpose I/O port
		PPG11		8/16-bit PPG ch. 1 output pin
23	27	P12	H	General-purpose I/O port
		DBG		DBG input pin
		EC0		8/16-bit composite timer ch. 0 clock input pin
24	28	P13	G	General-purpose I/O port
		PPG00		8/16-bit PPG ch. 0 output pin
25	29	P14	G	General-purpose I/O port
		UCK0		UART/SIO ch. 0 clock I/O pin
		PPG01		8/16-bit PPG ch. 0 output pin
26	30	P15	G	General-purpose I/O port
		UO0		UART/SIO ch. 0 data output pin
		PPG20		8/16-bit PPG ch. 2 output pin
27	31	P16	J	General-purpose I/O port
		UI0		UART/SIO ch. 0 data input pin
		PPG21		8/16-bit PPG ch. 2 output pin
28	32	P17	G	General-purpose I/O port
		TO1		16-bit reload timer ch. 1 output pin
		SNI0		Trigger input pin for the position detection function of the MPG waveform sequencer
29	1	PF2	A	General-purpose I/O port
		$\overline{RST}$		Reset pin Dedicated reset pin in MB95F332H/F333H/F334H

(Continued)

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function
LQFP32*1 & QFN32*2	SH-DIP32*3			
30	2	PF0	B	General-purpose I/O port
		X0		Main clock input oscillation pin
31	3	PF1	B	General-purpose I/O port
		X1		Main clock I/O oscillation pin
32	4	V_{SS}	—	Power supply pin (GND)

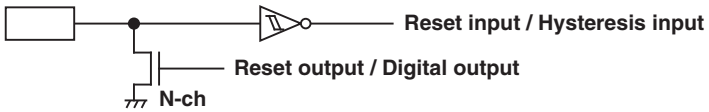
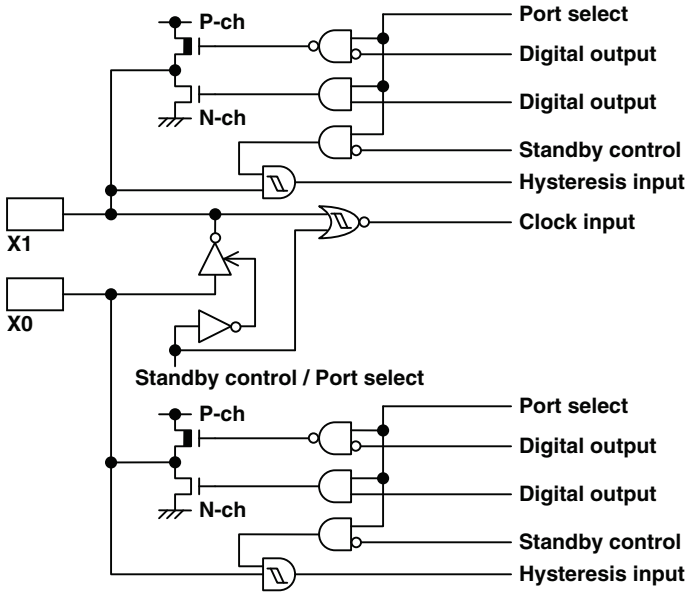
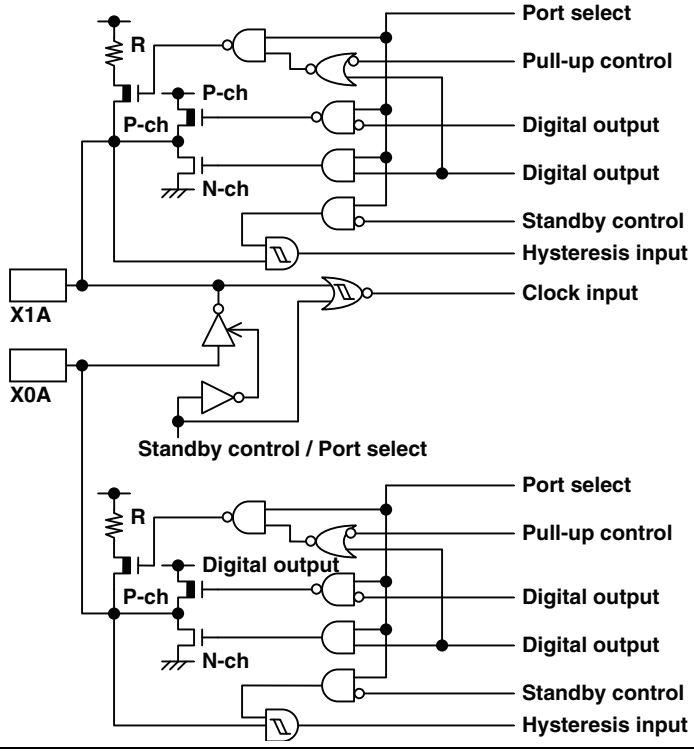
*1: Package code: FPT-32P-M30

*2: Package code: LCC-32P-M19

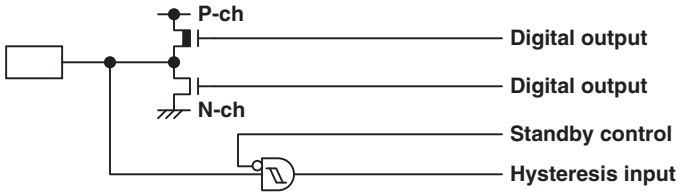
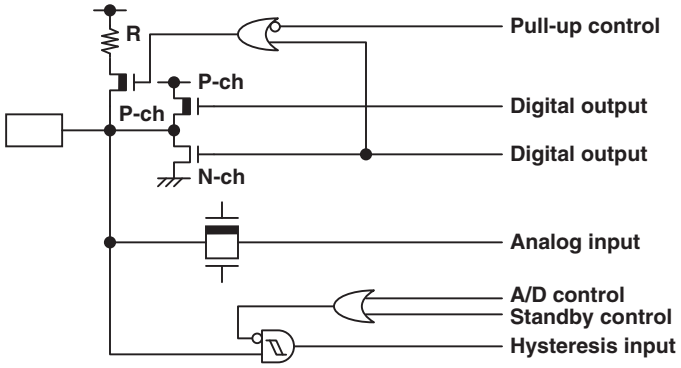
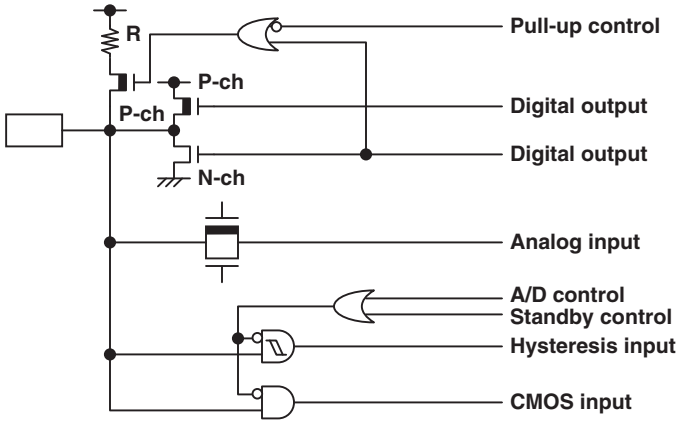
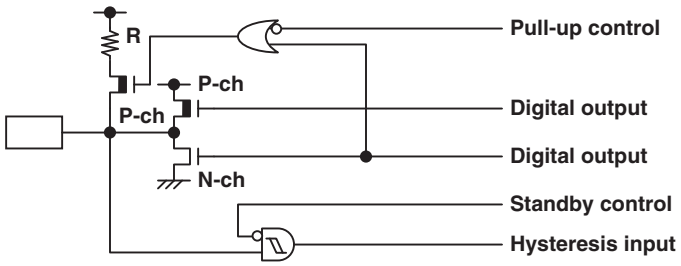
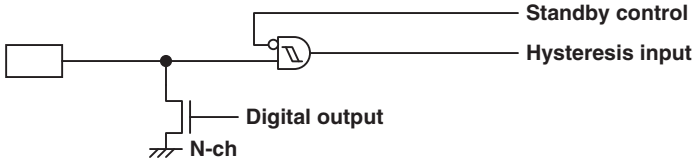
*3: Package code: DIP-32P-M06

*4: For the I/O circuit types, see “I/O Circuit Type”.

6. I/O Circuit Type

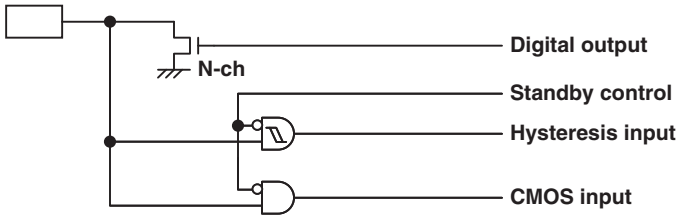
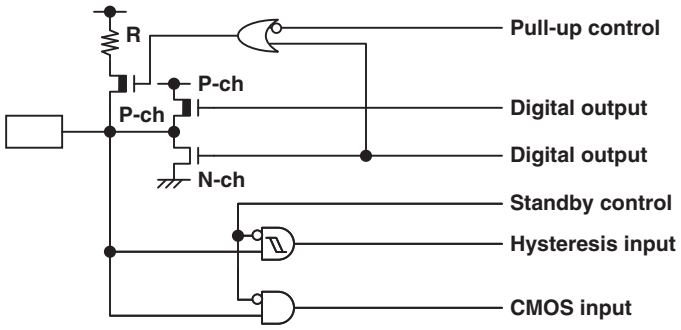
Type	Circuit	Remarks
A		■ N-ch open drain output ■ Hysteresis input ■ Reset output
B		■ Oscillation circuit ■ High-speed side Feedback resistance: approx. 1 MΩ ■ CMOS output ■ Hysteresis input
C		■ Oscillation circuit ■ Low-speed side Feedback resistance: approx.10 MΩ ■ CMOS output ■ Hysteresis input ■ Pull-up control available

(Continued)

Type	Circuit	Remarks
D		■ CMOS output ■ Hysteresis input
E		■ CMOS output ■ Hysteresis input ■ Pull-up control available
F		■ CMOS output ■ Hysteresis input ■ CMOS input ■ Pull-up control available
G		■ Hysteresis input ■ CMOS output ■ Pull-up control available
H		■ N-ch open drain output ■ Hysteresis input

(Continued)

(Continued)

Type	Circuit	Remarks
I		■ N-ch open drain output ■ Hysteresis input ■ CMOS input
J		■ CMOS output ■ Hysteresis input ■ CMOS input ■ Pull-up control available

7. Notes On Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "13.1 Absolute Maximum Ratings" of “■ Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

8. Pin Connection

■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

■ Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

■ $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

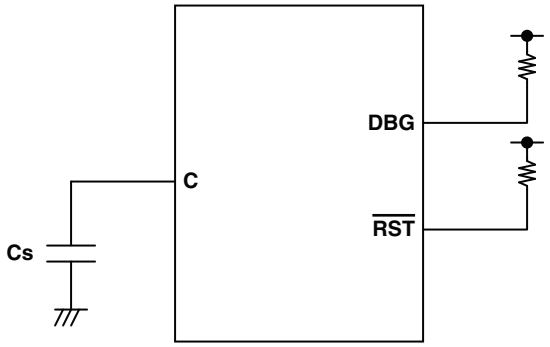
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The $\overline{\text{RST}}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the $\overline{\text{RST}}$/PF2 pin can be enabled by the RSTOE bit of the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

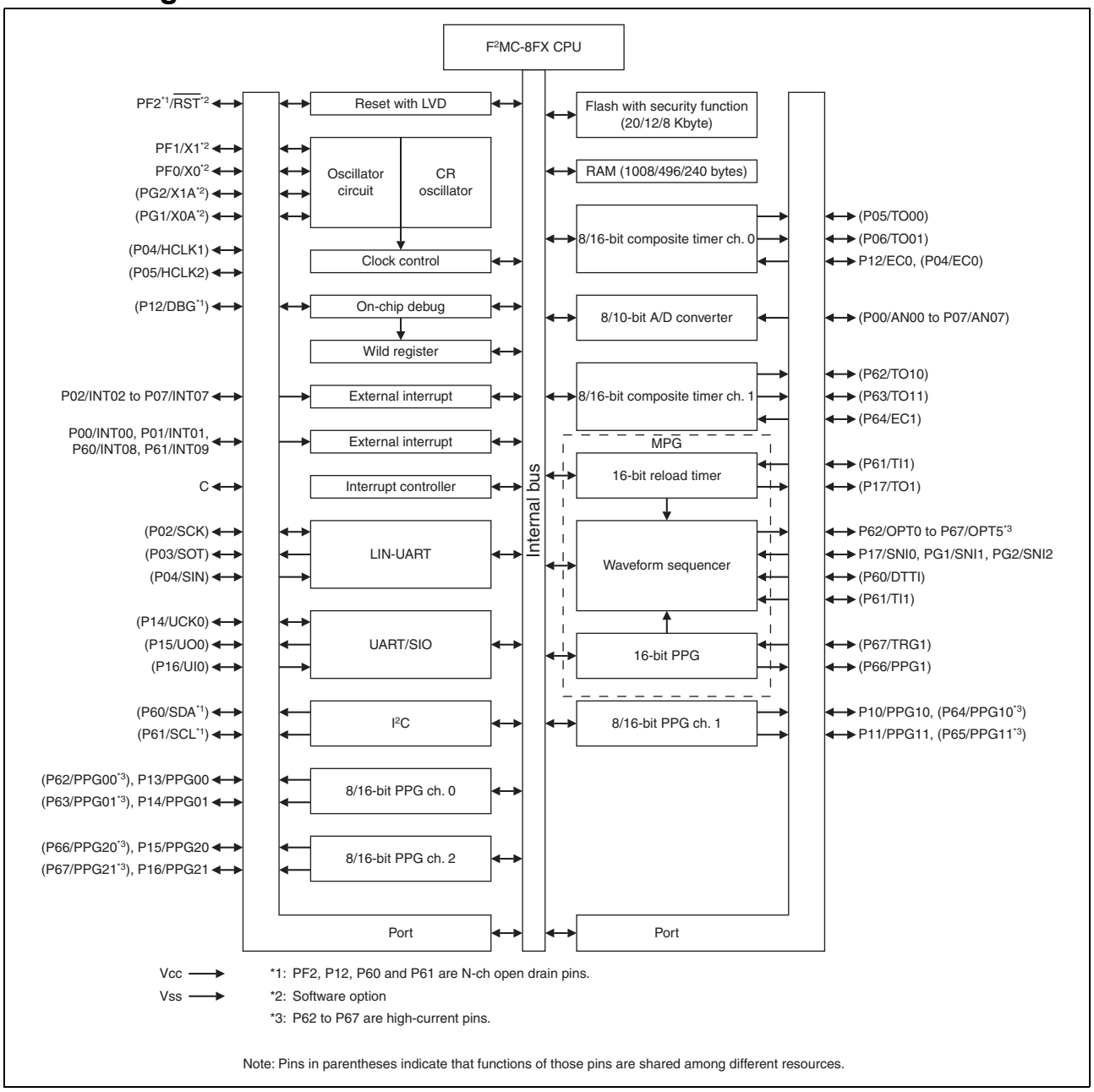
■ C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG/$\overline{\text{RST}}$/C pins connection diagram



9. Block Diagram

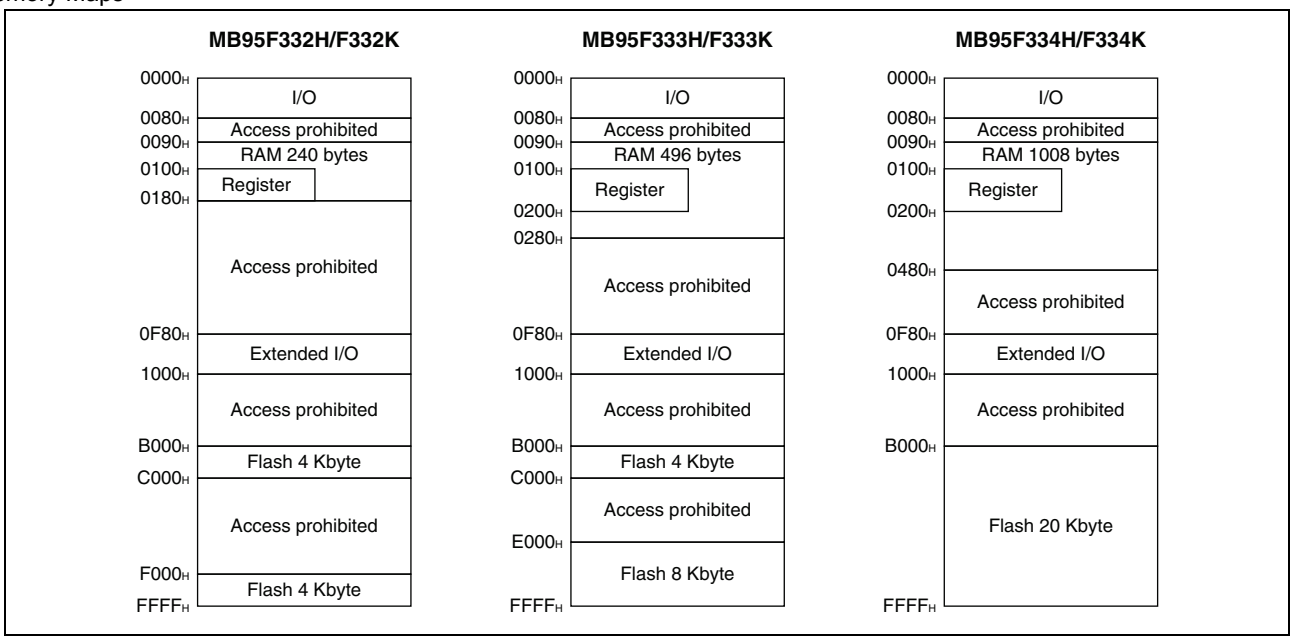


10. CPU Core

■ Memory Space

The memory space of the MB95330H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95330H Series are shown below.

■ Memory Maps


MB95F332H/F332K
0000H
I/O
0080H
Access prohibited
0090H
RAM 240 bytes
0100H
Register
0180H
Access prohibited
0F80H
Extended I/O
1000H
Access prohibited
B000H
Flash 4 Kbyte
C000H
Access prohibited
F000H
Flash 4 Kbyte
FFFFH
MB95F333H/F333K
0000H
I/O
0080H
Access prohibited
0090H
RAM 496 bytes
0100H
Register
0200H
0280H
Access prohibited
0F80H
Extended I/O
1000H
Access prohibited
B000H
Flash 4 Kbyte
C000H
Access prohibited
E000H
Flash 8 Kbyte
FFFFH
MB95F334H/F334K
0000H
I/O
0080H
Access prohibited
0090H
RAM 1008 bytes
0100H
Register
0200H
0480H
Access prohibited
0F80H
Extended I/O
1000H
Access prohibited
B000H
Flash 20 Kbyte
FFFFH

11. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$XXXXXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG timer 01 control register ch. 0	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG timer 00 control register ch. 0	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG timer 11 control register ch. 1	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG timer 10 control register ch. 1	R/W	00000000_B
$003E_H$	PC21	8/16-bit PPG timer 21 control register ch. 2	R/W	00000000_B
$003F_H$	PC20	8/16-bit PPG timer 20 control register ch. 2	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0040_H	TMCSRH1	16-bit reload timer control status register upper ch. 1	R/W	00000000_B
0041_H	TMCSRL1	16-bit reload timer control status register lower ch. 1	R/W	00000000_B
0042_H, 0043_H	—	(Disabled)	—	—
0044_H	PCNTH1	16-bit PPG status control register upper ch. 1	R/W	00000000_B
0045_H	PCNTL1	16-bit PPG status control register lower ch. 1	R/W	00000000_B
0046_H, 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$	EIC01	External interrupt circuit control register ch. 8/ch. 9	R/W	00000000_B
$004D_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status and data register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO serial input data register ch. 0	R	00000000_B
$005B_H$ to $005F_H$	—	(Disabled)	—	—
0060_H	IBCR00	I^2C bus control register 0	R/W	00000000_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBSR0	I^2C bus status register	R/W	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H	OPCUR	16-bit MPG output control register (upper)	R/W	00000000_B
0067_H	OPCLR	16-bit MPG output control register (lower)	R/W	00000000_B
0068_H	IPCUR	16-bit MPG input control register (upper)	R/W	00000000_B
0069_H	IPCLR	16-bit MPG input control register (lower)	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$006A_H$	NCCR	16-bit MPG noise cancellation control register	R/W	00000000_B
$006B_H$	TCSR	16-bit MPG timer control status register	R/W	00000000_B
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111_B
$0FA4_H$	PPGS	8/16-bit PPG startup register	R/W	00000000_B
$0FA5_H$	REVC	8/16-bit PPG output reverse register	R/W	00000000_B
$0FA6_H$	PPS21	8/16-bit PPG21 cycle setting buffer register ch. 2	R/W	11111111_B
$0FA7_H$	PPS20	8/16-bit PPG20 cycle setting buffer register ch. 2	R/W	11111111_B
$0FA8_H$	TMRH1	16-bit timer register (upper) ch. 1	R/W	00000000_B
	TMRLRH1	16-bit reload register (upper) ch. 1		
$0FA9_H$	TMRL1	16-bit timer register (lower) ch. 1	R/W	00000000_B
	TMRLRL1	16-bit reload register (lower) ch. 1		
$0FAA_H$	PDS21	8/16-bit PPG21 duty setting buffer register ch. 2	R/W	11111111_B
$0FAB_H$	PDS20	8/16-bit PPG20 duty setting buffer register ch. 2	R/W	11111111_B
$0FAC_H$ to $0FAF_H$	—	(Disabled)	—	—
$0FB0_H$	PDCRH1	16-bit PPG down counter register (upper) ch. 1	R	00000000_B
$0FB1_H$	PDCRL1	16-bit PPG down counter register (lower) ch. 1	R	00000000_B
$0FB2_H$	PCSRH1	16-bit PPG cycle setting buffer register (upper) ch. 1	R/W	11111111_B
$0FB3_H$	PCSRL1	16-bit PPG cycle setting buffer register (lower) ch. 1	R/W	11111111_B
$0FB4_H$	PDUTH1	16-bit PPG duty setting buffer register (upper) ch. 1	R/W	11111111_B
$0FB5_H$	PDUTL1	16-bit PPG duty setting buffer register (lower) ch. 1	R/W	11111111_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FB6_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000_B
$0FC0_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FC4_H$	OPDBRH0	16-bit MPG output data buffer register (upper) ch. 0	R/W	00000000_B
$0FC5_H$	OPDBRL0	16-bit MPG output data buffer register (lower) ch. 0	R/W	00000000_B
$0FC6_H$	OPDBRH1	16-bit MPG output data buffer register (upper) ch. 1	R/W	00000000_B
$0FC7_H$	OPDBRL1	16-bit MPG output data buffer register (lower) ch. 1	R/W	00000000_B
$0FC8_H$	OPDBRH2	16-bit MPG output data buffer register (upper) ch. 2	R/W	00000000_B
$0FC9_H$	OPDBRL2	16-bit MPG output data buffer register (lower) ch. 2	R/W	00000000_B
$0FCA_H$	OPDBRH3	16-bit MPG output data buffer register (upper) ch. 3	R/W	00000000_B
$0FCB_H$	OPDBRL3	16-bit MPG output data buffer register (lower) ch. 3	R/W	00000000_B
$0FCC_H$	OPDBRH4	16-bit MPG output data buffer register (upper) ch. 4	R/W	00000000_B
$0FCD_H$	OPDBRL4	16-bit MPG output data buffer register (lower) ch. 4	R/W	00000000_B
$0FCE_H$	OPDBRH5	16-bit MPG output data buffer register (upper) ch. 5	R/W	00000000_B
$0FCF_H$	OPDBRL5	16-bit MPG output data buffer register (lower) ch. 5	R/W	00000000_B
$0FD0_H$	OPDBRH6	16-bit MPG output data buffer register (upper) ch. 6	R/W	00000000_B
$0FD1_H$	OPDBRL6	16-bit MPG output data buffer register (lower) ch. 6	R/W	00000000_B
$0FD2_H$	OPDBRH7	16-bit MPG output data buffer register (upper) ch. 7	R/W	00000000_B
$0FD3_H$	OPDBRL7	16-bit MPG output data buffer register (lower) ch. 7	R/W	00000000_B
$0FD4_H$	OPDBRH8	16-bit MPG output data buffer register (upper) ch. 8	R/W	00000000_B
$0FD5_H$	OPDBRL8	16-bit MPG output data buffer register (lower) ch. 8	R/W	00000000_B
$0FD6_H$	OPDBRH9	16-bit MPG output data buffer register (upper) ch. 9	R/W	00000000_B
$0FD7_H$	OPDBRL9	16-bit MPG output data buffer register (lower) ch. 9	R/W	00000000_B
$0FD8_H$	OPDBRHA	16-bit MPG output data buffer register (upper) ch. A	R/W	00000000_B
$0FD9_H$	OPDBRLA	16-bit MPG output data buffer register (lower) ch. A	R/W	00000000_B
$0FDA_H$	OPDBRHB	16-bit MPG output data buffer register (upper) ch. B	R/W	00000000_B
$0FDB_H$	OPDBRLB	16-bit MPG output data buffer register (lower) ch. B	R/W	00000000_B
$0FDC_H$	OPDUR	16-bit MPG output data register (upper)	R	$0000XXXX_B$
$0FDD_H$	OPDLR	16-bit MPG output data register (lower)	R	$XXXXXXXX_B$
$0FDE_H$	CPCUR	16-bit MPG compare clear register (upper)	R/W	$XXXXXXXX_B$
$0FDF_H$	CPCLR	16-bit MPG compare clear register (lower)	R/W	$XXXXXXXX_B$

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FE0_H$, $0FE1_H$	—	(Disabled)	—	—
$0FE2_H$	TMBUR	16-bit MPG timer buffer register (upper)	R	$XXXXXXXX_B$
$0FE3_H$	TMBLR	16-bit MPG timer buffer register (lower)	R	$XXXXXXXX_B$
$0FE4_H$	CRTH	Main CR clock trimming register (upper)	R/W	$0XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (lower)	R/W	$00XXXXXX_B$
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (upper)	R	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (lower)	R	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$	WICR	Interrupt pin control register	R/W	01000000_B
$0FF0_H$ to $0FFF_H$	—	(Disabled)	—	—

■ R/W access symbols

R/W : Readable / Writable

R : Read only

W : Write only

■ Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

12. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0, ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 1, ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2, ch. 6	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 3, ch. 7	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
UART/SIO ch. 0, MPG (DTTI)	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
16-bit reload timer ch. 1, MPG (write timing/compare clear), I^2C	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
16-bit PPG timer ch. 1, MPG (position detection/compare match)	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
External interrupt ch. 8, ch. 9	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P62 to P67
	I_{OL2}		15		P62 to P67
"L" level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}	—	12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P62 to P67
	I_{OH2}	—	−15		P62 to P67
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}	—	−8		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

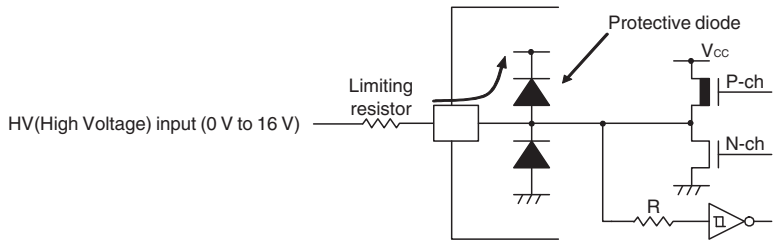
(Continued)

(Continued)

*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P10, P11, P13 to P17, P62 to P67, PF0, PF1, PG1 and PG2
- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit
  - Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

13.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

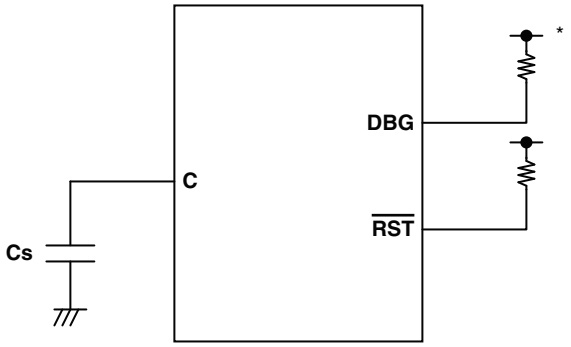
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: This value becomes 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG/EC0.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04, P16, P60, P61	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P60 to P67, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04, P16, P60, P61	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P60 to P67, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P60, P61, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P60 to P67, PF2	I_{OH} = −4 mA	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P62 to P67	I_{OH} = −8 mA	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P62 to P67	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P62 to P67	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, P10, P11, P13 to P17, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
				—	20.5	26.5	mA	Flash memory product (at writing and erasing)
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	10	13.2	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = +25°C	—	110	410	µA	

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25°C	—	3.5	22.5	µA	
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input levels of P04, P16, P60 and P61 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL}.
- See "4. AC Characteristics: (2) Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

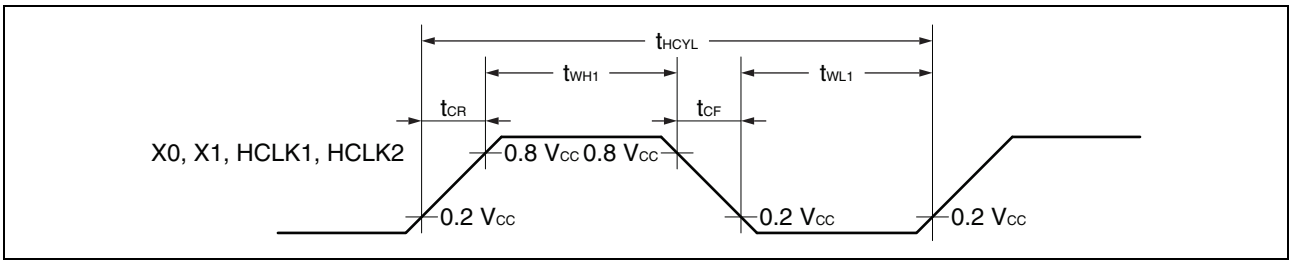
13.4 AC Characteristics

13.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

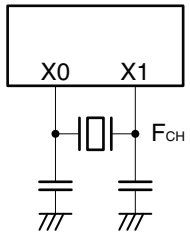
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
		HCLK1, HCLK2	—	1	—	32.5	MHz	
	F_{CRH}	—	—	12.25	12.5	12.75	MHz	When the main CR clock is used T_A = −10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—	—	12.1875	12.5	12.8125	MHz	When the main CR clock is used T_A = −40°C to −10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*	30.8	—	1000	ns	
		HCLK1, HCLK2	—	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
		HCLK1, HCLK2	—	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1: open	—	—	5	ns	When the external clock is used
		X0, X1	*	—	—	5	ns	
		HCLK1, HCLK2	—	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

*: The external clock signal is input to X0 and the inverted external clock signal to X1.

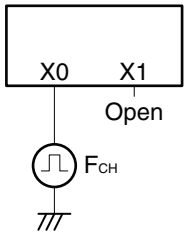


- Figure of main clock input port external connection

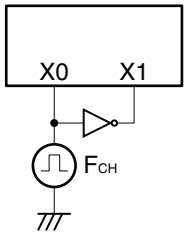
When a crystal oscillator or a ceramic oscillator is used



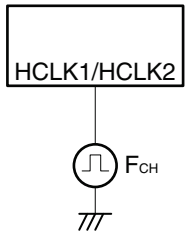
When the external clock is used (X1 is open)

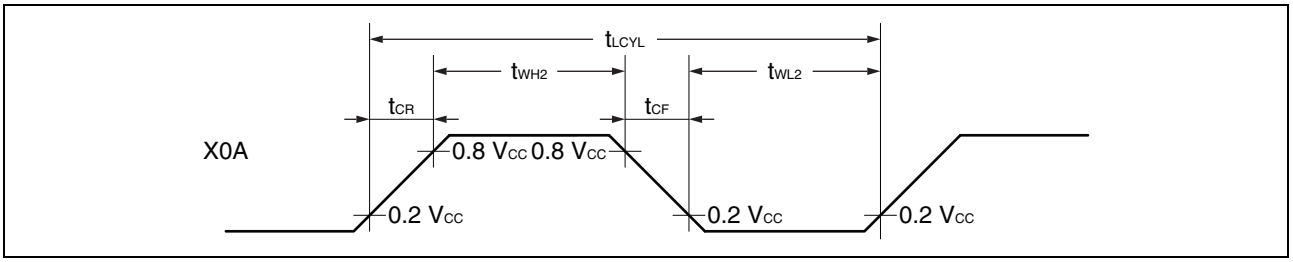


When the external clock is used



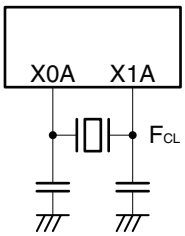
When the external clock is used



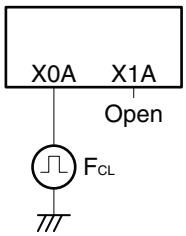


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



13.4.2 Source Clock/Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

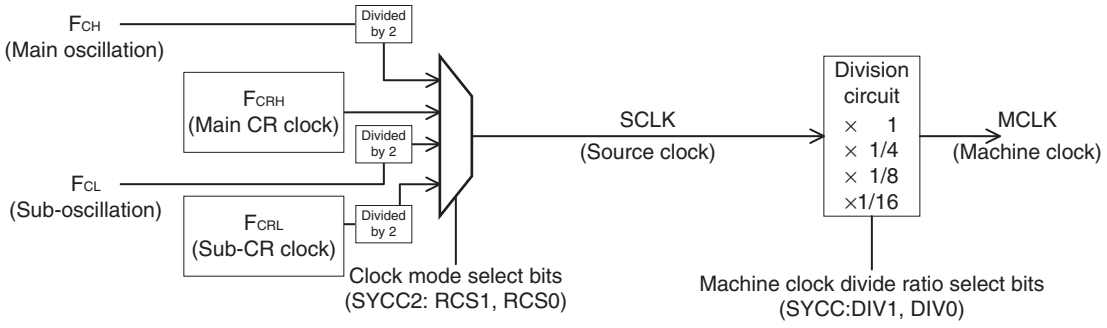
*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). This source clock is divided to become a machine clock according to the divide ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

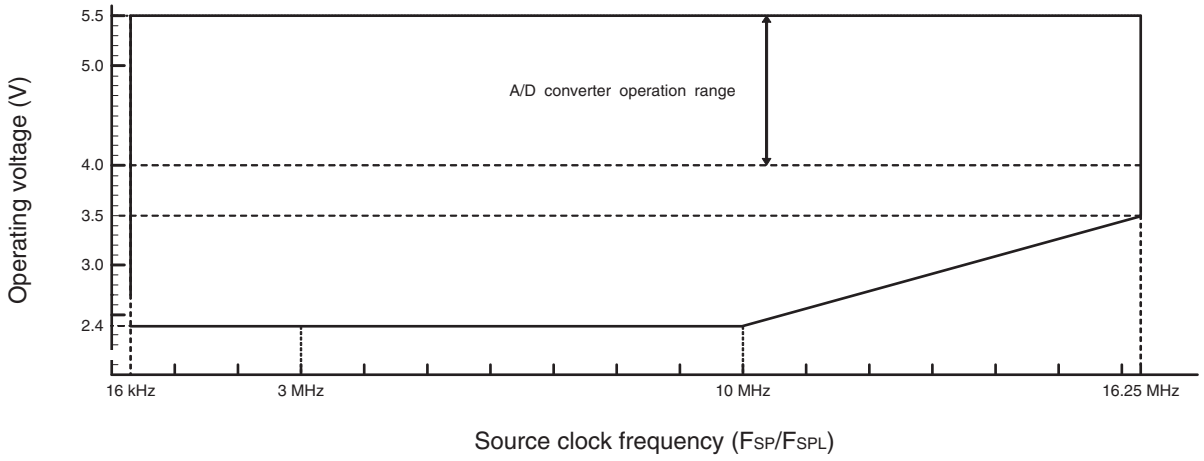
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

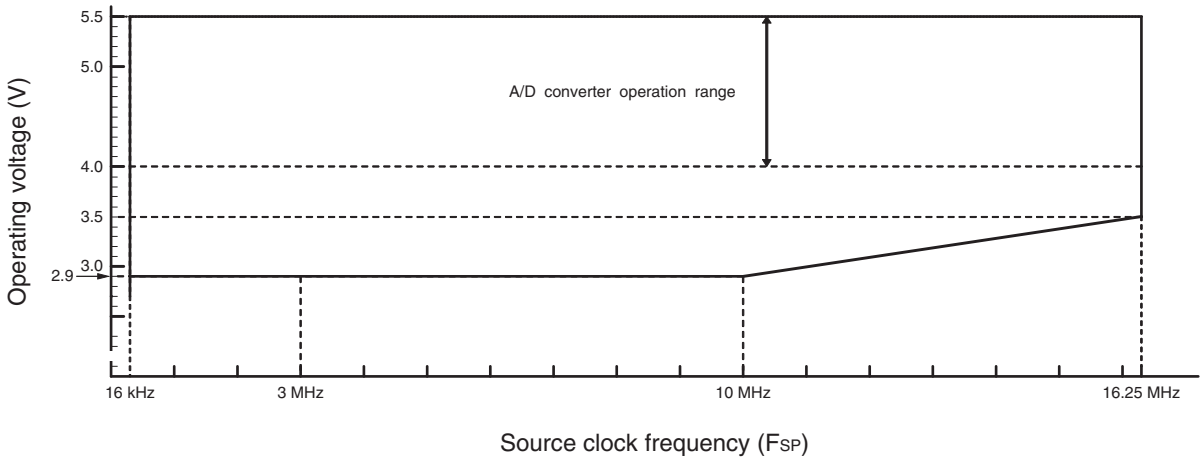
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  MB95330H (without the on-chip debug function)



- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  MB95330H (with the on-chip debug function)



13.4.3 External Reset

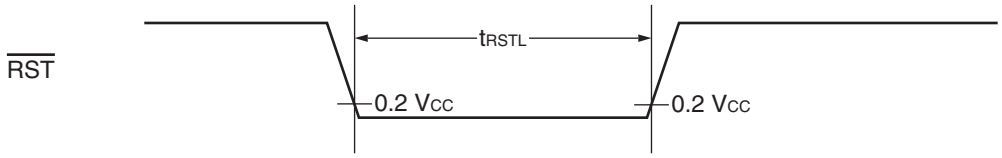
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

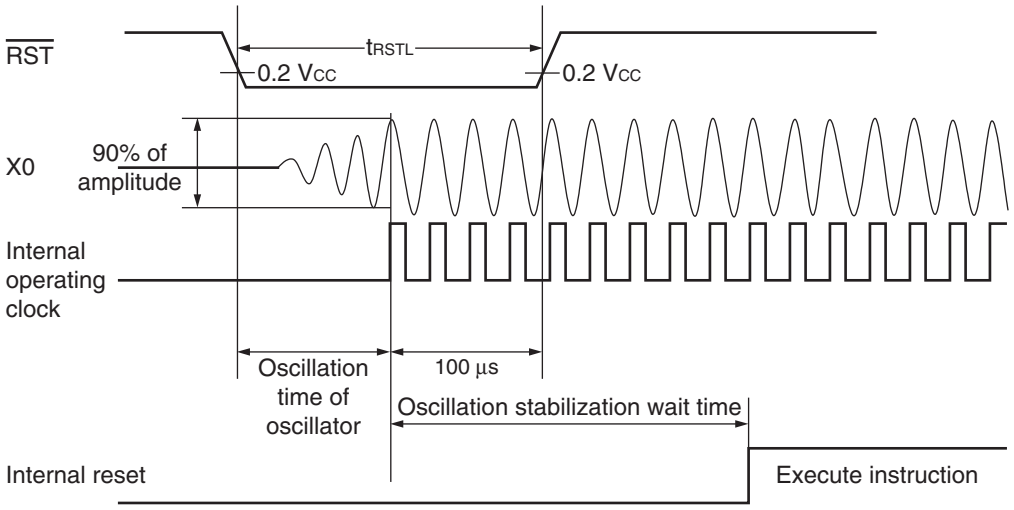
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



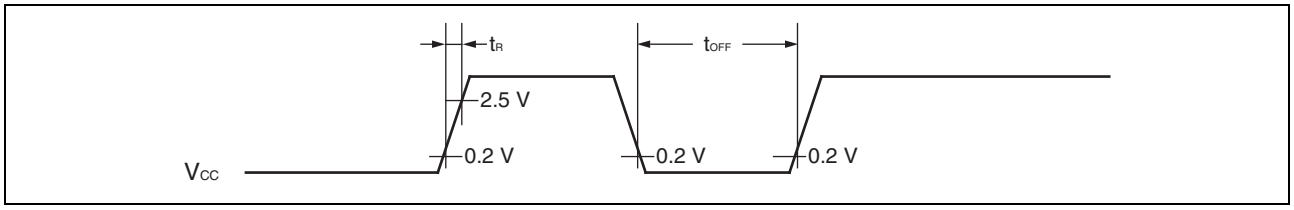
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



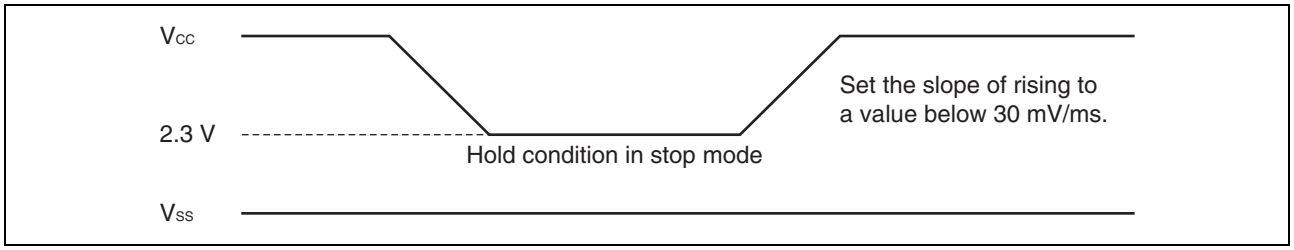
13.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

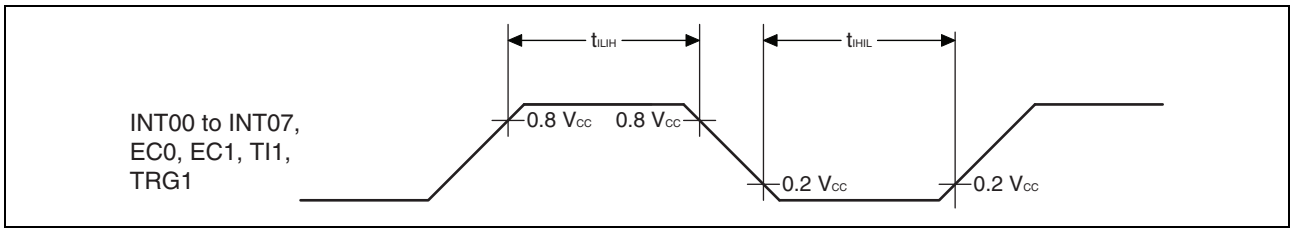


13.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT09, EC0, EC1,TI1, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



13.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

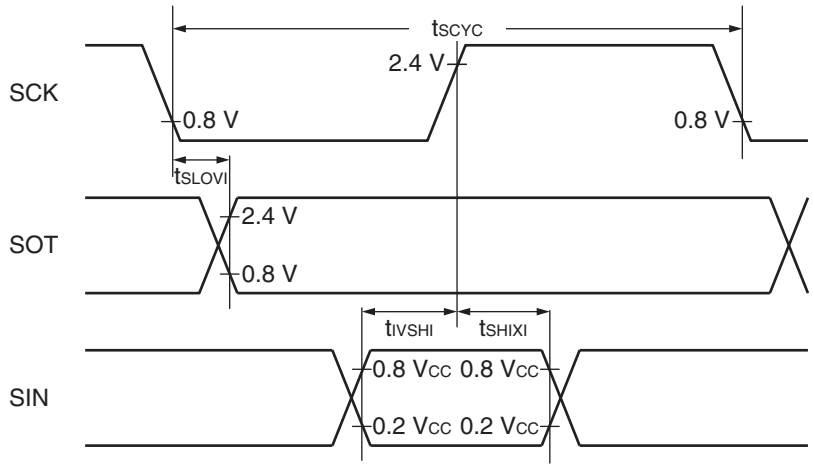
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

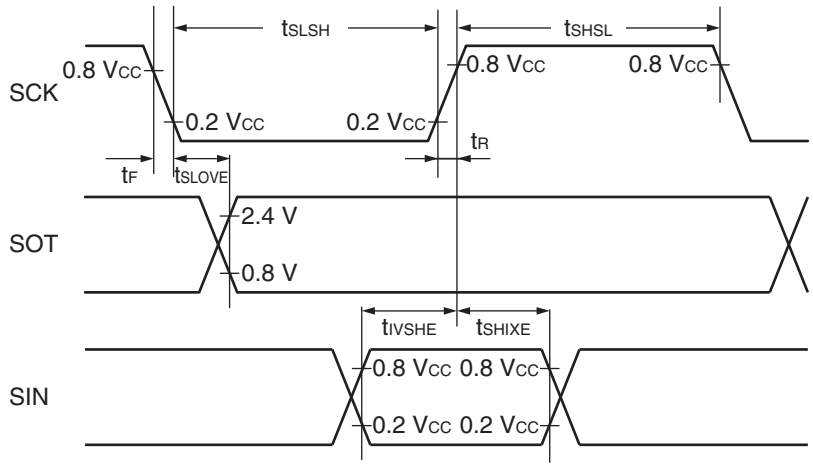
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

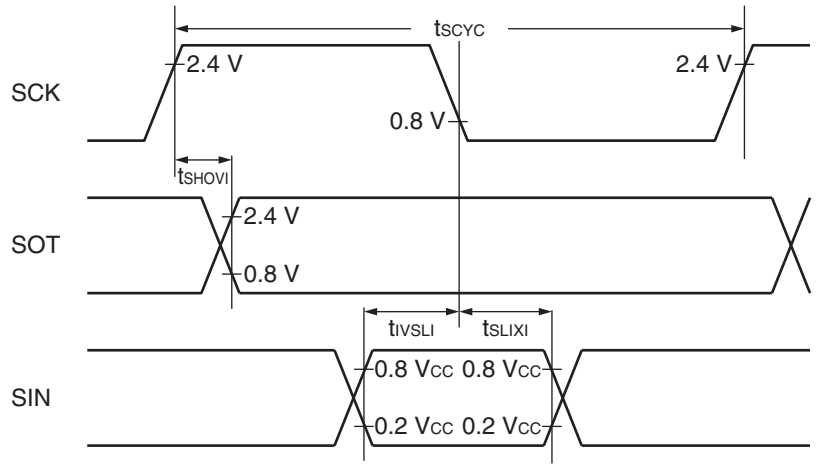
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

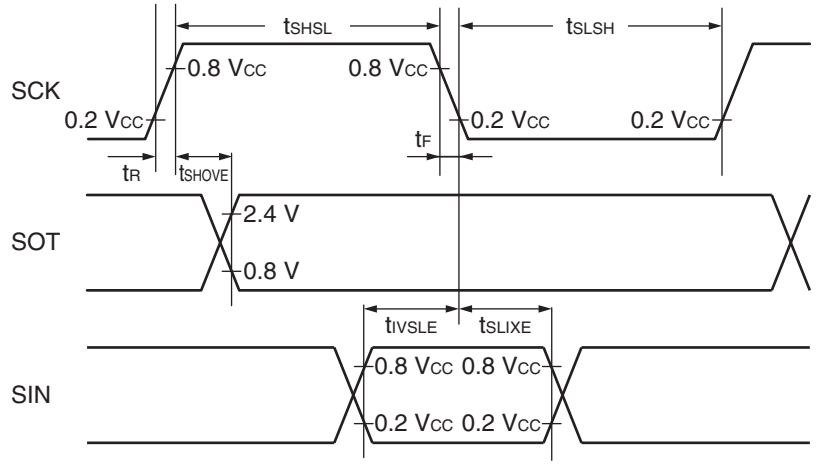
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

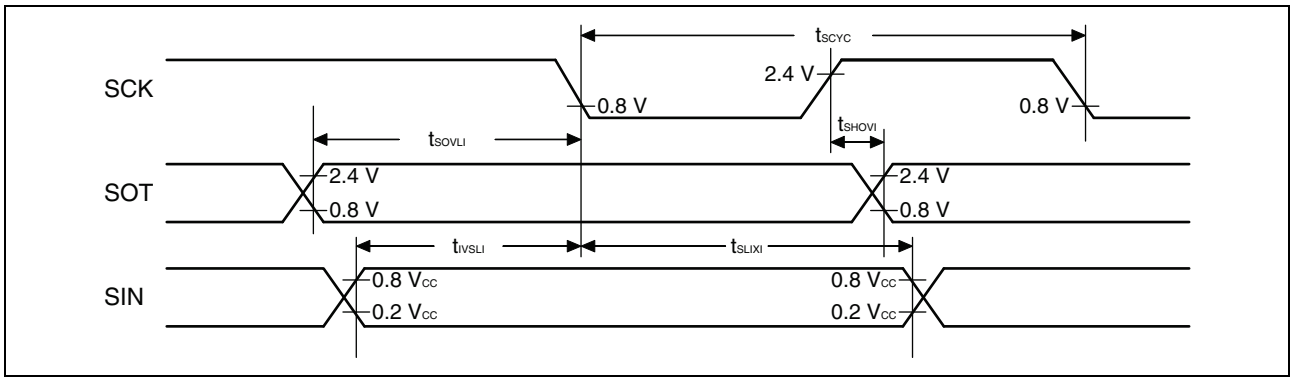
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

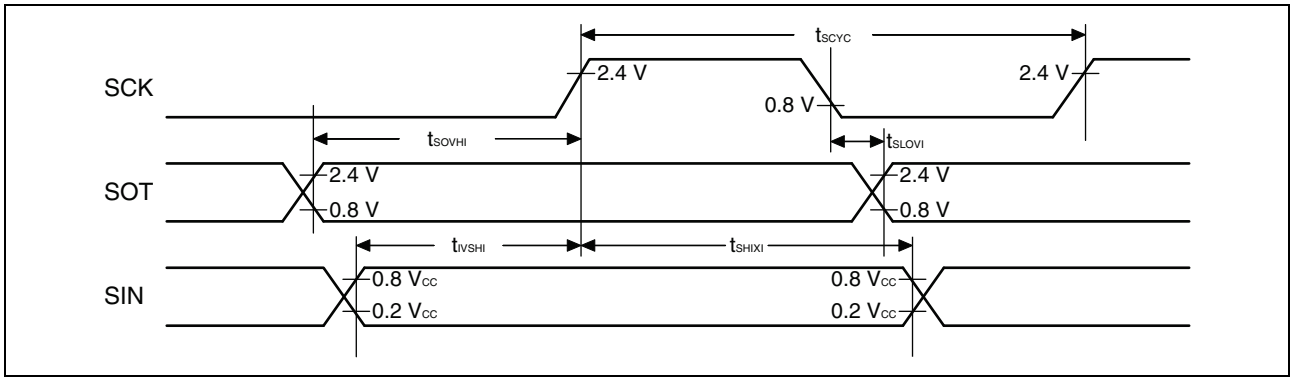
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

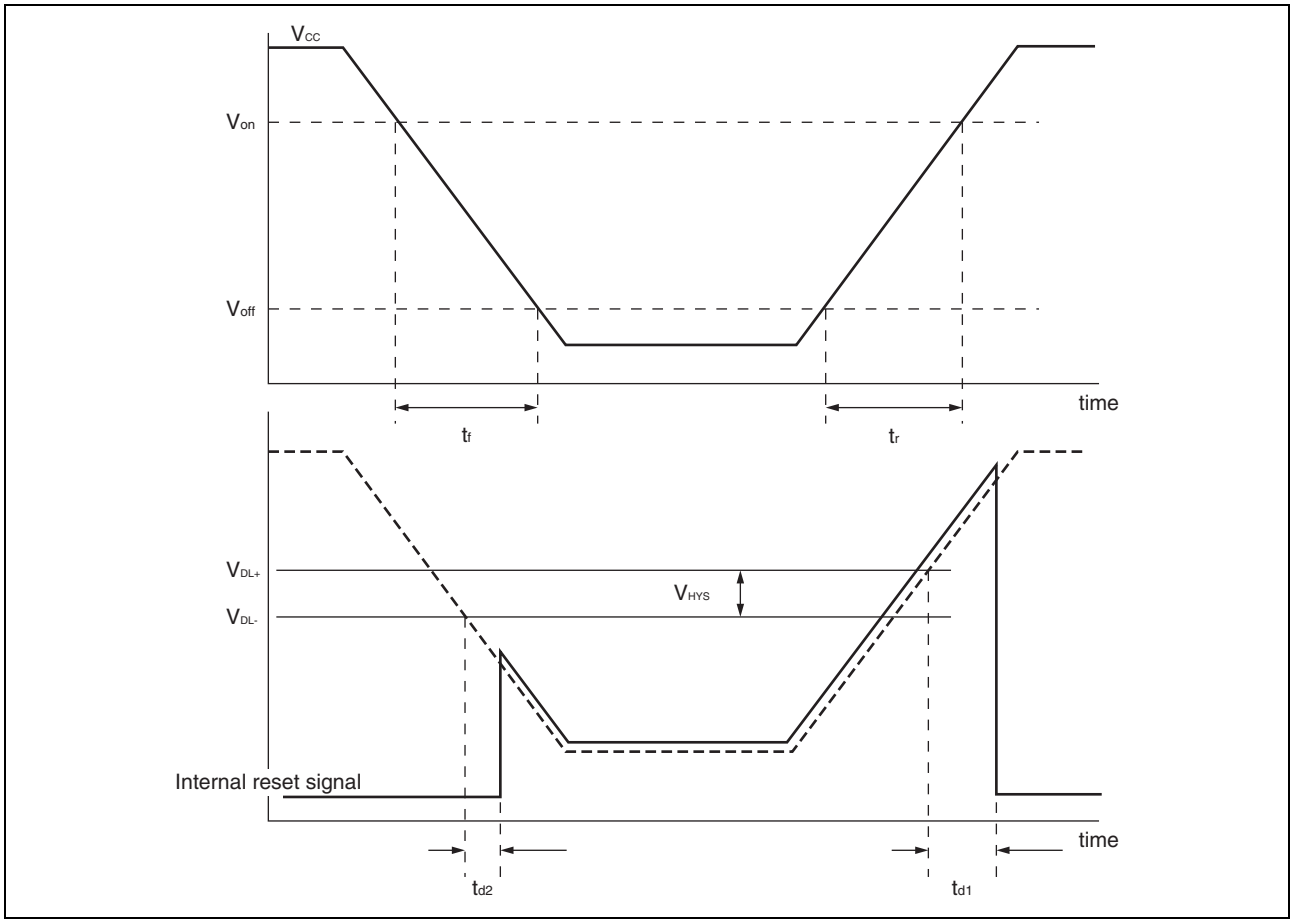
*3: See "(2) Source Clock/Machine Clock" for t_{MCLK}.



13.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	


V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

13.4.8 I²C Timing

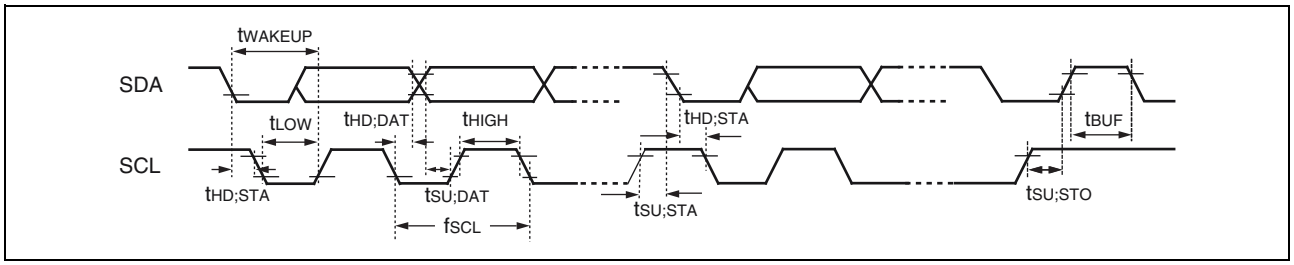
(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Stan-dard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition hold time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2\ nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to the interrupt at the 8th SCL↓.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} – 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} – 20	—	ns	At reception
SDA↓ → SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} – 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “(2) Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8): 0.9 MHz < $t_{MCLK} \leq$ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4): 0.9 MHz < $t_{MCLK} \leq$ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8): 0.9 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 98): 0.9 MHz < $t_{MCLK} \leq$ 10 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8): 3.3 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 22), (5, 4): 3.3 MHz < $t_{MCLK} \leq$ 8 MHz
  (m, n) = (6, 4): 3.3 MHz < $t_{MCLK} \leq$ 10 MHz

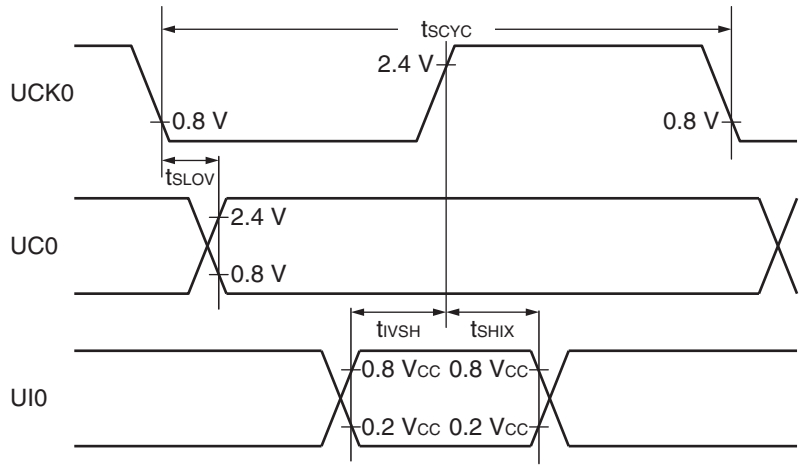
13.4.9 UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

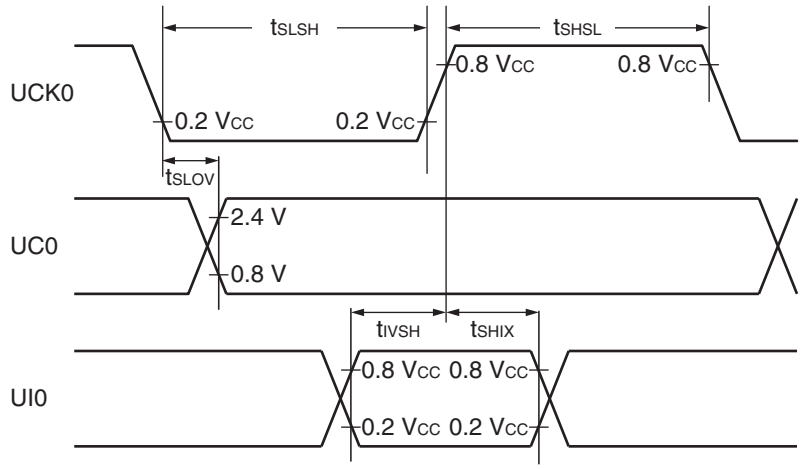
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		−190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



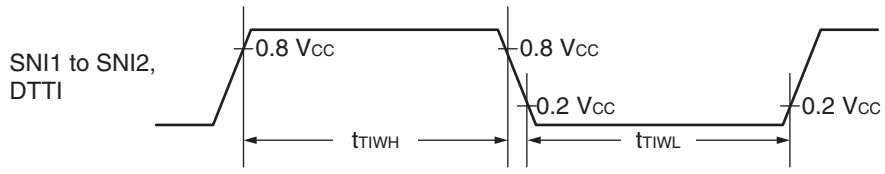
- External shift clock mode



13.4.10 MPG Input Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	SNI0 to SNI2, DTTI	—	4 t_{MCLK}	—	ns	



13.5 A/D Converter

13.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	

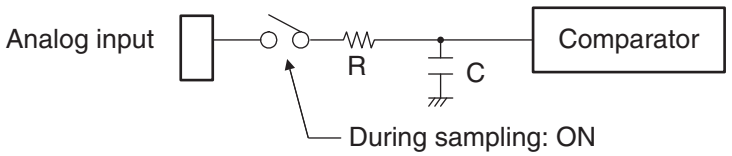
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Full-scale transition voltage	V_{FST}	V_{CC} − 4.5 LSB	V_{CC} − 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

13.5.2 Notes on Using the A/D Converter

■ **External impedance of analog input and its sampling time**

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

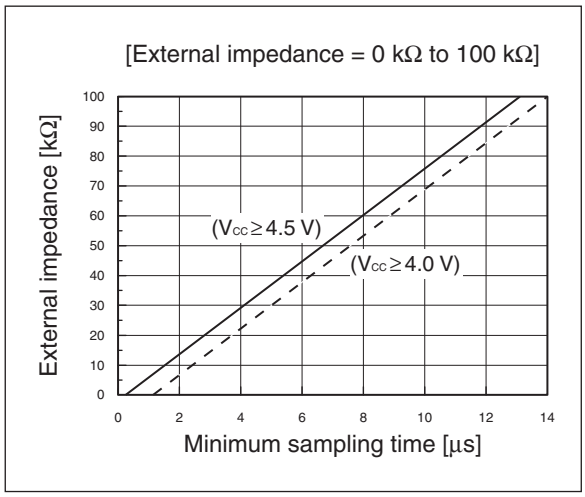
- Analog input equivalent circuit

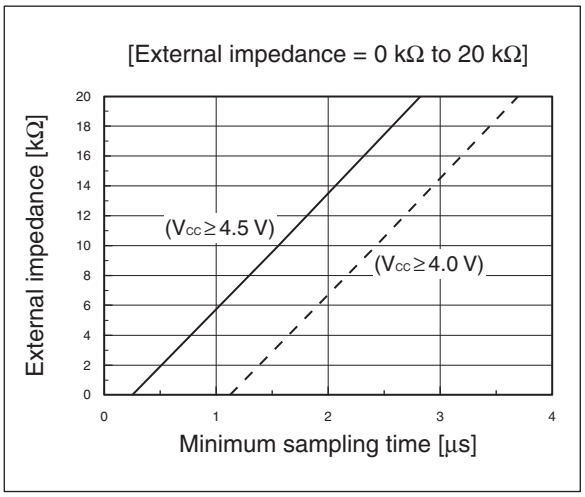


V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.95 kΩ (Max)	17 pF (Max)
4.0 V ≤ V_{CC} < 4.5 V	8.98 kΩ (Max)	17 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time





■ **A/D conversion error**

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

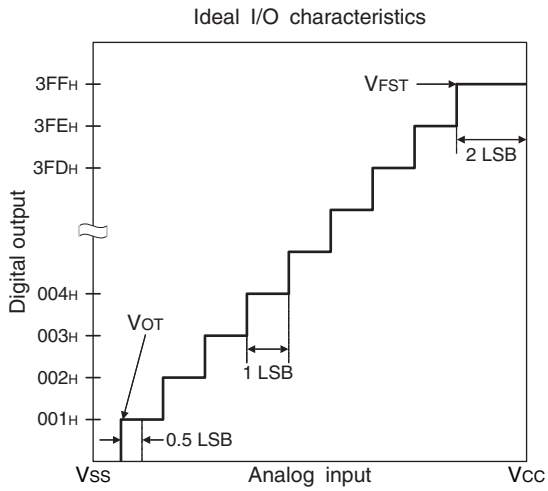
13.5.3 Definitions of A/D Converter Terms

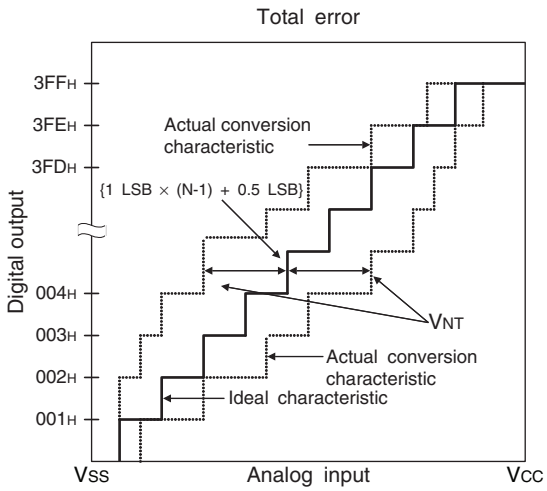
■ Resolution
It indicates the level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

■ Linearity error (unit: LSB)
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.

■ Differential linear error (unit: LSB)
It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

■ Total error (unit: LSB)
It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

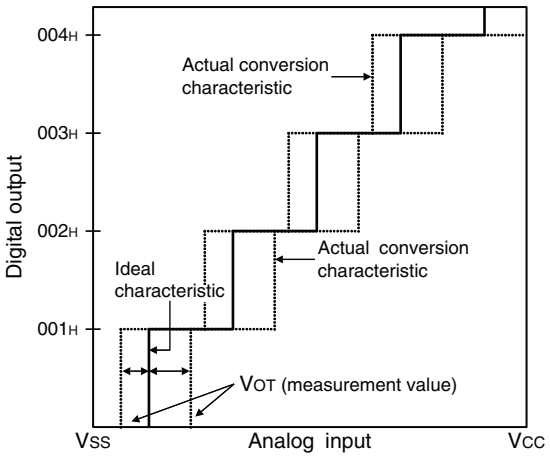
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

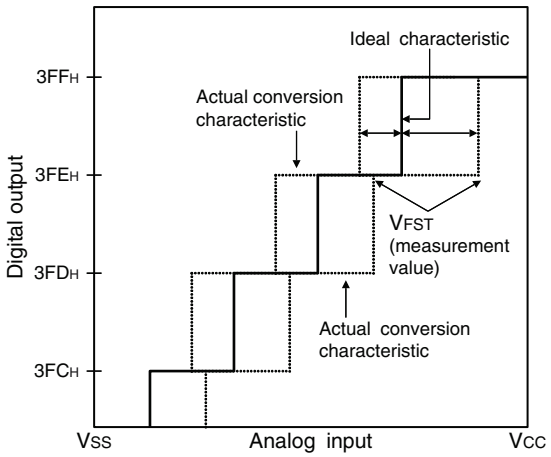
(Continued)

(Continued)

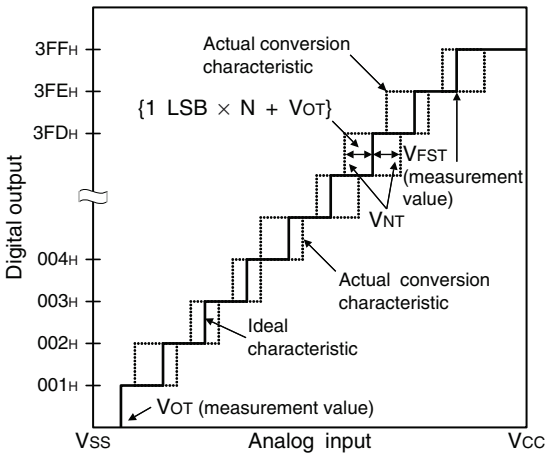
Zero transition error



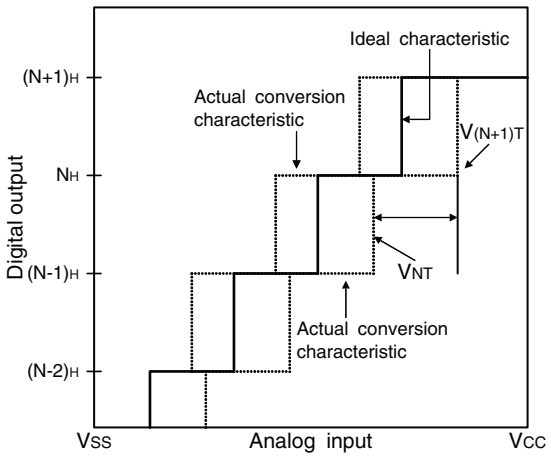
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

13.6 Flash Memory Write/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Erase/write cycle	100000	—	—	cycle	
Power supply voltage at erase/write	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

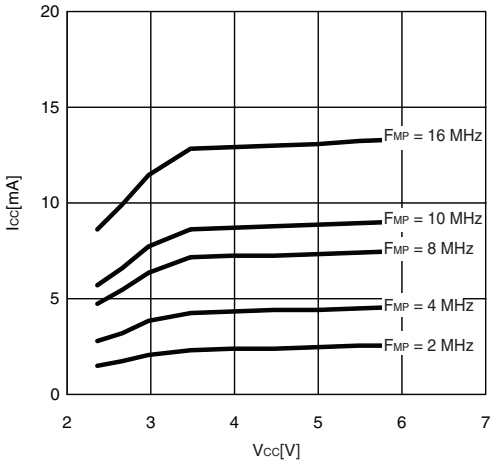
*2: T_A = +85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

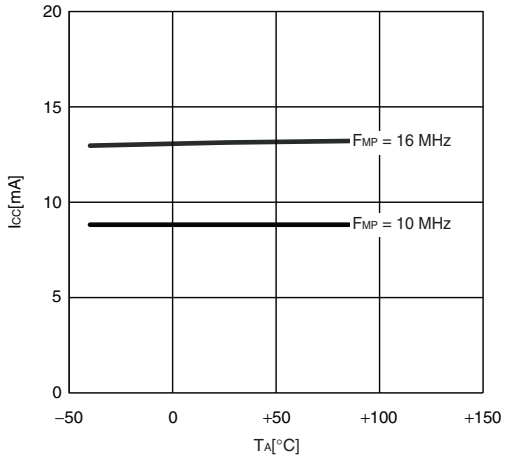
14. Sample Characteristics

■ Power supply current temperature characteristics

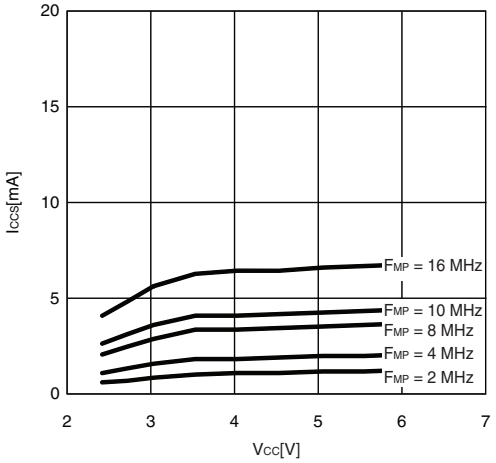
$I_{CC} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



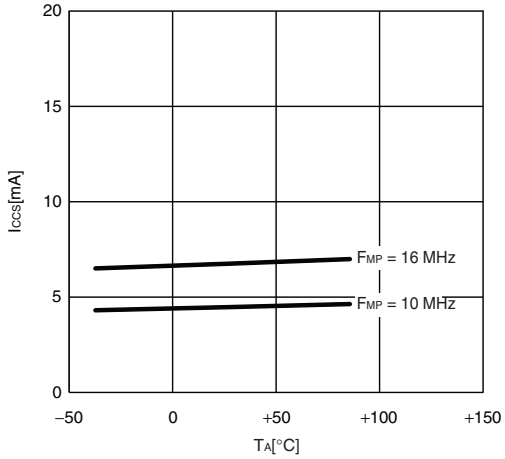
$I_{CC} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



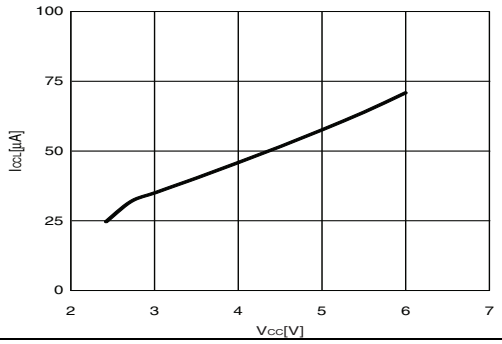
$I_{CCS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



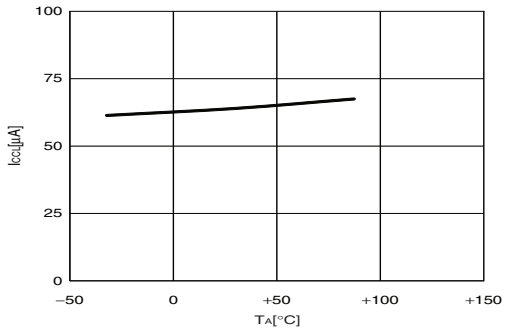
$I_{CCS} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



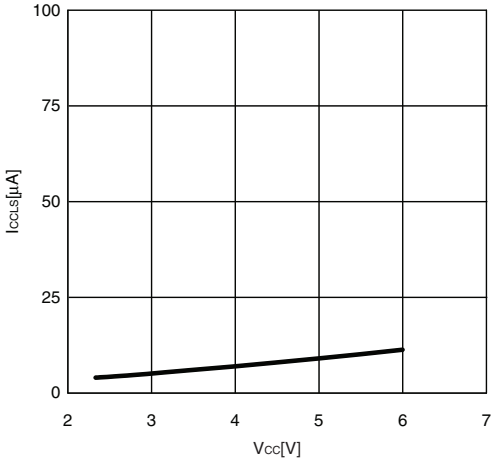
$I_{CCL} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



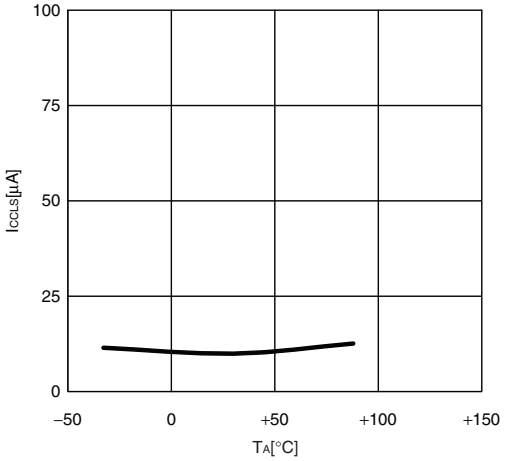
$I_{CCL} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



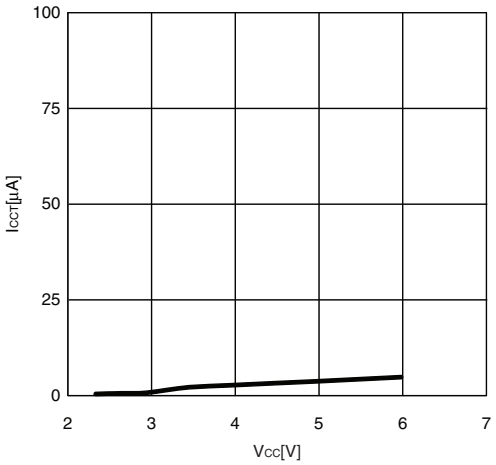
$I_{CCLS} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



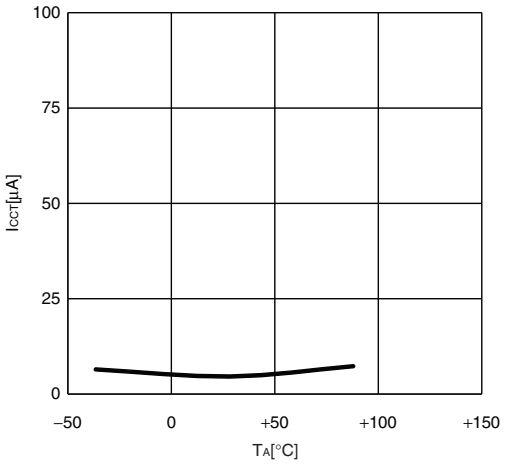
$I_{CCLS} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



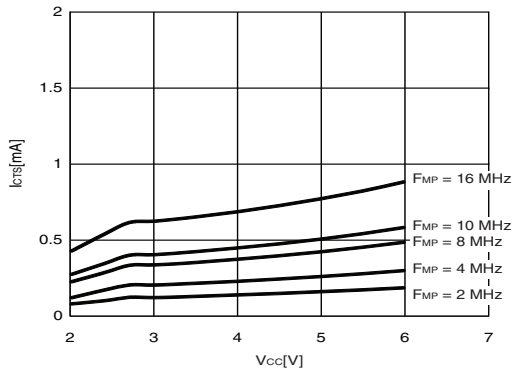
$I_{CCT} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



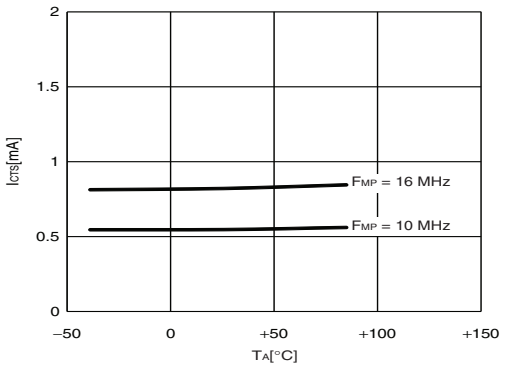
$I_{CCT} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



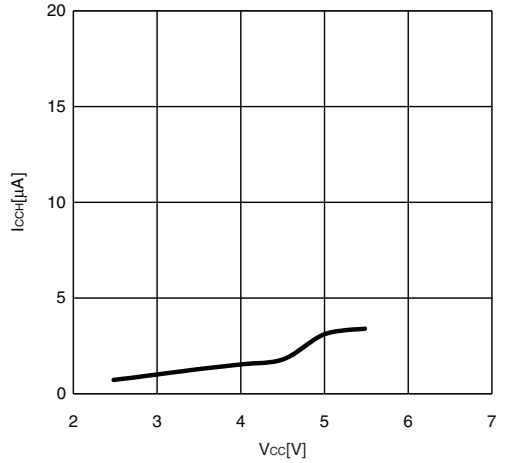
$I_{CTS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



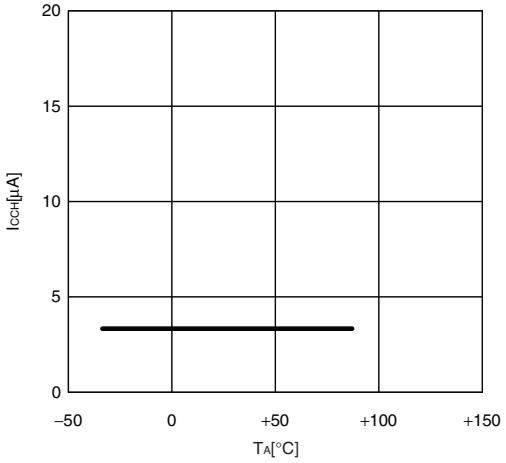
$I_{CTS} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



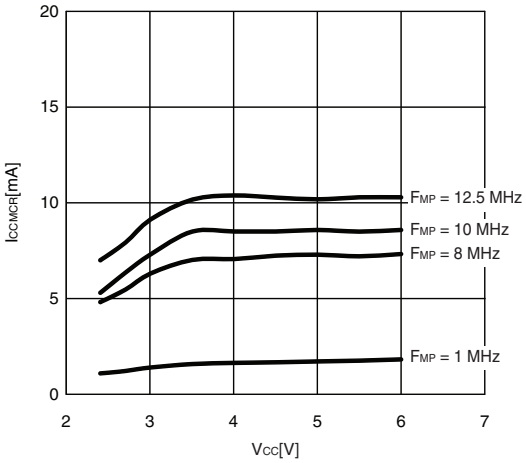
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



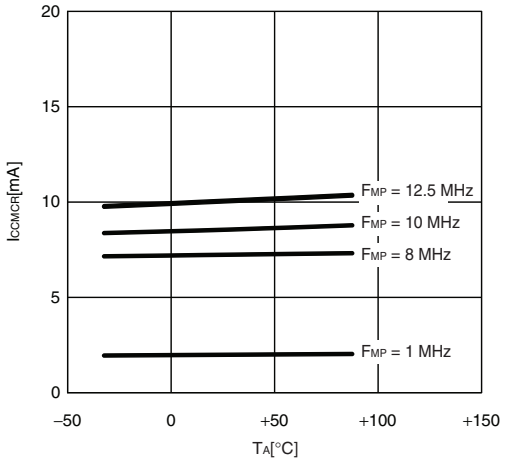
I_{CCH} – T_A
V_{CC} = 5.5 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



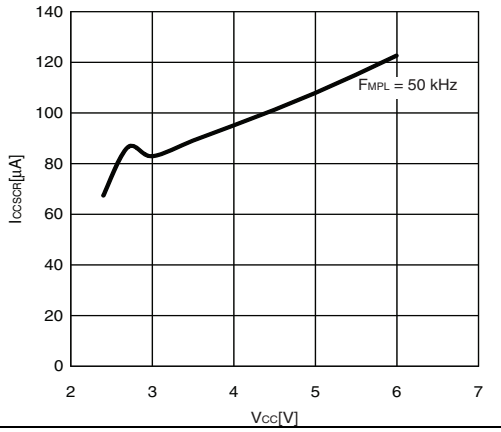
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



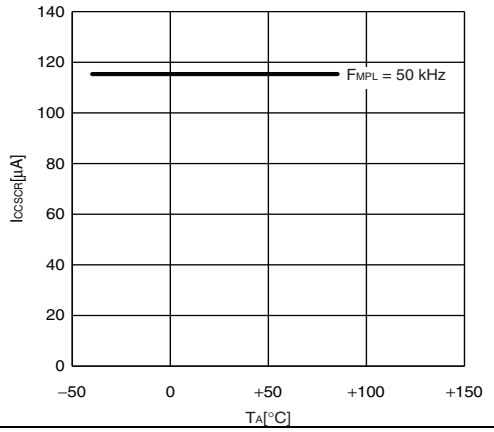
I_{CCMCR} – T_A
V_{CC} = 5.5 V F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



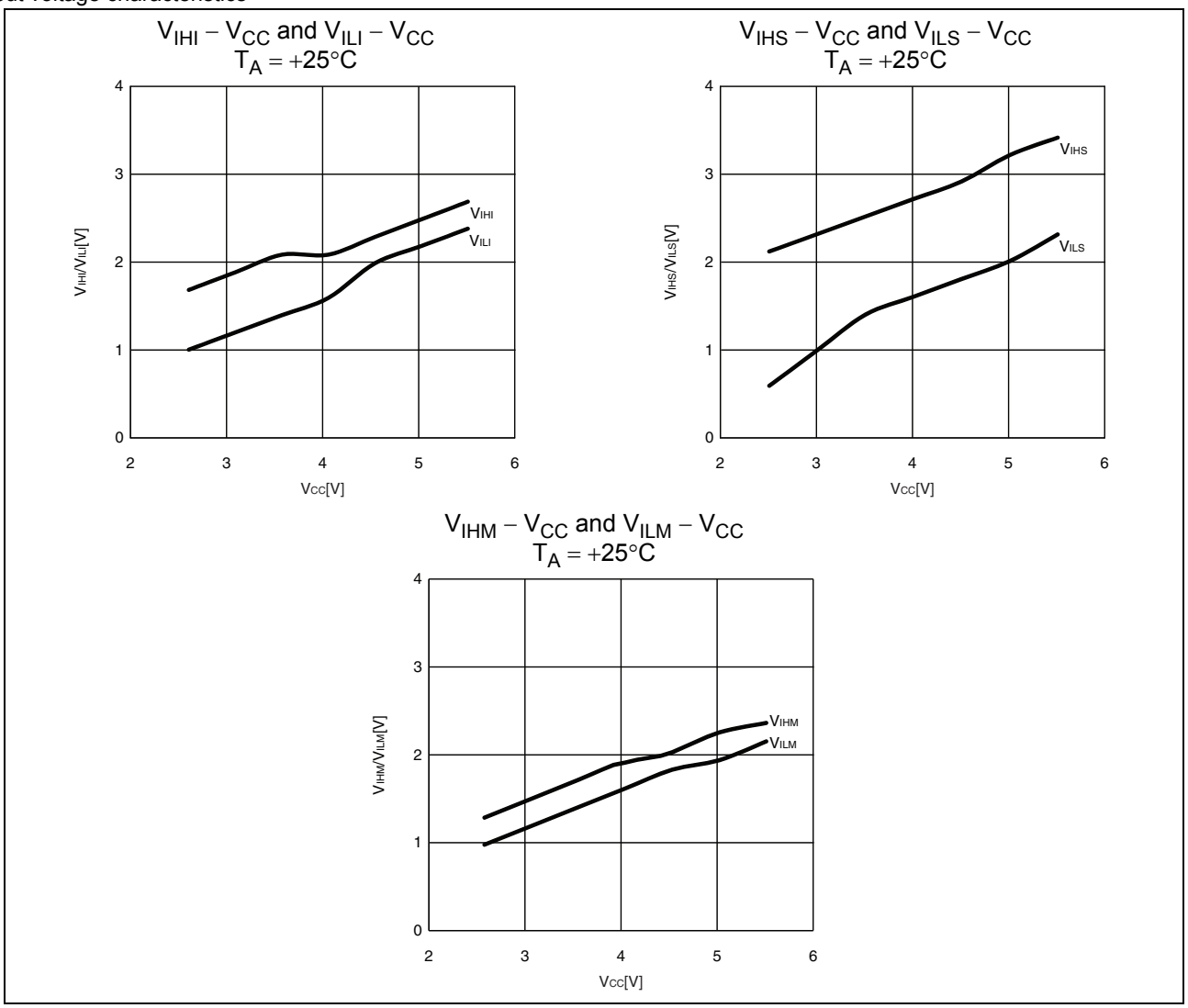
I_{CCSCR} – V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



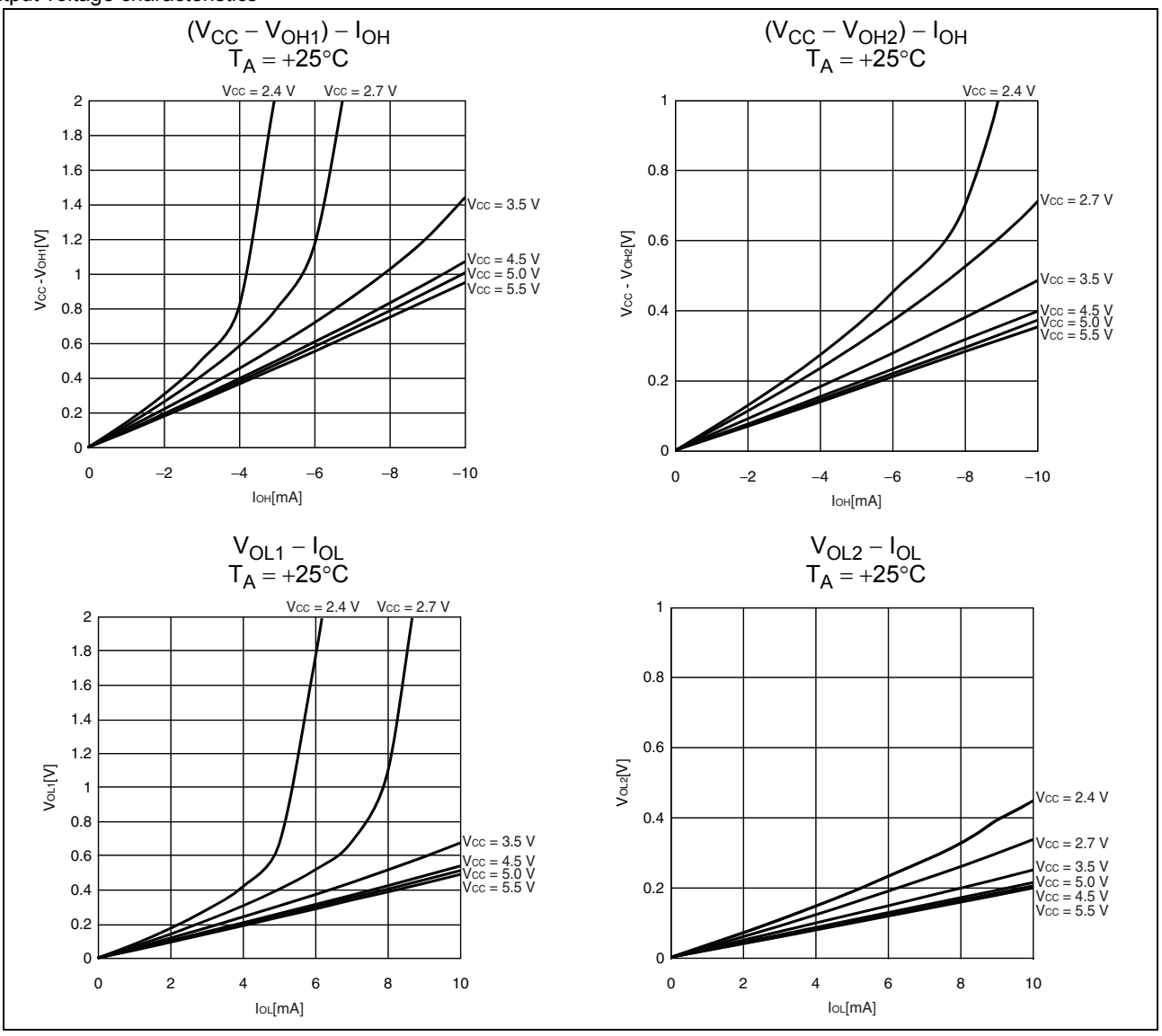
I_{CCSCR} – T_A
V_{CC} = 5.5 V F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



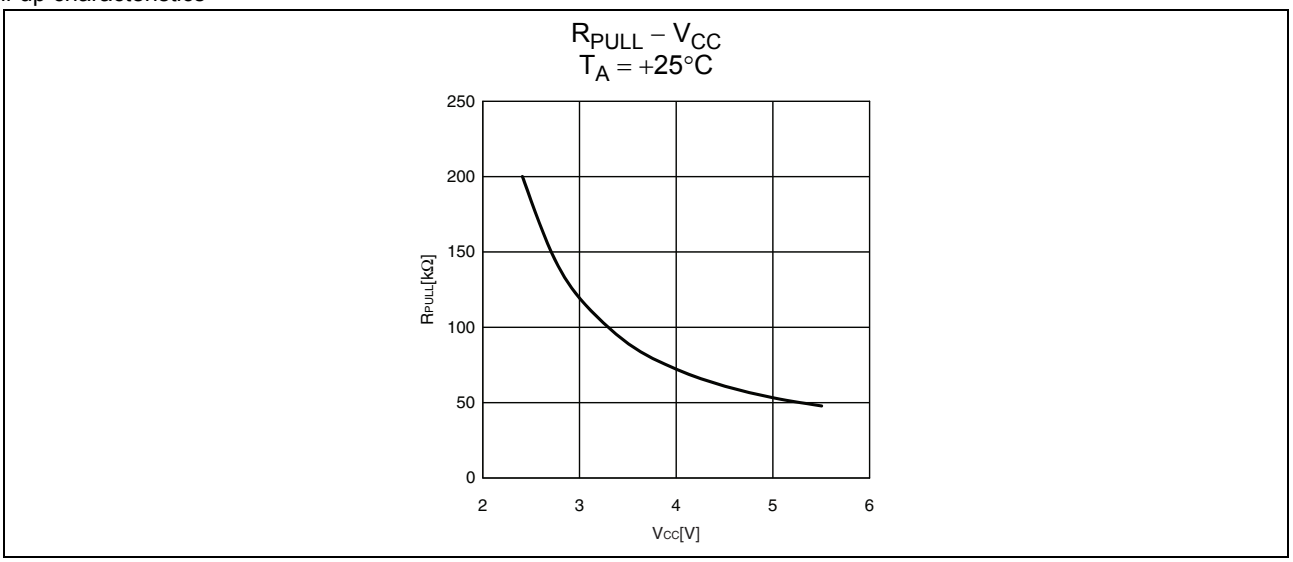
■ Input voltage characteristics



■ Output voltage characteristics



■ Pull-up characteristics



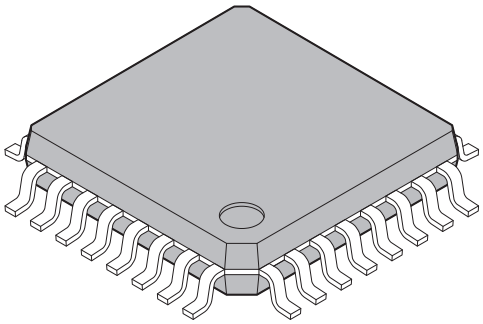
15. Mask Options

No.	Part Number	MB95F332H MB95F333H MB95F334H	MB95F332K MB95F333K MB95F334K
	Selectable/Fixed	**Fixed**	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

16. Ordering Information

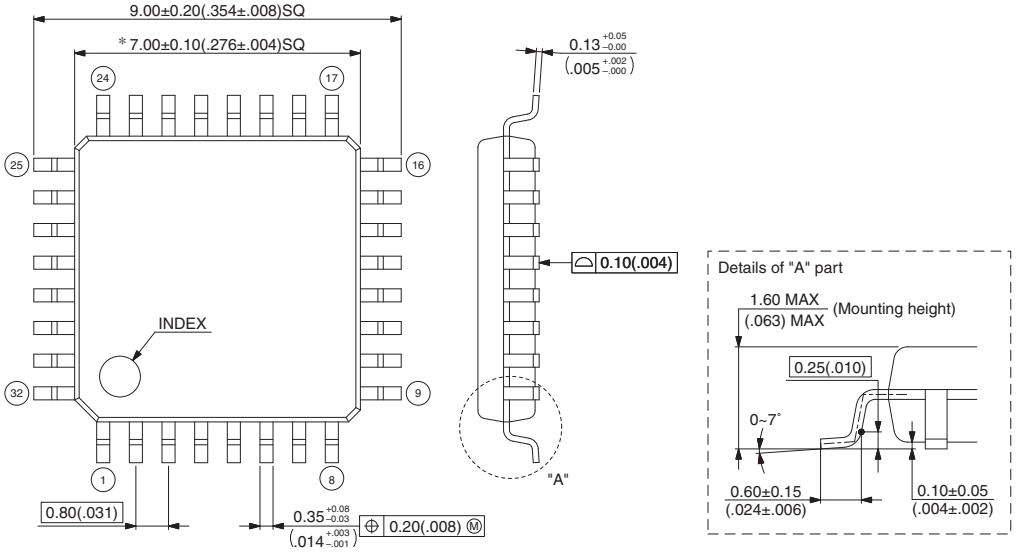
Part Number	Package
MB95F332HPMC-G-SNE2 MB95F332KPMC-G-SNE2 MB95F333HPMC-G-SNE2 MB95F333KPMC-G-SNE2 MB95F334HPMC-G-SNE2 MB95F334KPMC-G-SNE2	32-pin plastic LQFP (FPT-32P-M30)
MB95F332HP-G-SH-SNE2 MB95F332KP-G-SH-SNE2 MB95F333HP-G-SH-SNE2 MB95F333KP-G-SH-SNE2 MB95F334HP-G-SH-SNE2 MB95F334KP-G-SH-SNE2	32-pin plastic SH-DIP (DIP-32P-M06)
MB95F332HWQN-G-SNE1 MB95F332KWQN-G-SNE1 MB95F333HWQN-G-SNE1 MB95F333KWQN-G-SNE1 MB95F334HWQN-G-SNE1 MB95F334KWQN-G-SNE1	32-pin plastic QFN (LCC-32P-M19)

17. Package Dimension

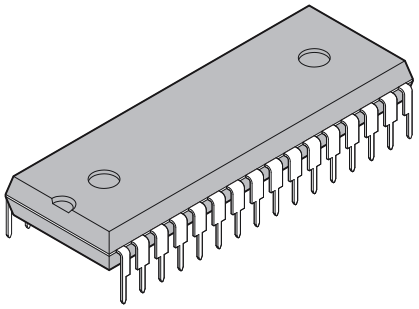
32-pin plastic LQFP		
 (FPT-32P-M30)	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX

32-pin plastic LQFP
(FPT-32P-M30)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

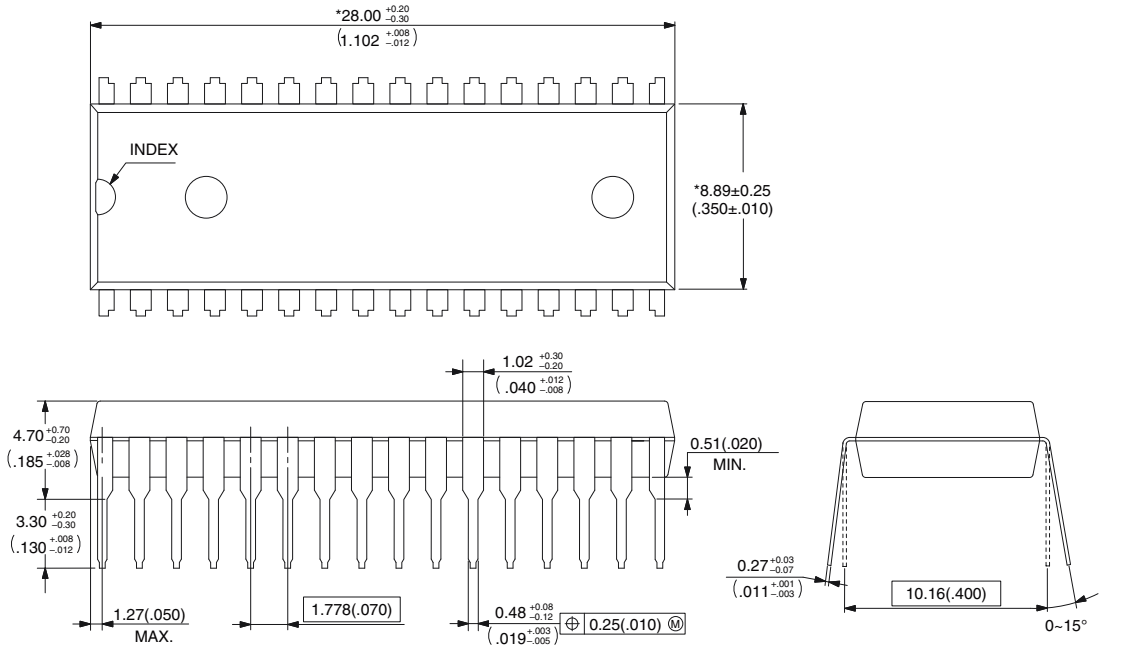


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

32-pin plastic SH-DIP		
	Lead pitch	1.778 mm
	Low space	10.16 mm
	Sealing method	Plastic mold
(DIP-32P-M06)		

32-pin plastic SH-DIP
(DIP-32P-M06)

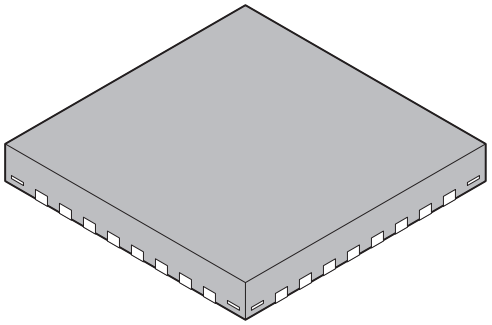
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



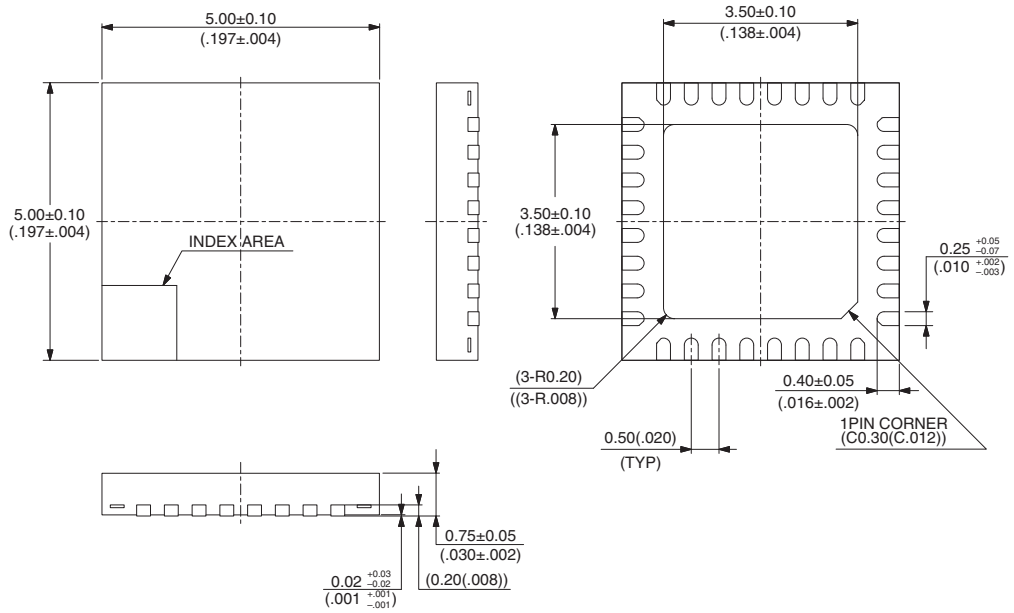
Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

(Continued)

32-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g
(LCC-32P-M19)		

32-pin plastic QFN
(LCC-32P-M19)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Document History

Document Title: MB95F332H/F332K/F333H/F333K/F334H/F334K F^{2}MC-8FX MB95330H Series 8-bit Microcontrollers Document Number: 002-07522				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	04/12/2010	Migrated to Cypress and assigned document number 002-07522. No change to document contents or format.
*A	5181238	AKIH	04/04/2016	Updated to Cypress template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

cypress.com/psoc

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/support

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MB95F332KP-G-SH-SNE2 on WIN SOURCE
- Infineon Technologies Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management