



**THE DATASHEET OF  
ZL30160GGG2**



### Features

- Four independent clock channels
- Programmable synthesizers generate any clock-rate from 1 kHz to 750 MHz
- Two precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- Two general purpose synthesizers generate a wide range of digital bus clocks
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 750 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential

### Ordering Information

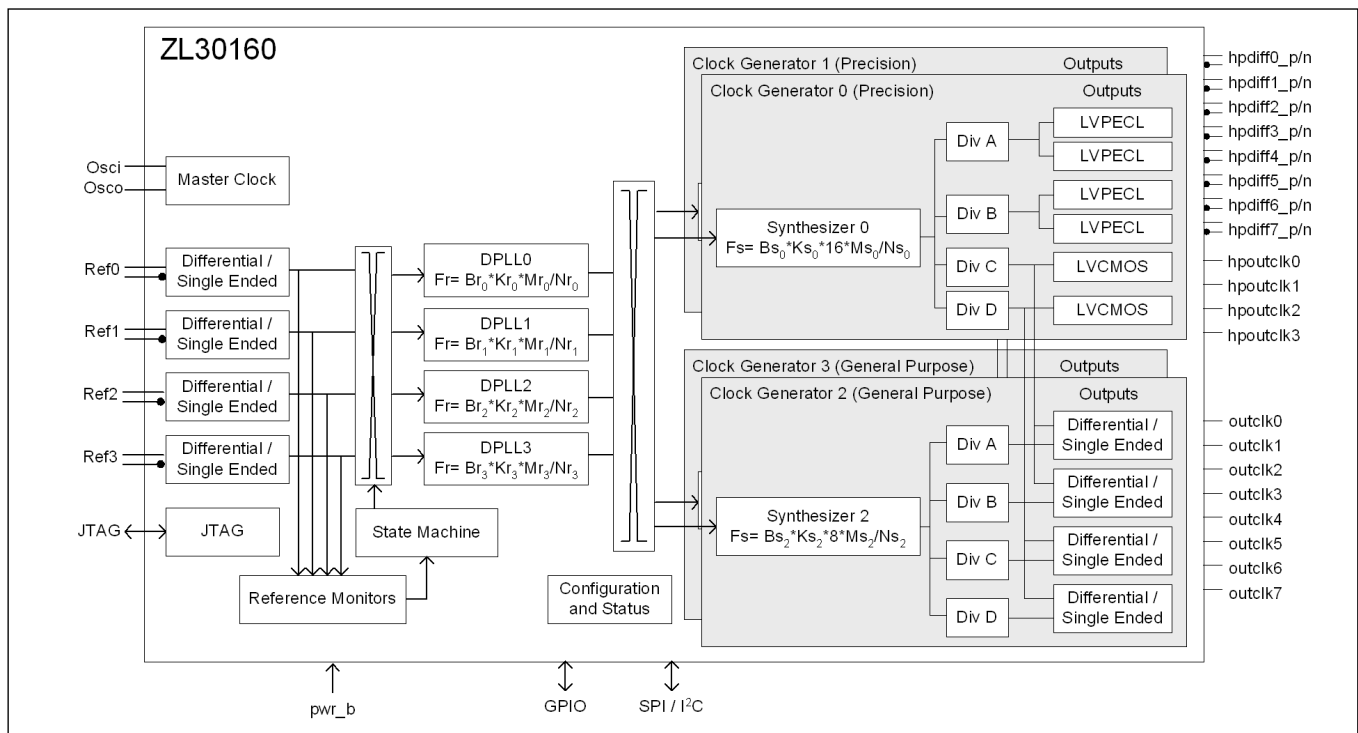
ZL30160GGG	100 Pin LPGA	Trays
ZL30160GGG2	100 Pin LPGA*	Trays

\*Pb Free Tin/Silver/Copper  
-40°C to +85°C

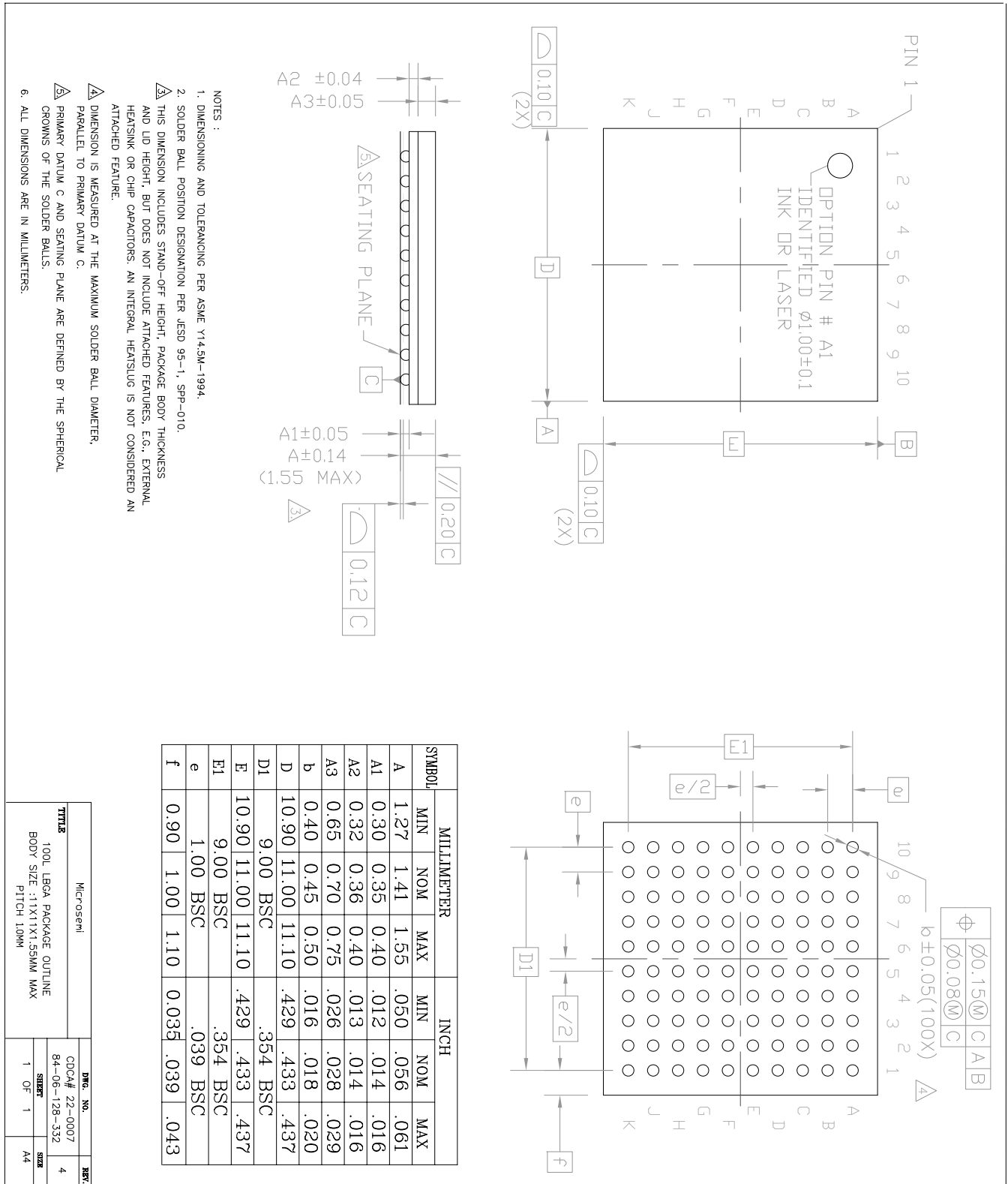
- Eight LVPECL outputs and four LVCMOS outputs
- Eight outputs configurable as LVCMOS or LVDS/LVPECL/HCSL
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

### Applications

- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI



**Figure 1 - Functional Block Diagram**

**Mechanical Drawing**


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