THE DATASHEET OF

Z86E2304PSC

Z86E23

KEYBOARD MICROCONTROLLER WITH 8K OTP

FEATURES

Device	EPROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86E23	8	236	32	4.5V to 5.5V

Note: *General-Purpose

- 40-Pin DIP or 44-Pin PLCC Package
- Low Power Consumption - 165 mW (max.) With Two Standby Modes: STOP & HALT
- All Digital Inputs are TTL Levels
- High-Voltage Protection on High-Voltage Inputs
- 8 KB of EPROM
- 256 Bytes of RAM (236 for General-Purpose)
- Two Programmable 8-Bit Counter/Timers Each With a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- System Clock Speeds up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive

GENERAL DESCRIPTION

The Z86E23 microcontroller is a member of the Z8® MCU single-chip family with 8 KB of EPROM and 236 bytes of general-purpose RAM.

The Z86E23 is a pin-compatible, One-Time-Programmable (OTP) version of the Z8614 and Z8602 Keyboard Controller.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low-cost and low-power consumption.

The Z86E23 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

There are two basic address spaces available to support this wide range of configurations: Program Memory and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing, the Z86E23 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

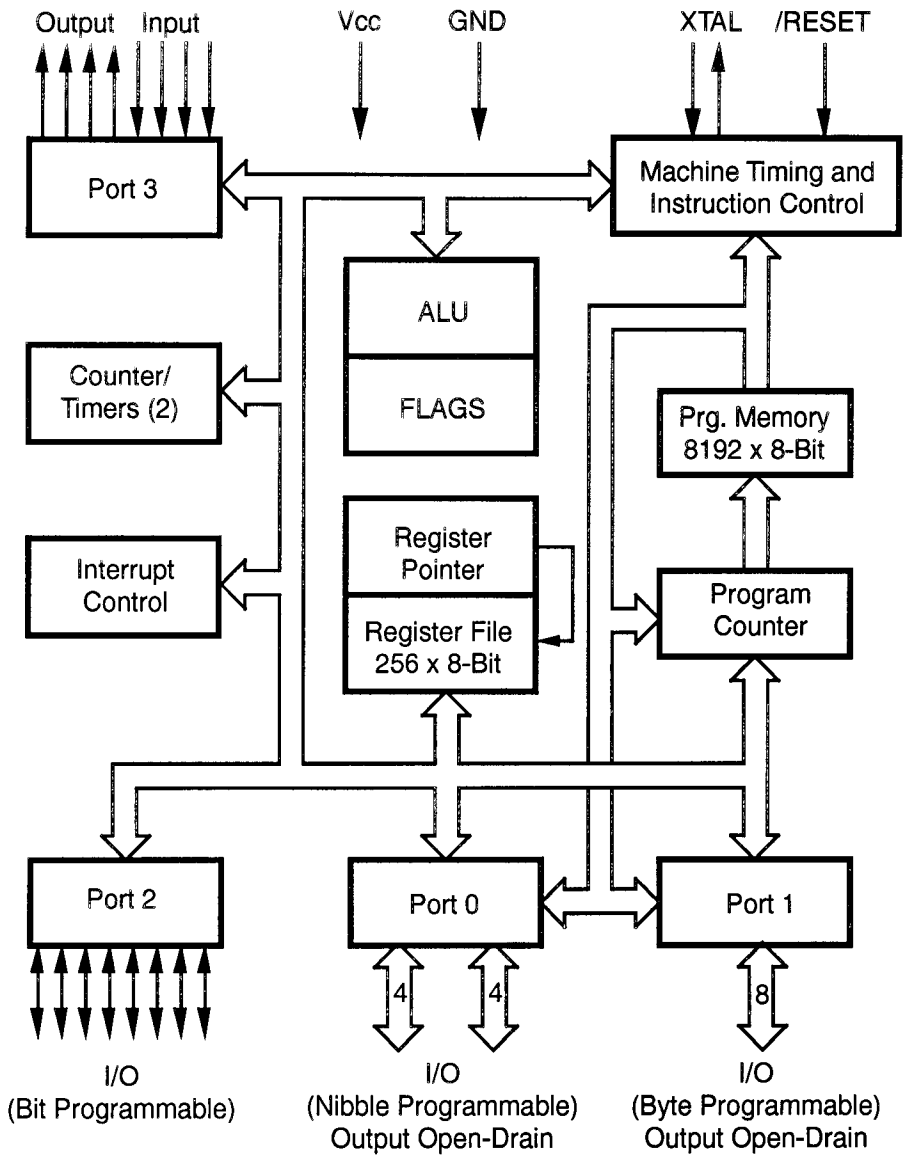


Figure 1. Functional Block Diagram

PIN DESCRIPTION

Standard Mode

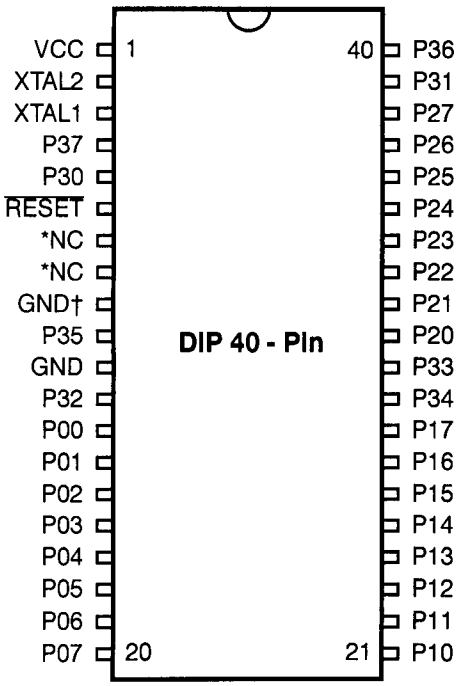


Figure 2. 40-Pin DIP Pin Configuration

Table 1. 40-Pin DIP Configuration

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	RESET	Reset	Input
7	*NC	No Connection	
8	*NC	No Connection	
9	GND†	Ground	Input
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-P27	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

Note:
*Pins 7 and 8 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 9 must be grounded.

PIN DESCRIPTION (Continued)

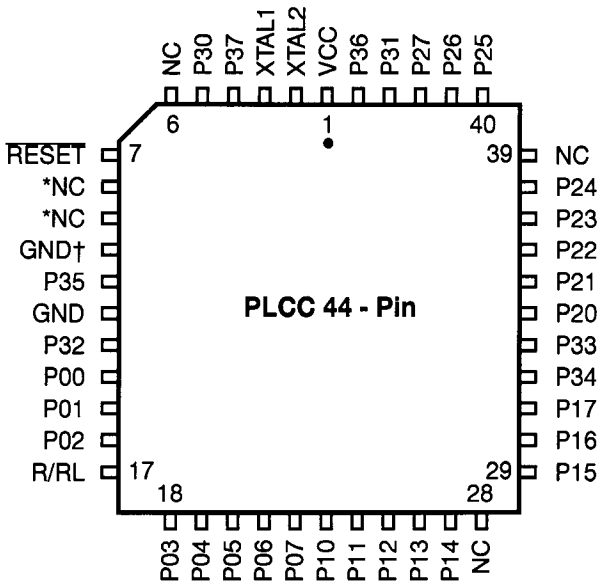


Figure 3. 44-Pin PLCC Pin Configuration

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	$\overline{\text{RESET}}$	Reset	Input
8	*NC	Not Connected	
9	*NC	Not Connected	
10	GND†	Ground	
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P00-P02	Port 0, Pins 0,1,2	In/Output
17	R/RL	ROM/ROMless Control	Input

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
18-22	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output
23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
28	NC	Not Connected	
29-31	P15-P17	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
39	NC	Not Connected	
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

Notes:
*Pins 8 and 9 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 10 must be grounded.

PIN DESCRIPTION

EPROM Mode

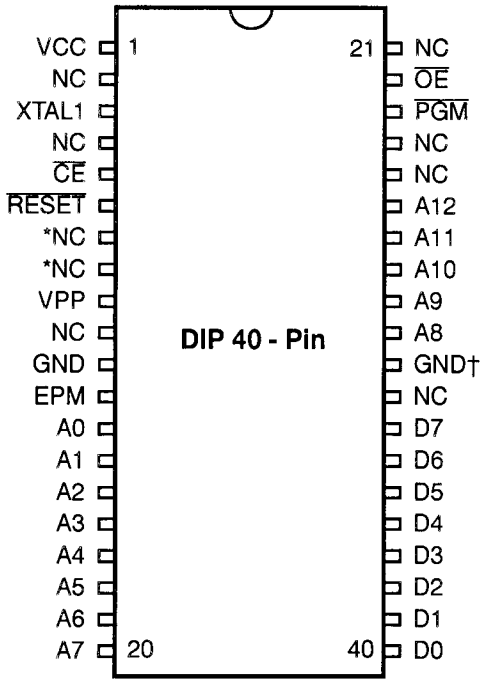


Figure 4. 40-Pin DIP Pin Configuration (EPROM Mode)

Table 3. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	NC	Not Connected	
3	XTAL1	Crystal, Oscillator Clock	Input
4	NC	Not Connected	Input
5	$\overline{CE}$	Chip Enable	Input
6	$\overline{RESET}$	Reset	Input
7	*NC	Not Connected	
8	*NC	Not Connected	
9	VPP	Prog Voltage	Input
10	NC	Not Connected	
11	GND	Ground	Input
12	EPM	EPROM Prog Mode	Input
13-20	A0-A7	Address 0,1,2,3,4,5,6,7	Input
21-28	D0-D7	Data 0,1,2,3,4,5,6,7	In/Output
29	NC	Not Connected	
30	GND†	Ground	Input
31-35	A8-A12	Address 8,9,10,11,12	Input
36-37	NC	Not Connected	
38	/PGM	Prog Mode	Input
39	/OE	Output Enable	Input
40	NC	Not Connected	

Notes:
*Pins 7 and 8 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 30 must be grounded.

PIN DESCRIPTION (Continued)

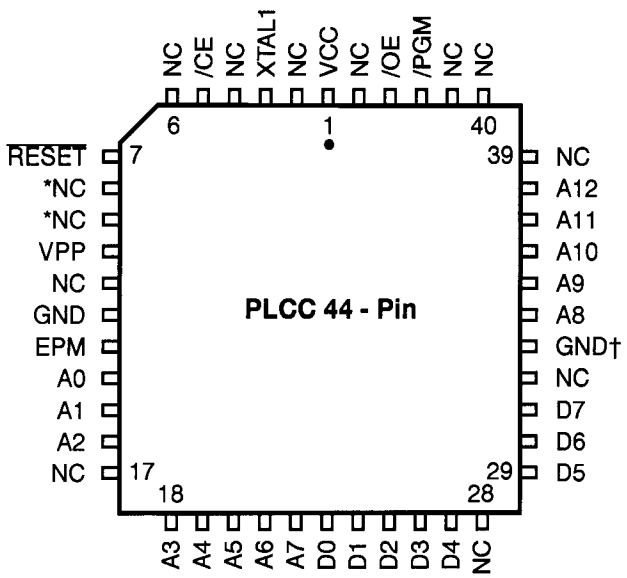


Figure 5. 44-Pin PLCC Pin Configuration (EPROM Mode)

Table 4. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	NC	Not Connected	
3	XTAL1	Crystal, Oscillator Clock	Input
4	NC	Not Connected	
5	/CE	Chip Enable	Input
6	NC	Not Connected	
7	$\overline{\text{RESET}}$	Reset	Input
8	*NC	Not Connected	
9	*NC	Not Connected	
10	V_{PP}	Prog Voltage	Input
11	NC	Not Connected	
12	GND	Ground	Input
13	EPM	EPROM Prog. Mode	Input
14-16	A0-A2	Address 0,1,2	Input
17	NC	Not Connected	
18-22	A3-A7	Address 3,4,5,6,7	Input

Table 4. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
23-27	D0-D4	Data 0,1,2,3,4	In/Output
28	NC	Not Connected	
29-31	D5-D7	Data 5,6,7	In/Output
32	NC	Not Connected	
33	GND†	Ground	Input
34-38	A8-A12	Address 8,9,10,11,12	Input
39-41	NC	Not Connected	
42	/PGM	Prog. Mode	Input
43	/OE	Output Enable	Input
44	NC	Not Connected	

Notes:
*Pins 8 and 9 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 33 must be grounded.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltages on all pins with respect to GND.
13.0 V Maximum on P33-P30.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

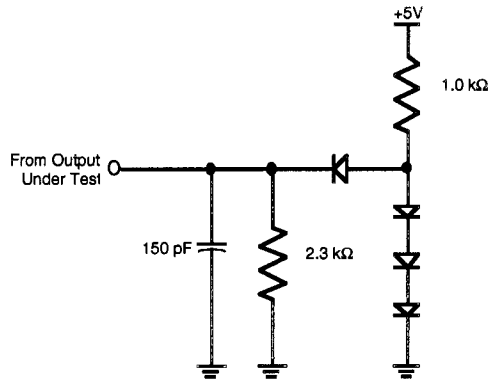


Figure 6. Test Load Diagram

DC CHARACTERISTICS

V_{CC} = 4.5V to 5.5V @ 0°C to +70°C

Sym	Parameter	Min	Max	Typ*	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	V_{CC}–0.4			V	I_{OH} = –2 mA (Ports 2 and 3 only.)
V_{OL1}	Output Low Voltage		0.4		V	I_{OL} = +4.0 mA
V_{OL2}	Output Voltage		0.8		V	I_{OL}= 10 mA (See Note 1 below.)
I_{IL}	Input Leakage	–3	3		µA	V_{IN} = 0V, 5.5V
I_{OL}	Output Leakage	–3	3		µA	V_{IN} = 0V, 5.5V
I_{AL}	Auto Latch Current	–15	15		µA	$0<V_{IN}<V_{CC}$
I_{IR}	Reset Input Current		–50		µA	V_{IN} = 0V, 5.5V
I_{CC}	V_{CC} Supply Current		30	25	mA	
I_{CC1}	Standby Current		6		mA	HALT Mode
I_{CC2}	Standby Current		20		µA	STOP Mode

Notes:

* Typical @ 25°C V_{CC}=5.0V

A combined total of six I/O pins from Ports 0, 1, 2 and 3 may be used to sink 10 mA each at 0.8V V_{OL} (max. three pins per port). These may be used for LEDs or as general-purpose outputs requiring high sink current.

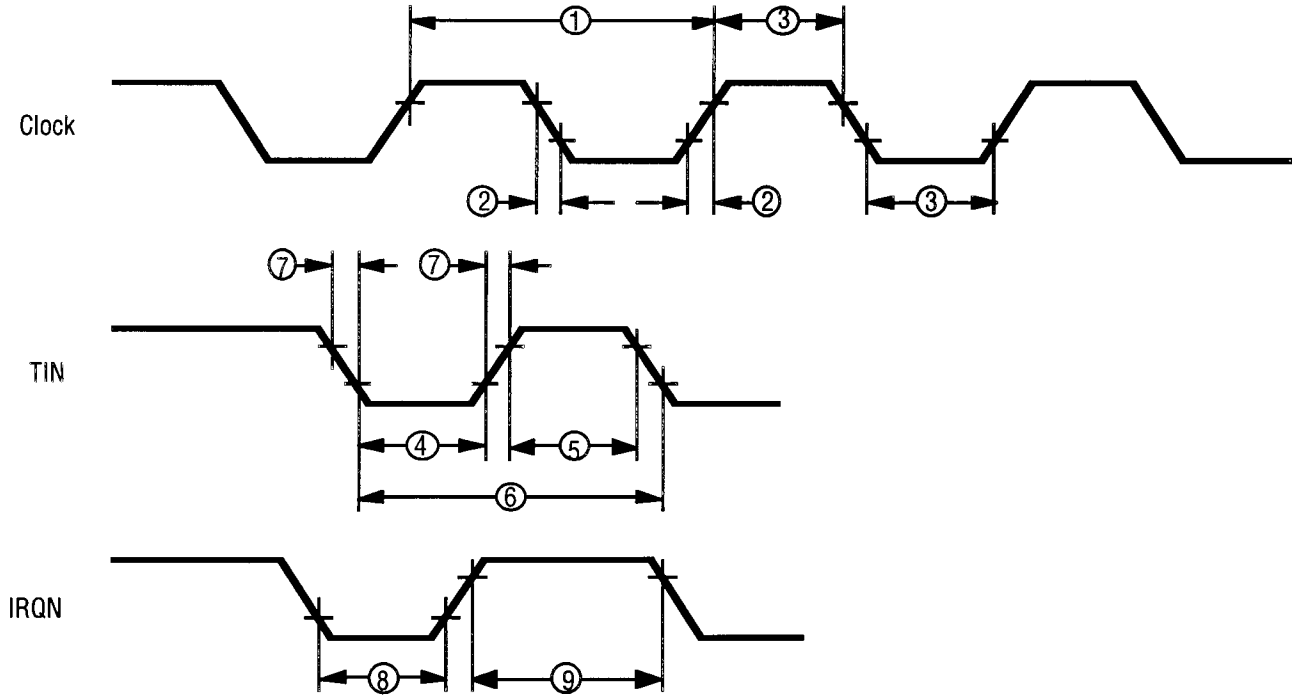


Figure 7. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

			T_A = 0°C to +70°C 4 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	250	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		25	ns	1
3	TwC	Input Clock Width	100		ns	1
4	TwTinL	Timer Input Low Width	100		ns	2
5	TwTinH	Timer Input High Width	3TpC			2
6	TpTin	Timer Input Period	8TpC			2
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		ns	2
8A	TwIL	Interrupt Request Input Low Times	100		ns	2,4
8B	TwIL	Interrupt Request Input Low Times	3TpC			2,5
9	TwIH	Interrupt Request Input High Times	3TpC			2,3

Notes:

1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request through Port 3.
4. Interrupt request through Port 3 (P33-P31).
5. Interrupt request through Port 30.

PIN FUNCTIONS

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86E23 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. When /RESET is deactivated, program execution begins at location 000CH. During power up, Reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Note: Reset pin has internal pull-up resistor to V_{CC}.

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal or an external single-phase clock to the on-chip clock oscillator and buffer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble-programmable, bidirectional, NMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. When used as an I/O port, inputs are standard NMOS and outputs are open-drain (Figure 8).

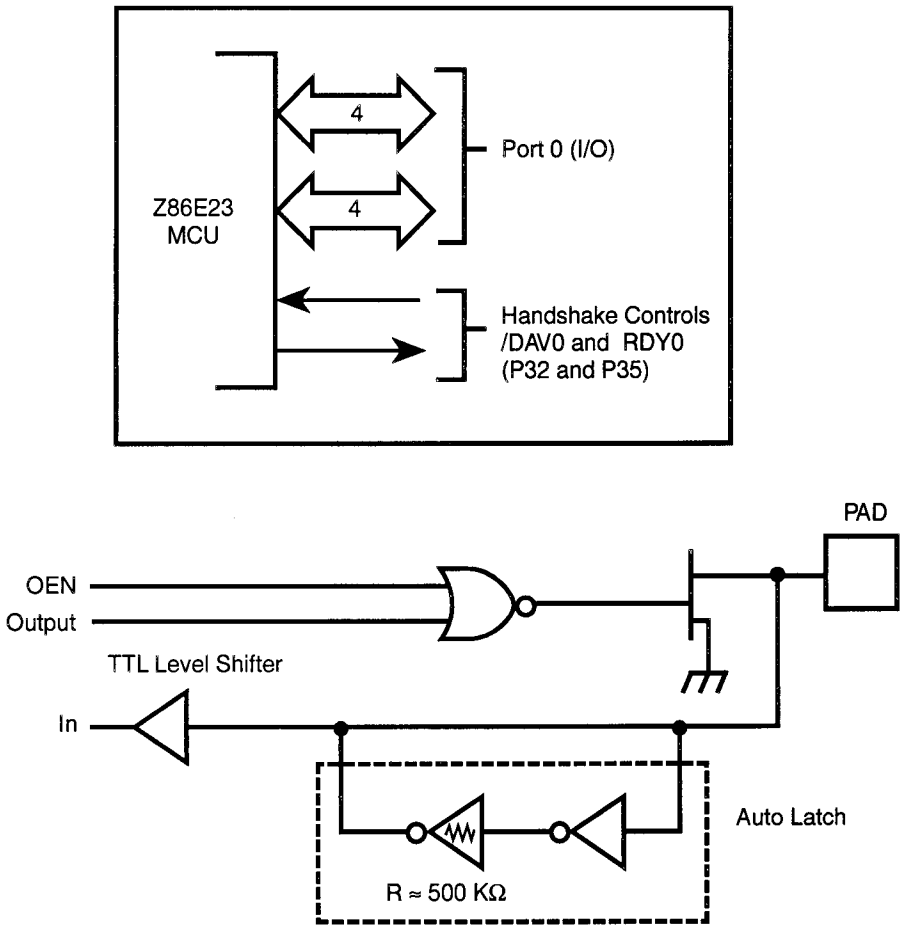


Figure 8. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte-programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under a software control program as a byte input port or as an open-drain output port. When used as an I/O port, inputs are standard TTL and outputs are open-drain (Figure 9).

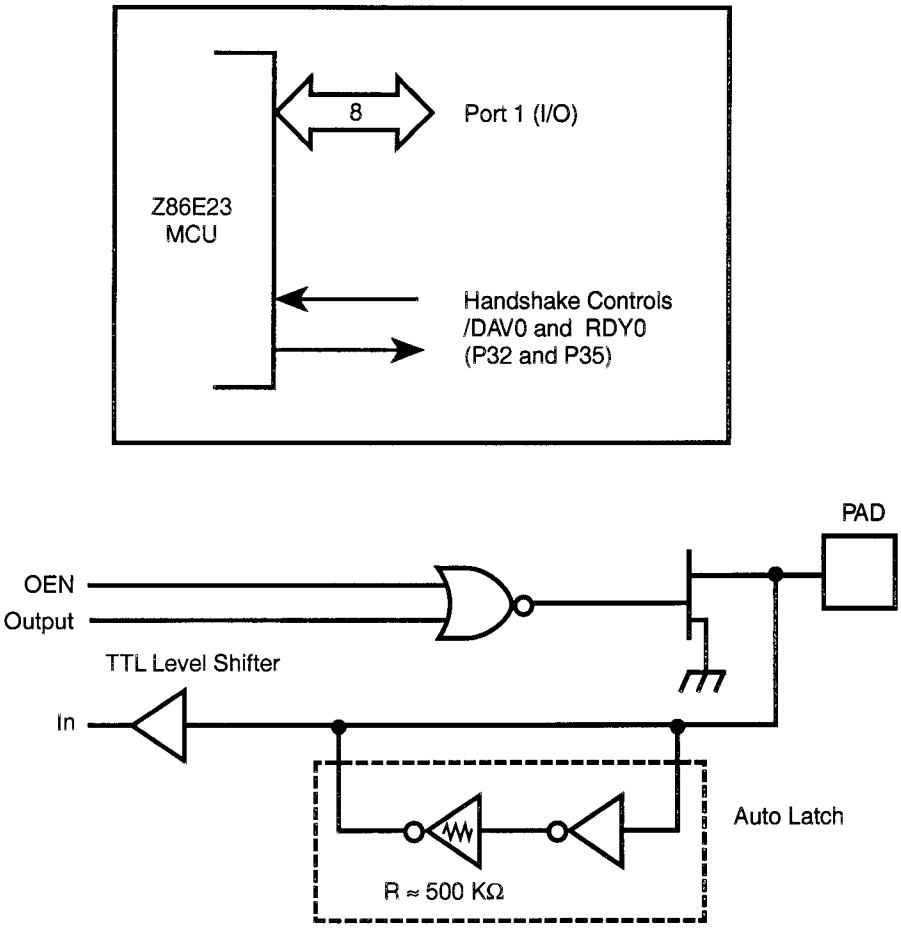


Figure 9. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit-programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation (Figure 10).

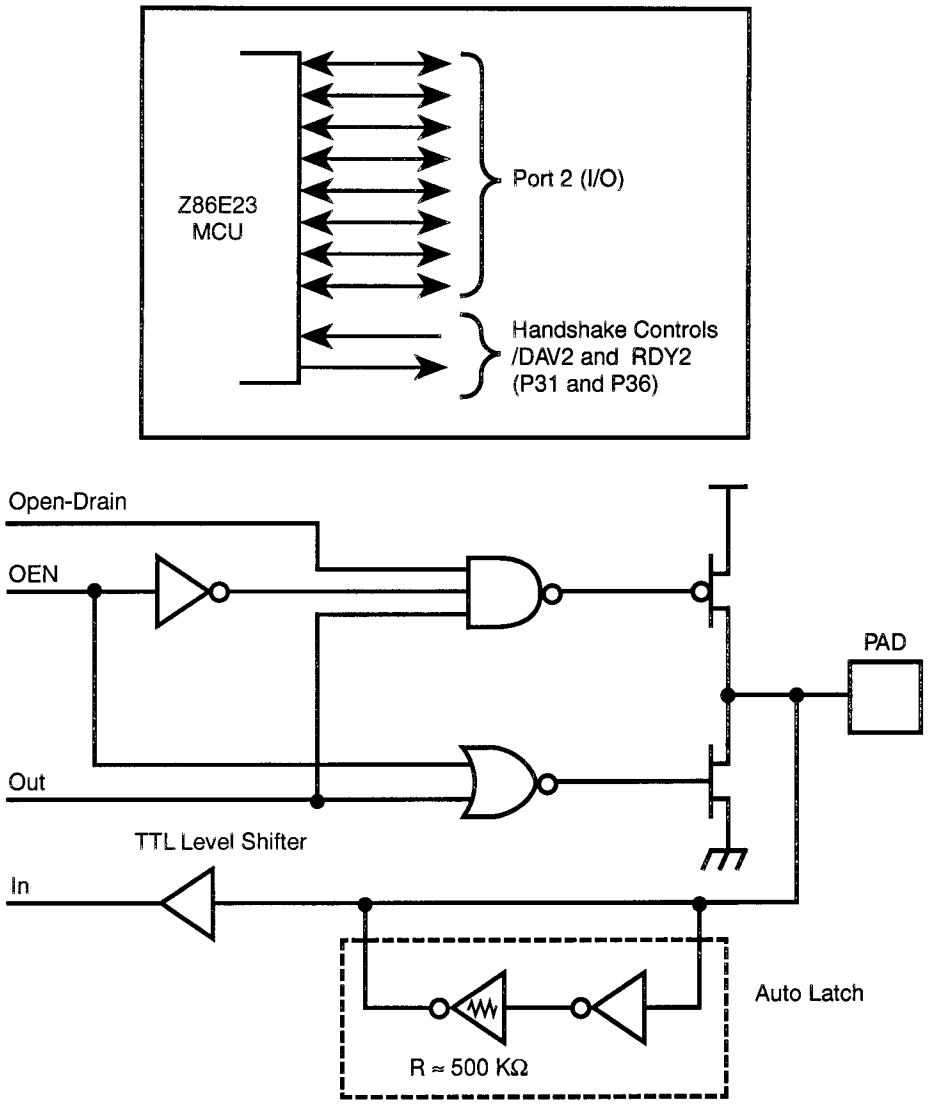


Figure 10. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3 outputs have the capability of driving LEDs directly with a pull-up resistor (output voltage of Port 3 is 0.8V @ 10 mA).

Port 3 is configured under software control to provide the following control functions: four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and EPROM control signals (P30=/CE, P31=/OE, P32=EPM and P33=GND) in Table 5.

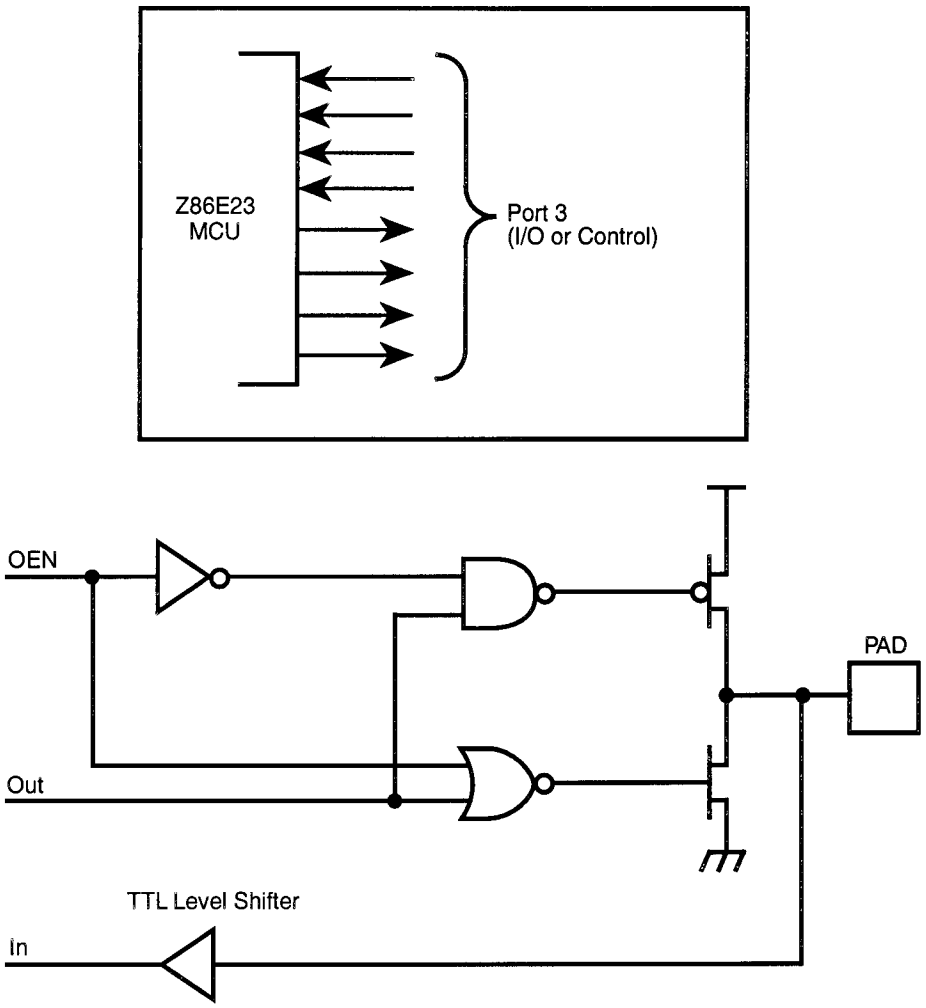


Figure 11. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin	I/O	CTC1	INT.	P0 HS	P1 HS	P2 HS	EXT	EPROM
P30	IN		IRQ3					CE
P31	IN	T_{IN}	IRQ2			D/R		OE
P32	IN		IRQ0	D/R				EPM
P33	IN		IRQ1		D/R			GND
P34	OUT				R/D			
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D	SCLK	
P37	OUT							
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source. The RESET and Port 3 inputs do not have Auto Latches.

Note: For P33-P30 inputs there is no clamping diode to V_{CC} due to the EPROM high-voltage detection circuits. Exceeding the VIH maximum specification during standard operating mode may cause the device to enter EPROM mode.

Program Memory. The 16-bit Program Counter can address 8 KB of program memory (Figure 12). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 8191 consists of on-chip EPROM. Addresses 8192 and above are reserved.

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 13 and Table 6). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E23 also allows short 4-bit register addressing using the Register Pointer (Figure 14). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4).

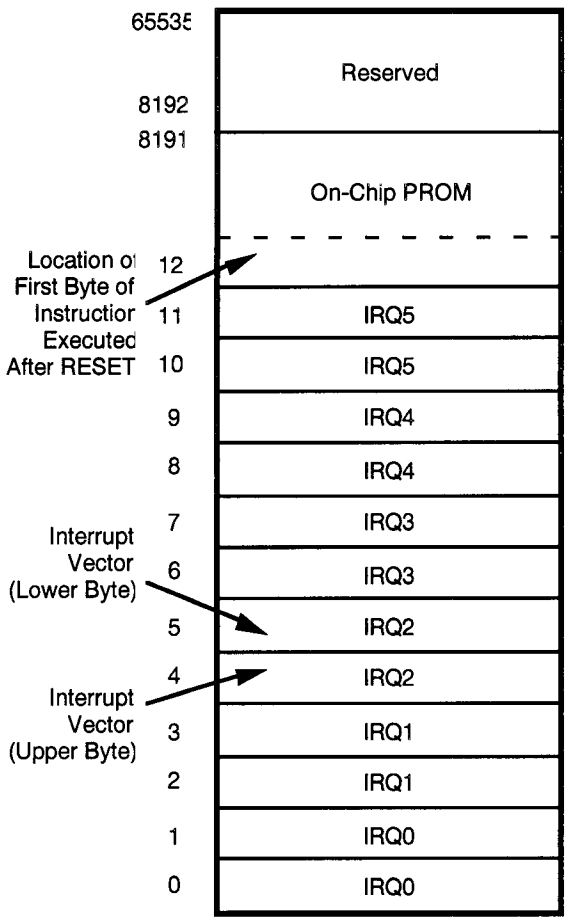


Figure 12. Program Memory Configuration

Table 6. Control Registers

		Reset Condition							
Addr.	Reg.	D7	D6	D5	D4	D3	D2	D1	D0
F1	TMR	0	0	0	0	0	0	0	0
F2	T1	U	U	U	U	U	U	U	U
F3	PRE1	U	U	U	U	U	U	0	0
F4	T0	U	U	U	U	U	U	U	U
F5	PRE0	U	U	U	U	U	U	U	0
F6	P2M	1	1	1	1	1	1	1	1
F7	P3M	0	0	0	0	0	0	0	0
F8	P01M	0	1	0	0	1	1	0	1
F9	IPR	U	U	U	U	U	U	U	U
FA	IRQ	U	U	0	0	0	0	0	0
FB	IMR	0	0	U	U	U	U	U	U
FC	FLAGS	U	U	U	U	U	U	U	U
FD	RP	0	0	0	0	0	0	0	0
FF	SPL	U	U	U	U	U	U	U	U
00	P0	U	U	U	U	U	U	U	U
01	P1	U	U	U	U	U	U	U	U
02	P2	U	U	U	U	U	U	U	U
03	P3	1	1	1	1	X	X	X	X

ADDRESS SPACE

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	General-Purpose Register	GPR
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Reserved	
R239	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 13. Register File

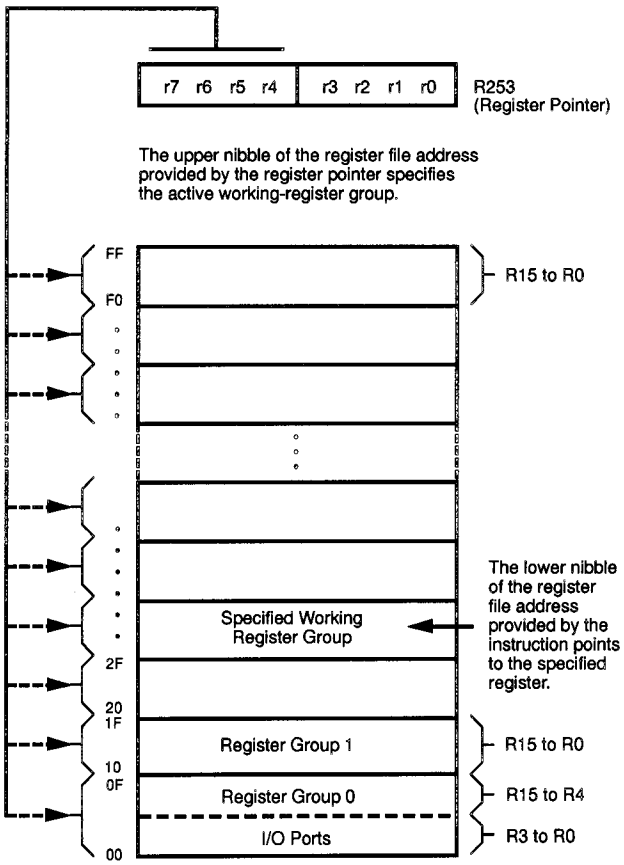


Figure 14. Register Pointer

FUNCTIONAL DESCRIPTION

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 also serves as a timer output (TOUT) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

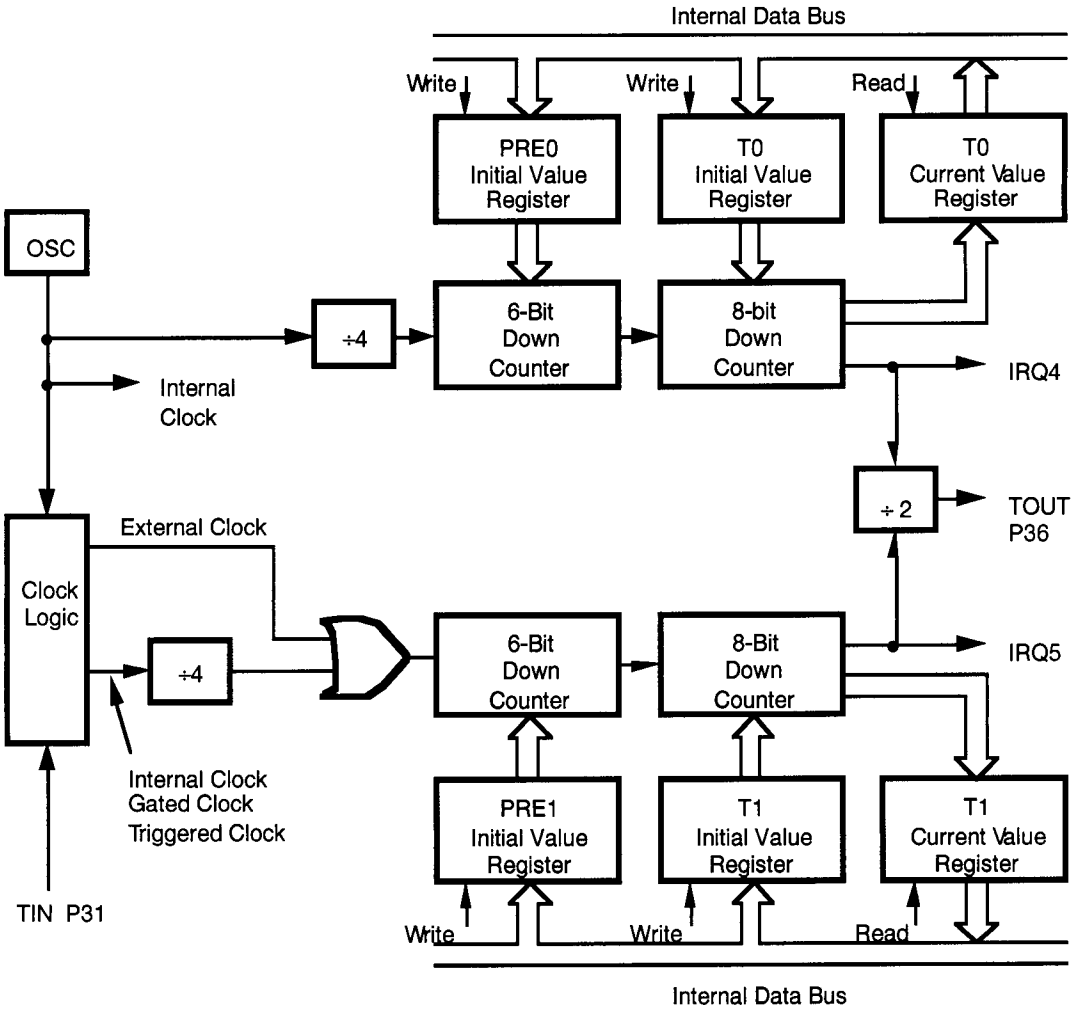


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z86E23 has six different interrupts from six different sources. The interrupts are maskable and prioritized. The six sources are divided as follows; four sources are claimed by Port 3 lines P33-P30, and two by the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z86E23 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 2.5 TpC before the falling edge of the last clock cycle of the currently executing instruction.

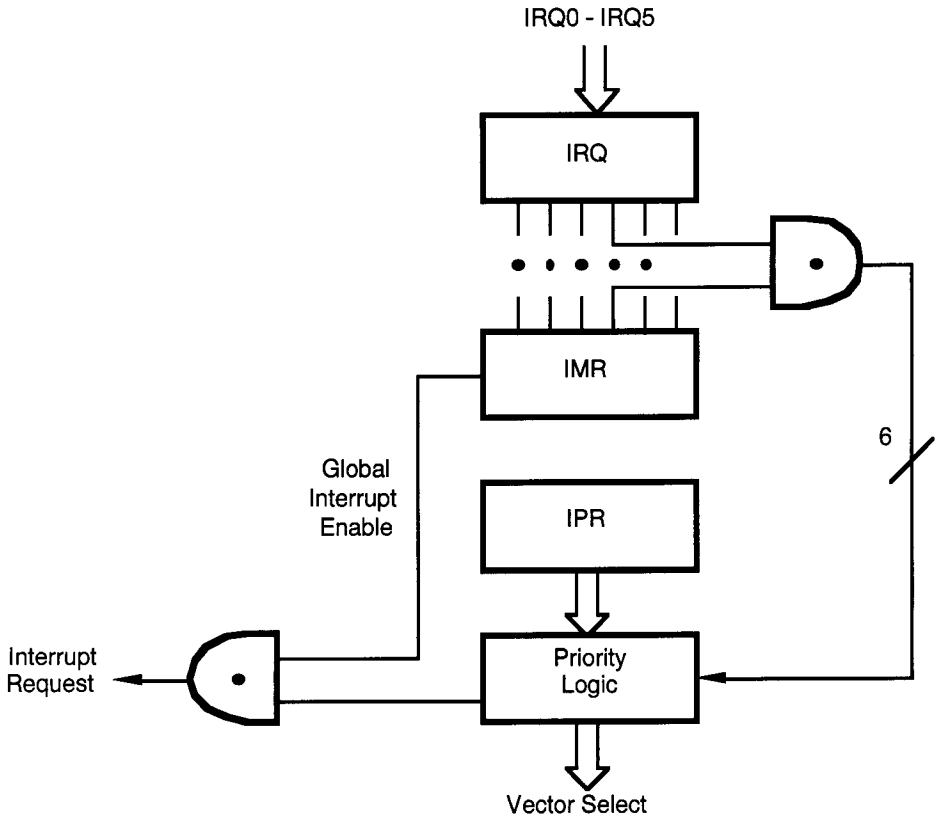


Figure 16. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E23 on-chip oscillator has a parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The crystal should be AT cut, 4 MHz max; series resistance (RS) is less than or equal to 100 ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 150 pF) from each pin to ground (Figure 17).

Note: Actual capacitor value specified by crystal manufacturer.

EMI. The Z86E23 offers low EMI emission. The internal divide-by-two circuit has been removed, and the on-chip oscillator has been modified to reduce EMI emission.

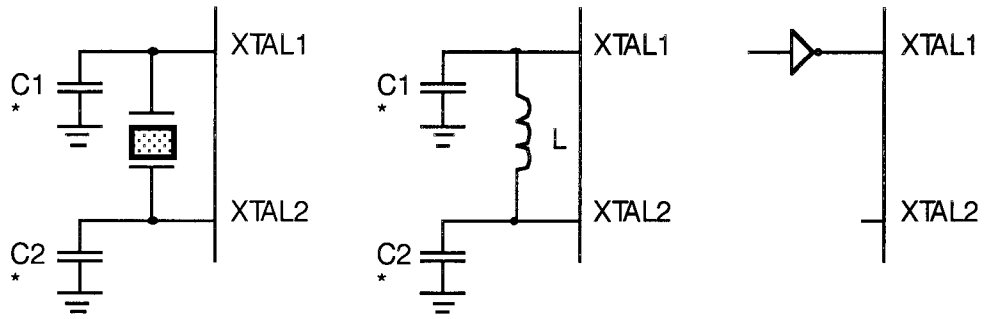


Figure 17. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 5 µA (Typical) or less. The STOP Mode is terminated by a reset, which cause the processor to restart the application program at address 000CH.

Note: In STOP mode, there is a pull-up resistor enabled on XTAL1.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, that is:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

In STOP or HALT Mode, the value of each output line prior to the HALT or STOP instruction is retained during execution.

PROGRAMMING

Z86E23 User Modes

The Z86E23 uses separate AC timing cycles for the different User Modes available. Table 7 shows the Z86E23 User Modes. Table 8 shows the timing of the programming waveforms. Port 1 Data Bus requires pull-up resistors for program/verify.

User MODE 1 EPROM Read

The Z86E23 EPROM read cycle is provided so that the user may read the Z86E23 as a standard 2764A EPROM. This is accomplished by driving the /EPM pin (P32) to VH and activating /CE and /OE. /PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 18.

User MODE 2 EPROM Program

The Z86E23 Program function conforms to the Intelligent programming algorithm. The device is programmed with VCC at 6.0V and VPP = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E23 programming cycle is shown in Figure 19.

User MODE 3 EPROM Verify

The Program Verify cycle is used as part of the Intelligent programming algorithm to ensure data integrity under worst-case conditions. It differs from the EPROM read cycle in that VPP is active and VCC must be driven to 6.0V. Timing is shown in Figure 19.

User MODES 4 and 5 EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E23. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit-6 of the IMR (R251). Timing is shown in Figure 20.

Table 7. EEPROM Rogram Modes

Mode	VPP	EPM	/CE	/OE	/PGM	VCC*	ADDR	Data
EPROM Read1	X	V_H	VIL	V_{IL}	V_{IH}	4.5	ADDR	OUT
EPROM Read2	X	V_H	VIL	V_{IL}	V_{IH}	5.5	ADDR	OUT
Program	V_H	X	VIL	V_{IH}	V_{IL}	6.0	ADDR	IN
Program Verify	V_H	X	VIL	V_{IL}	V_{IH}	6.0	ADDR	OUT
EPROM Protect Select	V_H	V_H	VH	V_{IH}	V_{IL}	6.0	NU	NU
RAM Protect	V_H	V_{IH}	VH	V_H	V_{IL}	6.0	NU	NU

Notes:

* Tolerance is ±0.25V

V_H = 12.5 ±0.5V

V_{IH} = As per DC specification.

V_{IL} = As per DC specification.

X = Not used, but must be set to either VH, VIH or VIL level.

NU = Not used, but must be set to either VIH or VIL.

I_{PP} during programming = 40 mA maximum.

I_{CC} during either programming, verify, or read = 40 mA maximum.

PROGRAMMING (Continued)

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

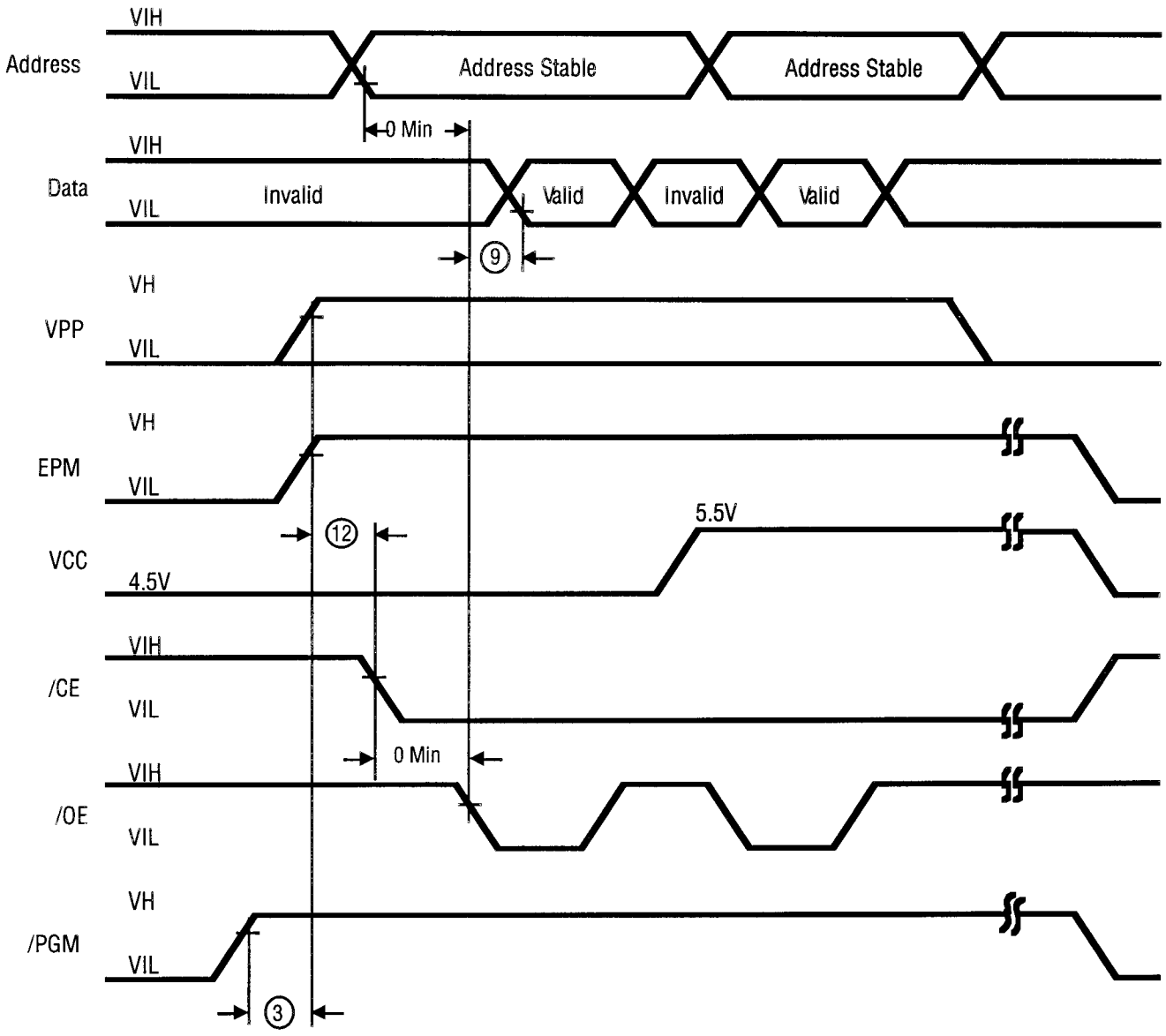


Figure 18. EPROM Read

PROGRAMMING (Continued)

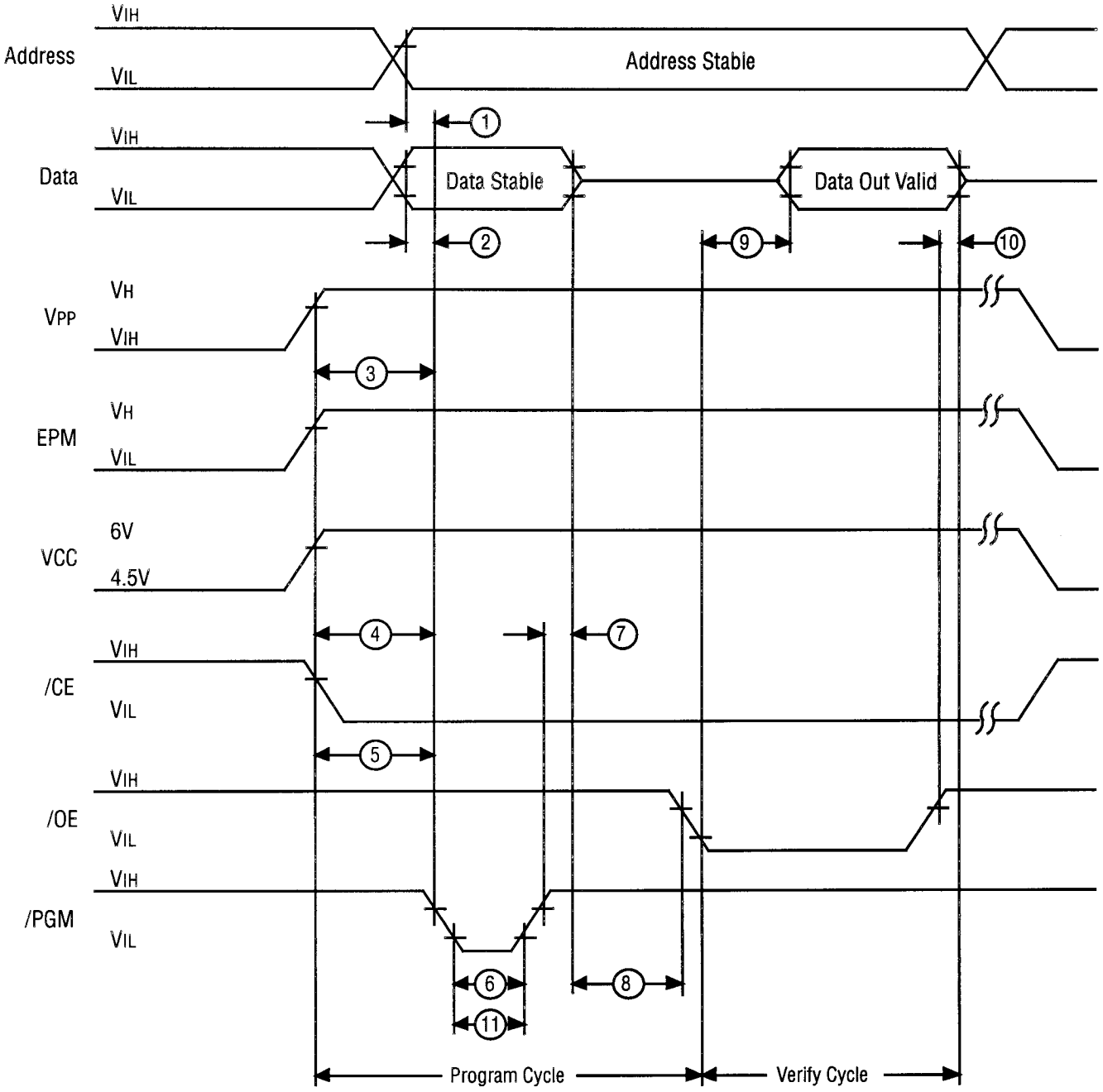


Figure 19. EPROM Program and Verify

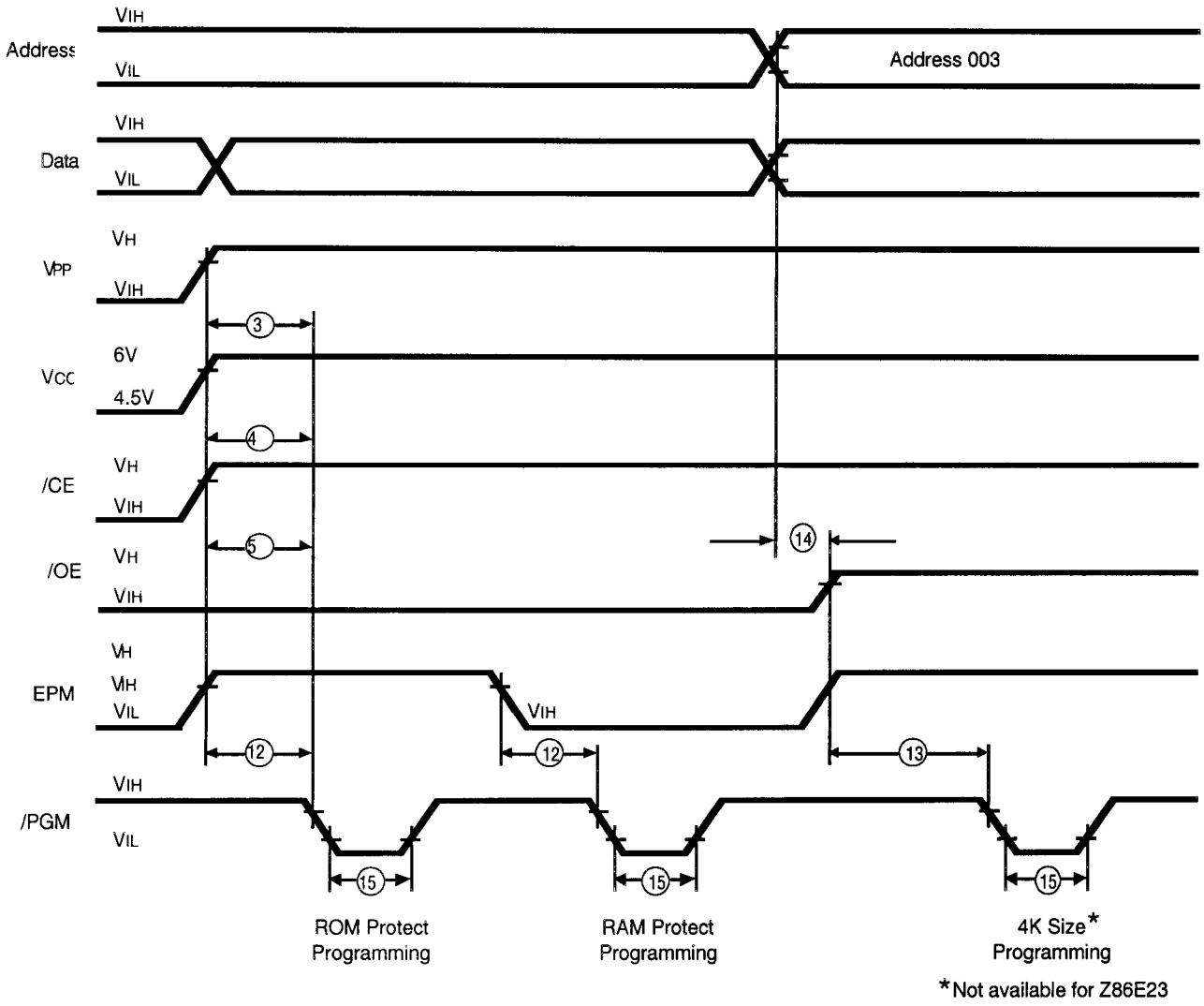


Figure 20. EPROM and RAM Protect and 4K Size Selection

PROGRAMMING (Continued)

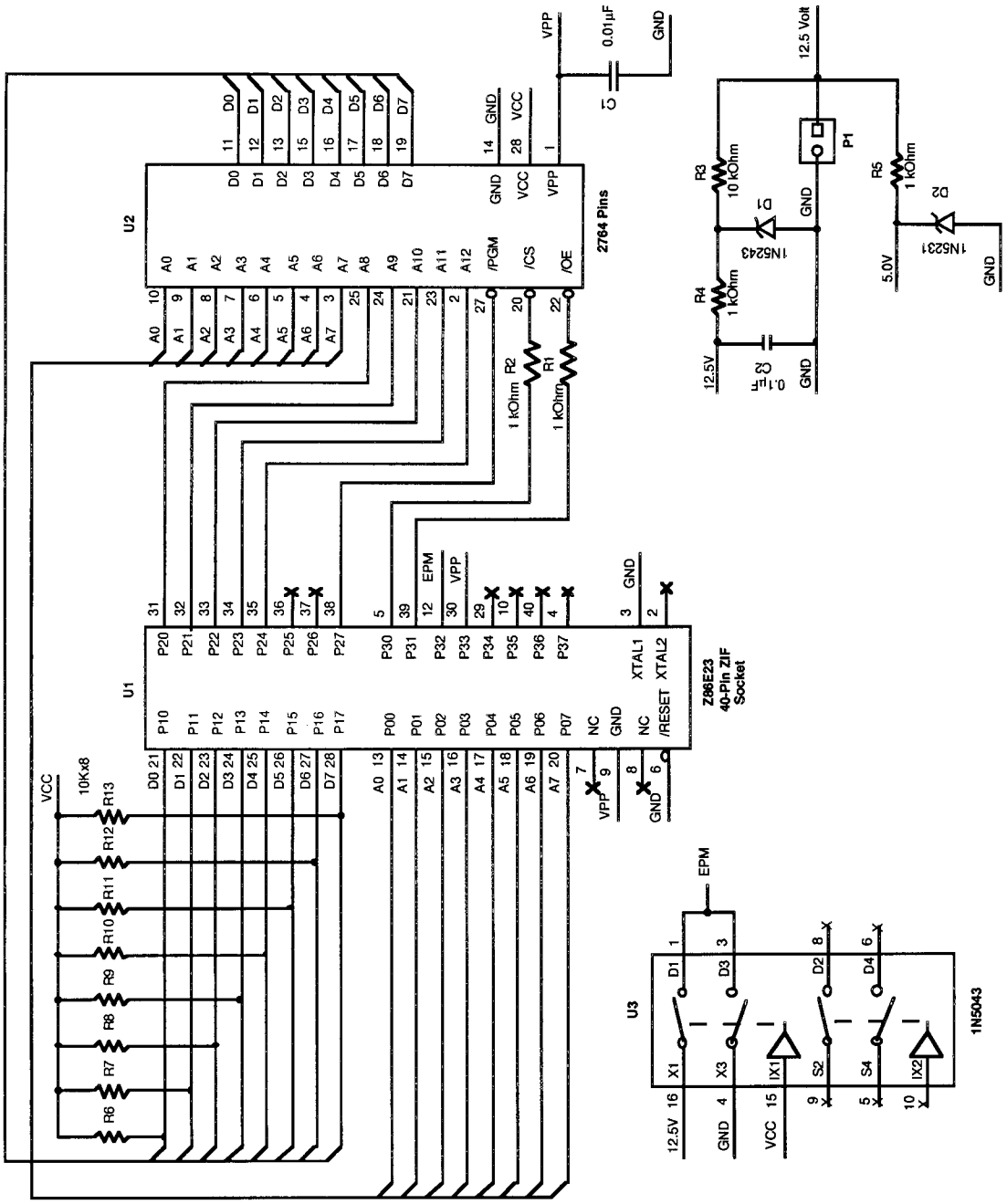


Figure 21. Z86E23 Z8 OTP Programming Adapter

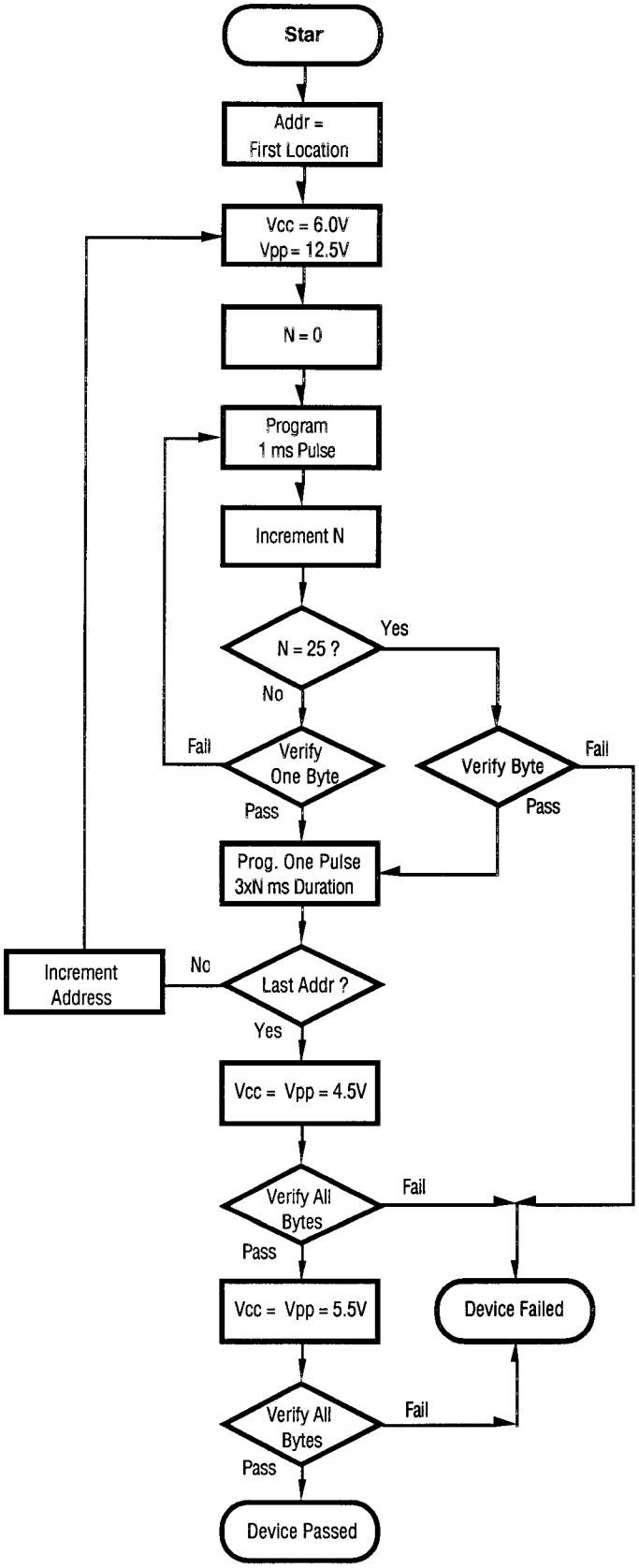


Figure 22. Intelligent Programming Flowchart

Z8 CONTROL REGISTER DIAGRAMS

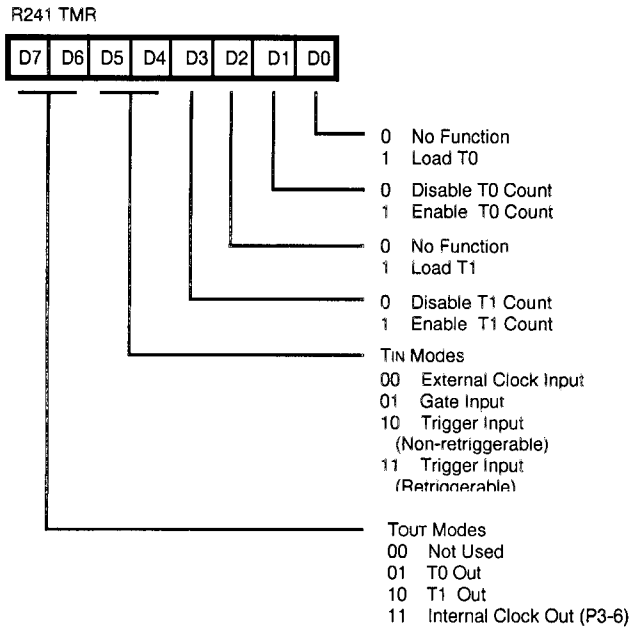


Figure 23. Timer Mode Register (F1H: Read/Write)

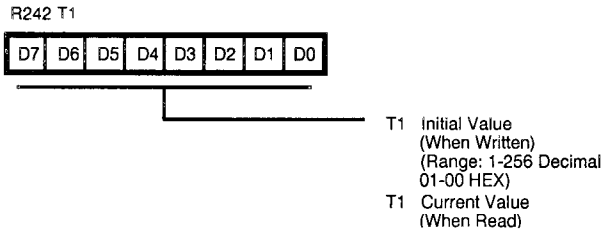


Figure 24. Counter/Timer 1 Register (F2H: Read/Write)

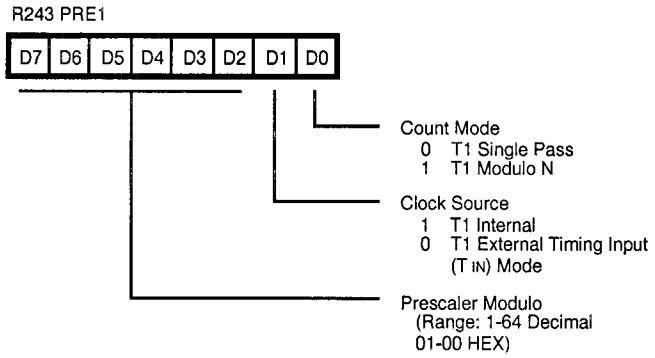


Figure 25. Prescaler 1 Register (F3H: Write Only)

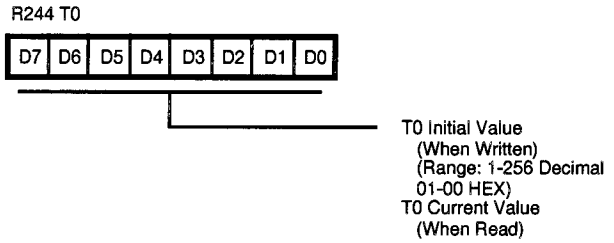


Figure 26. Counter/Timer 0 Register (F4H: Read/Write)

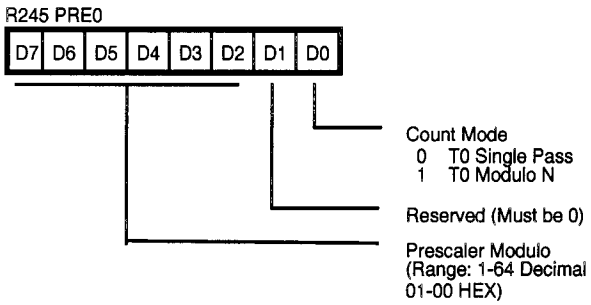


Figure 27. Prescaler 0 Register (F5H: Write Only)

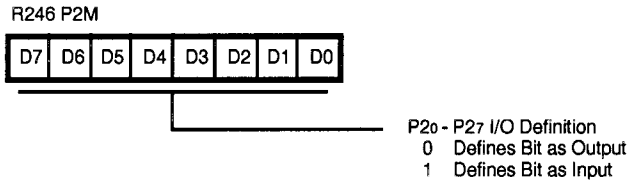


Figure 28. Port 2 Mode Register (F6H: Write Only)

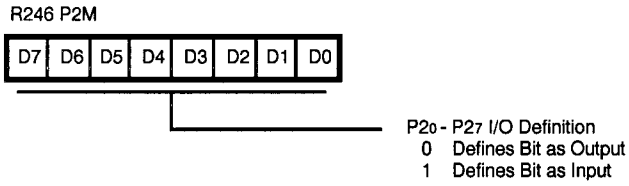


Figure 29. Port 3 Mode Register (F7H: Write Only)

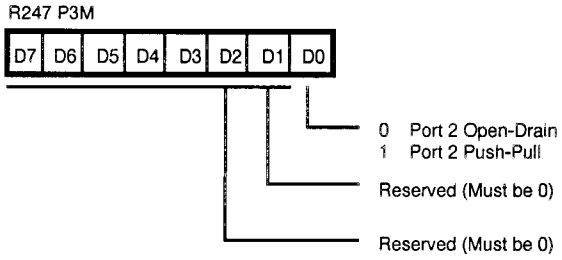


Figure 30. Port 0 and 1 Mode Register (F8H: Write Only)

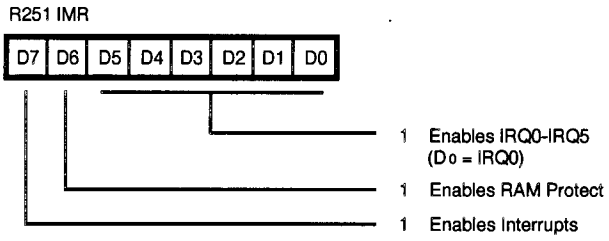


Figure 33. Interrupt Mask Register (FBH: Read/Write)

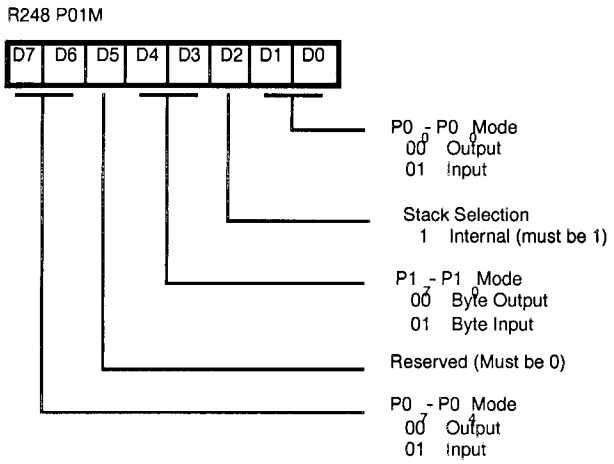


Figure 31. Interrupt Priority Register (F9H: Write Only)

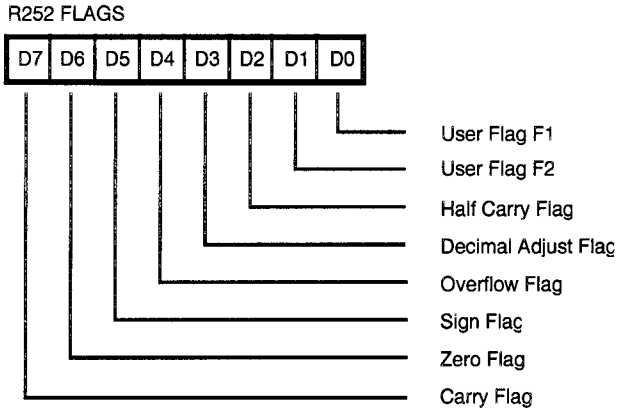


Figure 34. Flag Register (FCH: Read/Write)

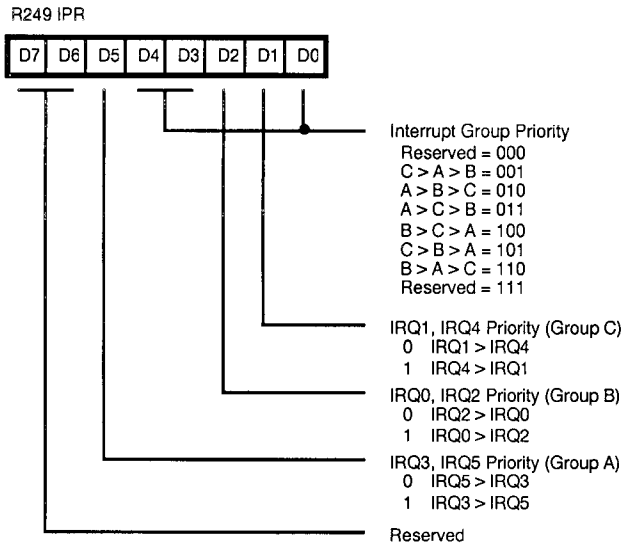


Figure 32. Interrupt Request Register (FAH: Read/Write)

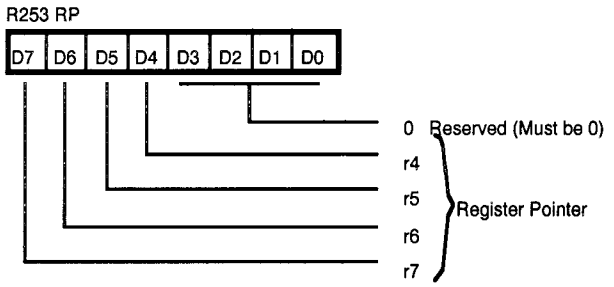


Figure 35. Register Pointer Register (FDH: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

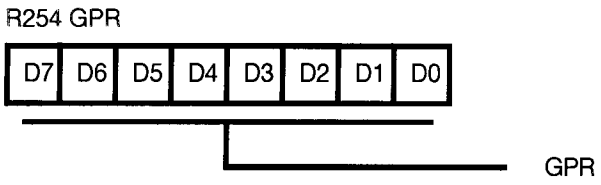


Figure 36. General Purpose Register (FEH: Read/Write)

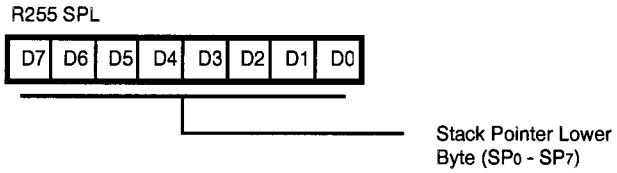
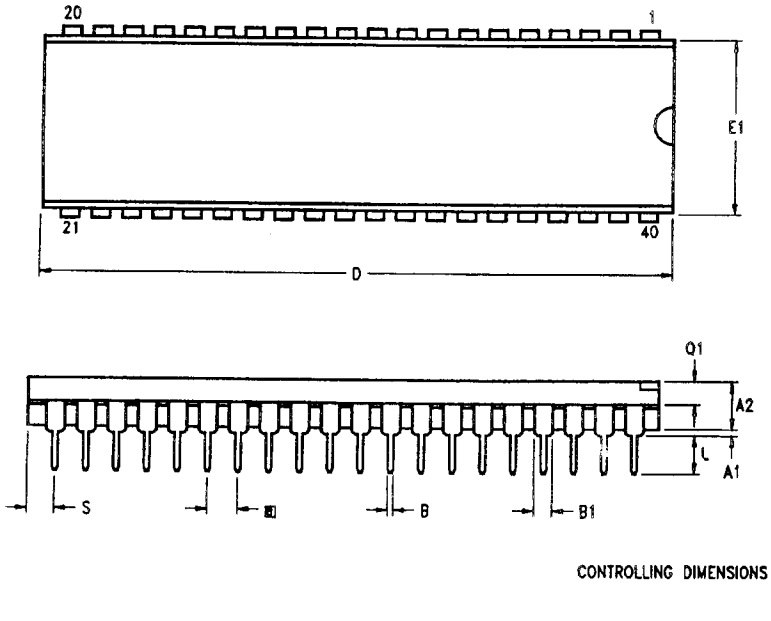


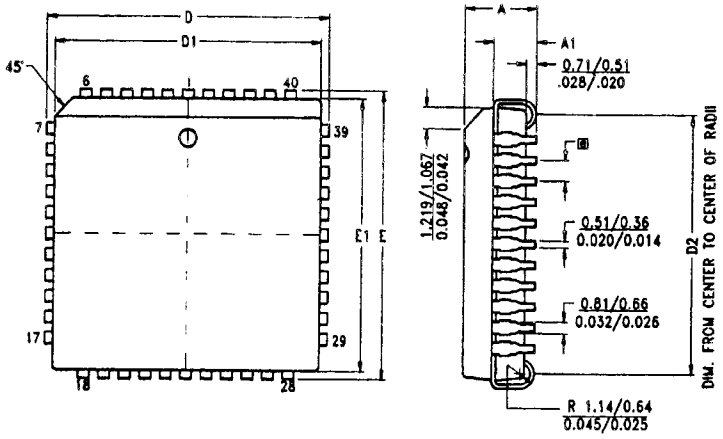
Figure 37. Stack Pointer Register (FFH: Read/Write)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 38. 40-Lead DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 39. 44-Lead PLCC Package Diagram

ORDERING INFORMATION

Z86E23

4 MHz

40-Pin DIP	44-Pin PLCC
Z86E2304PSC	Z86E2304VSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Temperature
S = 0°C to +70°C

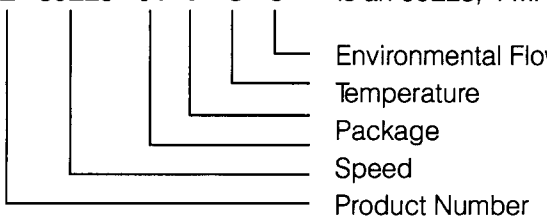
Speed
4 = 4 MHz

Environmental
C = Plastic Standard

Example:

Example:

Z 86E23 04 P S C is an 86E23, 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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