THE DATASHEET OF

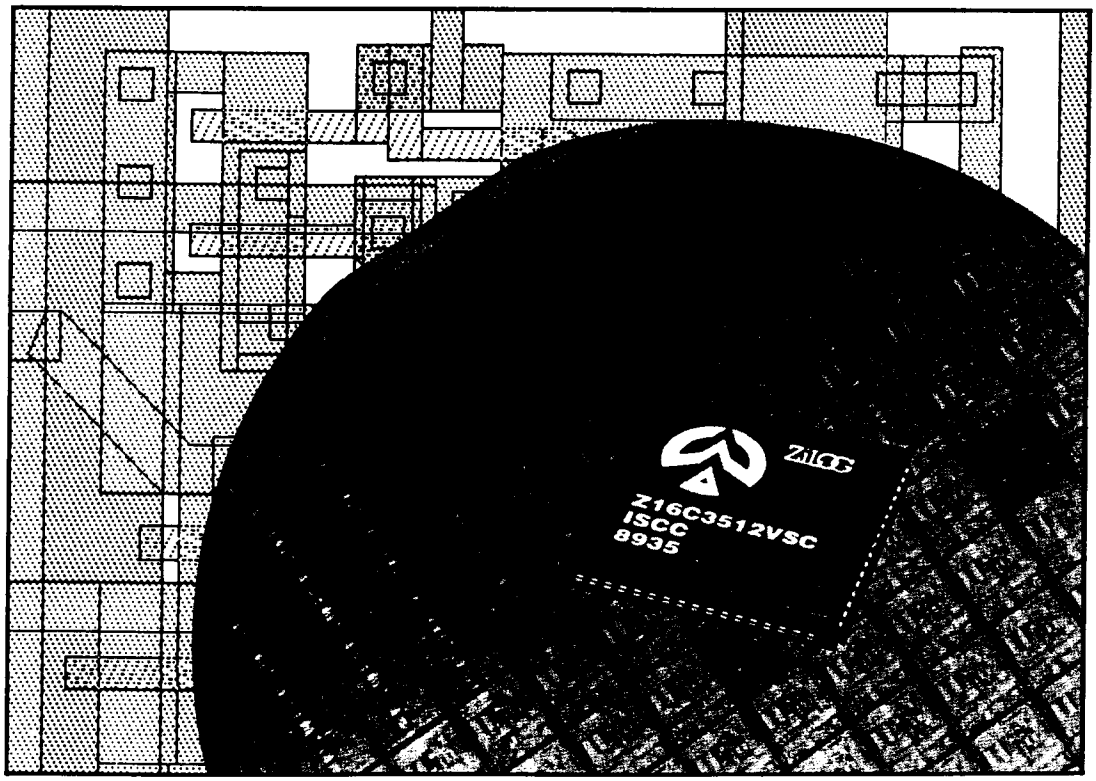
Z16C3516VSC00TR

ZiLOG

PRODUCT SPECIFICATION

Z16C35

CMOS ISCC INTEGRATED SERIAL COMMUNICATIONS CONTROLLER



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PRODUCT SPECIFICATION

Z16C35

CMOS ISCC INTEGRATED SERIAL COMMUNICATIONS CONTROLLER

FEATURES

- Low power CMOS technology
- Two general-purpose SCC channels, four DMA channels; and Universal Bus Interface Unit
- Software compatible to the Zilog CMOS SCC
- 4 DMA channels; two transmit and two receive channels to and from the SCC
- 4 gigabyte address range per DMA channel
- Flyby DMA transfer mode
- Programmable DMA channel priorities
- Independent DMA register set
- A Universal Bus Interface Unit providing simple interface to most CPUs multiplexed or non-multiplexed bus; compatible with 680x0 and 8x86 CPUs
- 32-bit addresses multiplexed to 16-pin address/data lines
- 8-bit data supporting high/low byte swapping
- 10 MHz timing
- 16 MHz timing planned
- 68-pin PLCC

Supports all Zilog CMOS SCC features:

- Two independent, 0 to 4.0 M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and digital phase-locked loop circuit for clock recovery.
- Multi-protocol operation under program control; programmable for NRZ, NRZI, or FM data encoding.
- Asynchronous mode with five to eight bits and one, one and one-half, or two stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.
- Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1's or 0's.
- SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and deletion, I-field residue handling, abort generation and detection, CRC generation and checking, and SDLC Loop mode operation.
- Local Loopback and Auto Echo modes
- Supports T1 digital trunk
- Enhanced SDLC 10x19 Status FIFO for DMA support
- Full CMOS SCC register set

GENERAL DESCRIPTION

The Z16C35 ISCC™ is a CMOS superintegrated device with a flexible Bus Interface Unit (BIU) connecting a built-in Direct Memory Access (DMA) cell to the CMOS Serial Communications Control (SCC) cell.

The ISCC is a dual-channel, multi-protocol data communications peripheral which easily interfaces to CPU's with either multiplexed or non-multiplexed address and data buses. The advanced CMOS process offers lower power

consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allow the ISCC to be configured for a wide variety of serial communications applications. The many on-chip features such as, streamlined bus interface, four channel DMA, baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features, including a 10x19 bit status FIFO, are added to support high speed SDLC transfers using on-chip DMA controllers.

The ISCC can address up to 4 gigabytes per DMA channel by using the /UAS and /AS signals to strobe out 32-bit multiplexed addresses.

The ISCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (terminals, printers, diskette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ISCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The standard Zilog interrupt daisy chain is supported for interrupt hierachy control. Internally, the SCC cell has higher interrupt priority than the DMA cell.

The DMA cell consists of four DMA channels; one for transmit and one for receive to and from each SCC channel, respectively. The cycle time for each DMA transfer is 400 ns for the 10 MHz version. There is no idle cycle between DMA transfers.

The DMA cell adopts a simple fly-by mode DMA transfer, allowing easy programming of the DMA cell and yet providing a powerful and efficient DMA access. The cell does not support memory-to-memory transfer.

Priorities between the four DMA channels are programmable to custom-fit user applications. Arbitration of Bus priority control signals between the ISCC DMA and other system DMA's should be handled outside the ISCC.

The BIU has a universal interface to most system/CPU bus structures and timing. The first write to the ISCC after a hardware reset will confirm the bus interface type being implemented.

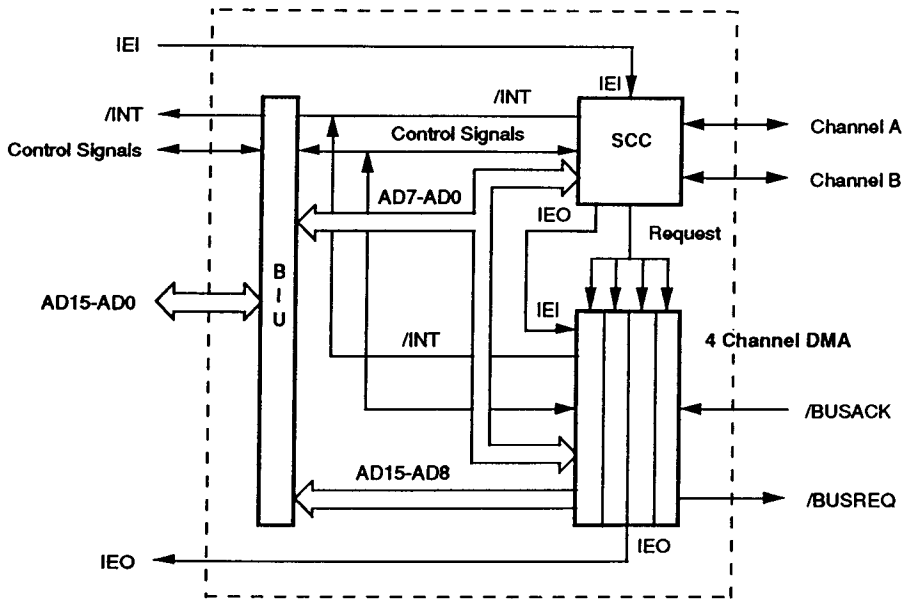


Figure 1. Block Diagram

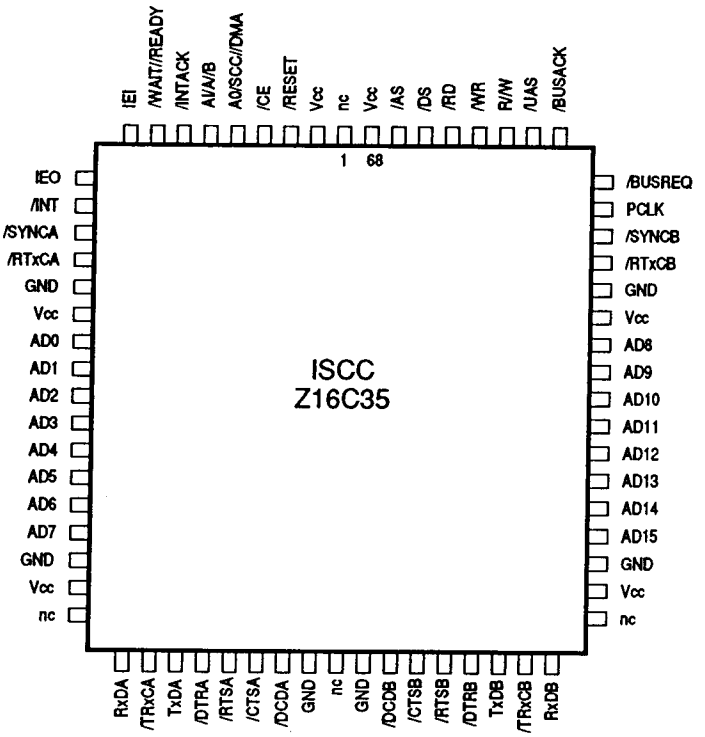


Figure 2. Pin Assignments

PIN DESCRIPTION

The following section describes the Z16C35 pin functions. Figures 1 and 2 detail the respective pin functions and pin assignments. All references to DMA are internal.

/CTSA, /CTSB. *Clear To Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC cell detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

/DCDA, /DCDB. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise they are used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC cell detects pulses on these pins and can interrupt the CPU on both logic level transitions.

/DTRA, /DTRB. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into the DTR bit.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt. The SCC cell has a higher interrupt priority than the DMA cell.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing the ISCC (SCC or DMA) interrupt, or the ISCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

PIN DESCRIPTION (Continued)

/INT. *Interrupt* (output, active Low). This signal is activated when the SCC or DMA requests an interrupt. Note that /INT is pulled high and is not an open-drain output.

/INTACK. *Interrupt Acknowledge* (input, active Low). This is a strobe which indicates that an interrupt acknowledge cycle is in progress. During this cycle, the SCC and DMA interrupt daisy chain is resolved. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle when RD or DS become high. INTACK may be programmed to accept a status acknowledge, a single pulse acknowledge, or a double pulse acknowledge. This is programmed in the Bus Configuration Register (BCR). The double pulse acknowledge is compatible with 8x86 family microprocessors.

PCLK. *Clock* (input). This is the master SCC and DMA clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

RxDA, RxDB. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

/RTxCA, /RTxCB. *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed to several modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

/RTSA, /RTSB. *Request To Send* (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 is set, the RTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

/SYNCA, /SYNCB. *Synchronization* (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, SYNC must be driven Low to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of SYNC.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous condition is not latched. These outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, the pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB. *Transmit Data* (outputs, active high). These output signals transmit serial data at standard TTL levels.

/TRxCA, /TRxCB. *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/CE. *Chip Enable* (input, active Low). This signal selects the ISCC for a peripheral read or write operation. This signal is not used when the ISCC is bus master.

AD15-AD0. *Data bus* (bidirectional, 3-state). These lines carry data and commands to and from the ISCC.

/RD. *Read* (bidirectional, active Low). When the ISCC is a peripheral (i.e. bus slave), this signal indicates a read operation and when the ISCC is selected, enables the ISCC's bus drivers. As an input, /RD indicates that the CPU wants to read from the ISCC read registers. During the Interrupt Acknowledge cycle, /RD gates the interrupt vector onto the bus if the ISCC is the highest priority device requesting an interrupt. When the ISCC is the bus master, this signal is used to read data. As an output, after the ISCC has taken control of the system buses, /RD indicates a DMA-controlled read from a memory or I/O port address.

/WR. *Write* (bidirectional, active Low). When the ISCC is selected, this signal indicates a write operation. As an input, this indicates that the CPU wants to write control or command bytes to the ISCC write registers. As an output, after the ISCC has taken control of the system buses /WR indicates a DMA-controlled write to a memory or I/O port address.

/DS. *Data Strobe* (bidirectional, active Low). A Low on this signal indicates that the AD15-AD0 bus is used for data transfer. When the ISCC is not in control of the system bus and the external system is transferring information to or from the ISCC, /DS is a timing input used by the ISCC to move data to or from the AD0-AD15 bus. Data is written into the ISCC by the external system on the Low to High /DS transition. Data is read from the ISCC by the external system while /DS is Low. There are no timing requirements between /DS as an input and ISCC clock; this allows use of the ISCC with a system bus which does not have a bussed clock.

During a DMA operation when the ISCC is in control of the system, DS is an output generated by the ISCC and used by the system to move data to or from the AD0-AD15 bus. When the ISCC has bus control, it writes to the external system by placing data on the AD15-AD0 bus before the High-to-Low DS transition and holds the data stable until after the Low-to-High DS transition; while reading from the external system, the Low-to-High transition of DS inputs data from the AD15-AD0 bus into the ISCC.

R/W. *Read/Write* (bidirectional). Read polarity is High and write polarity is Low. When the ISCC is bus master, R/W indicates the data direction of the current bus transaction, and is stable from when AS is High until the bus transaction ends. When the ISCC is not in control of the system bus and the external system is transferring information to or from the ISCC, R/W is a status input used by the ISCC to determine if data is entering or leaving on the AD0-AD15 bus during /DS time. In such a case, Read (High) indicates that the system is requesting data from the ISCC and Write (Low) indicates that the system is presenting data to the ISCC. The only timing requirements for R/W as an input are defined relative to DS. When the ISCC is in control of the system bus, R/W is an output generated by the ISCC, with Read indicating that data is being requested from the addressed location or device, and Write indicating that data is being presented to the addressed location or device.

/UAS. *Upper Address Strobe* (Output, active Low). This signal is used if the address is more than 16-bit. The upper address, A31-A16, can be latched externally by the rising edge of this signal. /UAS is active first before AS becomes active. This signal and AS are used by the DMA cell.

/AS. *Lower Address Strobe* (Bidirectional, active Low). When the ISCC is bus master, this signal when an output, is used as a lower address strobe for AD15-AD0. It is used in conjunction with UAS since the address is 32-bits. This signal and /UAS are used by the DMA cell when it is bus master. When ISCC is not bus master, this signal is used in the multiplexed bus modes to latch the address on the AD lines. The /AS signal is not used in the non-multiplexed bus modes and should be tied to Vcc in these cases.

/WAIT//RDY. *Wait/Ready* (bidirectional, active Low). It may be programmed to function either as a Wait signal or Ready signal during the BCR write. When the BCR is written to Channel A (A1/A//B High during the BCR write), this signal functions as a WAIT and thus supports the READY function of 8X86 microprocessors family. When the BCR writes to Channel B (A1/A//B Low), this signal functions as a READY and supports the DTACK function of the 680X0 microprocessor family.

This signal is an output when the ISCC in not bus master. In this case, the Wait/RDY signal indicates when the data is available during a read cycle; when the device is ready to receive data during a write cycle; and when a valid vector is available during an interrupt acknowledge cycle.

When the ISCC is the bus master (the DMA cell has taken control of the bus), the /Wait//RDY signal functions as a WAIT or READY input. Slow memories and peripheral devices can assert WAIT to extend /DS during bus transfers. Similarly, memories and peripherals use READY to indicate that its output is valid or that it is ready to latch input data.

/BUSACK. *Bus Acknowledge* (input, active Low). Signals the bus has been released to the DMA. If the /BUSACK is inactive before the DMA transfer is completed, the current DMA transfer is aborted.

/BUSREQ. *Bus Request* (output, active Low). This signal is used by the DMA to obtain the bus from the CPU.

A0/SCC//DMA. *DMA Channel/SCC Select/DMA Select* (bidirectional). When this pin is used as input, a high selects the SCC cell and a low selects the DMA cell. When this pin is used as output, the signal on this pin is used in conjunction with A1/A//B pin output to identify which DMA channel is active. This information can be used by the user to determine whether to issue a DMA abort command. A0/SCC//DMA and A1/A//B output encoding is shown below:

A1/A//B	A0/SCC//DMA	DMA channel
1	1	RxA
1	0	TxA
0	1	RxB
0	0	TxB

PIN DESCRIPTION (Continued)

A1/A/B. *DMA Channel/Channel A/Channel B* (bidirectional). This signal, when used as input, selects the SCC channel in which the read and write operation occurs. Note that A0/SCC//DMA pin must be held high to select this feature. When this pin is used as an output, it is used in conjunction with the A0/SCC//DMA pin output to identify which DMA channel is active. During a DMA peripheral access, the A1/A/B pin is ignored.

/RESET. (input, active Low). This signal resets the device to a known state. The first write to the ISCC after a reset accesses the BCR to select additional bus options for the device.

FUNCTIONAL DESCRIPTION

The functional capabilities of the ISCC are described in three blocks: the SCC cell, the DMA cell, and the Bus Interface Unit (BIU). Each of the blocks are described independently in the following sections with the ISCC architecture shown in Figure 3. Please refer to the ISCC Technical Manual for a detailed description of the functions outlined here.

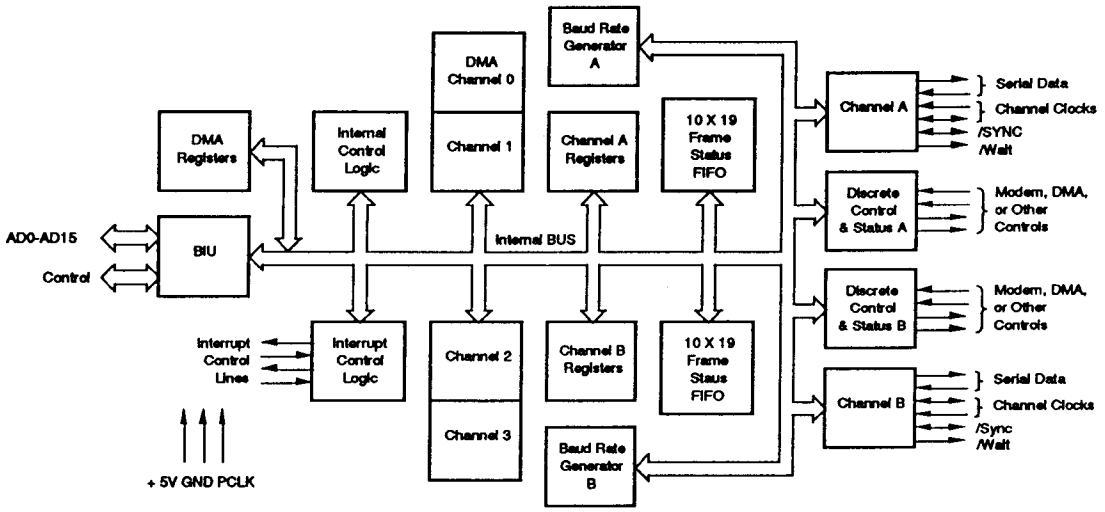


Figure 3. Block Diagram of ISCC Architecture

SCC Cell Data Communications Capabilities. The ISCC provides two independent full-duplex programmable channels for use in any common asynchronous or synchronous data communications protocol. The ISCC is built from Zilog's industry standard SCC core and is compatible with designs using Zilog's SCC to receive and transmit data.

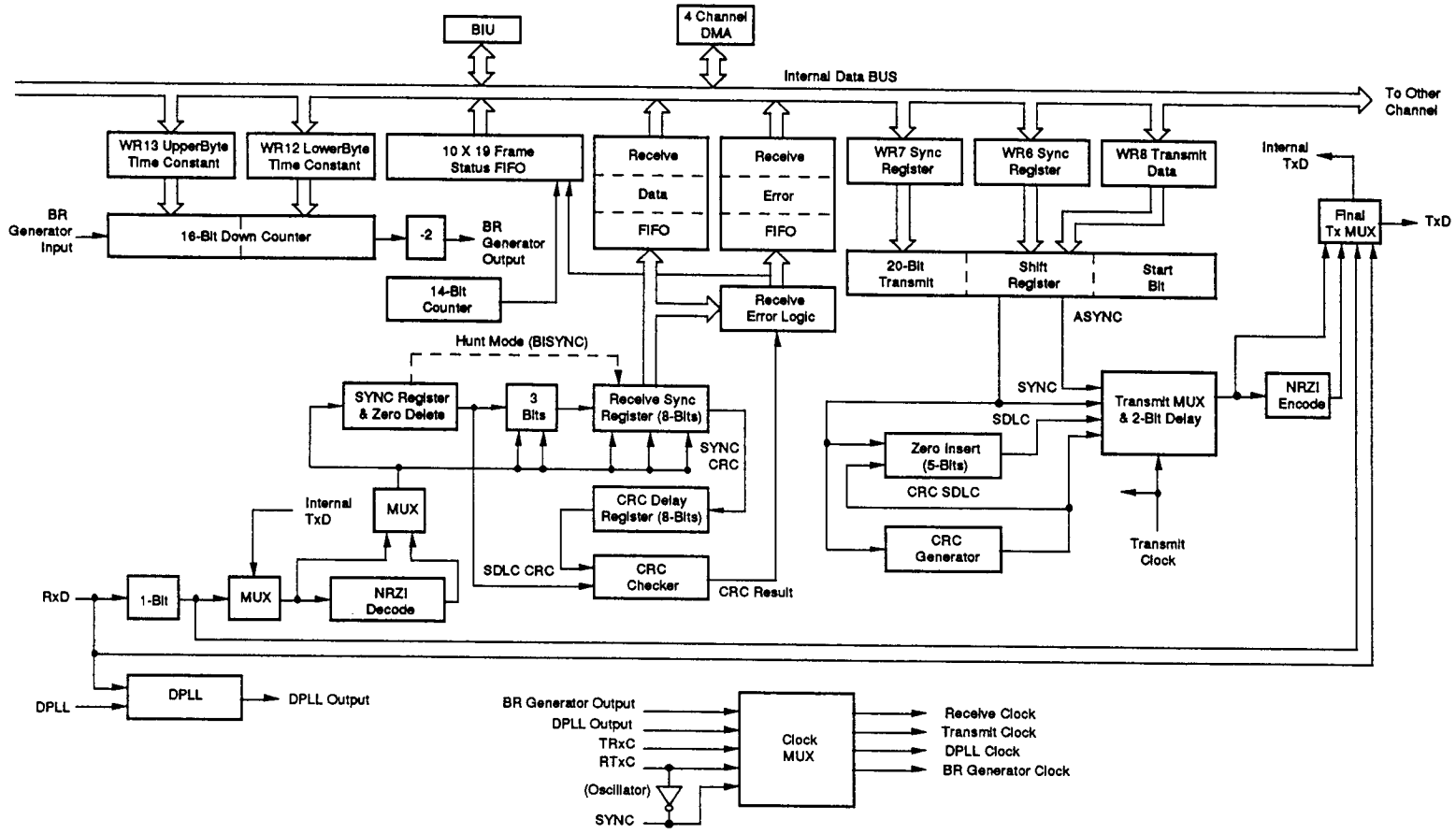


Figure 4. ISCC Data Path

Asynchronous Modes. Send and Receive can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half, or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 1). If the Low does not persist (e.g., a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ISCC does not require symmetric transmit and receive clock signals - a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate supplied to the receive and transmit clock inputs. In Asynchronous modes, the SYNC pin may be programmed as an input used for functions such as monitoring a ring indicator.

Synchronous Modes. The ISCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), and 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

Five or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the ISCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 5.

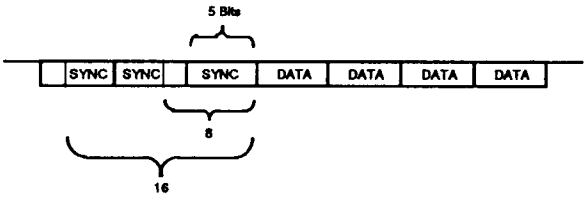


Figure 5. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all 1's or all 0's. The ISCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in Synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The ISCC supports Synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command is used to abort a frame in transmission. At the end of a message, the ISCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ISCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the SYNC pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0's inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ISCC must be programmed to use the SDLC CRC polynomial, but the generator and checker

may be preset to all 1's or all 0's. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1x mode. The parity options available in Asynchronous modes are available in Synchronous modes.

SDLC Loop Mode. The ISCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC Loop mode, the ISCC performs the functions of a secondary station while an ISCC operating in regular SDLC mode acts as a controller (Figure 6).

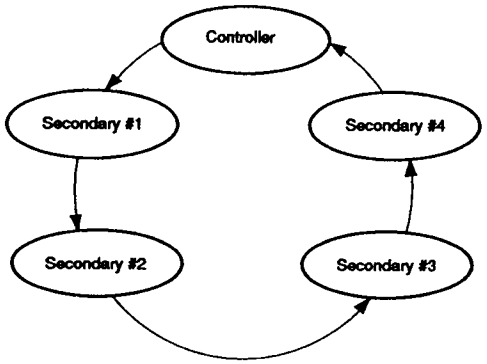


Figure 6. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, passes these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station places its own message on the loop only at specific times. The controller signals that secondary stations can transmit messages by sending a special character, called an EOP (End Of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit appends their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming message and are prohibited from placing messages on the loop (except upon recognizing an EOP.)

SDLC Loop mode is a programmable option in the ISCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

SDLC FIFO. The ISCC's ability to receive high speed back-to-back SDLC frames is maximized by a 10-bit deep by 19-bit wide status FIFO. When enabled (through WR15, bit D2), it provides the DMA the ability to continue to transfer data into memory so that the CPU can examine the message later. For each SDLC frame, a 14-bit byte count and 5 status/error bits are stored. The byte count and status bits are accessed through Read Registers 6 and 7. Read Registers are only accessible when the SDLC FIFO is enabled. The 10x19 status FIFO is separate from the 3 byte receive data FIFO.

Notes on the SDLC FIFO: When using the SDLC FIFO enhancment in channel B, it is necessary to enable the enhancment in channel A. There is no special requirement to enable the enhancement in channel A only , or to use it in both channels. Designs using only one channel should, therefore, use channel A.

When an SDLC frame is received with an abort condition, the byte counter in the FIFO enhancment is not reset. Therefore, after the abort is received, a dummy frame consisting of a flag should be sent by the transmitter. This resets the byte counter for the next frame. The aborted frame has a byte count which includes the byte count of the next dummy frame.

Baud Rate Generator. Each channel in the ISCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the TRxC pin, the output of the baud rate generator may be echoed out via the TRxC pin.

The following formula relates the time constant to the baud rate where PCLK or RTxC is the baud rate generator input frequency in Hertz. The clock mode is 1, 16, 32, or 64, as selected in Write Register 4, bits D6 and D7. Synchronous operation modes should select 1 and Asynchronous should select 16, 32 or 64.

$$\text{Time Constant} = \frac{\text{PCLK or RTxC Frequency}}{2(\text{Baud Rate})(\text{Clock Mode})} - 2$$

Digital Phase-Locked Loop. The ISCC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock is then used as the ISCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0, or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ISCC via the TRxC pin (if this pin is not being used as an input).

Data Encoding. The ISCC may be programmed to encode and decode the serial data in four different ways (Figure 7). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ISCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

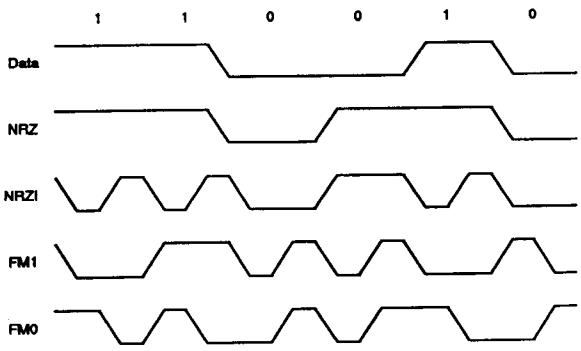


Figure 7. Data Encoding Methods

Auto Echo and Local Loopback. The ISCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay because the data stream is not decoded before retransmission. In Auto Echo mode, the /CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and /WAIT/REQUEST on transmit.

The ISCC is also capable of local loopback. In this mode TxD is RxD is just like Auto Echo mode. However, in Local Loopback mode the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The /CTS and /DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in Asynchronous, Synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

DMA Core. The ISCC contains four independent fly-by mode DMA channels. Each of the ISCC's transmit and receive channels has a DMA channel dedicated to it to move data to-and-from memory. The DMA channels are dedicated to the transmit and receive FIFO's, and therefore, can not be used for device initialization. Each DMA has a 32-bit address and a 16-bit byte counter. The DMA address may be incremented or decremented providing flexibility in doing block transfers.

See the I/O Interface Capabilities Section for more details on the DMA features.

BUS INTERFACE UNIT (BIU) DESCRIPTION

The ISCC contains a flexible bus interface that is compatible with a variety of microprocessors and microcontrollers. The device is designed to work with 8- or 16-bit bus systems and may be used with address/data multiplexed busses or non-multiplexed busses. The multiplexed bus is selected for the ISCC if there is an Address Strobe prior to or during the transaction which writes the BCR. If no Address Strobe is present prior to or during the transaction which writes the BCR, a non-multiplexed bus is selected.

When the ISCC is initialized for non-multiplexed operation, register addressing for the ISCC cell is (with the exception of WR0 and RR0), accomplished as follows. Programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 which contains four bits that point to the selected register (note point high command). The second write is the actual control word for the selected register. If the second operation is a read, the selected register is accessed. When in the non-multiplexed mode, all of the registers in the SCC cell of the ISCC, including the data registers, are accessed in this fashion. The pointer register is automatically cleared after the second read or write operation so that WR0 (or RR0) is addressed again. Note that when the DMA is not used to address the data, the data registers must be accessed by pointing to Register 8. This is in contrast to the Z8530 which allows direct addressing of the data registers through the C/D pin.

When the ISCC is initialized for non-multiplexed operation, register addressing for the DMA cell (with the exception of CSAR) is accomplished as follows and is completely independent of the SCC cell register addressing. Programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to the Command Status Address Register (CSAR) which contains five bits that point to the selected register (CSAR bits 4 - 0). The second write is the actual control word for the selected register. If the second operation is a read, the selected register is accessed. When in the non-multiplexed mode, all of the registers in the DMA cell of the ISCC may be accessed in this fashion. The pointer bits are automatically cleared after the second read or write operation so that CSAR is addressed again.

When the ISCC is initialized for multiplexed bus operation, all registers in the SCC cell are directly addressable with the register address occupying AD5 through AD1, or AD4 through AD0 (Shift Left / Shift Right modes). Two additional pins, A0/SCC//DMA and A1/A//B control the channel A/B register selection and the SCC channel /DMA selection. Refer to the A0/SCC//DMA and A1/A//B pin descriptions for the encoding of these signals.

The Shift Left / Shift Right modes for the address decoding for the internal registers (multiplexed bus) are separately programmable for the SCC cell and for the DMA cell. For the SCC cell the programming and operation is identical to that in the SCC; programming is accomplished through Write Register 0 (WR0), bits 1 and 0 (Figure 9-1).

The programming of the Shift Left / Shift Right modes for the DMA cell is accomplished in the BCR, bit 0. In this case, the shift function is similar to that for the SCC cell; with Shift left, the internal register addresses are decoded from bits AD5 through AD1 and with Shift Right, the internal register addresses are decoded from bits AD4 through AD0.

When the multiplexed bus mode is selected, Write Register 0 (WR0) takes on the form of WR0 in the Z8030 (Figure 9).

All data transfers to and from the ISCC are done in bytes even though the data can, at special times, occupy the lower or upper byte of the 16-bit bus. When accessed as a peripheral device (i.e., when the ISCC is not a bus master performing DMA transfers), all bus transactions are on the lower 8 bits of the bus with the following exception: When the ISCC registers are read, the byte data is present on both the lower 8 bits of the bus and the upper 8 bits of the bus. Data is accepted only on the lower 8 bits of the bus except in certain DMA transfers.

During DMA transfers, data may be transferred to or from the ISCC on the upper 8 bits of the bus for odd or even byte transfers. During DMA transfers to memory from the ISCC, byte data only is transferred and the data appears on both the lower 8 bits and is replicated on the upper 8 bits of the bus.

During DMA transfers to the ISCC from memory, byte data only is transferred and normally data is accepted only on the lower 8 bits of the bus. However, the byte swapping feature may be used to elect on which byte of the bus the data is accepted. The byte swapping feature is enabled by programming the Byte Swap Enable bit to a 1 in the BCR. The odd/even byte transfer selection is made by programming the Byte Swap Select bit in the BCR. If Byte Swap Select is a 1, then even address bytes (transfers where the DMA address has A0 equal 0) are transferred on the lower 8 bits of the bus and odd address bytes (transfers where the DMA address has A0 equal 1) are transferred on the upper 8 bits of the bus. If Byte Swap Select is a 0, then even address bytes (transfers where the DMA address has

A0 equal 0) are transferred on the upper 8 bits of the bus and odd address bytes(transfers where the DMA address has A0 equal 1) are transferred on the lower 8 bits of the bus.

I/O INTERFACE CAPABILITIES

The ISCC offers the choice of Polling, Interrupt (vectored or non-vectored), and DMA Transfer modes to transfer data, status, and control information to and from the CPU.

Polling. In this mode all interrupts and the DMA's are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. With polling, the CPU must periodically read a status register until the register contents indicate the need for some CPU action to be taken. Only one register in the SCC needs to be read; depending on the contents of the register, the CPU either reads data, writes data, or satisfies an error condition. Two bits in the register indicate the need for data transfer. An alternative is to poll the Interrupt Pending register to determine the source of an interrupt. The status for both SCC channels resides in one register.

Interrupts. When the ISCC responds to an Interrupt Acknowledge signal (INTACK) from the CPU, an interrupt vector is placed on the data bus. Both the SCC and the DMA contain vector registers. Depending on the source of interrupt, one of these vectors is returned. either unmodified or modified by the interrupt status to indicate the exact cause of the interrupt.

Each of the six sources in interrupts in the SCC (Transmit, Receive, and External/Status interrupts in both channels) and each DMA channel has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). If the IE bit is set for any given source of interrupt, then that source can request interrupts. The only exception to this rule is when the associate Master Interrupt Enable (MIE) bit is reset, then no interrupts are requested. Both the SCC and the DMA have an associated MIE bit. The IE bits in the SCC are write only, but the IE bits in the DMA are read write.

The ISCC provides for nesting of interrupt sources with an interrupt daisy chain using the IEI, IEO, and INTACK pins. As a microprocessor peripheral, the ISCC may request an interrupt only when no higher priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it enables the /INT signal. The CPU then responds with /INTACK, and the interrupting device places the vector on the data bus.

In the ISCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the /INT signal is activated, requesting an interrupt. In the SCC, if the IE bit is not set, then the IP for that source can never be set. The IP bits in the DMA are set independent of the IE bit.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ISCC and external to the ISCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ISCC being pulled Low and propagated to subsequent peripherals. Internally, the SCC is higher priority than the DMA. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

Within the SCC portion of the ISCC there are three types of interrupts: Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. This implies that the transmitter had a data character written into it to make it empty. When enabled, the receiver interrupts the CPU in one of three ways:

1. Interrupt on First Receive Character or Special Receive Condition

2. Interrupt on All Receive Characters or Special Receive Condition

3. Interrupt on Special Condition Only

Interrupt on First Character or Special Condition, and Interrupt on Special Condition Only, are typically used when doing block transfers with the DMA. A Special Receive Condition is one of the following: receiver overrun, framing error in Asynchronous mode, end-of-frame in SDLC mode and, optionally, a parity error. The Special Receive Condition interrupt is different from an Ordinary Receive Character Available interrupt only by the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt occurs from Special Receive Conditions any time after the First Receive Character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the /CTS, /DCD, and /SYNC pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break (Asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the ISCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic.

Each DMA in the ISCC has two sources of interrupt, which share an IP bit and an IUS bit, but have independent enables: Terminal Count and Abort. The Abort interrupt is generated when an active DMA channel is forced to terminate its transfers because /BUSACK is de-asserted during a transfer. The Terminal Count interrupt is generated when the DMA transfer count reaches zero. The DMA channels themselves are prioritized in a fixed order: Receive A, Transmit A, Receive B, and Transmit B.

DMA Transfer. In this mode, the on-chip DMA channels transfer data directly to the transmit buffers or directly from the receive buffers. No other transfers are possible (for initialization, for example). The request signals from the receivers and transmitters are hard-wired to the request inputs of the DMA channels internally. Each DMA channel provides a 32-bit address which is either incremented or decremented with a 16-bit transfer length. Whenever a DMA channel receives a request from its associated receiver or transmitter and the DMA channel is enabled, the ISCC activates the /BUSREQ signal. Upon receipt of an active /BUSACK, the DMA channel transfers data between memory and the SCC. This transfer continues until the receiver or transmitter stops requesting a transfer, until the terminal count is reached, or /BUSACK is deactivated. The four DMA channels operate independently when the Request Per Channel option is selected; otherwise, all requests pending at the time of bus acquisition will be serviced before the bus is released. Each DMA channel is independently enabled and disabled.

Bus Interface. The ISCC contains a flexible bus interface that provides the resources necessary to interface the ISCC to virtually any type of bus. The ISCC directly supports either an 8-bit or a 16-bit bus, although all transfers to and from the device are limited to 8-bits at a time. The control signals provided allow connection to either a multiplexed address/data type bus or to a separate address and data type bus. While the ISCC is bus master, the upper address, lower address, and data are multiplexed on AD0-15. Interrupt Acknowledge is signaled through the /INTACK signal, which may be programmed as either a status input, a pulsed input, or a double-pulsed input. The ISCC also contains a /WAIT//RDY input for synchronizing CPU or DMA and memory accesses. This pin may be programmed to act as either a /WAIT signal or a /READY signal. The appropriate signal is provided by the ISCC when it is not bus master, and is sampled by the ISCC when it is bus master. The ISCC requests the bus via a /BUSREQ signal and assumes bus mastership upon receipt of a /BUSACK signal.

REGISTERS

The ISCC contains separate register sets for the SCC core and the DMA core. Access to each set is controlled by the A0/SCC//DMA pin. When this pin is an input, a High selects the SCC core and a Low selects the DMA core. The first write to the ISCC after reset is always to the Bus Configuration Register (BCR), see Figure 8. If an /AS is present before the BCR is written to, a multiplexed bus is selected. If no /AS is present before the BCR write, a non-multiplexed bus is selected. The BCR cannot be changed without resetting the ISCC.

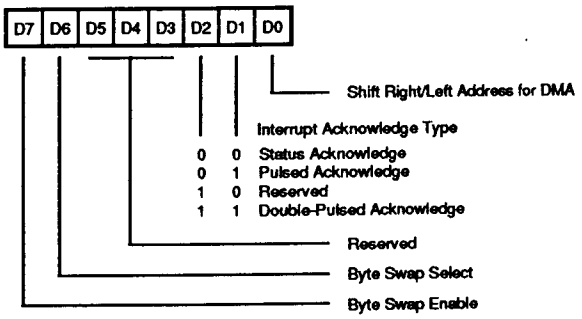


Figure 8. Bus Configuration Register (BCR)

SCC Cell. The SCC core contains 13 write registers (14 counting the transmit buffer) and ten read registers (11 counting the receive buffer) in each channel. Two of the write registers are shared (WR2 and WR9) and are accessed by both channels. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Table 1 is a list of the SCC write registers and Table 2 is a list of the SCC read registers. Figures 9 and 10 show the write and read register formats. Read Registers 6 and 7 are only accessible when the SDLC FIFO is enabled. When the SDLC FIFO is not enabled, Read Registers 6 and 7 are images of Read Registers 2 and 3, respectively.

DMA Cell. The DMA cell contains 17 registers (counting the BCR). All of the registers are write/read except the BCR, CCAR and ICSR. The ISCC also has two status registers, the DMA status register (DSR) and the Interrupt Status Register (ISR), which are addressed by reading the CCAR and ICSR. The DMA also reserves two addresses for future use and should not be addressed or should be written with all zeros to prevent unexpected operation and maintain compatibility with future products. Each DMA channel has a 32-bit wide address register providing an addressing range of 4 gigabytes. Each channel also has a 16-bit count register for up to 64K byte data packet sizes.

Table 1. SCC Write Registers

Bit	Description
WR0	Register Pointers, various initialization commands
WR1	Transmit and Receive interrupt enables, WAIT/DMA commands
WR2	Interrupt Vector
WR3	Receive parameters and control modes
WR4	Transmit and Receive modes and parameters
WR5	Transmit parameters and control modes
WR6	Sync Character or SDLC address
WR7	Sync Character or SDLC flag
WR8	Transmit buffer
WR9	Master Interrupt control and reset commands
WR10	Miscellaneous transmit and receive control bits
WR11	Clock mode controls for receive and transmit
WR12	Lower byte of baud rate generator
WR13	Upper byte of baud rate generator
WR14	Miscellaneous control bits
WR15	External status interrupt enable control

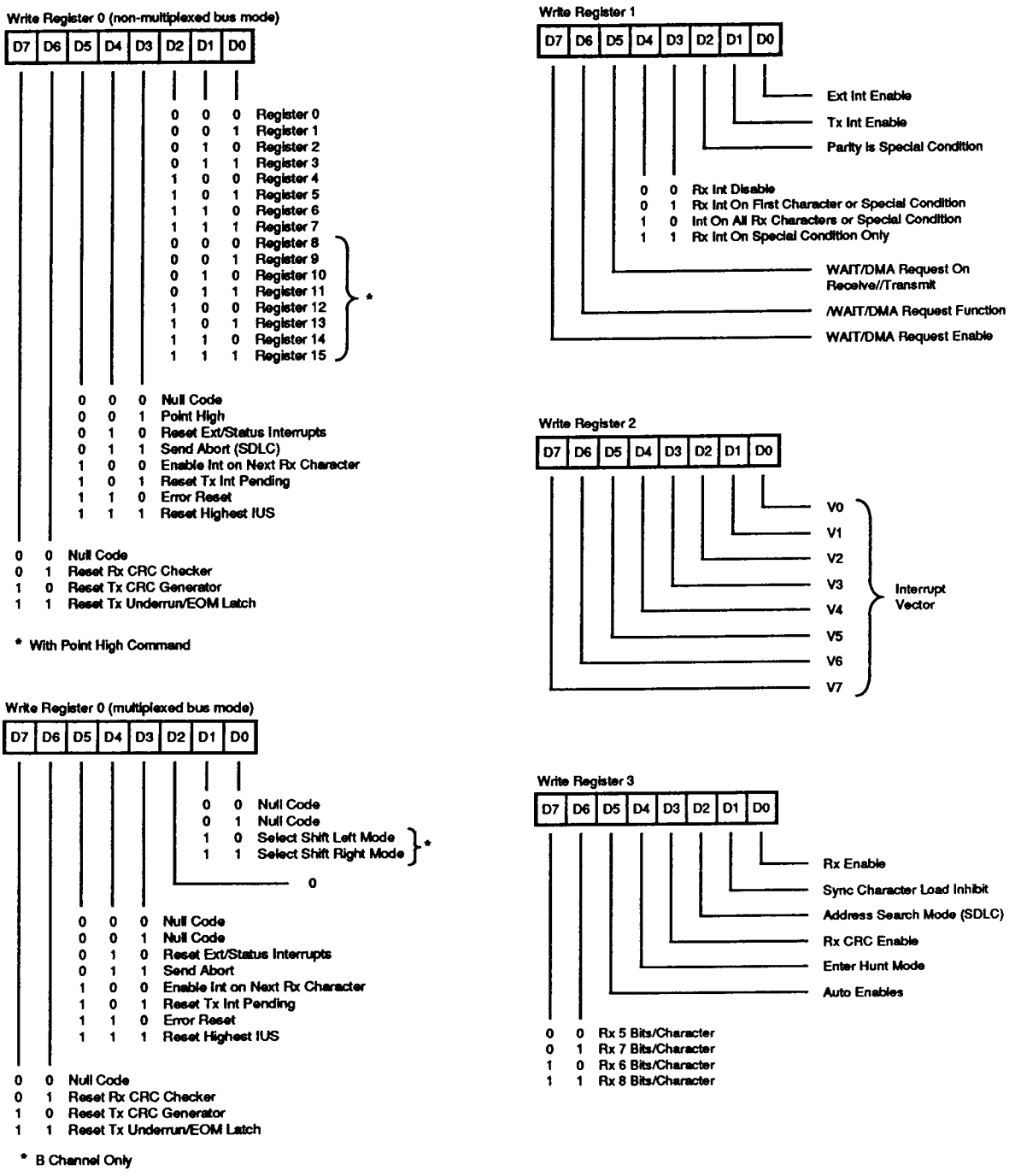


Figure 9. Write Register Bit Functions

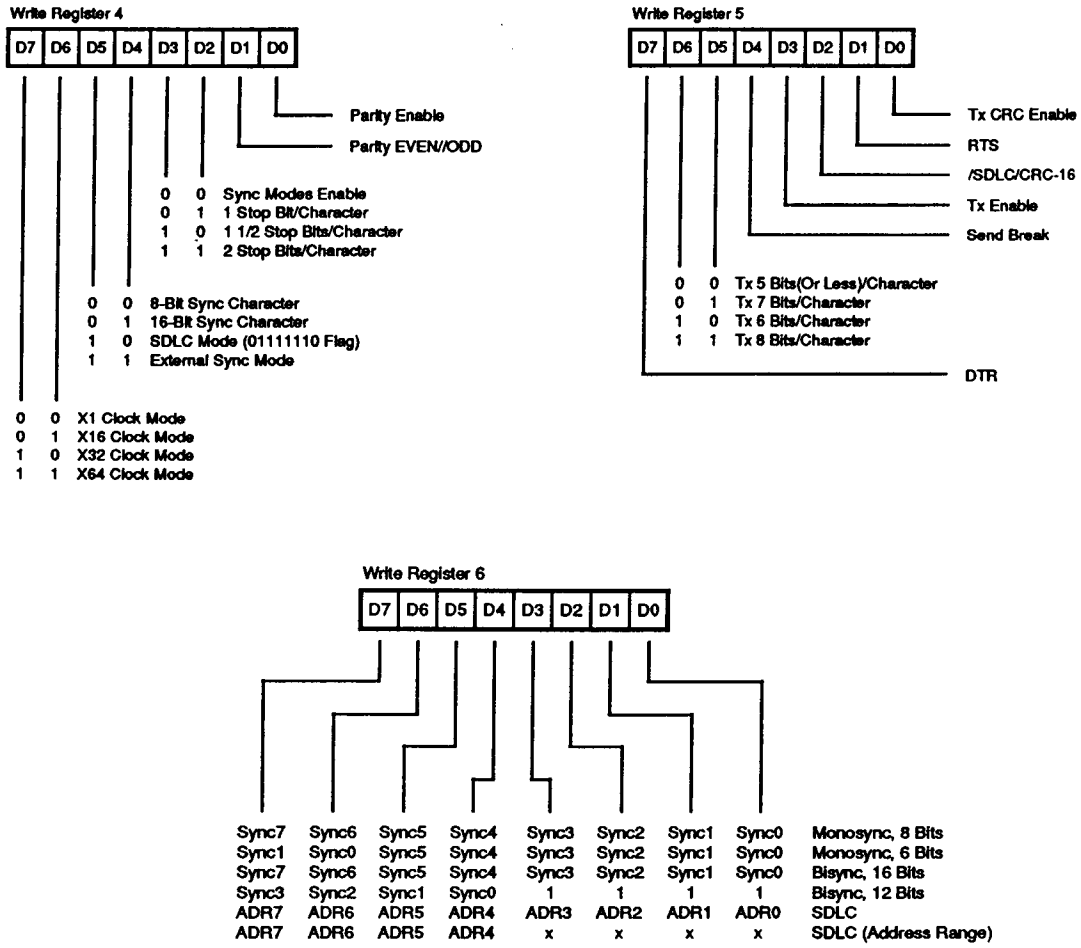


Figure 9. Write Register Bit Functions (Continued)

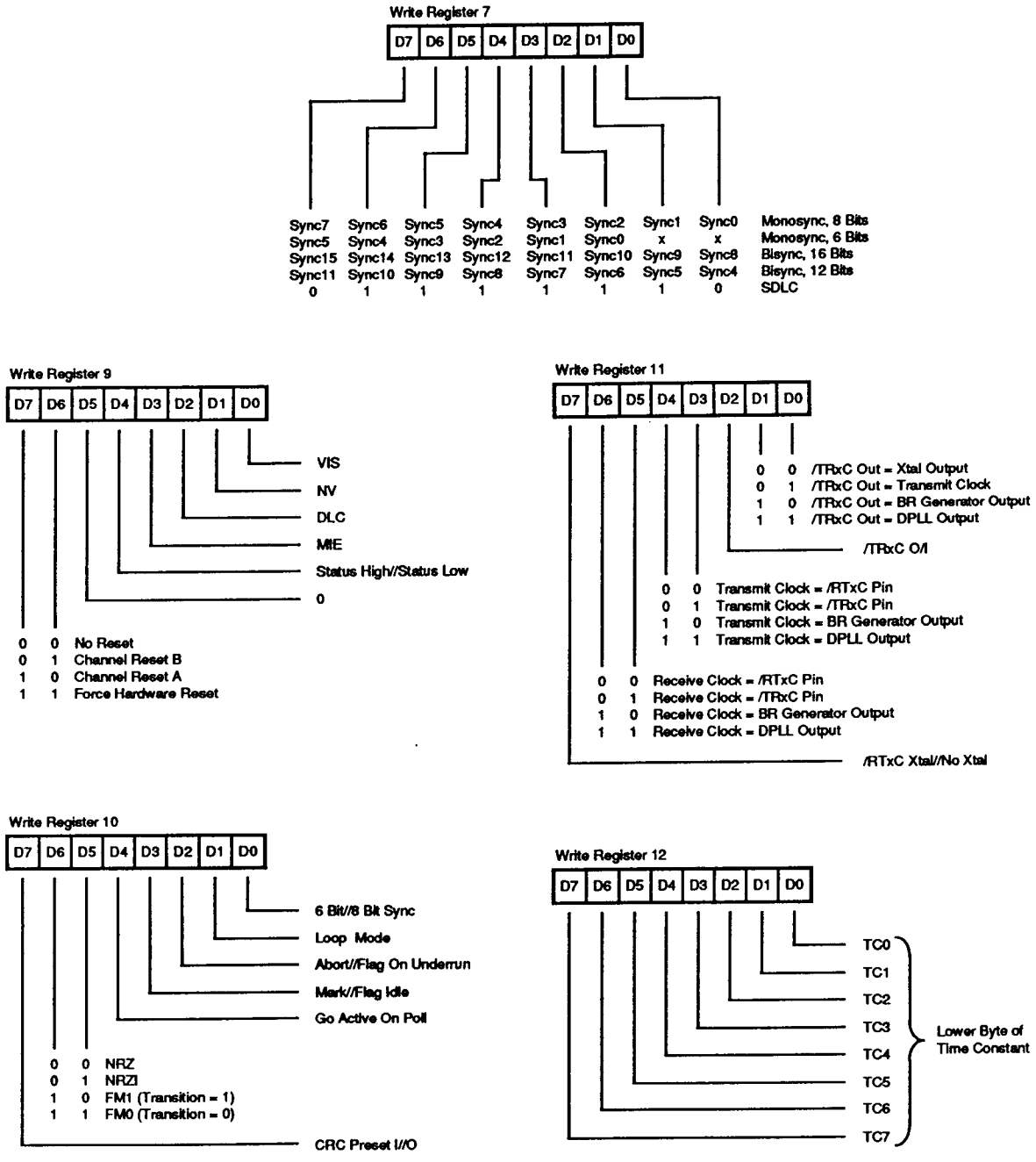


Figure 9. Write Register Bit Functions (Continued)

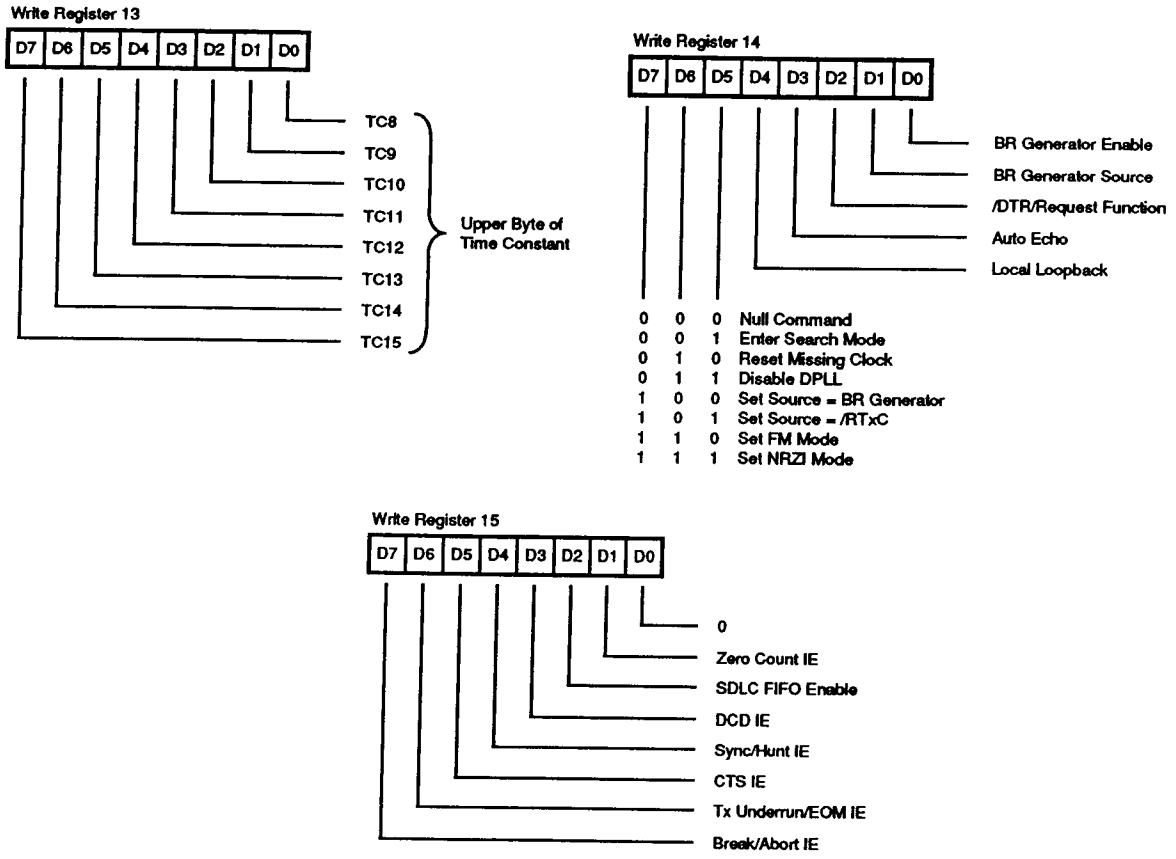


Figure 9. Write Register Bit Functions (Continued)

Table 2. SCC Read Registers

Bit	Description
RR0	Transmit and Receive buffer status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only), Unmodified interrupt vector (Channel A only)
RR3	Interrupt pending bits (Channel A only)
RR6	SDLC FIFO byte counter lower byte (only when enabled)
RR7	SDLC FIFO byte count and status (only when enabled)
RR8	Receive buffer
RR10	Miscellaneous status bits
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External Status interrupt information

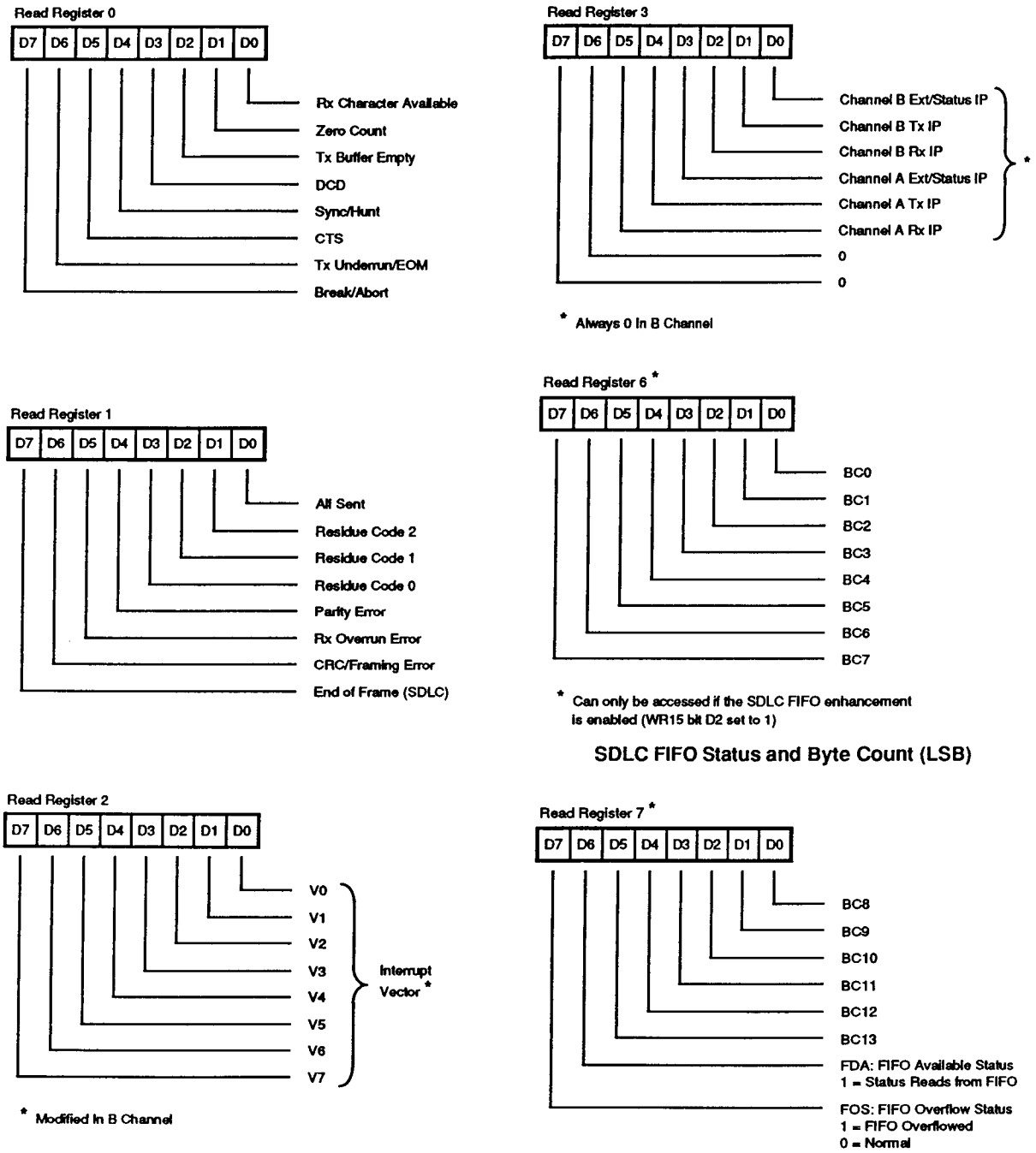


Figure 10. Read Register Bit Functions

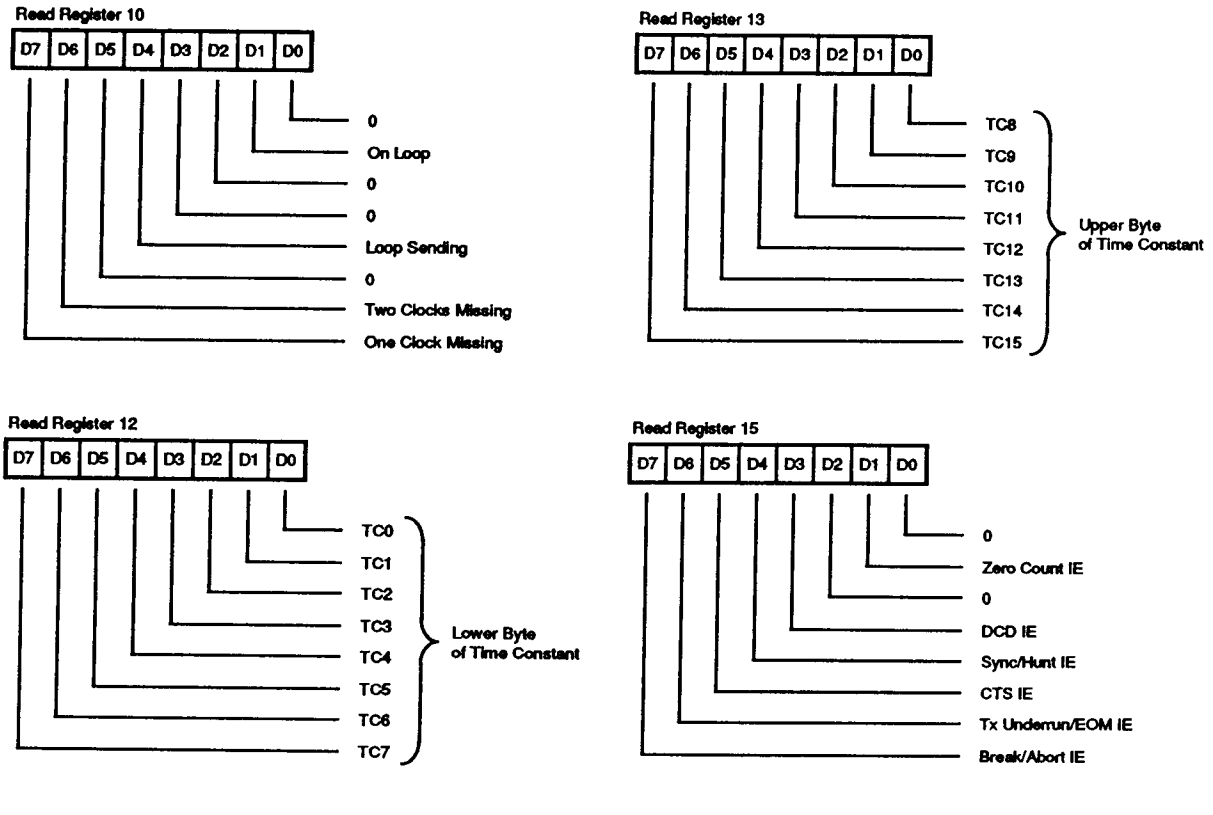


Figure 10. Read Register Bit Functions (Continued)

Table 3. DMA Cell Register Description

Address	Name	Description
xxxxx	BCR	Bus Configuration Register
00000	CCAR	Channel Command/Address Register (Write)
00000	DSR	DMA Status Register (Read)
00001	ICR	Interrupt Control Register
00010	IVR	Interrupt Vector Register
00011	ICSR	Interrupt Command Register (Write)
00011	ISR	Interrupt Status Register (Read)
00100	DER	DMA Enable/Disable Register
00101	DCR	DMA Control Register
00110		Reserved Address
00111		Reserved Address
01000-01001	RDCRA	Receive DMA Count Register Channel A (Low-high byte)
01010-01011	TDCRA	Transmit DMA Count Register Channel A
01100-01101	RDCRB	Receive DMA Count Register Channel B
01110-01111	TDCRB	Transmit DMA Count Register Channel B
10000-10011	RDARA	Receive DMA Address Register Channel A
10100-10111	TDARA	Transmit DMA Address Register Channel A
11000-11011	RDARB	Receive DMA Address Register Channel B
11100-11111	TDARB	Transmit DMA Address Register Channel B

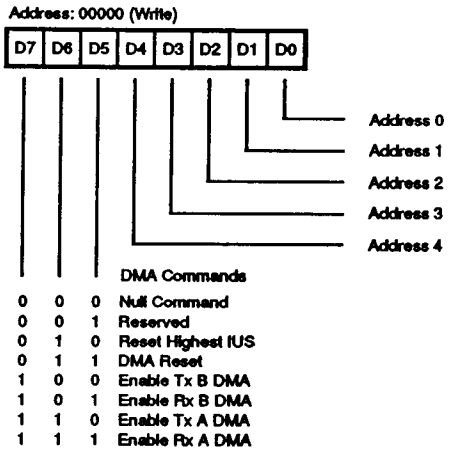


Figure 11. Channel Command/Address Register

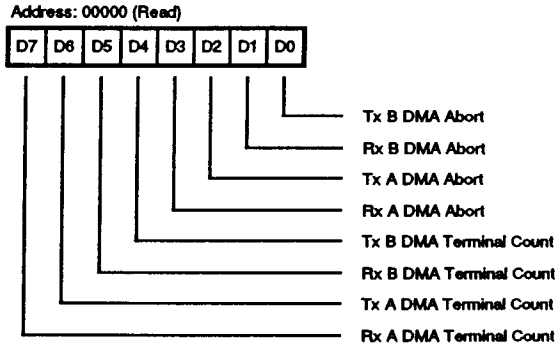


Figure 12. DMA Status Register

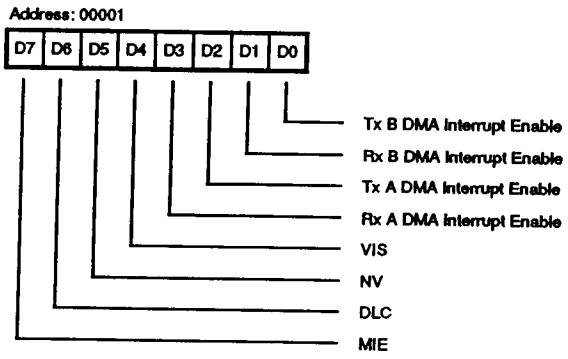


Figure 13. Interrupt Control Register

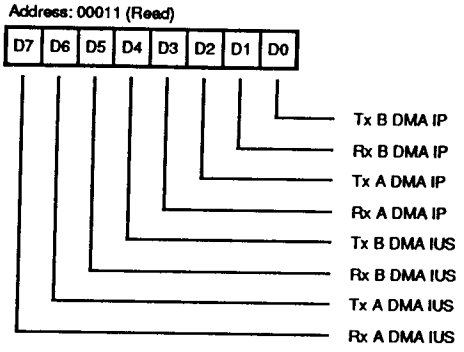


Figure 16. Interrupt Status Register

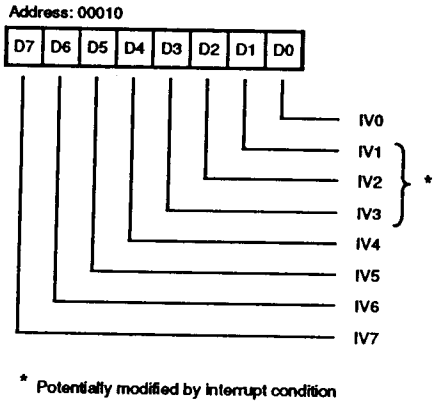


Figure 14. Interrupt Vector Register

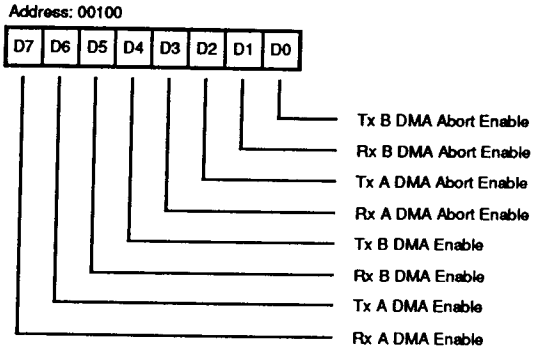


Figure 17. DMA Enable Register

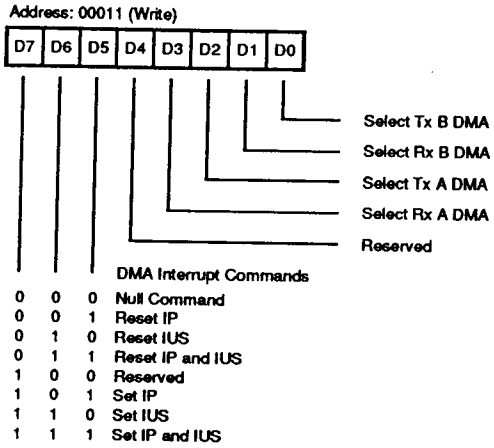


Figure 15. Interrupt Command/Register

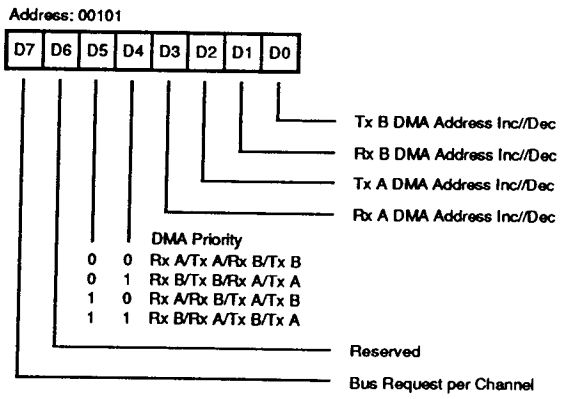


Figure 18. DMA Control Register

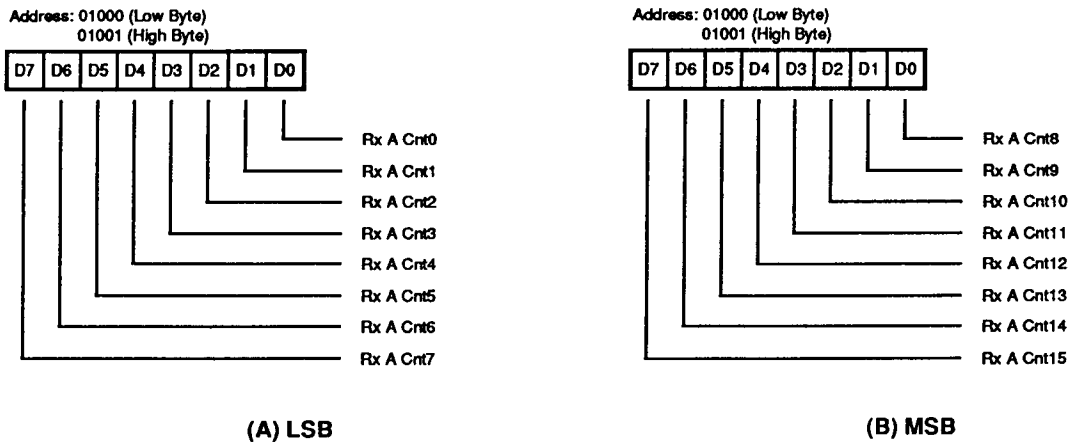


Figure 19. Receive DMA Count Register Channel A

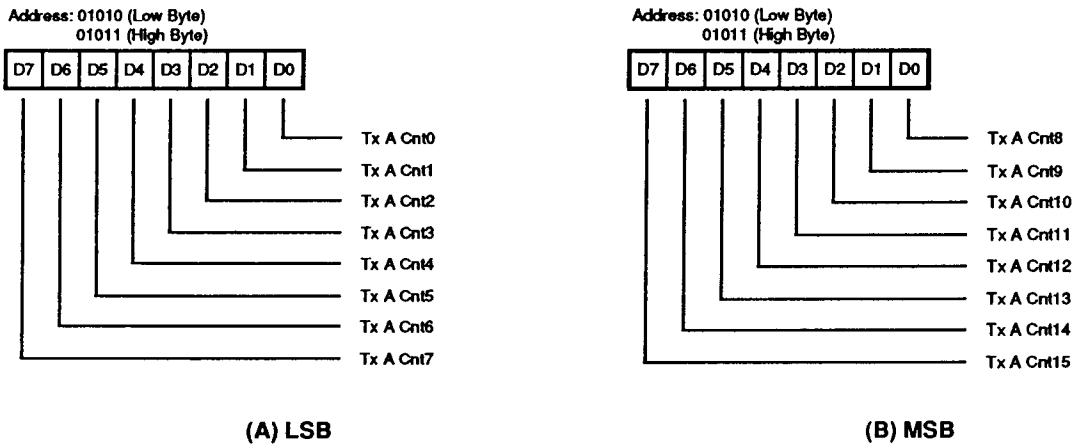


Figure 20. Transmit DMA Count Register Channel A

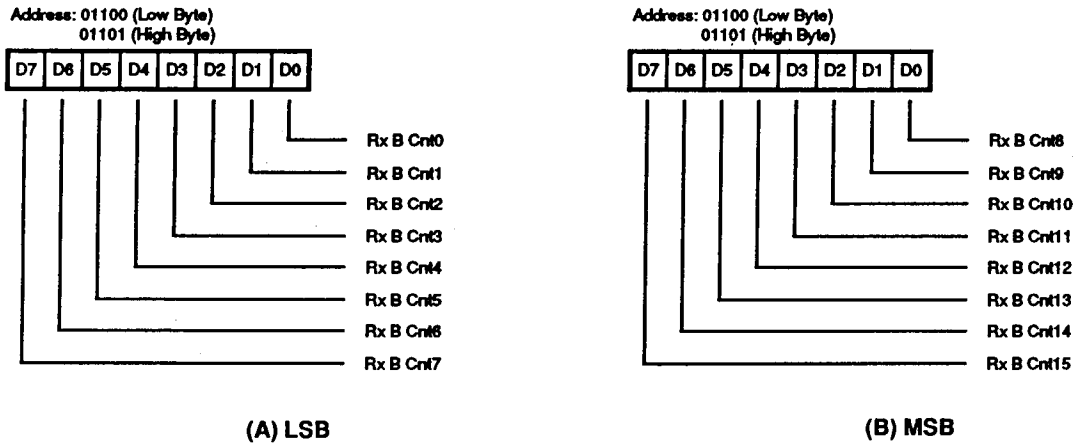


Figure 21. Receive DMA Count Register Channel B

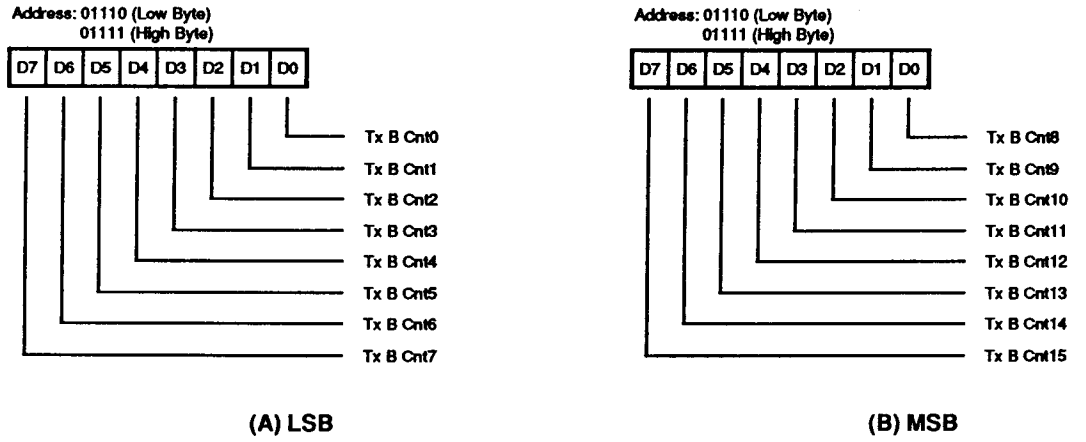


Figure 22. Transmit DMA Count Register Channel B

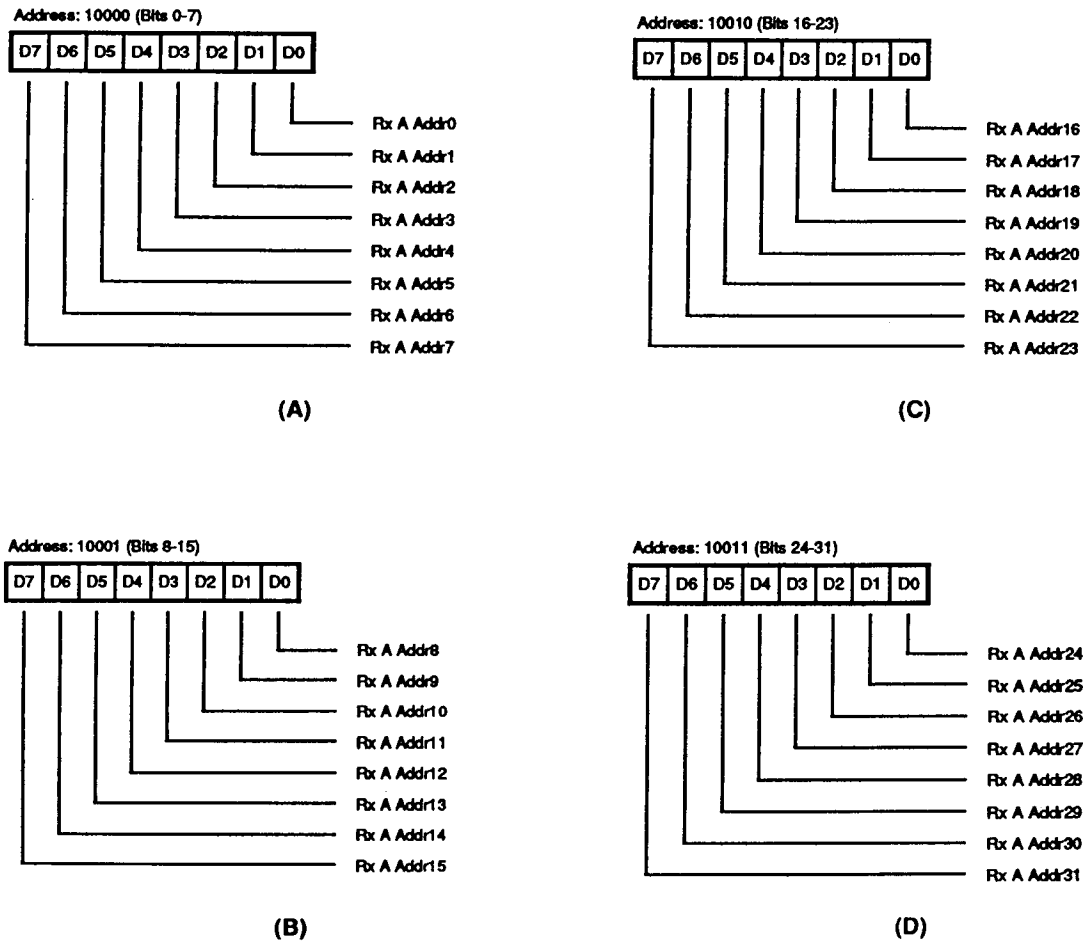


Figure 23. Receive DMA Address Register Channel A

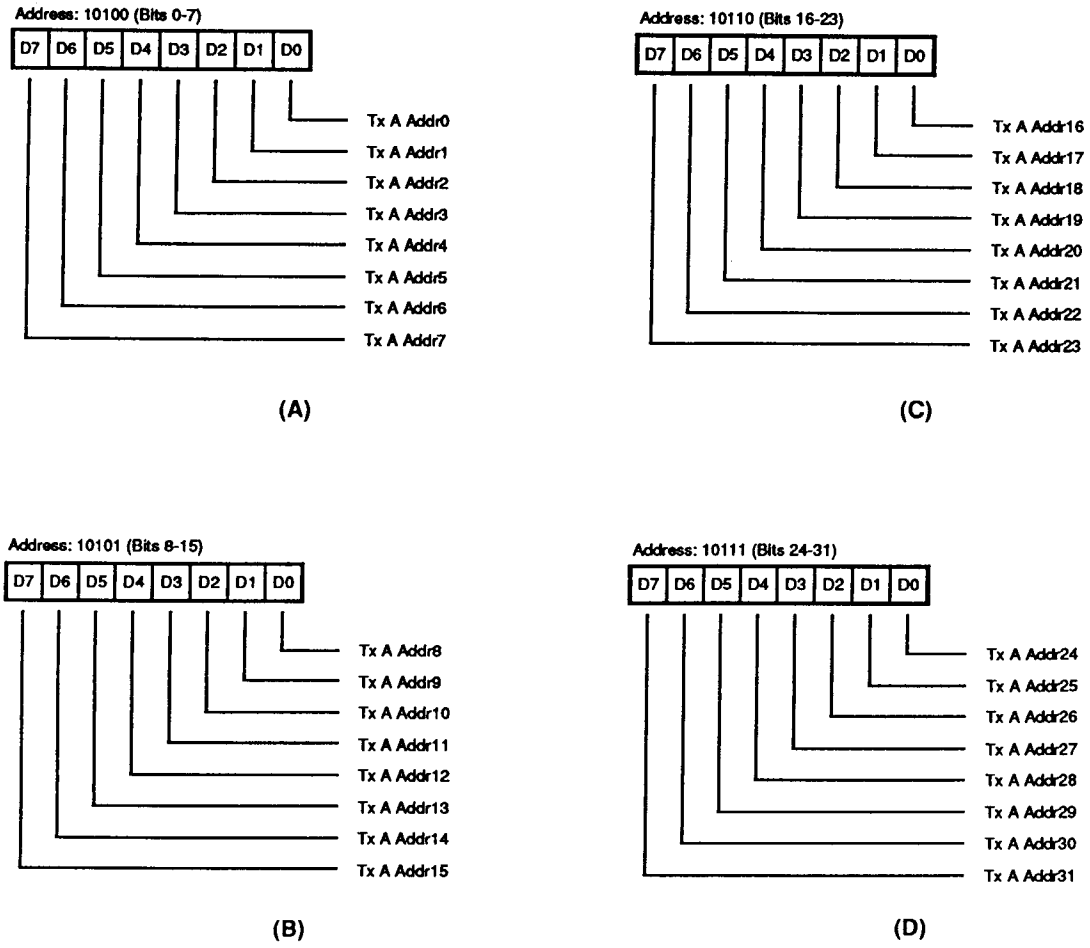


Figure 24. Transmit DMA Address Register Channel A

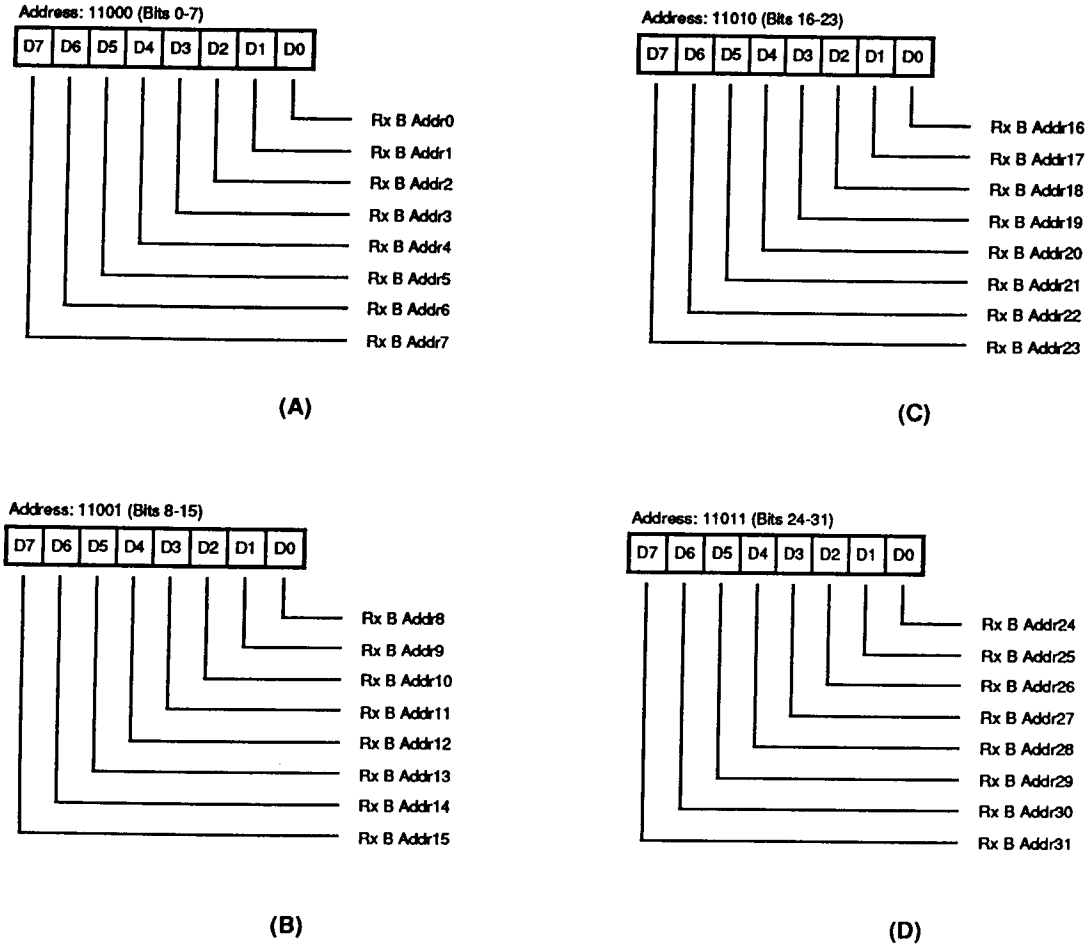


Figure 25. Receive DMA Address Register Channel B

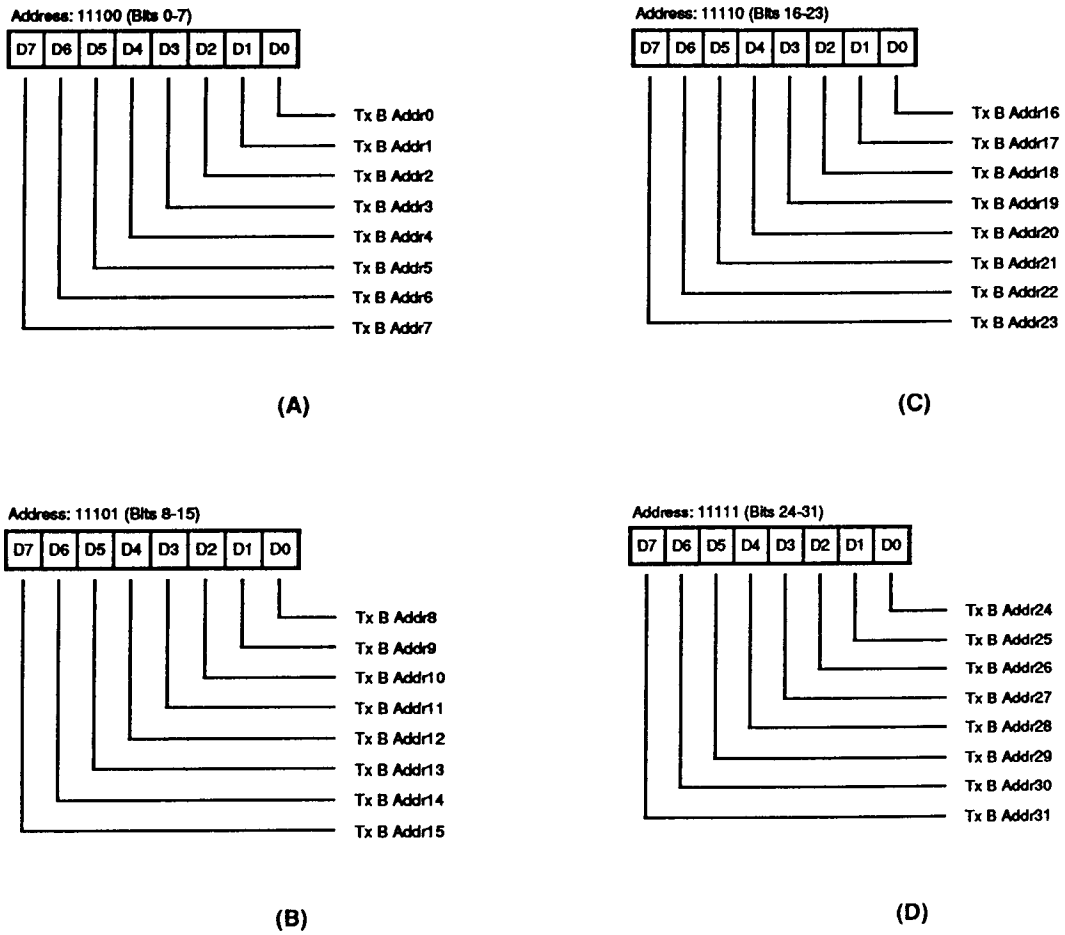


Figure 26. Transmit DMA Address Register Channel B

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins, with respect to GND ..... -0.3 V to +7.0 V
Operating Ambient Temperature ..... See Ordering Information
Storage Temperature ..... -85°C to 150°C
Voltages on all inputs, with respect to GND ..... -0.3 V to V_{CC} + 0.3 V

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75 V ≤ Vcc ≤ 5.25 V
GND = 0 V
T_A as specified in Ordering Information

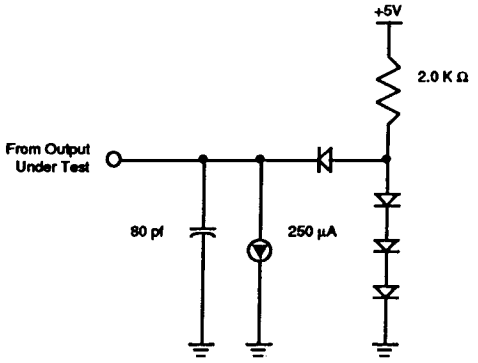


Figure 27. Standard Test Load

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance		15	pF	Returned to Ground
$C_{I/O}$	Bidirectional Capacitance		20	pF	

f = 1 MHz over specfied temperature range.
Unmeasured pins returned to ground.

Miscellaneous: Transistor Count 52,047

Z16C35 DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = -1.6 mA
V_{OH2}	Output High Voltage	V_{CC} -0.8			V	I_{OH} = -250 µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = +2.0 mA
I_{IL}	Input Leakage			± 10.00 µA		0.4 < V_{IN} < + 2.4 V
I_{OL}	Output Leakage			± 10.00 µA		0.4 < V_{OUT} < +2.4V
I_{CCI}	V_{CC} Supply Current		7	50	mA	V_{CC} = 5 V, V_{IH} = 4.8 V, V_{IL} = 0.2V

V_{CC} = 5 V ± 5% unless otherwise specified, over specified temperature range.

AC CHARACTERISTICS

No	Symbol	Parameter	10MHz * Min	Max	Notes
1	Tcyc	Bus Cycle Time	4TcPC		
2	TwASl	/AS Low Width	40		
3	TwASh	/AS High Width	90		
4	TwDSl	/DS Low Width	70		
5	TwDSh	/DS High Width	60		
6	TdAS(DS)	/AS↑ to /DS↓ Delay Time	5		
7	TdDS(AS)	/DS↑ to /AS↓ Delay Time	5		
8	TdDS(DRa)	/DS↓ to Data Active Delay	0		
9	TdDS(DRv)	/DS↓ to Data Valid Delay		85	
10	TdDS(DRn)	/DS↑ to Data Not Valid Delay	0		
11	TdDS(DRz)	/DS↑ to Data Float Delay		20	
12	TsCS(AS)	/CS to /AS↑ Setup Time	15		
13	ThCS(AS)	/CS to /AS↑ Hold Time	0		
14	TsADD(AS)	Direct Address to /AS↑ Setup Time	15		[1]
15	ThADD(AS)	Direct Address to /AS↑ Hold Time	5		[1]
16	TsSIA(AS)	Status /INTACK to /AS↑ Setup Time	15		
17	ThSIA(AS)	Status /INTACK to /AS↑ Hold Time	5		
18	TsAD(AS)	Adress to /AS↑ Setup Time	15		
19	ThAD(AS)	Address to /AS↑ Hold Time	5		
20	TsRW(DS)	R/W to /DS↓ Setup Time	0		
21	ThRW(DS)	R/W to /DS↓ Hold Time	25		
22	TdDSf(RDY)	/DS↓ to /READY↓ Delay		50	
23	TdDSr(RDY)	/DS↑ to /READY↑ Delay		40	
24	TsDW(DS)	Write Data to /DS↓Setup Time	0		
25	ThDW(DS)	Write Data to /DS↓Hold Time	25		
26	TdRDY(DRv)	/READY↓ to Data Valid Delay		40	
28	TwRDl	/RD Low Width	70		
29	TwRDh	/RD High Width	60		
30	TdAS(RD)	/AS↑ to /RD↓ Delay Time	5		
31	TdRD(AS)	/RD↑to /AS↓ Delay Time	5		
32	TdRD(DRa)	/RD↓ to Data Active Delay	0		
33	TdRD(DRv)	/RD↓ to Data Valid Delay		85	
34	TdRD(DRn)	/RD↑ to Data Not Valid Delay	0		
35	TdRD(DRz)	/RD↑to Data Float Delay		20	
36	TdRDf(RDY)	/RD↓to /READY↓ Delay		50	
37	TdRDr(RDY)	/RD↑ to /READY↑ Delay		40	
38	TwWRl	/WR Low Width	70		
39	TwWRh	/WR High Width	60		
40	TdAS(WR)	/AS↑ to /WR↓ Delay Time	5		
41	TdWR(AS)	/WR↑to AS↓ Delay Time	5		

* Units in nanoseconds.

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	10MHz * Min	Max	Notes
42	TsDW(WR)	Write Data to /WR↓ Setup Time	0		
43	ThDW(WR)	Write Data to /WR↓ Hold Time	25		
44	TdWRf(RDY)	/WR↓ to /READY↓ Delay		50	
45	TdWRr(RDY)	/WR↑ to /READY↓Delay		40	
46	TsCS(DS)	/CS to /DS↓ Setup Time	0		[2]
47	ThCS(DS)	/CS to /DS↓ Hold Time	25		[2]
48	TsADD(DS)	Direct Address to /DS↓ Setup Time	0		[1,2]
49	ThADD(DS)	Direct Address to /DS↓ Hold Time	25		[1,2]
50	TsSIA(DS)	Status /INTACK to /DS↓ Setup Time	0		[2]
51	ThSIA(DS)	Status /INTACK to /DS↓ Hold Time	25		[2]
52	TsCS(RD)	/CS to /RD↓ Setup Time	0		[2]
53	ThCS(RD)	/CS to /RD↓ Hold Time	25		[2]
54	TsADD(RD)	Direct Address to /RD↓Setup Time	0		[1,2]
55	ThADD(RD)	Direct Address to /RD↓ Hold Time	25		[1,2]
56	TsSIA(RD)	Status /INTACK to /RD↓ Setup Time	0		[2]
57	ThSIA(RD)	Status /INTACK to /RD↓ Hold Time	25		[2]
58	TsCS(WR)	/CS to /WR↓ Setup Time	0		[2]
59	ThCS(WR)	/CS to /WR↓ Hold Time	25		[2]
60	TsADD(WR)	Direct Address to /WR↓ Setup Time	0		[1,2]
61	ThADD(WR)	Direct Address to /WR↓ Hold Time	25		[1,2]
62	TsSIA(WR)	Status /INTACK to /WR↓ Setup Time	0		[2]
63	ThSIA(WR)	Status /INTACK to /WR↓ Hold Time	25		[2]
78	TdDSI(RDY)	/DS↓ (Intack) to /READY↓ Delay		300	[4]
81	TsIEI(DSI)	IEI to /DS↓ (Intack) Setup Time	60		
82	ThIEI(DSI)	IEI to /DS↑ (Intack) Hold Time	0		
83	TdIEI(IEO)	IEI to IEO Delay		60	
84	TdAS(IEO)	/AS↑ or Status Intack to IEO Delay		60	
85	TdDSI(INT)	/DS↓ (Intack) to /INT Inactive Delay		200	
86	TdDSI(Wf)	/DS↓ (Intack) to /WAIT↓ Delay		40	
87	TdDSI(Wr)	/DS↓ (Intack) to /WAIT↑ Delay		300	[4]
88	TdW(DRy)	/WAIT↑ to Data Valid Delay		40	
89	TdRDI(RDY)	/RD↓ (Intack) to /READY↓ Delay		300	[4]
91	TsIEI(RDI)	IEI to /RD↓ (Intack) Setup Time	60		
92	ThIEI(RDI)	IEI to /RD↑ (Intack) Hold Time	0		
93	TdRDI(INT)	/RD↓ (Intack) to /INT Inactive Delay		200	
94	TdRDI(Wf)	/RD↓ (Intack) to /WAIT↓ Delay		40	
95	TdRDI(Wr)	/RD↓ (Intack) to /WAIT↑ Delay		300	[4]
96	TwPIA l	Pulsed /INTACK Low Width	70		
97	TwPIAh	Pulsed /INTACK High Width	60		
98	TdAS(PIA)	/AS↑ to Pulsed /INTACK↓ Delay Time	5		

* Units in nanoseconds.

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	10MHz * Min	Max	Notes
99	TdPIA(AS)	Pulsed /INTACK↑ to /AS↓ Delay Time	5		
100	TdPIA(DRa)	Pulsed /INTACK↓ to Data Active Delay	0		
101	TdPEA(DRn)	Pulsed /INTACK↑ to Data Not Valid Delay	0		
102	TdPIA(DRz)	Pulsed /INTACK↑ to Data Float Delay		20	
103	TsIEI(PIA)	IEI to Pulsed /INTACK↓ Setup Time	60		
104	ThIEI(PIA)	IEI to Pulsed /INTACK↑ Hold Time	0		
105	TdPIA(IEO)	Pulsed /INTACK↓ to IEO Delay		60	
106	TdPIA(INT)	Pulsed /INTACK↓ to /INT Inactive Delay		200	
107	TdPIAf(RDY)	Pulsed /INTACK↓ to /READY↓ Delay		300	[4]
108	TdPIAr(RDY)	Pulsed /INTACK↑ to /READY↑ Delay		40	
109	TdPIA(Wf)	Pulsed /INTACK↓ to /WAIT↓ Delay		40	
110	TdPIA(Wr)	Pulsed /INTACK↓ to /WAIT↑ Delay		300	[4]
111	TdSIA(INT)	Status /INTACK↓ to /INT Inactive Delay		200	[2]
113	TwRESI	/RESET Low Width	170		
114	TwRESh	/RESET High Width	60		
115	TdRES(STB)	/RESET↑ to /Strobe↓	60		[3]
116	TdPC(BUSa)	PCLK↑ to Bus Active Delay		40	[5]
117	TdPC(BRQ)	PCLK↑ to /BUSREQ Delay		40	
118	TsBAK(PC)	/BUSACK to PCLK↑ Setup Time	10		
119	ThBAK(PC)	/BUSACK to PCLK↑Hold Time	30		
120	TwPCl	PCLK Low Width	35		
121	TwPCh	PCLK High Width	35		
122	TcPC	PCLK Cycle Time	100		
123	TfPC	PCLK Fall Time		10	
124	TrPC	PCLK Rise Time		10	
125	TdPCr(UAS)	PCLK↑ to /UAS Delay		30	[5]
126	TwUASI	/UAS Low Width	30		[5,6]
127	TdPCf(UAS)	PCLK↓ to /UAS Delay		30	[5]
128	TdPCr(AS)	PCLK↑to /AS Delay		30	[5]
129	TwASI	/AS Low Width	30		[5,6]
130	TdPCf(AS)	PCLK↓ to /AS Delay		30	[5]
131	TdAS(DSr)	/AS↑ to /DS↓ (Read) Delay	30		[5,7]
132	TdDS(PCr)	PCLK↑ to /DS Delay		30	[5]
133	TwDSlr	/DS Low Width (Read)	135		[5,8]
134	TdPCf(DS)	PCLK↓ to /DS Delay		30	[5]
135	TsDR(DS)	Read Data to /DS↑ Setup Time	30		[5]
136	ThDR(DS)	Read Data to /DS↑ Hold Time	0		[5]
137	TdPC(RW)	PCLK↑ to R/W Delay		30	[5]
138	TdAS(RD)	/AS↑ to /RD↓ Delay	30		[5,7]
139	TdPCr(RD)	PCLK↑ to /RD Delay		30	[5]

* Units in nanoseconds.

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	10MHz * Min	Max	Notes
140	TwRDI	/RD Low Width	135		[5,8]
141	TdPCf(RD)	PCLK↓ to /RD Delay		30	[5]
142	TsDR(RD)	Read Data to /RD↑ Setup Time	30		[5]
143	ThDR(RD)	Read Data to /RD↑ Hold Time	0		[5]
144	TdPC(ADD)	PCLK↑ to Direct Address Delay		30	[1,5]
145	TdPC(AD)	PCLK↑ to Address Delay		40	[5]
146	ThAD(PC)	Address to PCLK↑ Hold Time	0		[5]
147	TdPC(ADz)	PCLK↑ to Address Float Delay		50	[5]
148	TdPC(ADa)	PCLK↑ to Address Active Delay		40	[5]
149	TsAD(UAS)	Address to /UAS↑ Setup Time	20		[5]
150	ThAD(UAS)	Address to /UAS↑ Hold Time	20		[5]
151	TsAD(AS)	Address to /AS↑ Setup Time	20		[5]
152	ThAD(AS)	Address to /AS↑Hold Time	20		[5]
153	TsW(PC)	/WAIT to PCLK↓ Setup Time	10		[5]
154	ThW(PC)	/WAIT to PCLK↓ Hold Time	30		[5]
155	TsRDY(PC)	/READY to PCLK↓ Setup Time	10		[5]
156	ThRDY(PC)	/READY to PCLK↓ Hold Time	30		[5]
157	ThDW(PC)	Write Data to PCLK↑ Hold Time	0		[5]
158	TdAS(DSw)	/AS↑ to /DS↓ (Write) Delay	85		[5,9]
159	TsDW(DS)	Write Data to /DS↓ Setup Time	30		[5,6]
160	TwDSlw	/DS Low Width (Write)	90		[5,10]
161	ThDW(DS)	Write Data to /DS↑ Hold Time	30		[5, 7]
162	TdAS(WR)	/AS↑ to /WR↓ Delay	85		[5,9]
163	TsDW(WR)	Write Data to /WR↓ Setup Time	30		[5,6]
164	TwWRI	/WR Low Width	90		[5,10]
165	ThDW(WR)	Write Data to /WR↑ Hold Time	30		[5,7]
166	TdPC(WR)	PCLK↓ to /WR Delay		30	[5]
167	TdPC(BUSz)	PCLK↑ to Bus Float Delay		50	[5]

Notes:
[1] Direct address is A1/A//B or A0/SCC//DMA.
[2] The parameter applies only when /AS is not present.
[3] /Strobe is any of /DS, /RD, /WR or Pulsed /INTACK.
[4] Clock-cycle dependent, 2TcPC + TwPCI + TfPC + 55.
[5] Parameter applies only while ISCC is bus master.
[6] Clock-cycle dependent, TwPCh + TfPC - 15.
[7] Clock-cycle dependent, TwPC1 + TrPC - 15.
[8] Clock-cycle dependent, TcPC + TwPCh + TrPC - 10.
[9] Clock-cycle dependent, TcPC - 15.
[10] Clock-cycle dependent, TcPC - 10.

* Units in nanoseconds.

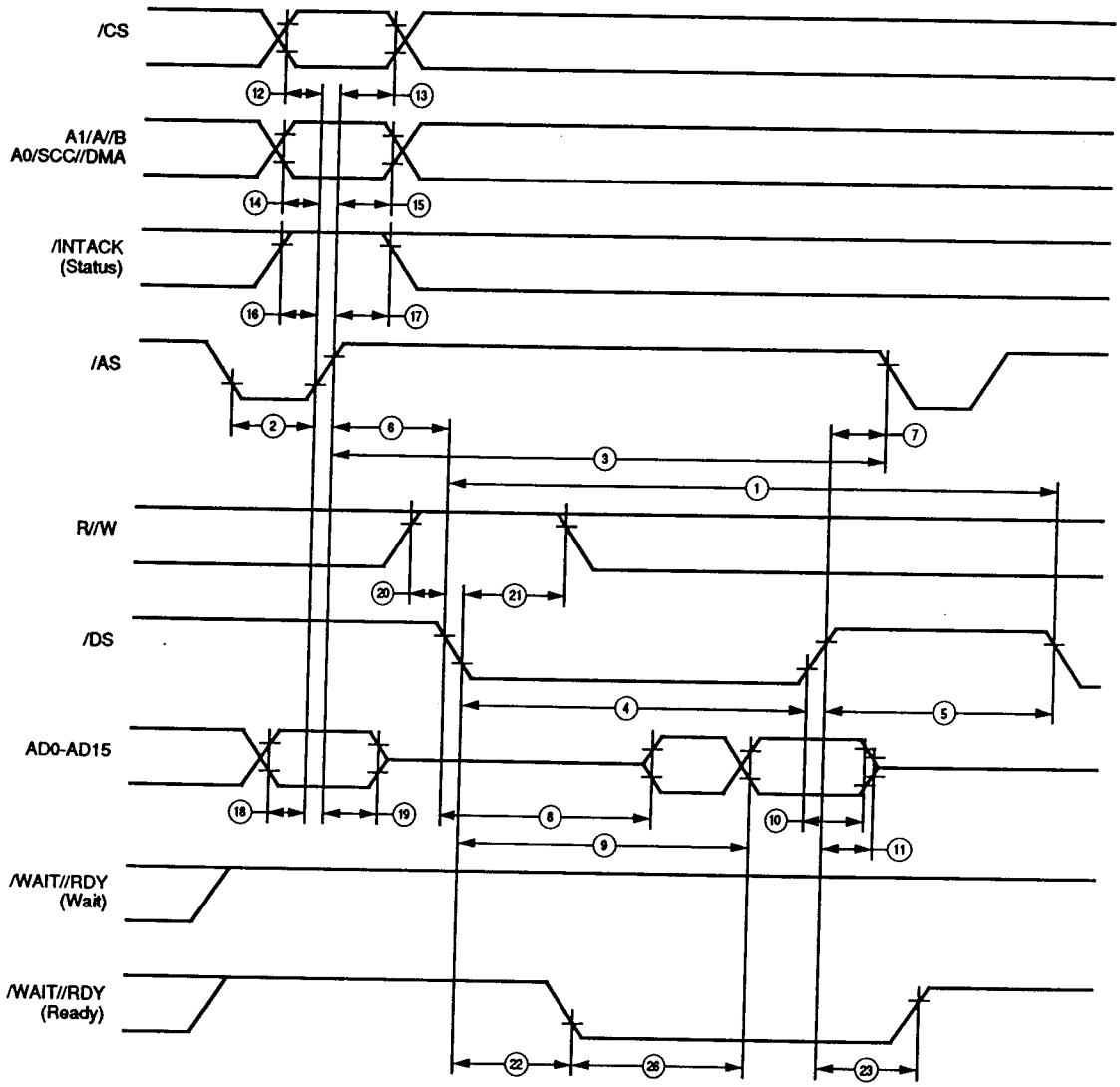


Figure 28. Multiplexed /DS Read Cycle

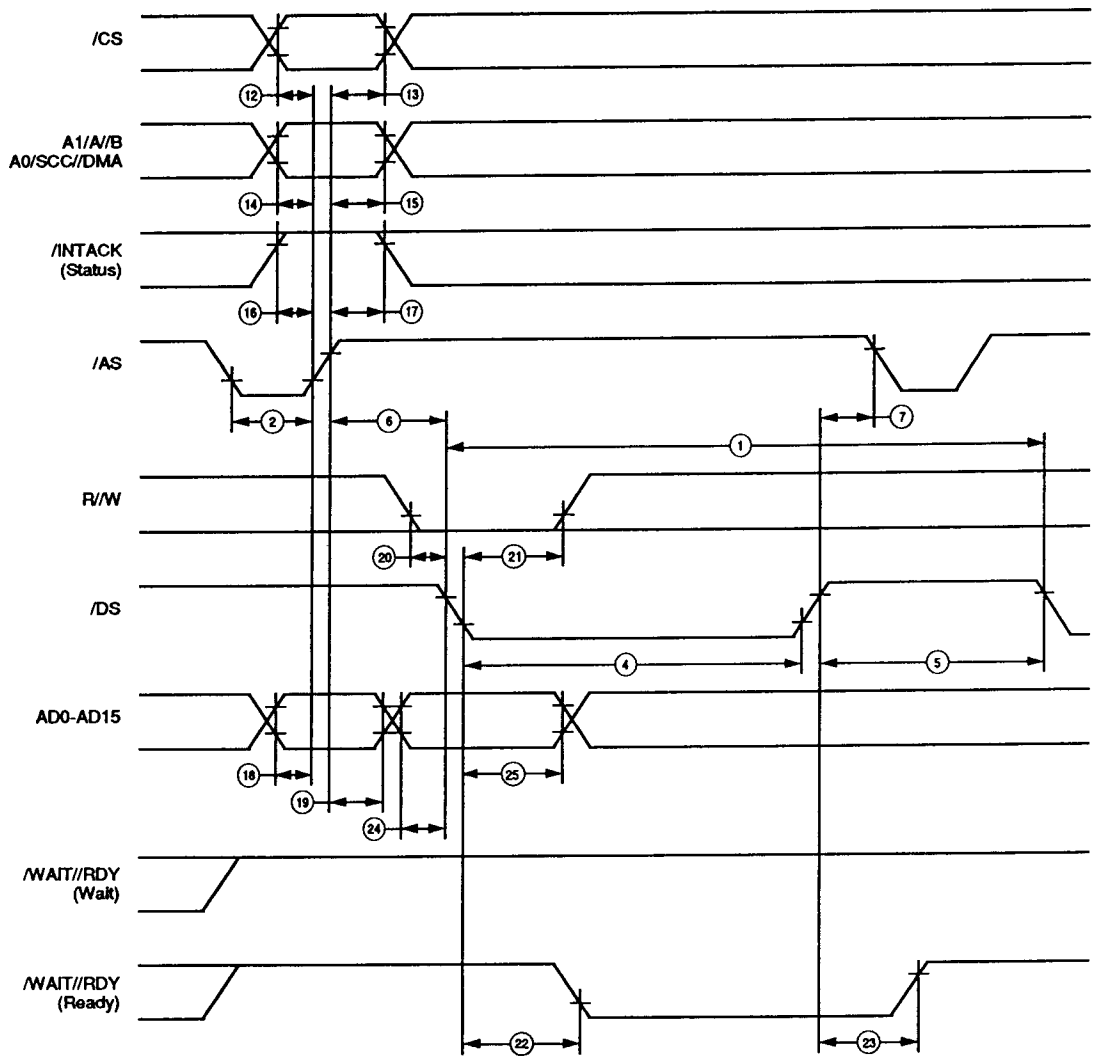


Figure 29. Multiplexed /DS Write Cycle

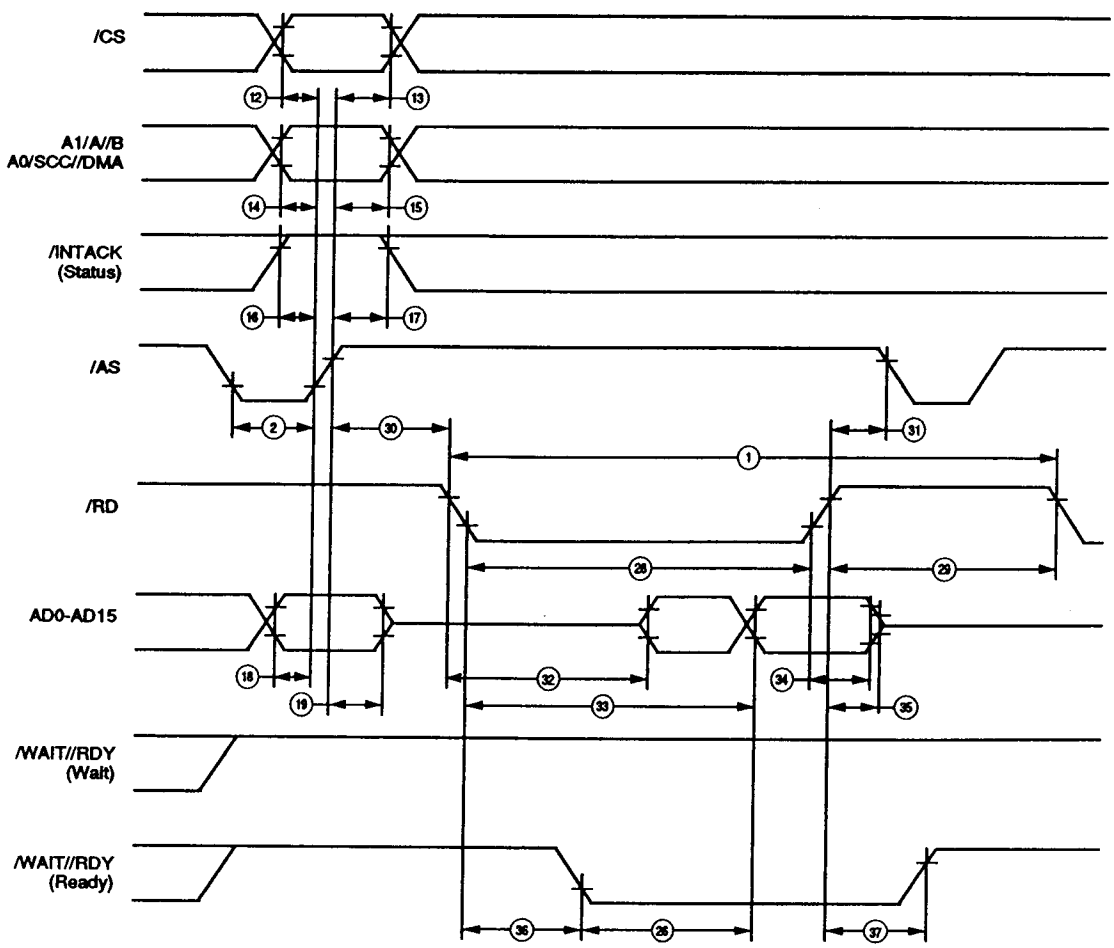


Figure 30. Multiplexed /RD Read Cycle

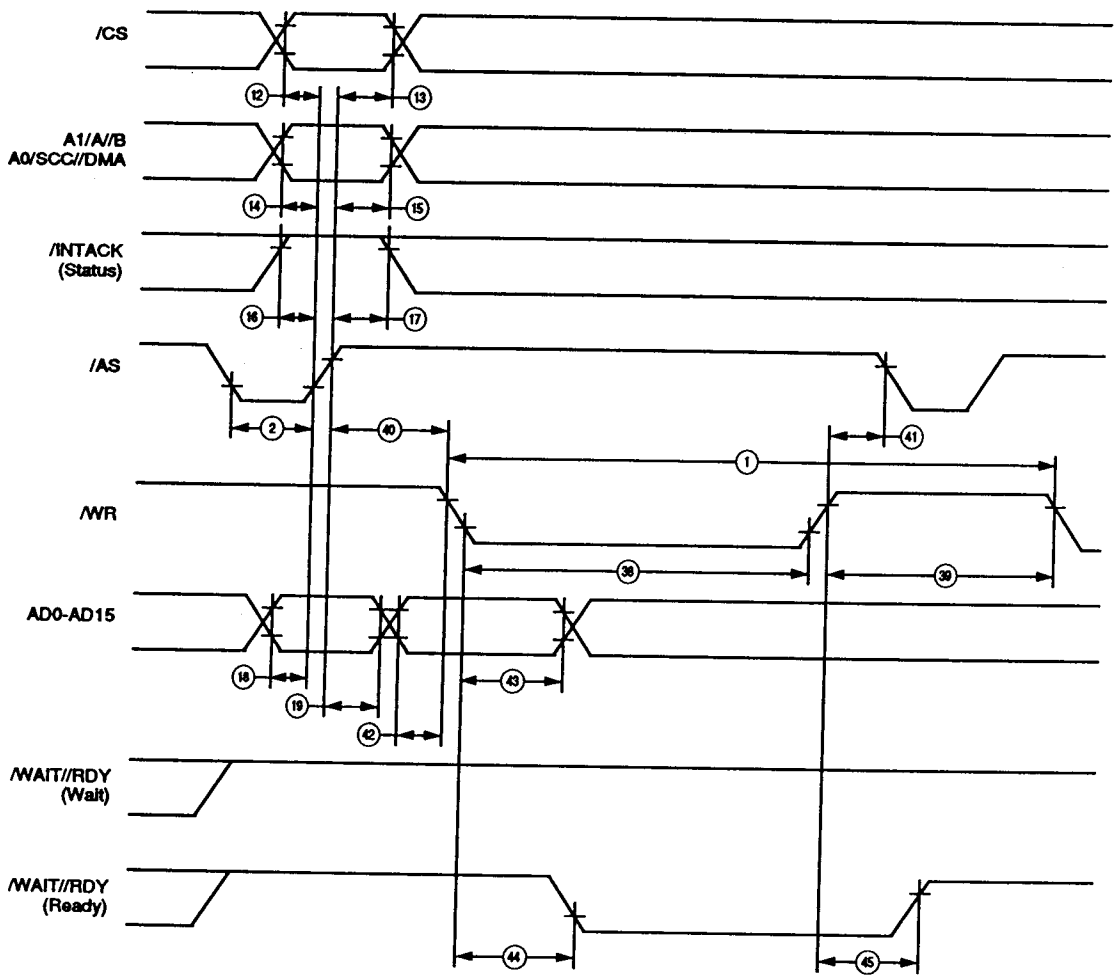


Figure 31. Multiplexed /WR Write Cycle

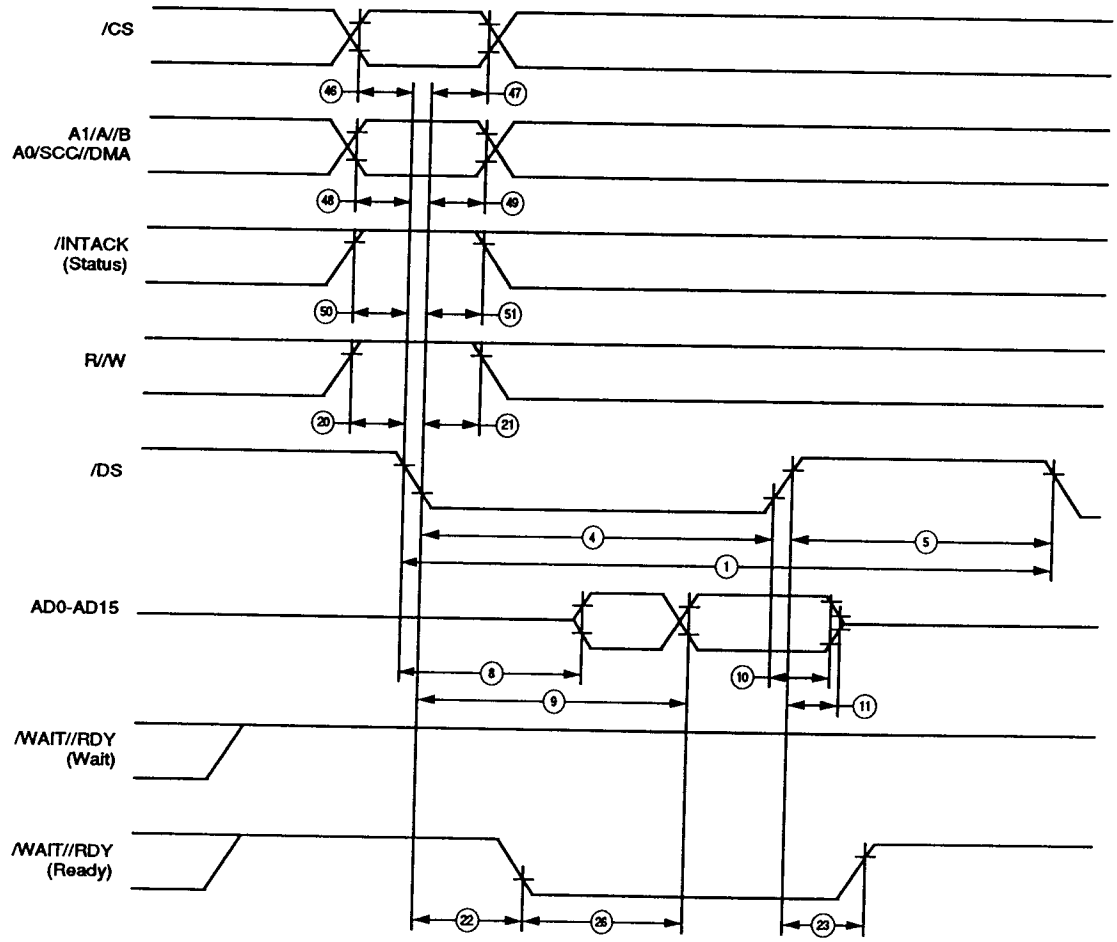


Figure 32. Non-multiplexed /DS Read Cycle

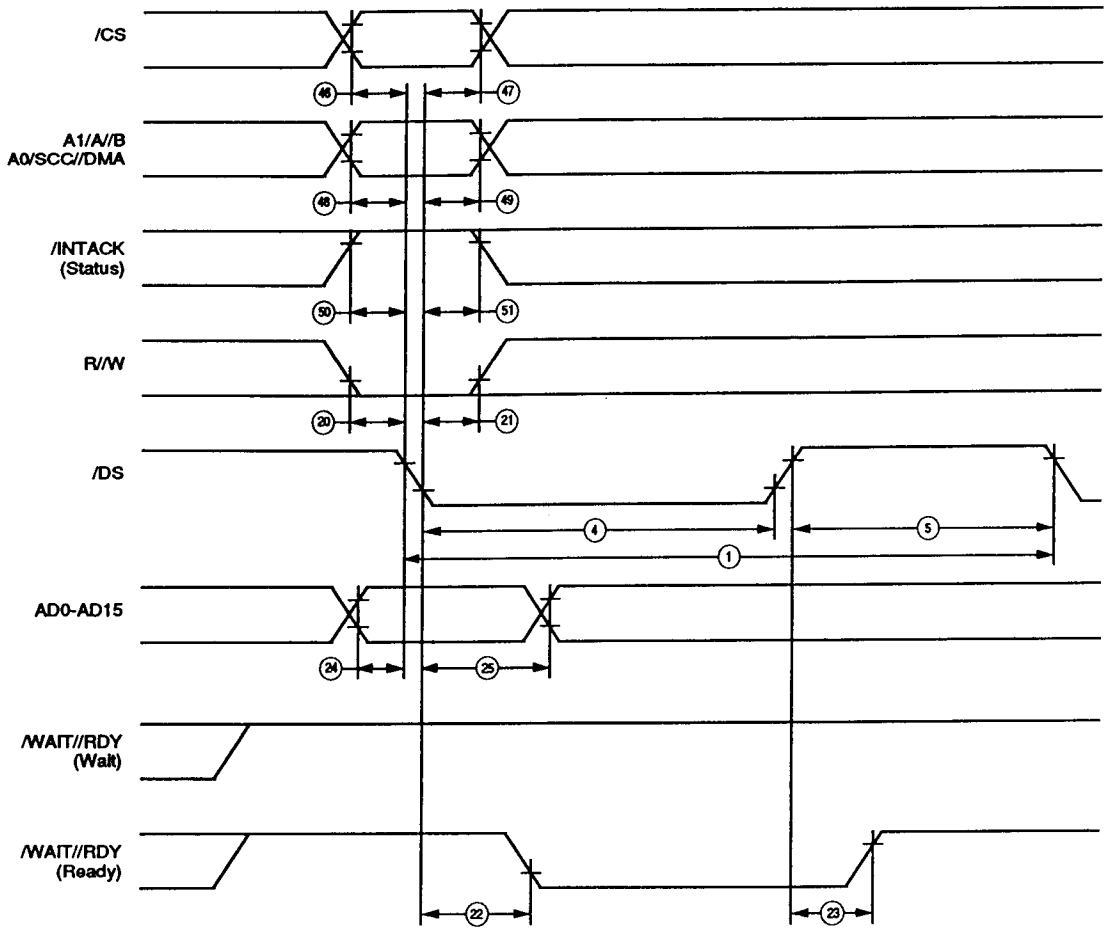


Figure 33. Non-multiplexed /DS Write Cycle

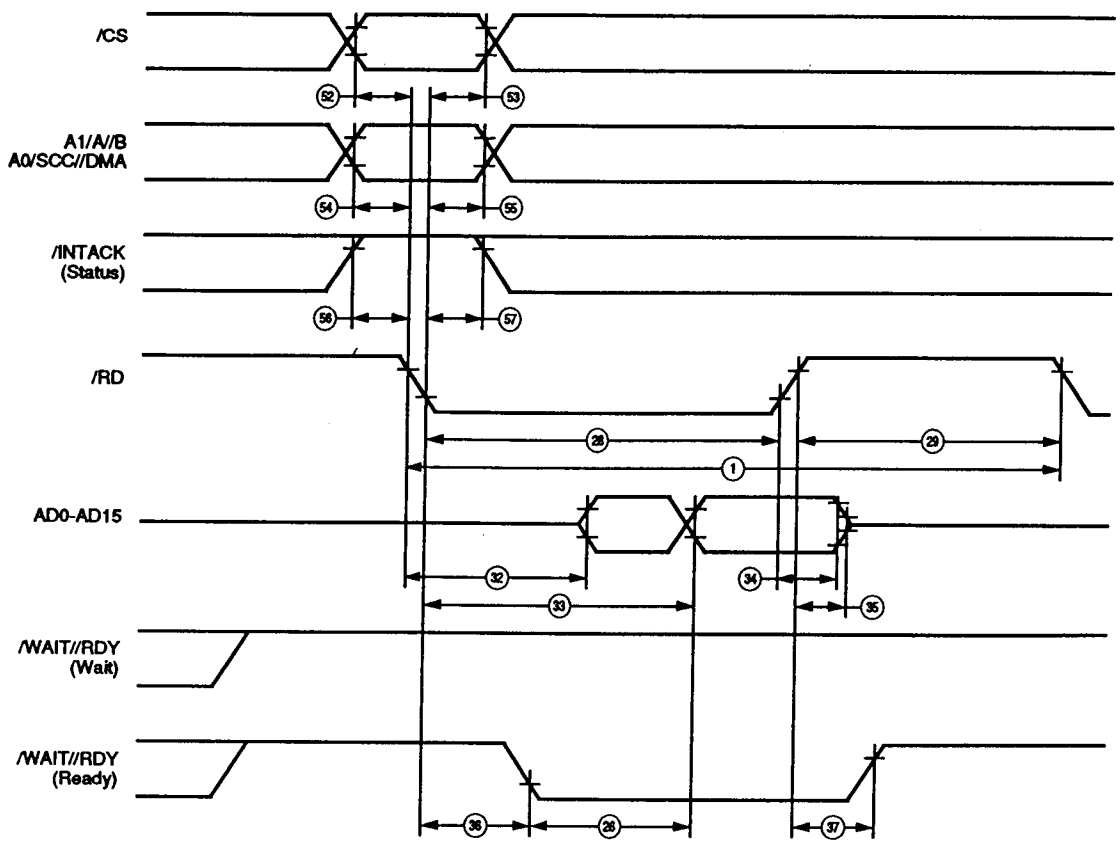


Figure 34. Non-multiplexed /RD Read Cycle

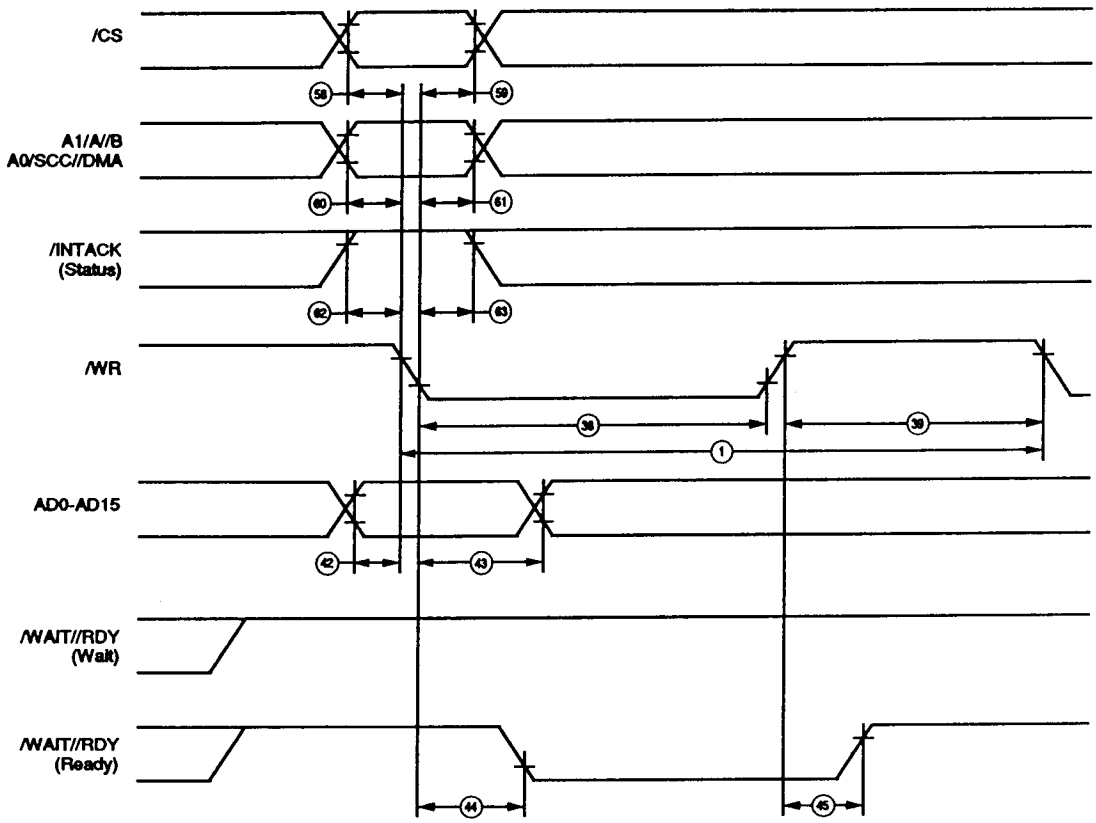


Figure 35. Non-multiplexed /WR Write Cycle

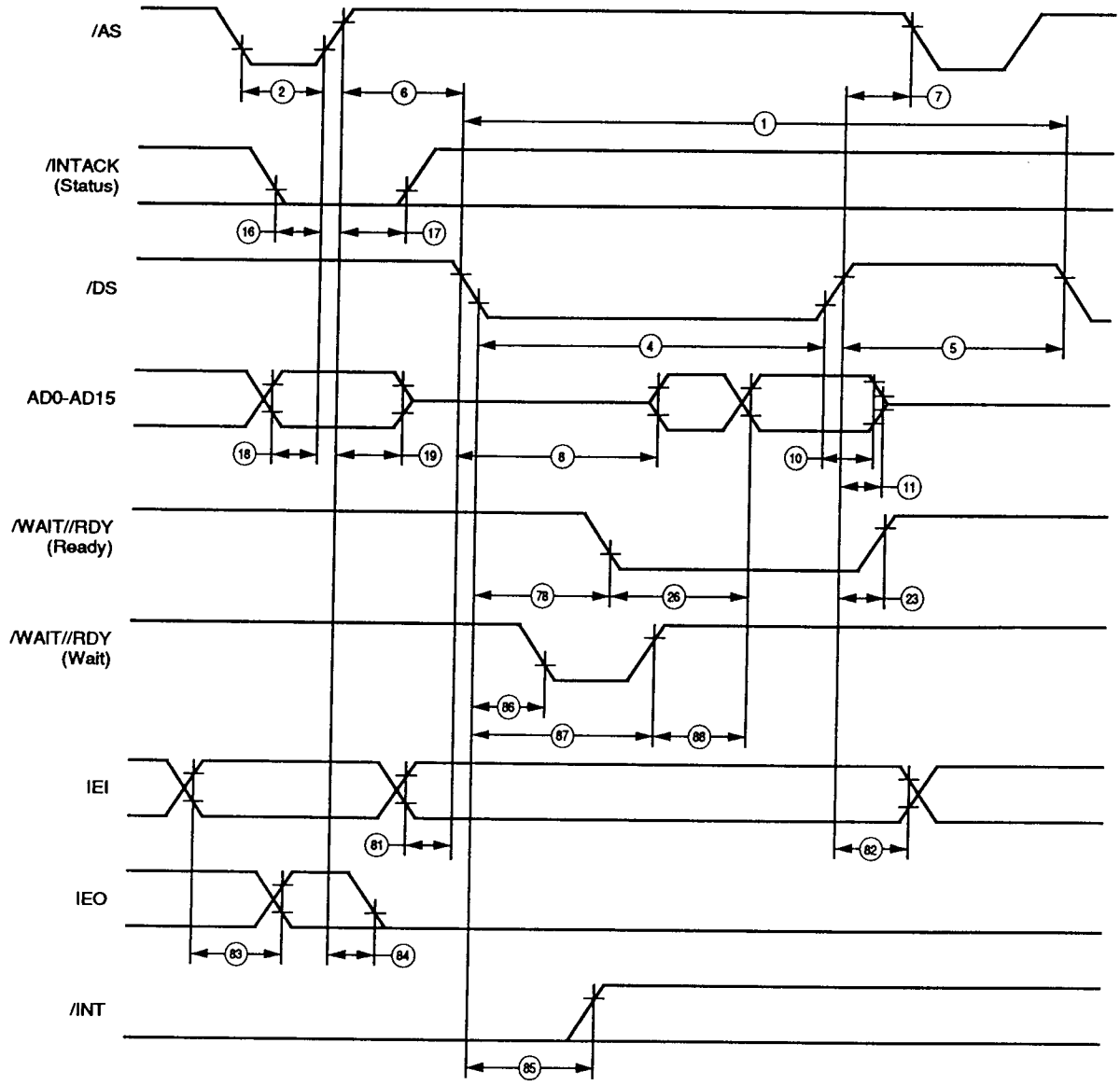


Figure 36. Multiplexed /DS Status INTACK Cycle

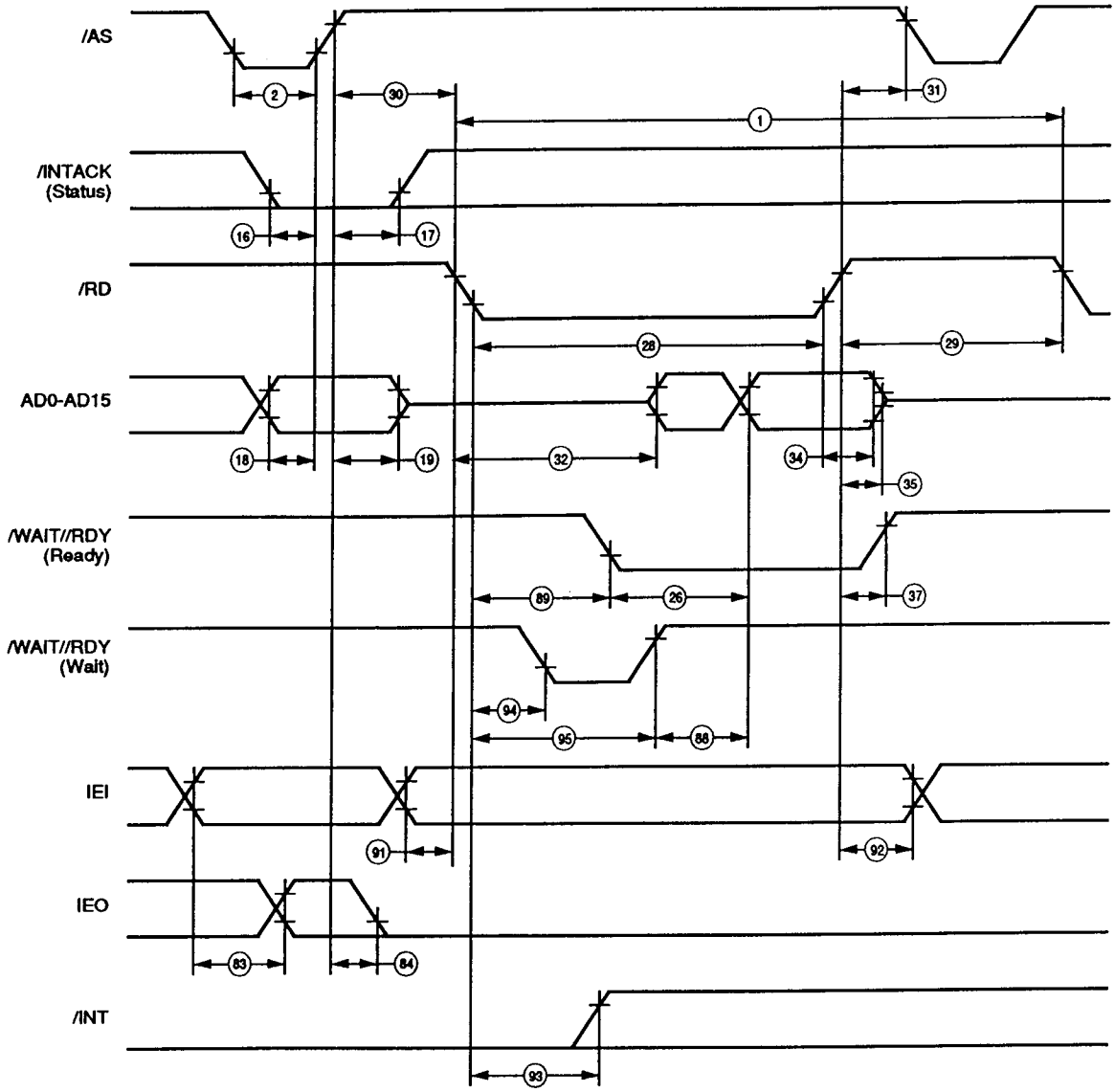


Figure 37. Multiplexed /RD Status INTACK Cycle

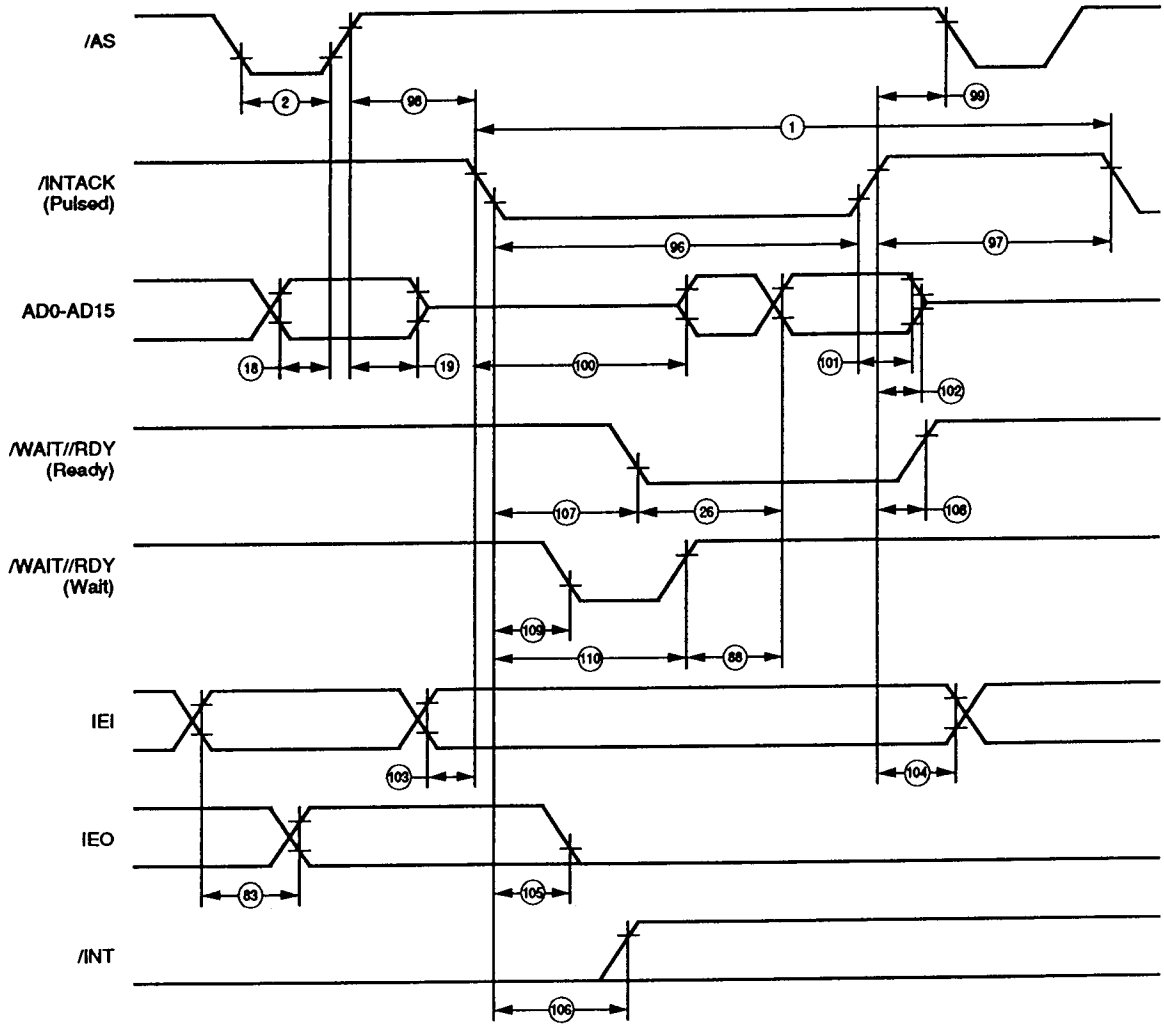


Figure 38. Multiplexed Pulsed INTACK Cycle

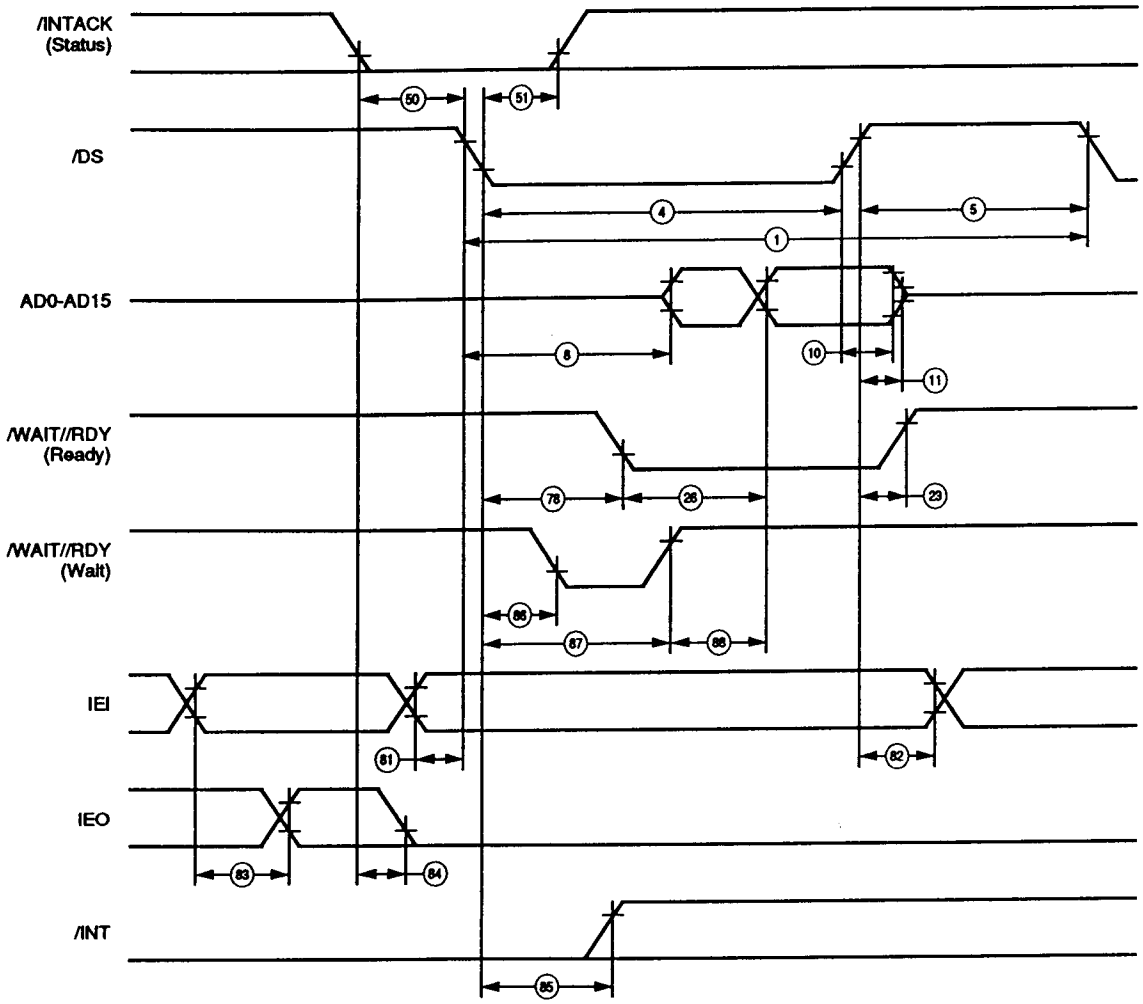


Figure 39. Non-multiplexed /DS INTACK Cycle

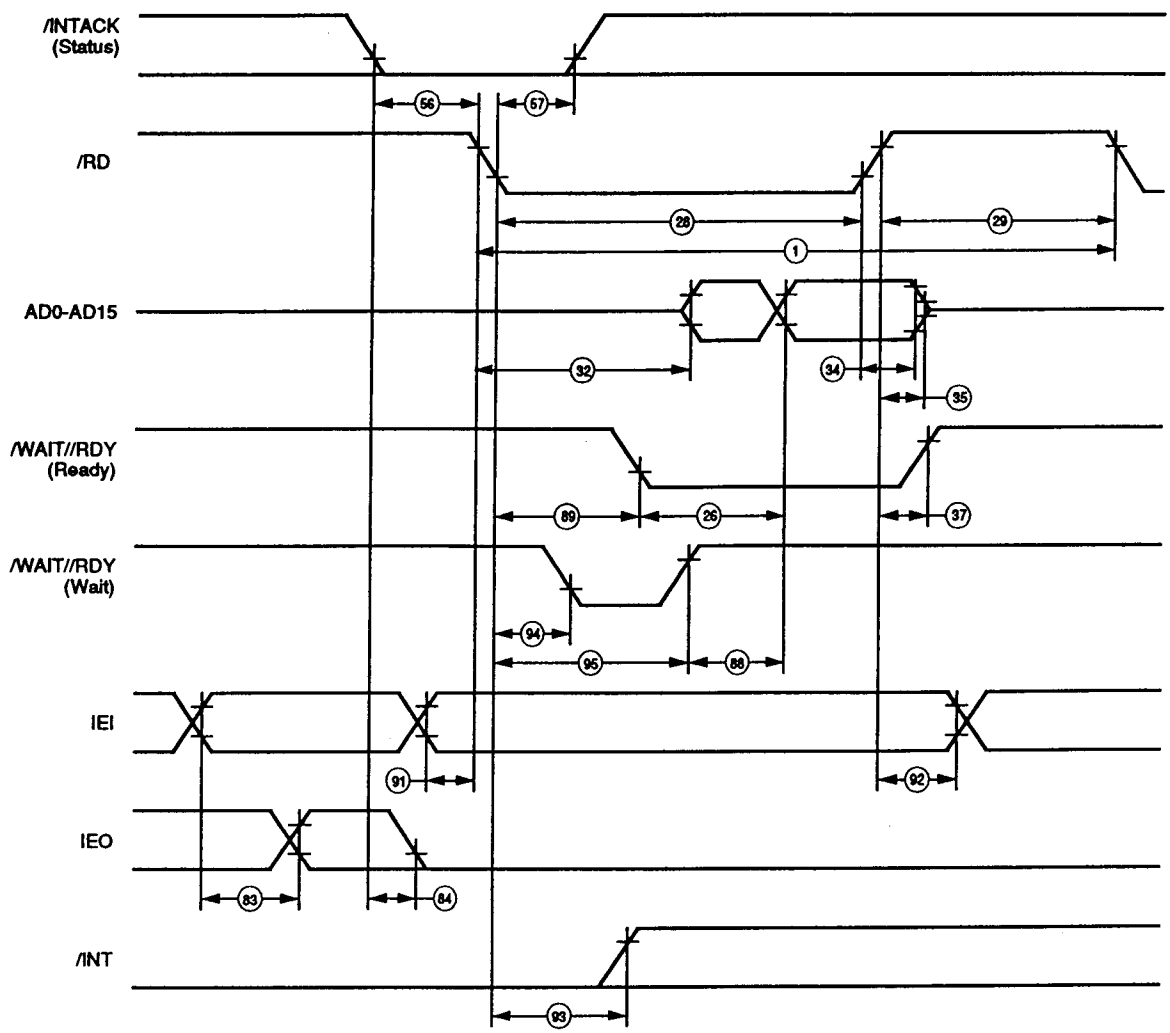


Figure 40. Non-multiplexed /RD Status INTACK Cycle

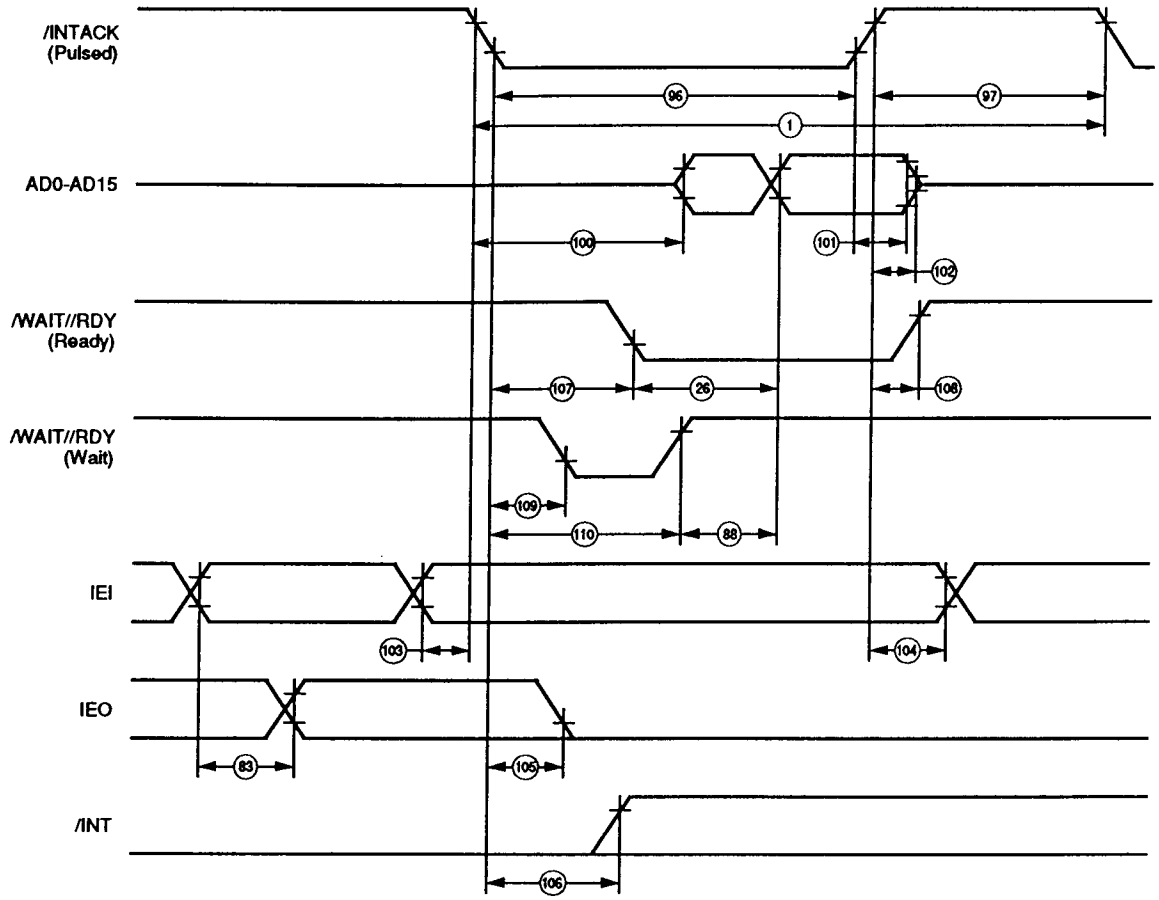


Figure 41. Non-multiplexed Pulsed INTACK Cycle

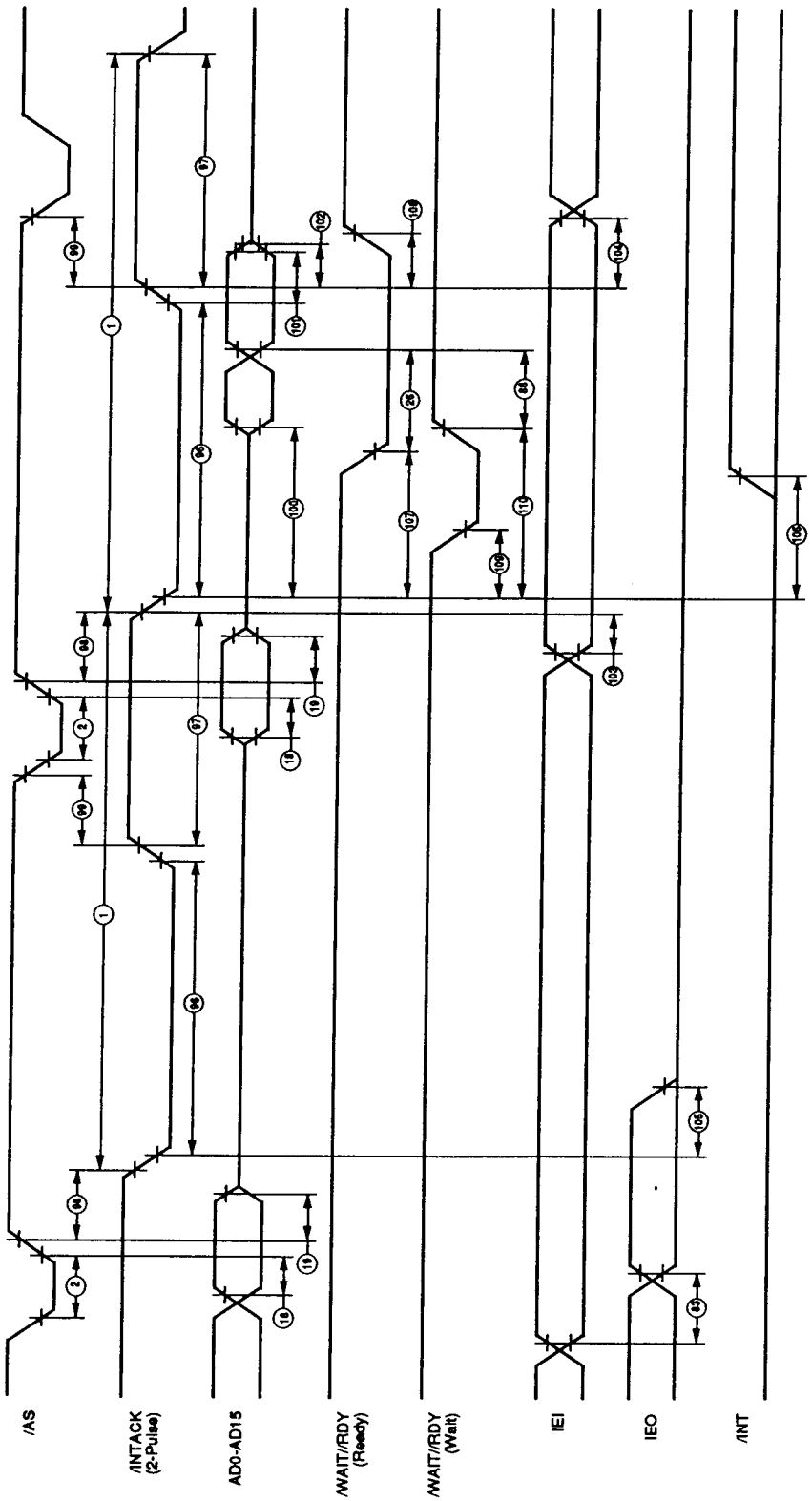


Figure 42. Multiplexed Double-Pulse INTACK Cycle

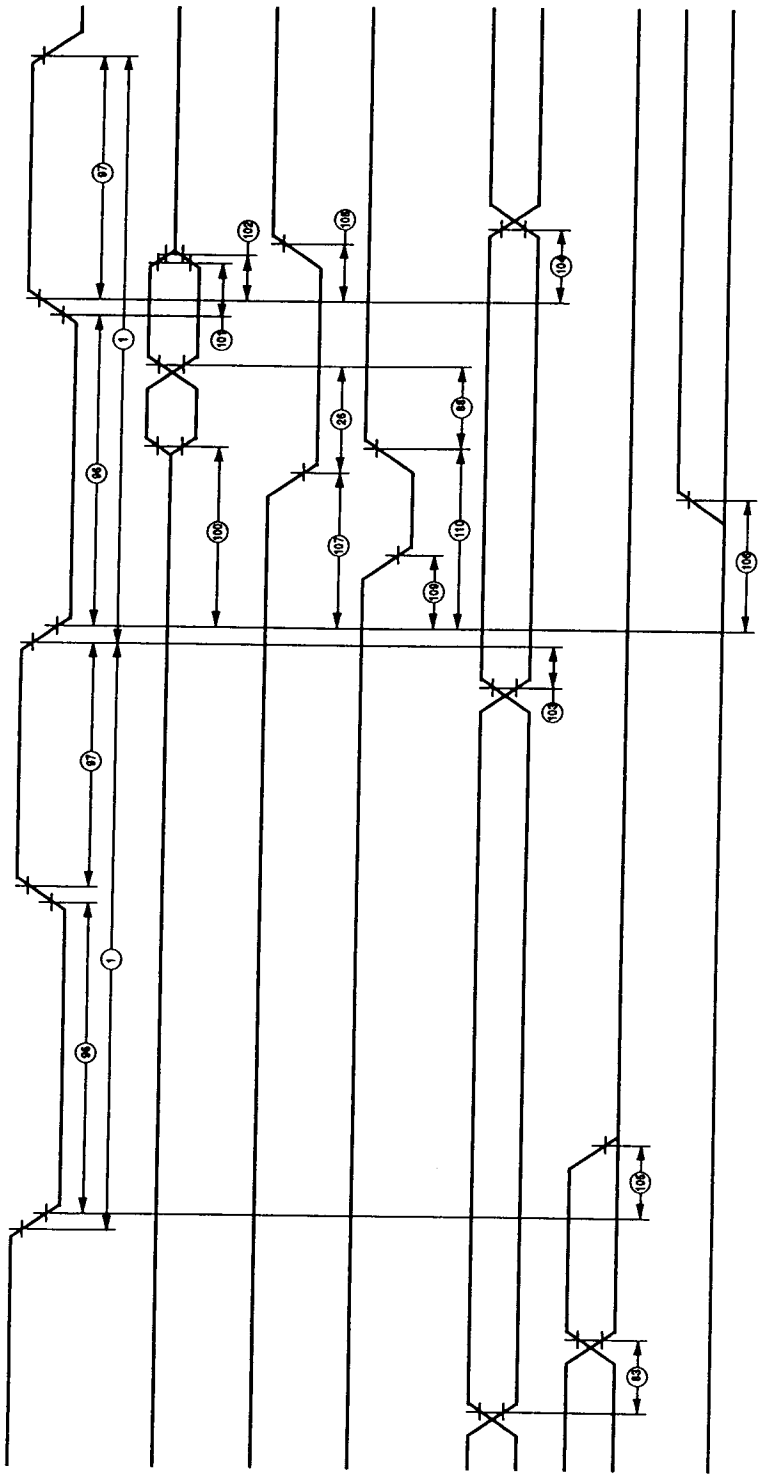


Figure 43. Non-multiplexed Double-Pulse INTACK Cycle

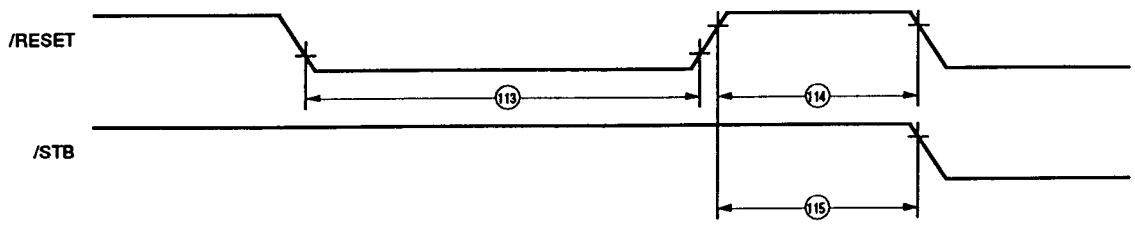


Figure 44. Reset

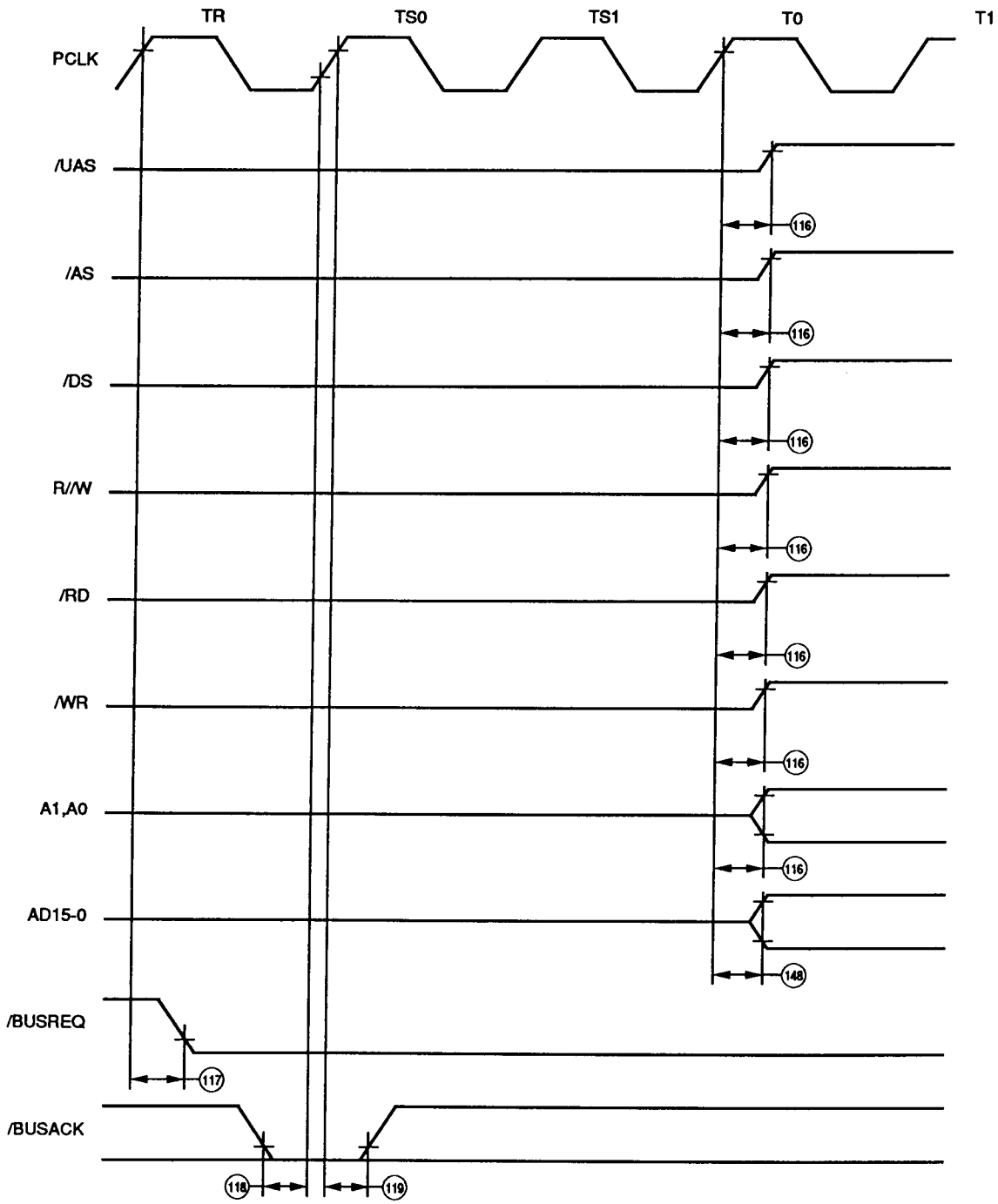


Figure 45. Z16C35 Start-up

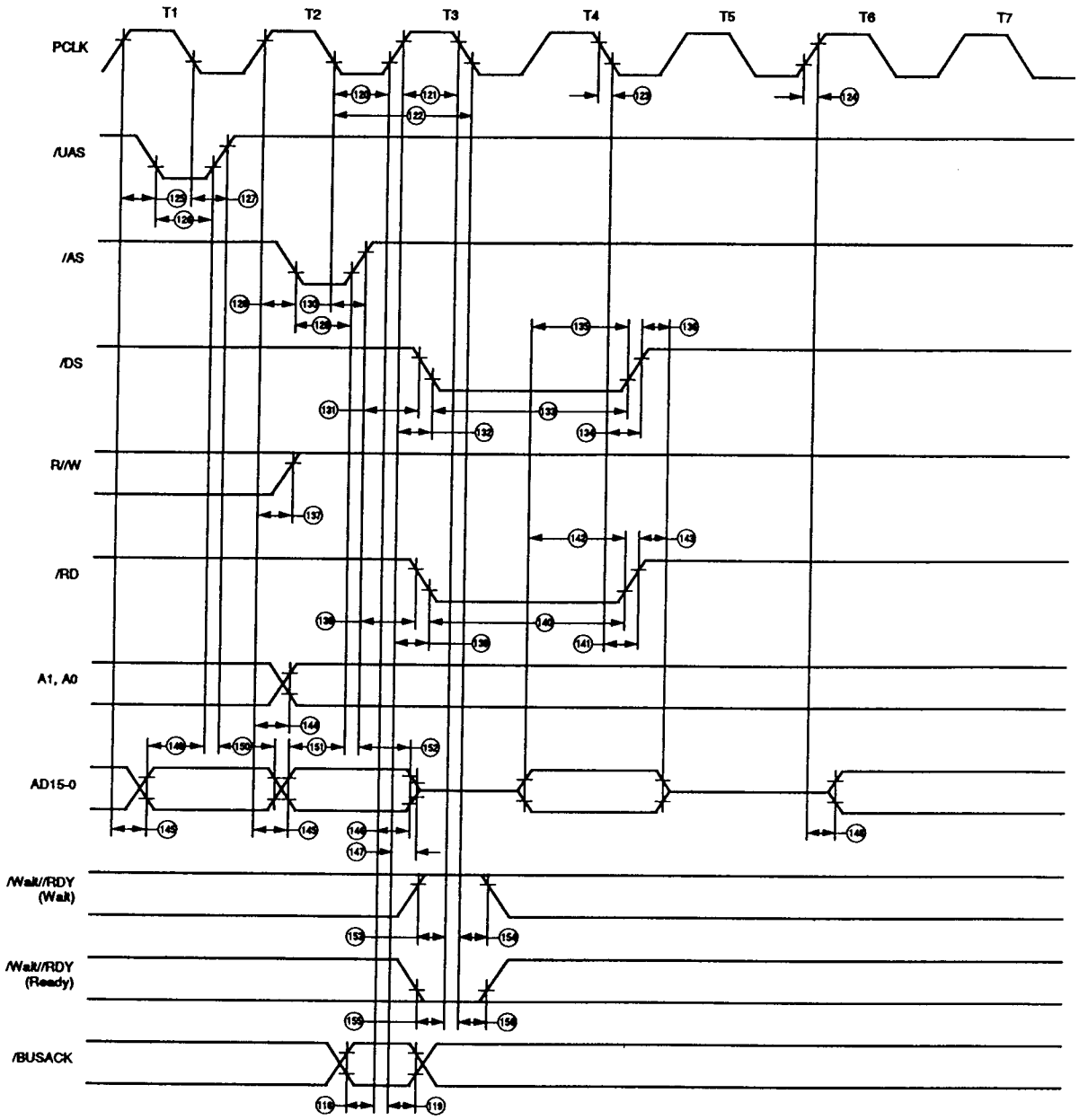


Figure 46. Z16C35 Memory Read

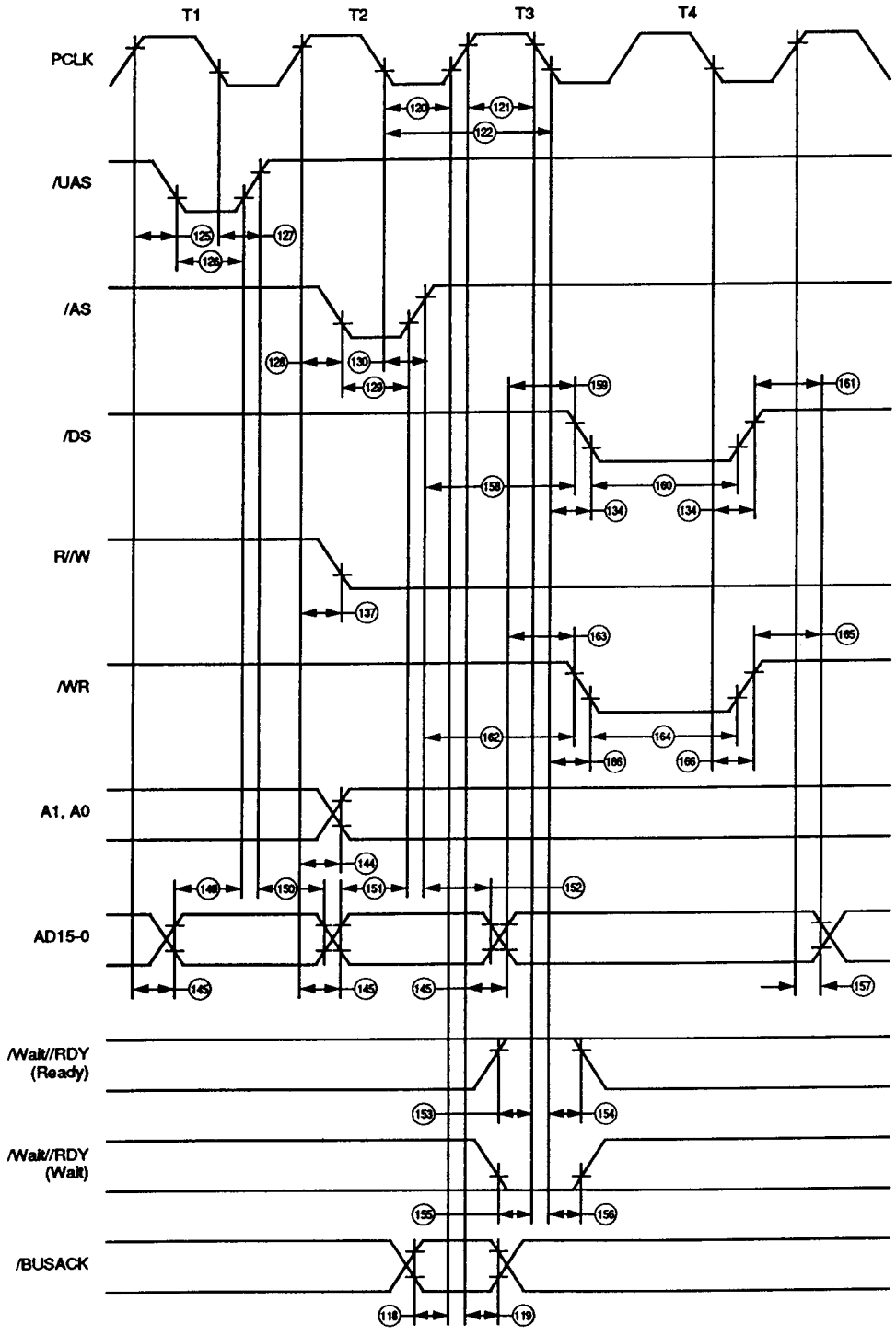


Figure 47. Z16C35 Memory Write

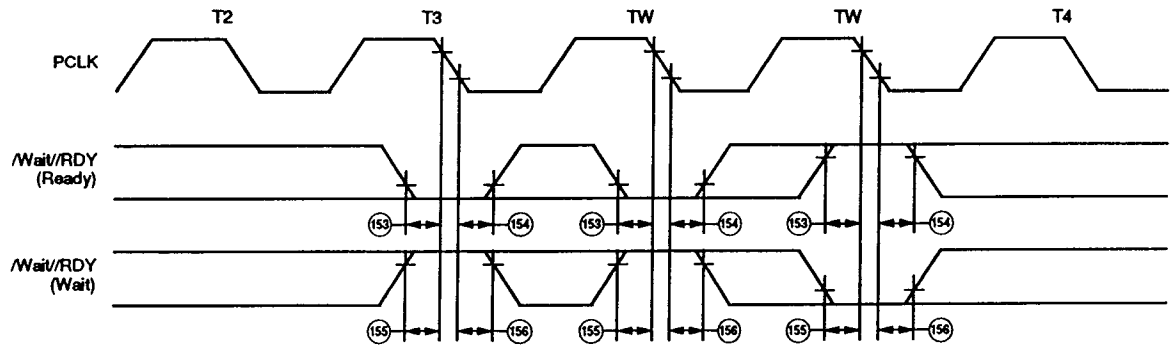


Figure 48. Wait and Ready Timing

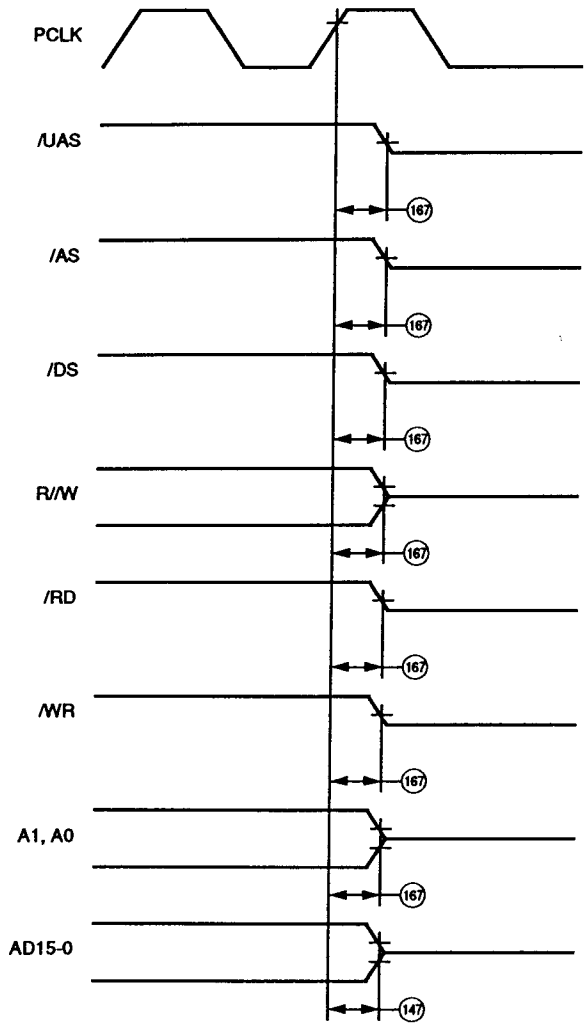


Figure 49. BUS Release

AC CHARACTERISTICS

No	Symbol	Parameter	10MHz * Min	Max	Notes
1	TsRXD(RXCr)	RxD to /RxC↑ Setup Time (x1 mode)	0		[1]
2	ThRXD(RXCr)	RxD to /RxC↑ Hold Time (x1 mode)	150		[1]
3	TsRXD(RXCf)	RxD to /RxC↓ Setup Time (x1 mode)	0		[1,5]
4	ThRXD(RXCf)	RxD to /RxC↓ Hold Time (x1 mode)	150		[1,5]
5	TsSY(RXC)	/SYNC to /RxC↑ Setup Time	-200		[1]
6	ThSY(RXC)	/SYNC to RxC↑ Hold Time	5TcPc		[1]
7	TsTXC(PC)	/TxC to PCLK Setup Time	0		[2,4]
8	TdTXCf(TXD)	/TxC↓ to TxD Delay (x1 mode)		150	[2]
9	TdTxCr(TXD)	/TxC↑ to TxD Delay (x1 mode)		150	[2,5]
10	TdTXD(TRX)	TxD to /TRXC Delay (Send Clock Echo)		200	
11	TwRTXh	/RTxC High Width	150		[6]
12	TwRTXl	/RTxC Low Width	150		[6]
13	TcRTX	/RTxC Cycle Time (RxD, TxD)	400		[6,7]
14	TcRTXX	Crystal Oscillator Period	100	1000	[3]
15	TwTRXh	/TRxC High Width	150		[6]
16	TwTRXl	/TRxC Low Width	150		[6]
17	TcTRX	/TRxC Cycle Time (RxD, TxD)	400		[6,7]
18	TwEXT	/DCD or /CTS Pulse Width	200		
19	TwSY	/SYNC Pulse Width	200		

* Units in nanoseconds.

Notes:
[1] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[2] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[3] Both /RTxC and /SYNC have 30 pf capacitors to ground connected to them.
[4] Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between /RxC and PCLK or/TxC and PCLK is required.
[5] Parameter applies only to FM encoding/decoding.
[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator requirements are identical to case PCLK requirements.
[7] The maximum receive or transmit data rate is one-fourth PCLK.

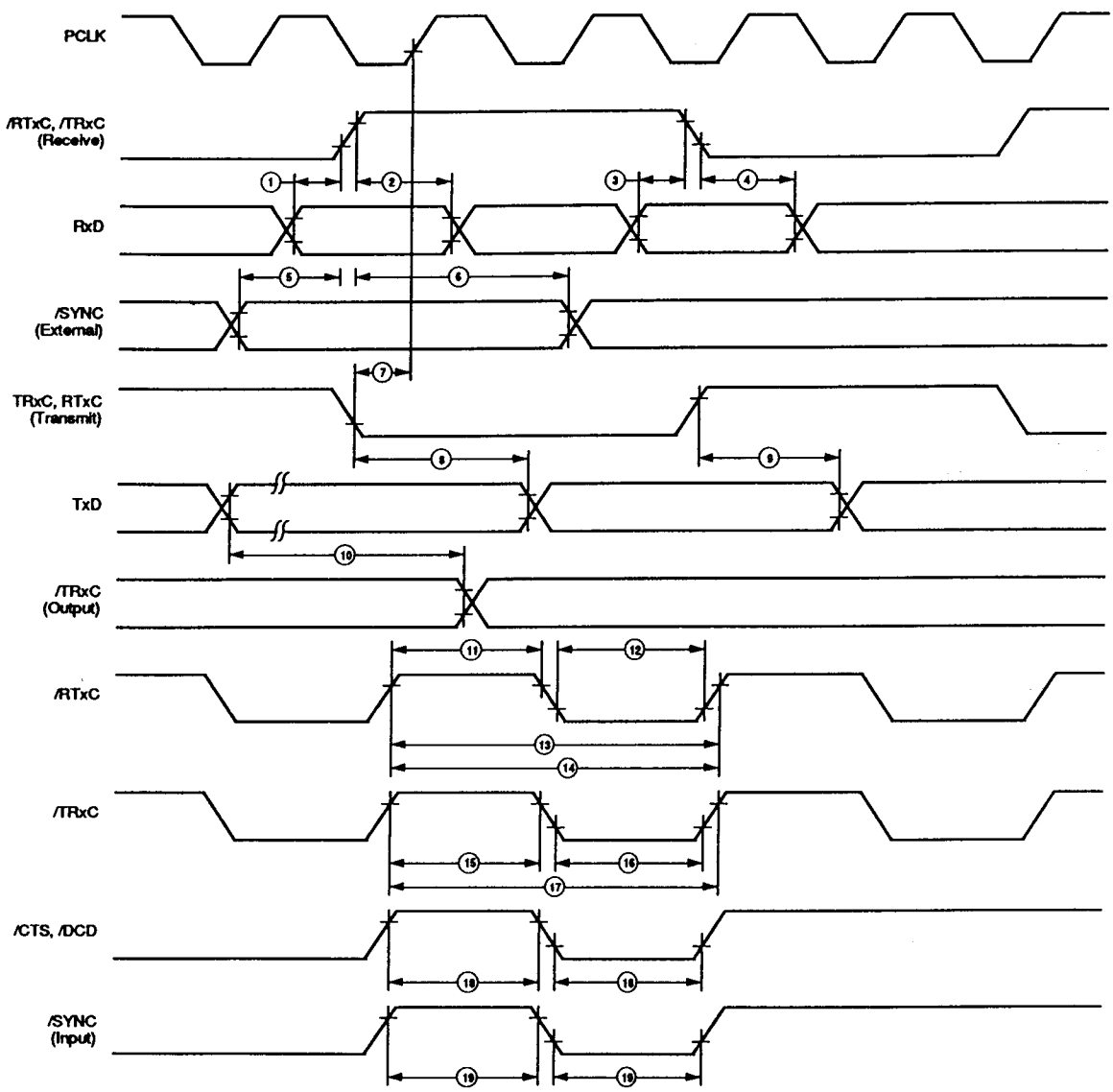


Figure 50. Z16C35 General Timing

AC CHARACTERISTICS
System Timing

No	Symbol	Parameter	10MHz Min	10MHz Max	Notes †
1	TdRXC(SY)	/RxC↑ to /SYNC	4	7	1
2	TdRXC(INT)	RxC↑ to /INT Valid Delay	10	16	1
3	TdTXC(INT)	/TxC↓ to /INT Valid Delay	6	10	
4	TdSY(INT)	/SYNC Transition to /INT Valid Delay	2	6	
5	TdEXT(INT)	/DCD or /CTS Transition to /INT Valid Delay	2	6	

† Units equal to TcPc.

Notes:
1. /RxC is /RTXC or /TRxC, whichever is supplying the receive clock.
2. /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

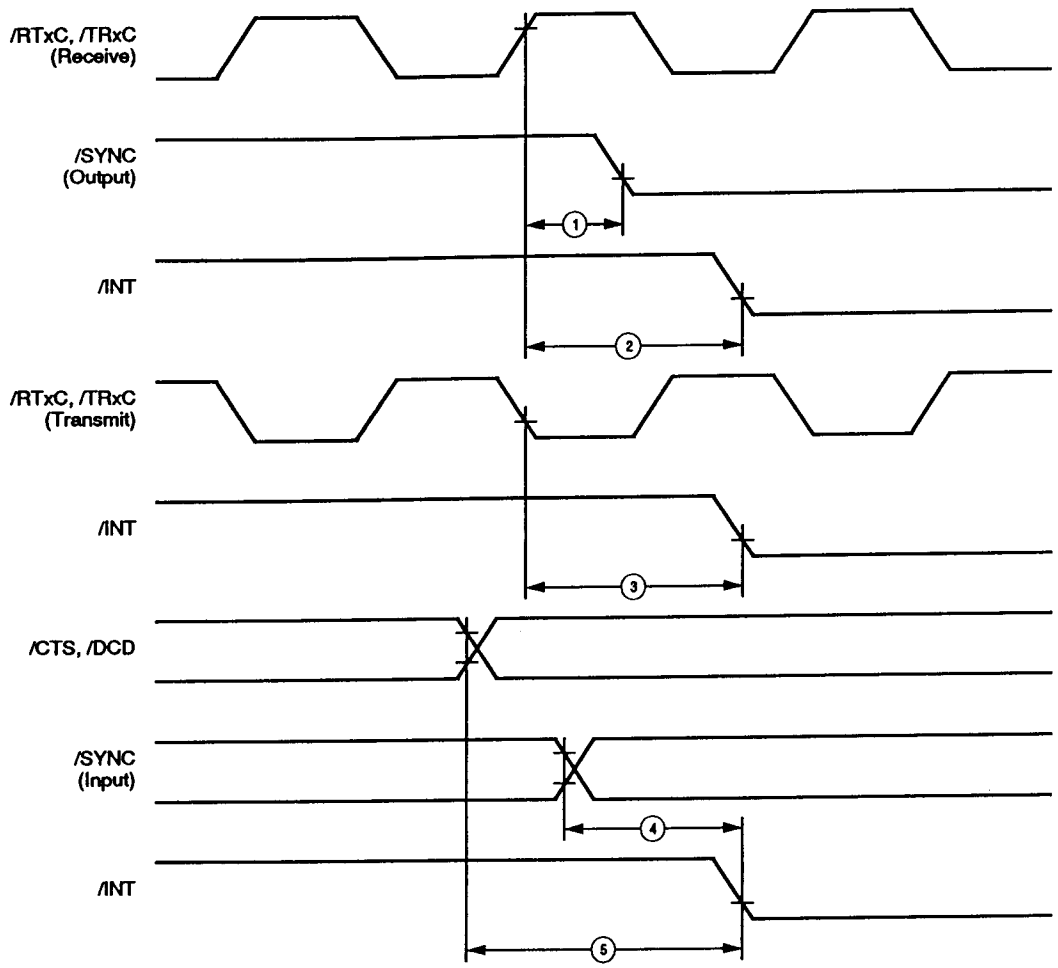
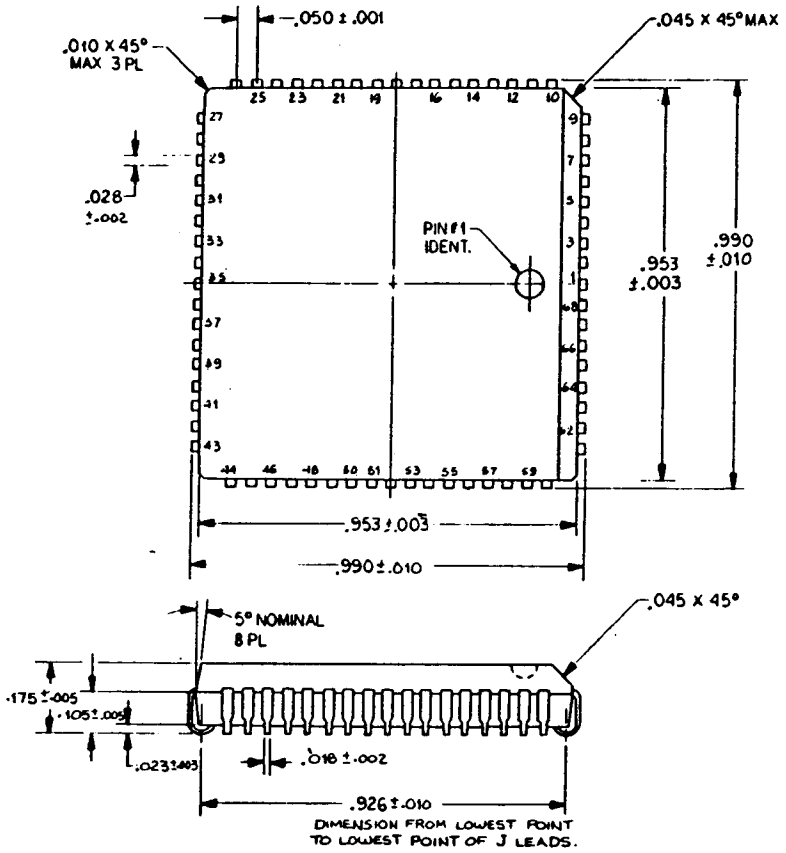


Figure 51. Z16C35 System Timing

PACKAGE INFORMATION



68-Lead Plastic Chip Carrier

ORDERING INFORMATION

Z16C35 ISCC 10 MHz
68-Pin PLCC
Z16C3510VSC

CODES

PACKAGE

Preferred
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack
G = Ceramic PGA (Pin Grid Array)
L = Ceramic LCC
Q = Ceramic Quad-in-Line

TEMPERATURE

Preferred
S = 0°C to +70°C

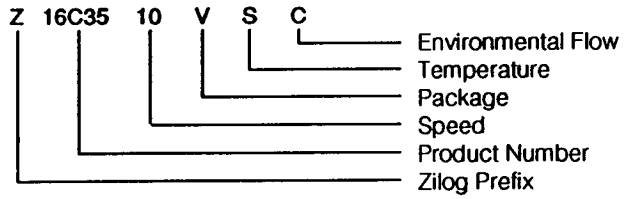
Longer Lead Time
E = -40°C to +85°C

ENVIRONMENTAL

Preferred
C = Plastic Standard
E = Hermetic Standard

Longer Lead Time
D = Plastic Stressed

Example:
Z16C3510VSC 16C35, 10MHz, Plastic PLCC, 0°C to 70°C, Plastic Standard Flow



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