



**THE DATASHEET OF  
Z0853006VSC**





**Z08030/8530**

***Serial Communications  
Controller***

**Customer Procurement Specification**

PS011301-0601



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DC Characteristic	Symbol	Parameter	Min	Max	Unit	Condition
		$V_{IH}$ Input High Voltage	2.0 <sup>a</sup>	$V_{CC} + 0.3^c$	V	
		$V_{IL}$ Input Low Voltage	-0.3 <sup>c</sup>	0.8 <sup>a</sup>	V	$I_{OL} = -250 \mu A$
		$V_{OH}$ Output High Voltage	2.4 <sup>b</sup>		V	$I_{OL} = +2.0 mA$
		$V_{OL}$ Output Low Voltage	0.4 <sup>b</sup>		V	$0.4 \leq V_{IH} \leq +2.4V$
		$I_{IL}$ Input Leakage	$\pm 10.00$		$\mu A$	$0.4 \leq V_{OH} \leq +2.4V$
		$I_{OL}$ Output Leakage	$\pm 10.00$		$\mu A$	
		$V_{CC}$ Supply Current	250		mA	

$V_{CC} = 5V \pm 5\%$  unless otherwise specified, over specified temperature range.

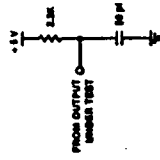
- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

### Standard Test Conditions

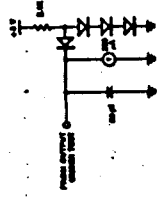
The DC characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $V_{CC} = 5V$
- $GND = 0V$
- $I_A$  as specified in Ordering Information
- All ac parameters assume a load capacitance of 50 pF max.



Open-Drain Test Load

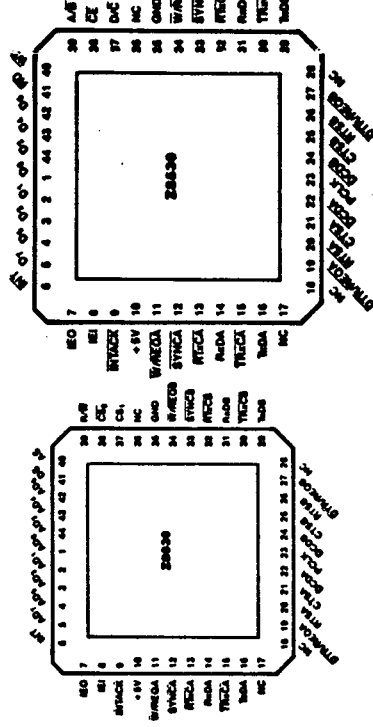


Standard Test Load

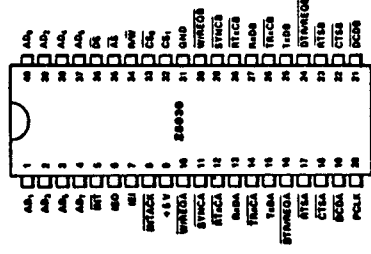
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Absolute Maximum Ratings  
 Voltages on all pins with respect to GND ..... -0.3V to +7.0V  
 Operating Ambient Temperature ..... See Ordering Information

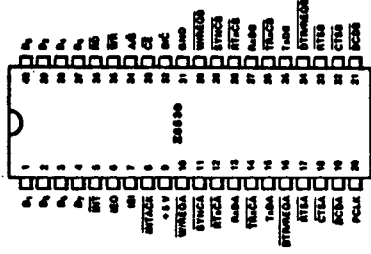
Storage Temperature ..... -65°C to +150°C  
 Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Chip Carrier Pin Assignments: Z8000



Chip Carrier Pin Assignments: Z8650



00-2817-02

DIP Pin Assignments: Z8000

DIP Pin Assignments: Z8650

50

Z8030 AC CHARACTERISTICS

Z8030 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes <sup>††</sup>
			Min	Max	Min	Max	Min	Max	
1	TwAS	AS Low Width	70 <sup>a</sup>		50 <sup>a</sup>		35 <sup>a</sup>		
2	TdS(AS)	DS ↑ to AS ↓ Delay	50 <sup>c</sup>		25 <sup>c</sup>		15 <sup>c</sup>		
3	TcSO(AS)	CS <sub>0</sub> to AS ↑ Setup Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		1
4	ThCS(AS)	CS <sub>0</sub> to AS ↑ Hold Time	60 <sup>a</sup>		40 <sup>a</sup>		30 <sup>a</sup>		1
5	TcS1(DS)	CS <sub>1</sub> to DS ↓ Setup Time	100 <sup>a</sup>		80 <sup>a</sup>		65 <sup>a</sup>		1
6	ThCS1(DS)	CS <sub>1</sub> to DS ↓ Hold Time	55 <sup>c</sup>		40 <sup>c</sup>		30 <sup>c</sup>		1
7	TtA(AS)	RTACK to AS ↑ Setup Time	10 <sup>c</sup>		10 <sup>c</sup>		10 <sup>c</sup>		
8	ThA(AS)	RTACK to AS ↑ Hold Time	250 <sup>a</sup>		200 <sup>a</sup>		150 <sup>a</sup>		
9	TtRW(DS)	RW (Read) to DS ↓ Setup Time	100 <sup>a</sup>		80 <sup>a</sup>		65 <sup>a</sup>		
10	ThRW(DS)	RW to DS ↓ Hold Time	55 <sup>a</sup>		40 <sup>a</sup>		35 <sup>a</sup>		
11	TtRW(DS)	RW (Write) to DS ↓ Setup Time	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
12	TcAS(DS)	AS ↑ to DS ↓ Delay	60 <sup>c</sup>		40 <sup>c</sup>		30 <sup>c</sup>		
13	TwCS	DS Low Width	240 <sup>a</sup>		200 <sup>a</sup>		150 <sup>a</sup>		
14	TtC	Valid Access Recovery Time	4TcPC <sup>a</sup>		4TcPC <sup>a</sup>		4TcPC <sup>a</sup>		2
15	TtA(AS)	Address to AS ↑ Setup Time	30 <sup>a</sup>		10 <sup>a</sup>		10 <sup>a</sup>		1
16	ThA(AS)	Address to AS ↑ Hold Time	50 <sup>a</sup>		30 <sup>a</sup>		25 <sup>a</sup>		1
17	TtDW(DS)	Write Data to DS ↓ Setup Time	30 <sup>a</sup>		20 <sup>a</sup>		15 <sup>a</sup>		
18	ThDW(DS)	Write Data to DS ↓ Hold Time	30 <sup>a</sup>		20 <sup>a</sup>		20 <sup>a</sup>		
19	TcDS(DA)	DS ↓ to Data Active Delay	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
20	TcDS(DR)	DS ↓ to Read Data Not Valid Delay	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		
21	TcDS(DR)	DS ↓ to Read Data Valid Delay	250 <sup>a</sup>		180 <sup>a</sup>		140 <sup>a</sup>		
22	TcAS(DR)	AS ↑ to Read Data Valid Delay	520 <sup>a</sup>		300 <sup>a</sup>		250 <sup>a</sup>		

NOTES:

1. Parameter does not apply to interrupt acknowledge transactions.
2. Parameter applies only between transactions involving the SCC.

<sup>††</sup>Times are preliminary and subject to change.

<sup>a</sup>Units in nanoseconds (ns).

<sup>a</sup> Tested

<sup>b</sup> Guaranteed by Design

<sup>c</sup> Guaranteed by Characterization

Number	Symbol	Parameter
23	TdS(DR)	DS ↑ to Read Data Post Delay
24	TtADR	Address Required Valid to Read Data Valid Delay
25	TtDS(W)	DS ↓ to Wait Valid Delay
26	TcDS(W)	DS ↓ to W/REO Not Valid Delay
27	TcDS(W)	DS ↓ to DTR/REO Not Valid Delay
28	TtDS(W)	AS ↑ to RT Valid Delay
29	TtDS(W)	AS ↑ to DS ↓ (Acknowledge) Delay
30	TtDS(W)	DS (Acknowledge) Low Width
31	TtDS(W)	DS ↓ (Acknowledge) to Read Data Valid Delay
32	TtDS(W)	DS ↓ (Acknowledge) Setup Time
33	TtDS(W)	DS ↓ (Acknowledge) Hold Time
34	TtDS(W)	DS ↓ (Acknowledge) Delay
35	TtDS(W)	AS ↑ to IEO Delay
36	TtDS(W)	DS ↓ (Acknowledge) to RT Inactive Delay
37	TtDS(W)	DS ↑ to AS ↓ Delay for No Reset
38	TtDS(W)	AS ↑ to DS ↓ Delay for No Reset
39	TtDS(W)	AS and DS Concurrent Low for Reset
40	TtDS(W)	PCLK Low Width
41	TtDS(W)	PCLK High Width
42	TtDS(W)	PCLK Cycle Time
43	TtDS(W)	PCLK Rise Time
44	TtDS(W)	PCLK Fall Time

NOTES:

1. Post delay is defined as the time required for a 5.0V change in the output signal.
2. Parameter is system dependent. For any Z80C in the delay chain, TdS(W) is defined as the delay chain, TdS(W) for the Z80C, and TdS(W) for the Z80C.
3. Parameter applies only to Z80C pulling I/O Lines at the beginning of the internal clock period.
4. Internal delay is defined as the time required for the Z80C to recognize the internal clock period.
5. Times are preliminary and subject to change. All timing references are to the Z80C.

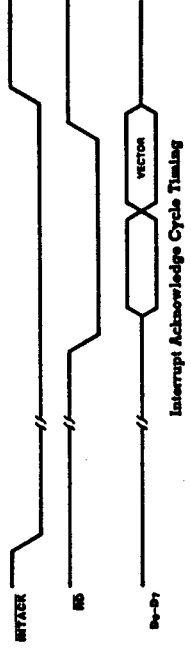
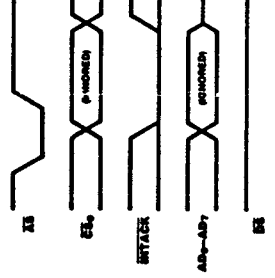
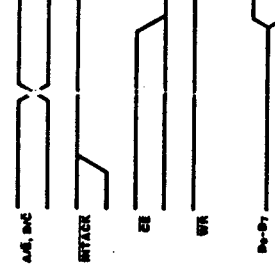
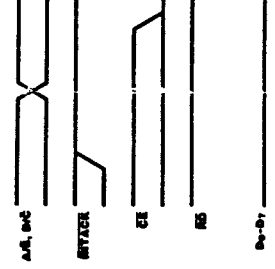
# Z80S3/Z80S30 SYSTEM TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes†
			Min	Max	Min	Max	Min	Max	
1	TdRXQ(REQ)	RXC ↓ to W/REQ Valid Delay	8	12	8	12	8	12	2
2	TdRXQ(W)	RXC ↑ to Wait Inactive Delay	8	14	8	14	8	14	1,2
3	TdRXQ(SY)	RXC ↑ to SYNC Valid Delay	4	7	4	7	4	7	2
4a.	TdRXQ(INT), Z80S30	RXC ↑ to INT Valid Delay	10	16	10	16	10	16	1,2
4b.	TdRXQ(INT), Z8030		8	12	8	12	8	12	1,2
			+2	+3	+2	+3	+2	+3	4
5	TdTXQ(REQ)	TRC ↓ to W/REQ Valid Delay	5	8	5	8	5	8	3
6	TdTXQ(W)	TRC ↓ to Wait Inactive Delay	5	11	5	11	5	11	1,3
7	TdTXQ(DRC)	TRC ↓ DTR/REQ Valid Delay	4	7	4	7	4	7	3
8a.	TdTXQ(INT), Z80S30	TRC ↓ to INT Valid Delay	6	10	6	10	6	10	1,3
8b.	TdTXQ(INT), Z8030		4	6	4	6	4	6	1,3
			+2	+3	+2	+3	+2	+3	4
9a.	TdSY(INT), Z80S30	SYNC Transition to INT Valid Delay	2	6	2	6	2	6	1
9b.	TdSY(INT), Z8030		2	3	2	3	2	3	1,4
10a.	TdEXT(INT), Z80S30	DOD or CTS Transition to INT Valid Delay	2	6	2	6	2	6	1
10b.	TdEXT(INT), Z8030		2	3	2	3	2	3	1,4

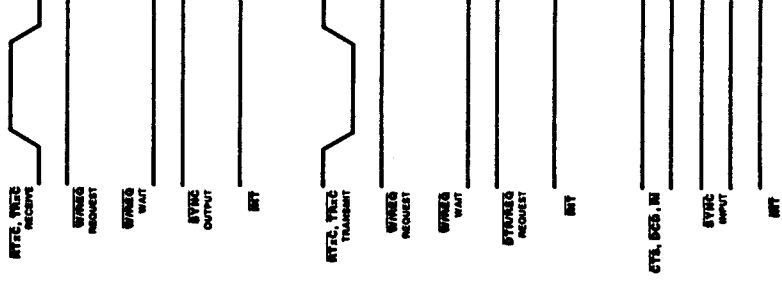
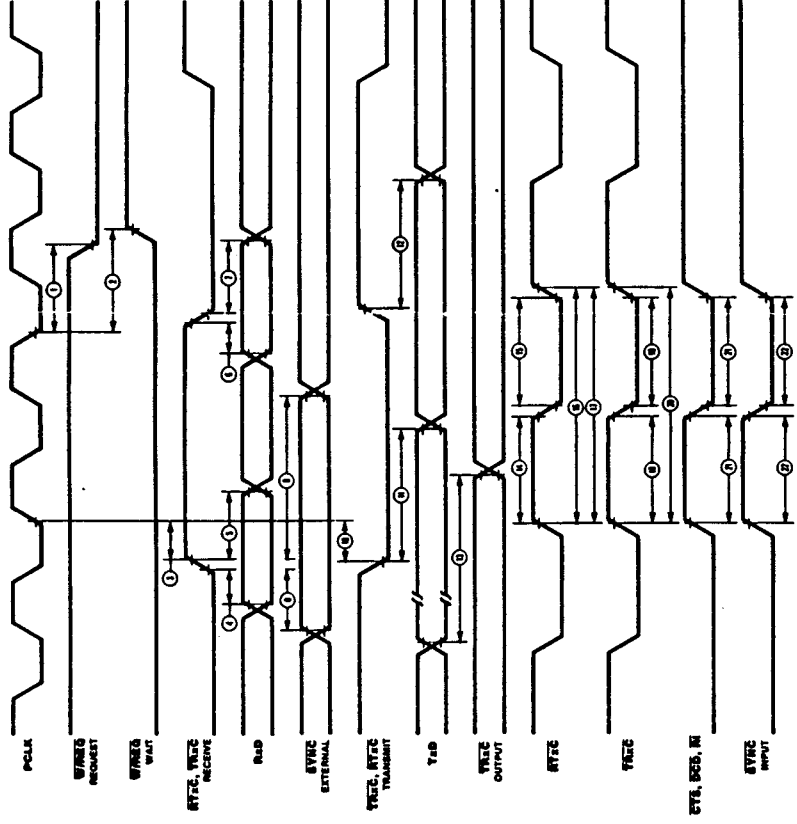
**NOTES:**

- Open-drain output, measured with open-drain test load
- RxC is RTRxC or TRxC, whichever is supplying the receive clock.
- TRc is TRRxC or RTxC, whichever is supplying the transmit clock.
- Units equal to NS.

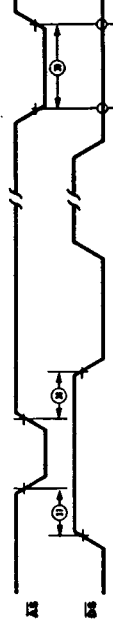
\*Timings are preliminary and subject to change.  
†Units equal to TdPC.



**General  
Timing**



**Reset  
Timing  
Z8030**



Z8530 AC CHARACTERISTICS

Z8530 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes <sup>††</sup>
			Min	Max	Min	Max	Min	Max	
1	TwPCI	PCLK Low Width	105 <sup>a</sup>	2000 <sup>a</sup>	70 <sup>a</sup>	1000 <sup>a</sup>	50 <sup>a</sup>	1000 <sup>a</sup>	
2	TwPCh	PCLK High Width	105 <sup>a</sup>	2000 <sup>a</sup>	70 <sup>a</sup>	1000 <sup>a</sup>	50 <sup>c</sup>	1000 <sup>a</sup>	
3	TIPC	PCLK Fall Time		20 <sup>a</sup>		10 <sup>a</sup>		10 <sup>a</sup>	
4	TrPC	PCLK Rise Time		20 <sup>a</sup>		10 <sup>a</sup>		10 <sup>a</sup>	
5	TcPC	PCLK Cycle Time	250 <sup>a</sup>	4000 <sup>a</sup>	165 <sup>a</sup>	2000 <sup>a</sup>	125 <sup>a</sup>	2000 <sup>a</sup>	
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80 <sup>a</sup>		80 <sup>a</sup>		70 <sup>a</sup>		
7	TtA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80 <sup>a</sup>		80 <sup>a</sup>		70 <sup>a</sup>		
9	TtA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
10	TsA(PC)	INTACK to PCLK ↑ Setup Time	10 <sup>a</sup>		10 <sup>a</sup>		10 <sup>a</sup>		
11	TsA(WR)	INTACK to $\overline{WR}$ ↓ Setup Time	200 <sup>a</sup>		160 <sup>a</sup>		145 <sup>a</sup>		1
12	TtA(WR)	INTACK to $\overline{WR}$ ↑ Hold Time	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
13	TsA(RD)	INTACK to $\overline{RD}$ ↓ Setup Time	200 <sup>a</sup>		160 <sup>a</sup>		145 <sup>a</sup>		1
14	TtA(RD)	INTACK to $\overline{RD}$ ↑ Hold Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		
15	TtA(PC)	INTACK to PCLK ↑ Hold Time	100 <sup>a</sup>		100 <sup>a</sup>		85 <sup>a</sup>		
16	TsCE(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		
17	TtCE(WR)	$\overline{CE}$ High to $\overline{WR}$ ↑ Hold Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		
18	TsCE(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100 <sup>a</sup>		70 <sup>a</sup>		60 <sup>a</sup>		
19	TsCE(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		1
20	TtCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		1
21	TsCE(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time	100 <sup>a</sup>		70 <sup>a</sup>		60 <sup>a</sup>		1
22	TwRD	$\overline{RD}$ Low Width	390 <sup>a</sup>		200 <sup>a</sup>		150 <sup>a</sup>		1
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0 <sup>c</sup>		0 <sup>c</sup>		0 <sup>c</sup>		
24	TdRD(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0 <sup>a</sup>		0 <sup>a</sup>		0 <sup>a</sup>		
25	TdRD(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay	250 <sup>a</sup>		180 <sup>a</sup>		140 <sup>a</sup>		
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay	70 <sup>a</sup>		45 <sup>a</sup>		40 <sup>a</sup>		2

NOTES:

1. Parameter does not apply to Interrupt Acknowledge transactions.
  2. Float delay is defined as the time required for a ±0.5V change at the output with a maximum dc load and minimum ac load.
- <sup>a</sup>Timings are preliminary and subject to change.  
<sup>†</sup>Units in nanoseconds (ns).

Number	Symbol	Parameter
27	TsA(DR)	Address Required Valid to Valid Delay <sup>†</sup>
28	TtWR	$\overline{WR}$ Low Width
29	Td(WR)	Write Data to $\overline{WR}$ ↓ Setup
30	Td(WR)	Write Data to $\overline{WR}$ ↑ Hold Time
31	Tt(WR)	$\overline{WR}$ ↓ to Wait <sup>†</sup> Valid Delay
32	Td(W)	$\overline{RD}$ ↓ Wait Valid Delay
33	Tt(WR(REQ))	$\overline{WR}$ ↓ to $\overline{WR}$ (REQ) Not Valid
34	Td(WR(REQ))	$\overline{RD}$ ↓ to $\overline{WR}$ (REQ) Not Valid
35	Tt(WR(REQ))	$\overline{WR}$ ↓ DTR(REQ) Not Valid
36	Td(WR(REQ))	$\overline{RD}$ ↓ to DTR(REQ) Not Valid
37	Tt(PCINT)	PCLK ↓ to INT Valid Delay
38	TtA(RD)	INTACK to $\overline{RD}$ ↓ (Acknowledge)
39	TwRDA	$\overline{RD}$ (Acknowledge) Width
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Valid Delay
41	TtE(RDA)	EI to $\overline{RD}$ ↓ (Acknowledge) to Read Time
42	TtE(RDA)	EI to $\overline{RD}$ ↓ (Acknowledge) to Read Delay
43	TtE(REQ)	EI to REQ Delay Time
44	Tt(PCREQ)	PCLK ↑ to REQ Delay
45	TdRDA(INT)	$\overline{RD}$ ↓ to INT Inactive Delay
46	Td(WR(REQ))	$\overline{WR}$ ↓ to $\overline{WR}$ ↓ Delay for Not Valid
47	Td(WR(REQ))	$\overline{WR}$ ↓ to $\overline{RD}$ ↓ Delay for Not Valid
48	Tt(WRES)	$\overline{WR}$ and $\overline{RD}$ coincident L <sub>U</sub> Valid Access Recovery Time
49	TtC	Valid Access Recovery Time

- NOTES:
1. Parameter applies only between transactions involving the output.
  2. Parameter applies only between transactions involving the output, measured with open-circuit test load.
  3. Parameter is system dependent. For any FCC in the delay chain, TtE(RDA) for the SCC, and TtE(RD) for the delay chain, TtE(RDA) for the SCC, and TtE(RD) for the delay chain.
  4. Timings are preliminary and subject to change.
  5. Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Character

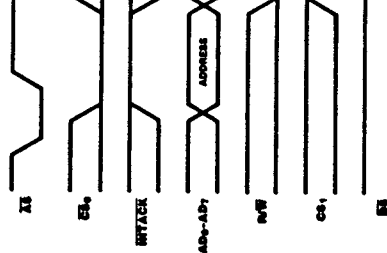
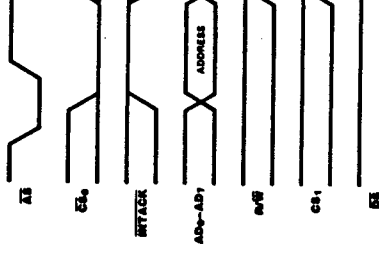
## Z8030/Z8530 GENERAL TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz			6 MHz			8 MHz			Notes*†
			Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	
1	TdPC(REQ)	PCLK ↓ to $\overline{W}/\overline{REQ}$ Valid Delay	250 <sup>a</sup>	350 <sup>a</sup>	250 <sup>a</sup>	250 <sup>a</sup>	350 <sup>a</sup>	250 <sup>a</sup>	350 <sup>a</sup>	250 <sup>a</sup>	350 <sup>a</sup>	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay										
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (PCLK + 4 case only)	80	0 <sup>a</sup>	70	70	0 <sup>a</sup>	60	0 <sup>a</sup>	60	0 <sup>a</sup>	1, 4
4	TsRXD(RXC)	RxD to RxC ↑ Setup Time (X1 Mode)	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	1
5	TsRXD(RXC)	RxD to RxC ↑ Hold Time (X1 Mode)	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	1
6	TsRXD(RXC)	RxD to RxC ↓ Setup Time (X1 Mode)	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	1, 5
7	TsRXD(RXC)	RxD to RxC ↓ Hold Time (X1 Mode)	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	150 <sup>c</sup>	1, 5
8	TsY(RXC)	SYNC to RxC ↑ Setup Time	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	-200 <sup>a</sup>	1
9	TsY(RXC)	SYNC to RxC ↑ Hold Time	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	3TcPC <sup>c</sup>	
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time	+400	+320	0 <sup>a</sup>	0 <sup>a</sup>	+250	0 <sup>a</sup>	+250	0 <sup>a</sup>	+250	1
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	0 <sup>a</sup>	2, 4
11	TdTXC(TXD)	TxC ↓ to TxD Delay (X1 Mode)	300 <sup>a</sup>	300 <sup>a</sup>	230 <sup>a</sup>	230 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	2
12	TdTxCr(TXD)	TxC ↑ to TxD Delay (X1 Mode)	300 <sup>a</sup>	300 <sup>a</sup>	230 <sup>a</sup>	230 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	2, 5
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	
14	TwRTXh	RTxC High Width	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	6
15	TwRTXl	RTxC Low Width	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	6
16	TcRTX	RTxC Cycle Time (RxD, TxD)	1000 <sup>a</sup>	1000 <sup>a</sup>	640 <sup>a</sup>	640 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	6, 7
17	TcRTXX	Crystal Oscillator Period	250 <sup>c</sup>	1000 <sup>c</sup>	165 <sup>c</sup>	1000 <sup>c</sup>	125 <sup>c</sup>	1000 <sup>c</sup>	1000 <sup>c</sup>	1000 <sup>c</sup>	1000 <sup>c</sup>	3
18	TwTRXh	TRxC High Width	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	6
19	TwTRXl	TRxC Low Width	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	180 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	150 <sup>a</sup>	6
20	TcTRX	TRxC Cycle Time	1000 <sup>a</sup>	1000 <sup>a</sup>	640 <sup>a</sup>	640 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	500 <sup>a</sup>	6, 7
21	TwEXT	DCD or CTS Pulse Width	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	
22	TwSY	SYNC Pulse Width	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	200 <sup>a</sup>	

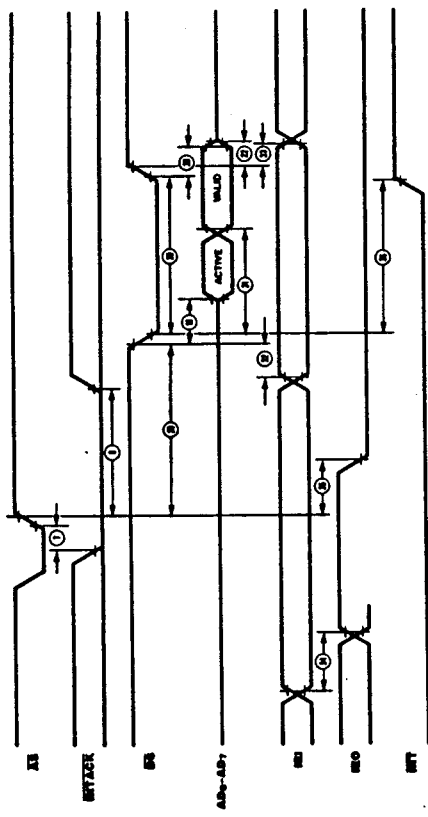
### NOTES

- RxC is RTxC or TRxC, whichever is supplying the receive clock.
- TxC is TRxC or RTxC, whichever is supplying the transmit clock.
- Both RTxC and SYNC have 30 pF capacitors to ground connected to them.
- Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
- Parameter applies only to FM encoding/decoding.
- Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
- The maximum receive or transmit data is 1/4 PCLK.
- \*Timings are preliminary and subject to change.
- †Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization



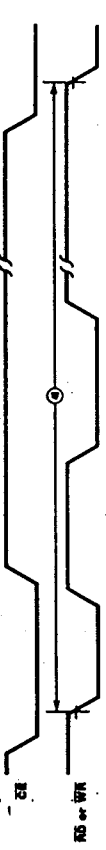
**Interrupt  
Acknowledge  
Timing  
Z8030**



**Reset  
Timing  
Z8530**



**Cycle  
Timing  
Z8530**



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