THE DATASHEET OF

Z0803606VSC

ZiLOG

CUSTOMER PROCUREMENT SPECIFICATION

Z8036 Z8000®
COUNTER/TIMER AND PARALLEL I/O UNIT

GENERAL DESCRIPTION

The Z8036 Z-CIO Counter/Timer and Parallel I/O element is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique address so that it can be accessed directly—no special sequential operations are required. The Z-CIO is directly Z-Bus compatible.

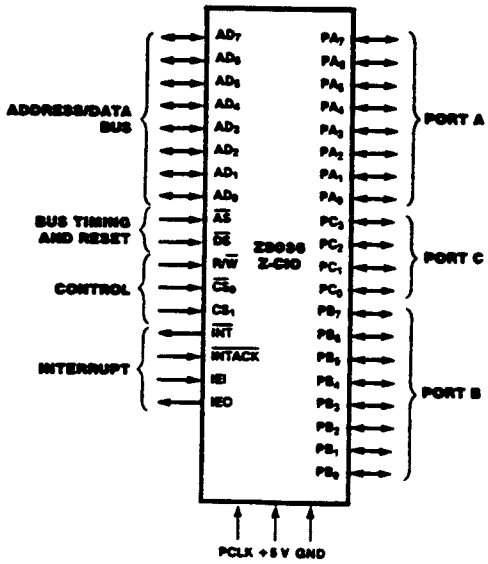


Figure 1. Pin Functions

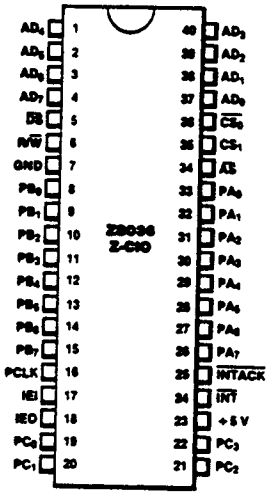


Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments

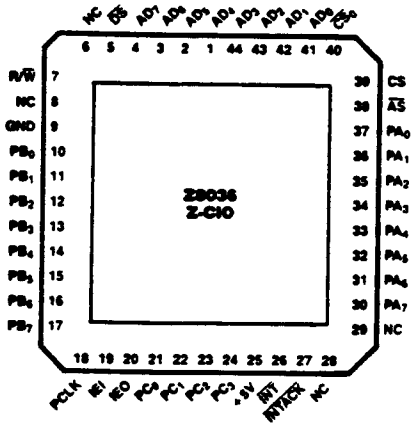


Figure 2b. 44-pin Chip Carrier, Pin Assignments

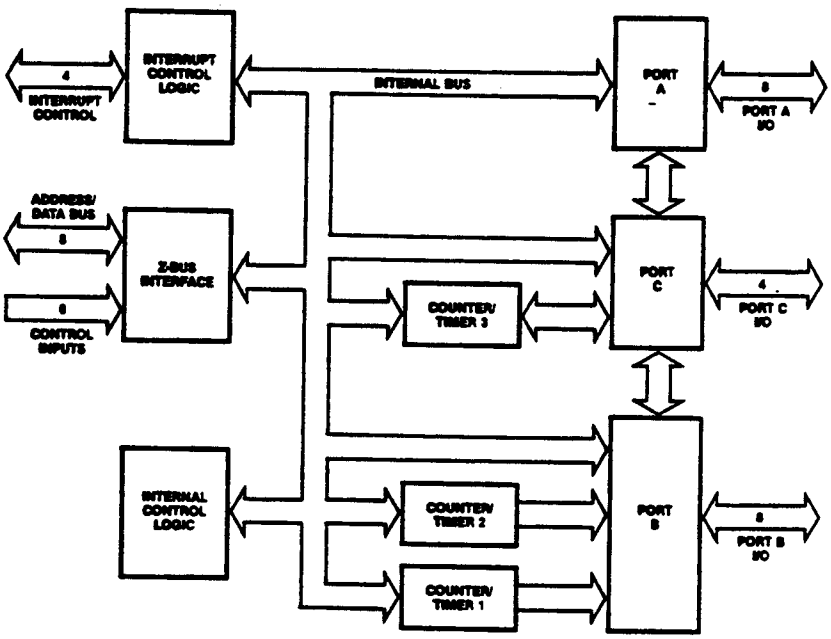


Figure 3. Z-CIO Block Diagram

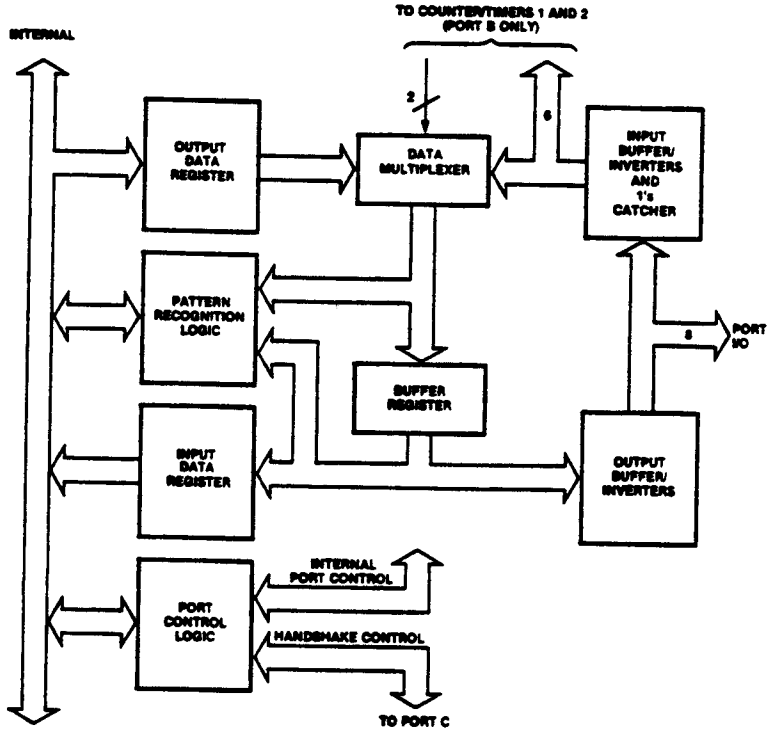


Figure 4. Ports A and B Block Diagram

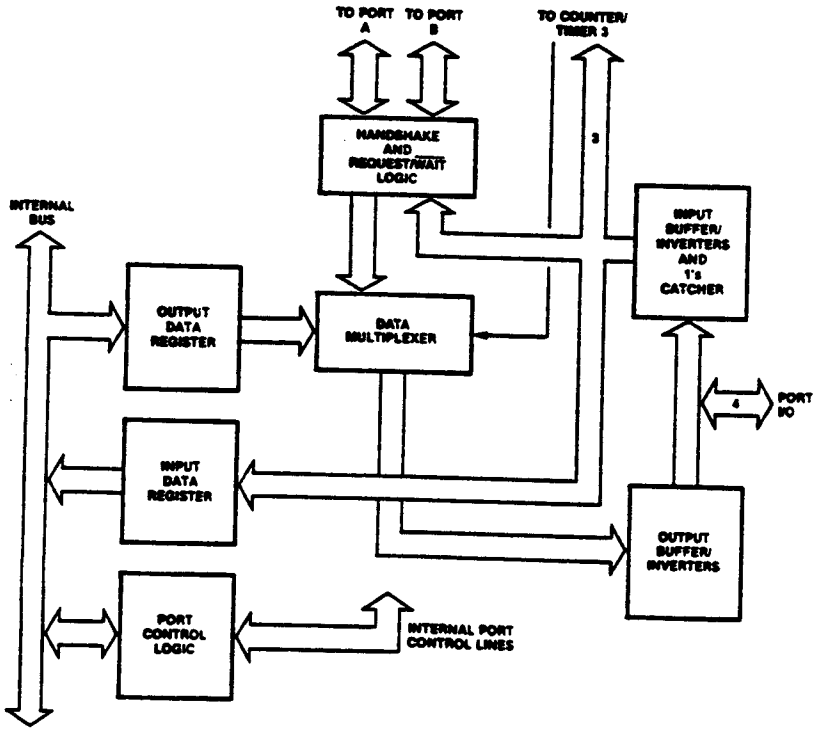


Figure 5. Port C Block Diagram

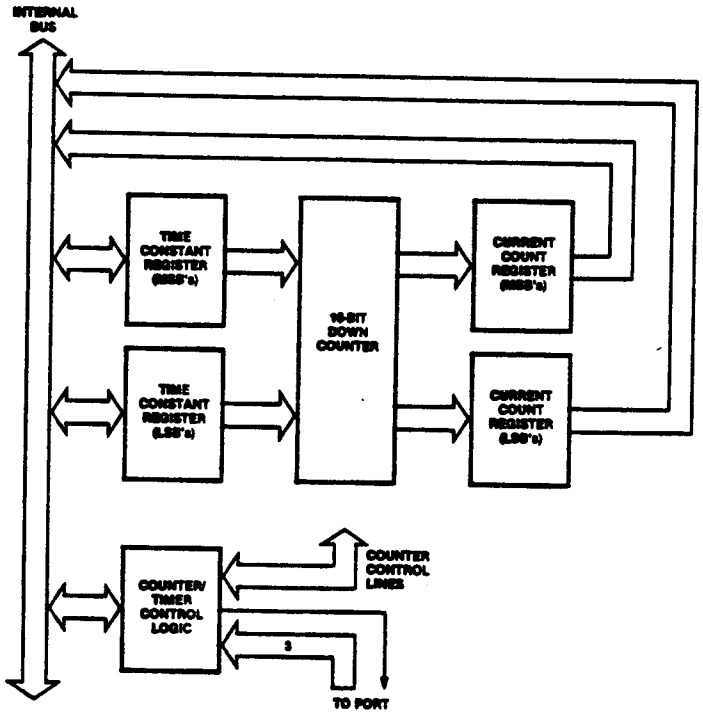


Figure 6. Counter/Timer Block Diagram

GENERAL DESCRIPTION (Continued)

Absolute Maximum Ratings

Voltages on all pins with respect to GND . . . . . −0.3V to +7.0V
Operating Ambient Temperature . . . . . See Ordering Information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.75\ V \leq V_{CC} \leq +5.25\ V$
- GND = 0 V
- T_A as specified in Ordering Information

All ac parameters assume a load capacitance of 50 pf max.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section in this book. Refer to the Literature List for additional documentation.

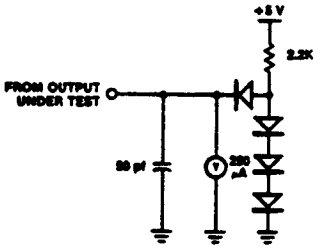


Figure 21. Standard Test Load

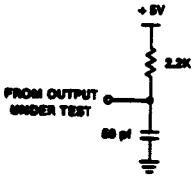


Figure 22. Open-Drain Test Load

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -250\ \mu A$
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = +2.0\ mA$
			0.5	V	$I_{OL} = +3.2\ mA$
I_{IL}	Input Leakage		±10.0	µA	$0.4 \leq V_{IN} \leq +2.4\ V$
I_{OL}	Output Leakage		±10.0	µA	$0.4 \leq V_{OUT} \leq +2.4\ V$
I_{CC}	V_{CC} Supply Current		200	mA	

V_{CC} = 5 V ± 5% unless otherwise specified, over specified temperature range.

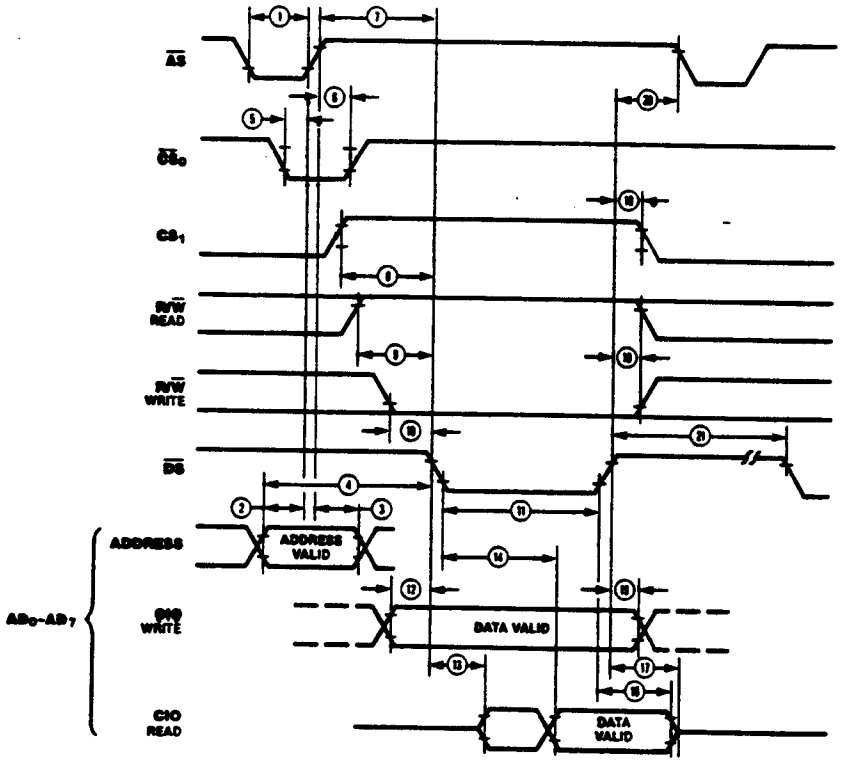
Capacitance

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance		10	pf	
C_{OUT}	Output Capacitance		15	pf	
$C_{I/O}$	Bidirectional Capacitance		20	pf	

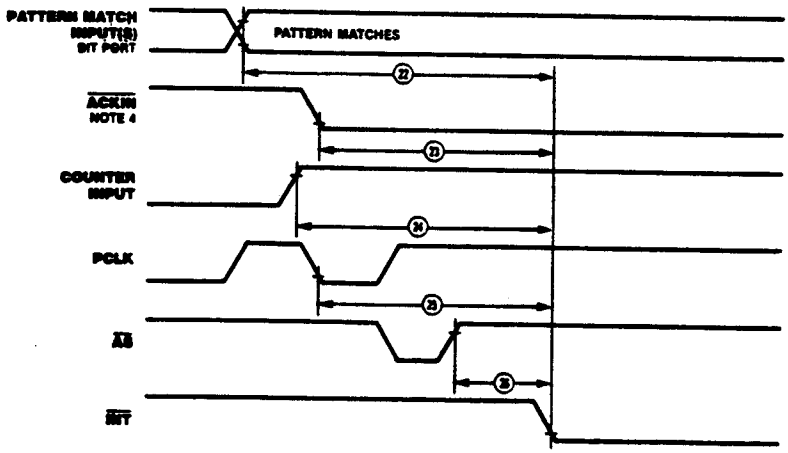
f = 1 MHz, over specified temperature range.
Unmeasured pins returned to ground.

TIMING DIAGRAMS

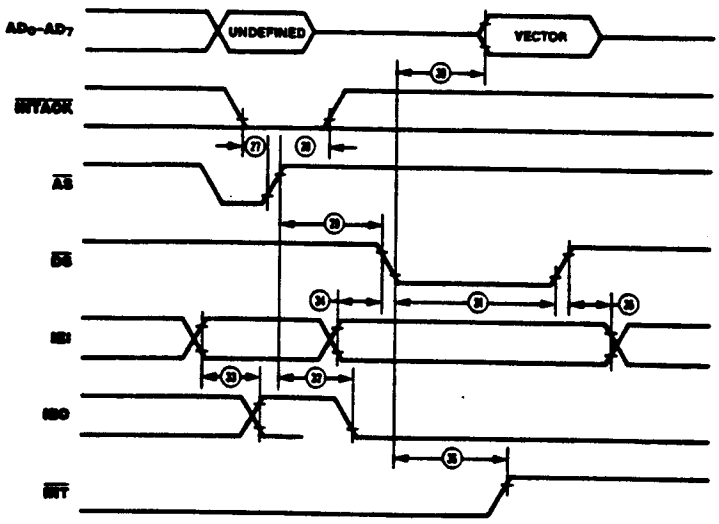
CPU Interface Timing



Interrupt Timing



Interrupt Acknowledge Timing



AC CHARACTERISTICS

No.	Symbol	Parameter	6 MHz Min	6 MHz Max	Notes*
1	TwAS	$\overline{AS}$ Low Width	50	2000	
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	10		1
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	30		1
4	TsA(DS)	Address to $\overline{DS}$ ↓ Setup Time	100		1
5	TsCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time	0		1
6	ThCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time	40		1
7	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	40		1
8	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	80		
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	80		
10	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		
11	TwDS	$\overline{DS}$ Low Width	250		
12	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	20		
13	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0		
14	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		180	
15	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	20		
16	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		
17	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		45	2
18	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	40		
19	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	40		
20	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	25		
21	Trc	Valid Access Recovery Time	650		3
22	TdPM(INT)	Pattern Match to $\overline{INT}$ Delay (Bit Port)		1+800	6
23	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake)		4+600	4,6
24	TdCI(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		1+700	6
25	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		1+700	6
26	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay			
27	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		
28	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		
29	TsAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Setup Time	250		5
30	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		180	
31	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	250		
32	TdAS(IEO)	$\overline{AS}$ ↑ to IEO ↓ Delay ($\overline{INTACK}$ Cycle)		250	5
33	TdIEI(IEO)	IEI to IEO Delay		100	5
34	TsIEI(DSA)	IEO to $\overline{DS}$ (Acknowledge) ↓ Setup Time	70		5
35	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	70		
36	TdDSA(INT)	$\overline{DS}$ (Acknowledge) ↓ to $\overline{INT}$ ↑ Delay		600	

NOTES:

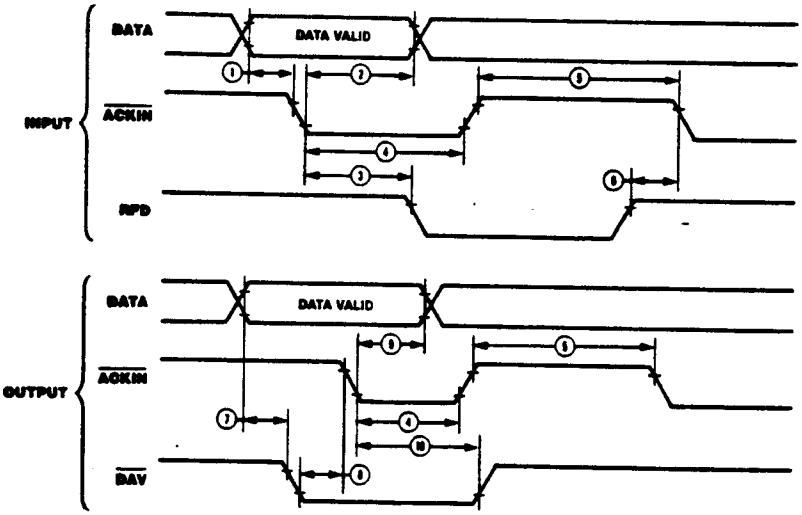
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
3. This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.
4. The delay is from DAV ↑ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake. One additional AS cycle is required for ports in the Single Buffered mode.

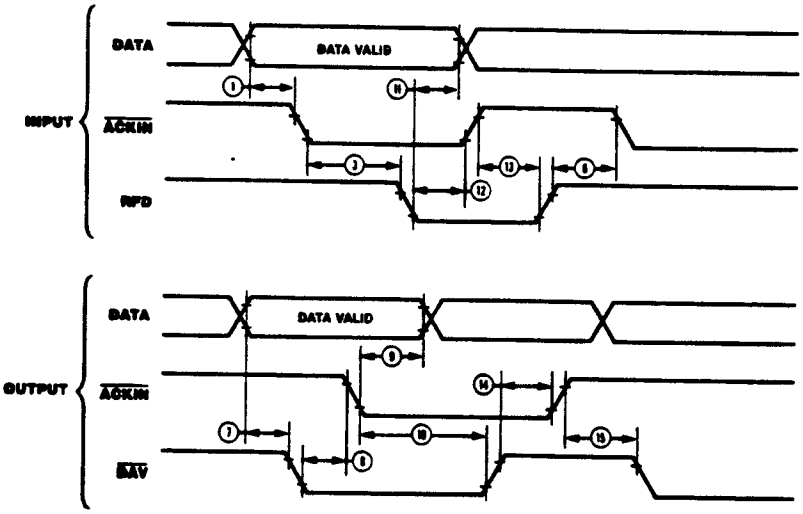
* Units in nanoseconds (ns), except as noted.

5. The parameters for the devices in any particular daisy chain must meet the following constraint: the delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.
6. Units equal to $\overline{AS}$ cycle + ns.
7. The $\overline{AS}$ functions as the clock to the 8036. If $\overline{AS}$ strobe stops, then data does not get clocked through the device. $\overline{AS}$ cycle functions similar to a clock cycle, following $\overline{AS}$ timing specifications. Refer to 7-1 of the Technical Manual.

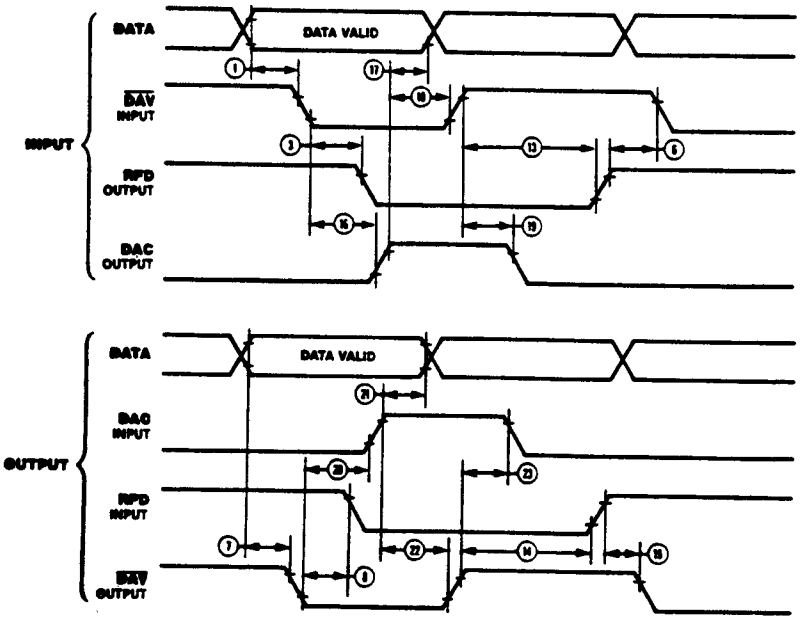
TIMING DIAGRAMS

Interlocked Handshake





3-Wire Handshake



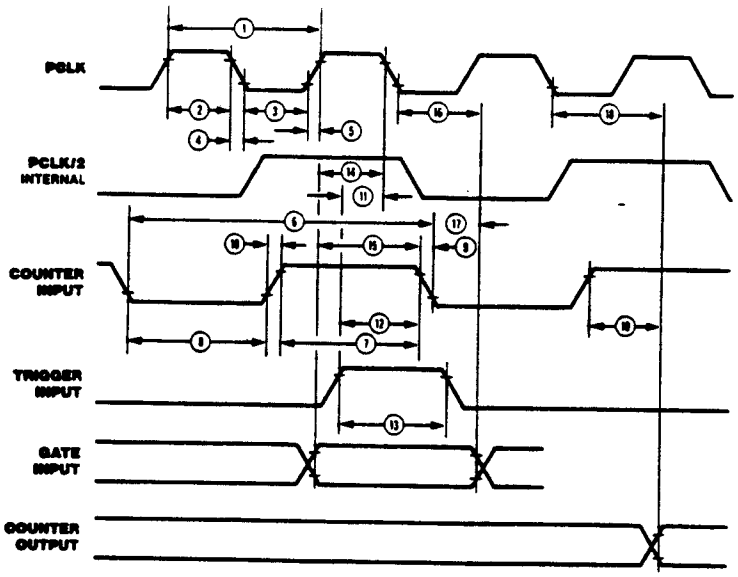
TIMING DIAGRAMS (Continued)

No.	Symbol	Parameter	6 MHz Min	6 MHz Max	Notes*
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Setup Time	0		
2	ThDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Hold Time - Strobed Handshake	330		
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0		
4	TwACKl	$\overline{ACKIN}$ Low Width - Strobed Handshake	165		
5	TwACKh	$\overline{ACKIN}$ High Width - Strobed Handshake	165		
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		
7	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	20		1
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		
9	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↓ Hold Time	1		2
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	1		2
11	ThDI(RFD)	Data Input to RFD ↓ Hold Time - Interlocked Handshake	0		
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay - Interlocked Handshake	0		
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay - Interlocked and 3-Wire Handshake	0		
14	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑) - Interlocked and 3-Wire Handshake	0		
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑)to $\overline{DAV}$ ↓ Delay - Interlocked and 3-Wire Handshake	0		
16	TdDAVlf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay - Input 3-Wire Handshake	0		
17	ThDI(DAC)	Data Input to DAC ↑ Hold Time - 3-Wire Handshake	0		
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay - Input 3-Wire Handshake	0		
19	TdDAVlr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay - Input 3-Wire Handshake	0		
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay - Output 3-Wire Handshake	0		
21	ThDO(DAC)	Data Output to DAC ↑ Hold Time - 3-Wire Handshake	1		2
22	TdDACIr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay - Output 3-Wire Handshake	1		2
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay - Output 3-Wire Handshake	0		

NOTES:
1. This time can be extended through the use of the deskew timers.
2. Units equal to $\overline{AS}$ cycle.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
Units in nanoseconds (ns), except as noted.

Counter/ Timer Timing



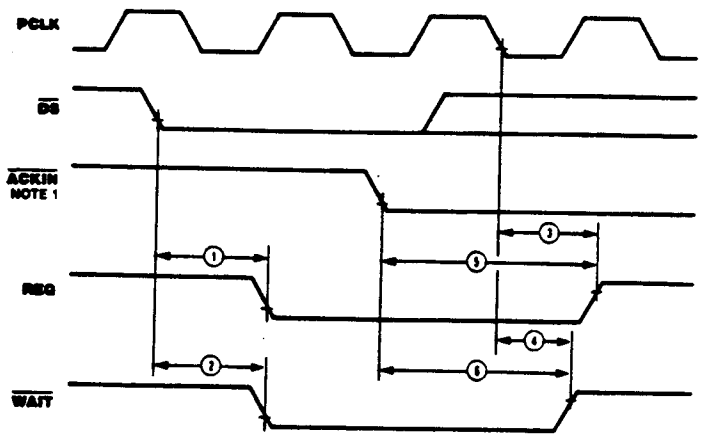
No.	Symbol	Parameter	6 MHz Min	Max	Notes*
1	TcPC	PCLK Cycle Time	165	4000	1
2	TwPCh	PCLK High Width	70	2000	
3	TwPCl	PCLK Low Width	70	2000	
4	TfPC	PCLK Fall Time		10	
5	TrPC	PCLK Rise Time		10	
6	TcCI	Counter Input Cycle Time	330		
7	TCIh	Counter Input High Width	150		
8	TwCIl	Counter Input Low Width	150		
9	TfCI	Counter Input Fall Time		15	
10	TrCI	Counter Input Rise Time		15	
11	TsTI(PC)	Trigger Input to PCLK ↓ Setup Time (Timer Mode)	120		2
12	TsTI(CI)	Trigger Input to Counter Input ↓ Setup Time (Counter Mode)	100		2
13	TwTI	Trigger Input Pulse Width (High or Low)	130		
14	TsGI(PC)	Gate Input to PCLK ↓ Setup Time (Timer Mode)	100		2
15	TsGI(CI)	Gate Input to Counter Input ↓ Setup Time (Counter Mode)	80		2
16	ThGI(PC)	Gate Input to PCLK ↓ Hold Time (Timer Mode)	70		2
17	ThGI(CI)	Gate Input to Counter Input ↓ Hold Time (Counter Mode)	70		2
18	TdPC(CO)	PCLK to Counter Output Delay (Timer Mode)		320	
19	TdCI(CO)	Counter Input to Counter Output Delay (Counter Mode)		420	

NOTES:
1. PCLK is only used with the counter/timers (in Timer mode), the deskew timers, and the REQUEST/WAIT logic. If these functions are not used, the PCLK input can be held low.
2. These parameters must be met to guarantee that trigger or gate are valid for the next counter/timer cycle.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
Units in nanoseconds (ns), except as noted.

AC CHARACTERISTICS (Continued)

REQUEST/ WAIT Timing

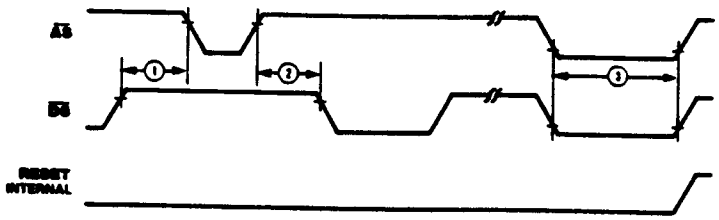


No.	Symbol	Parameter	6 MHz Min	6 MHz Max	Notes*
1	TdDS(REQ)	$\overline{DS}$ ↓ to REQ ↓ Delay		450	
2	TdDS(WAIT)	$\overline{DS}$ ↓ to $\overline{WAIT}$ ↓ Delay		450	
3	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay		320	
4	TdPC(WAIT)	PCLK ↓ to $\overline{WAIT}$ ↑ Delay		300	
5	TdACK(REQ)	ACKIN ↓ to REQ ↑ Delay		3+2 +900	1,2
6	TdACK(WAIT)	ACKIN ↓ to $\overline{WAIT}$ ↑ Delay		10+500	3

NOTES:
1. The Delay is from DAV ↓ for the 3-Wire Input Handshake. The delay is from DAC ↑ for the 3-Wire Output Handshake.
2. Units equal to AS cycles + PCLK cycles + ns.
3. Units equal to PCLK cycles + ns.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0". Units in nanoseconds (ns), except as noted.

Reset Timing

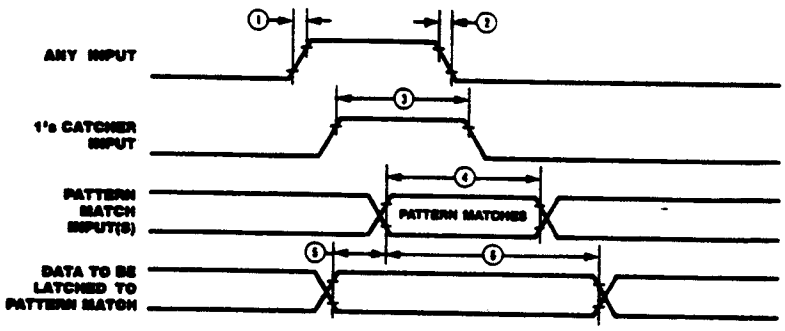


No.	Symbol	Parameter	6 MHz Min	6 MHz Max	Notes*
1	TdDSQ(AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for No Reset	15		
2	TdASQ(DS)	Delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for No Reset	30		
3	TwRES	Minimum Width of $\overline{AS}$ and $\overline{DS}$ both Low for Reset	170		1

NOTES:
1. Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held Low while $\overline{AS}$ pulses) to be sufficient.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0". Units in nanoseconds (ns), except as noted.

Miscellaneous Port Timing

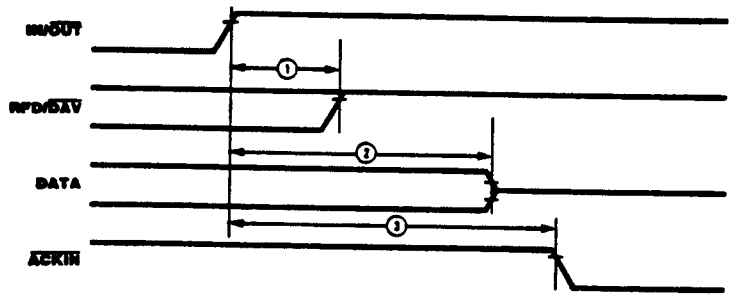


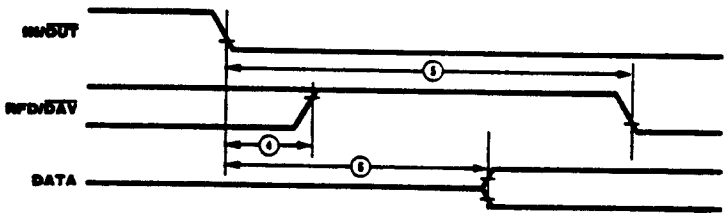
No.	Symbol	Parameter	8 MHz Min	8 MHz Max	Notes*†
1	TrI	Any Input Rise Time		100	
2	TfI	Any Input Fall Time		100	
3	Tw1's	1's Catcher High Width	170		1
4	TwPM	Pattern Match Input Valid (Bit Port)	500		
5	TsPMD	Data Latched on Pattern Match Setup Time (Bit Port)	0		
6	ThPMD	Data Latched on Pattern Match Hold Time (Bit Port)	650		

NOTES:
1. If the input is programmed inverting, a Low-going pulse of the same width will be detected.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0". Units in nanoseconds (ns), except as noted.

Bidirectional Port Timing





No.	Symbol	Parameter	8 MHz Min	8 MHz Max	Notes*†
1	TdIOr(DAV)	I/$\overline{O}$ ↑ to RFD/$\overline{DAV}$ High Delay		500	
2	TdIOr(DRZ)	I/$\overline{O}$ ↑ to Data Float Delay		500	
3	TdIOr(ACK)	I/$\overline{O}$ ↑ to $\overline{ACKIN}$ ↓ Delay			2
4	TdIOf(RFD)	I/$\overline{O}$ ↓ to RFD/$\overline{DAV}$ High Delay		500	
5	TdIOf(DAV)	I/$\overline{O}$ ↓ to RFD/$\overline{DAV}$ ↓ Delay	3		1
6	TdDO(IO)	I/$\overline{O}$ ↓ to Data Bus Driven	2		1

NOTES:
1. Units equal to $\overline{AS}$ cycles.
2. Minimum delay is four $\overline{AS}$ cycles or one $\overline{AS}$ cycle after the corresponding IP is cleared, whichever is longer.

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0". Units in nanoseconds (ns), except as noted.

Z8036/8536 COUNTER/TIMER AND PARALLEL I/O UNIT
Errata Information

1. Caution in the use of the device. RJA bit in 8036 only. Boots up and only uses D6 - D1 (D0 is not used.). Setting the RJA bit right justifies the data.

2. External Linking of the counters.
   If the counters are cascaded externally (output of one counter drives the gate of another counter), the output of the driving counter opens the gate of the cascaded counter for 1 PCLOCK. But, the output of the driving counter violates the set-up time of the Gate input on the cascaded counter. See page 9 of the data sheet, parameters 14 and 16. It has been verified that for certain windows the device will not clock the cascaded counter or the clocking will occur on a different clock edge than the one that the designer would expect.

3. Changing the ports from input to output and vise versa is very slow. No times given.

4. RESET, whether software or hardware, causes a glitch on the outputs. If the I/O was programmed as an input before the RESET, RESET will cause the I/O to glitch to an output at logic 0.

5. In the 8536 only, entering State 1 freezes the internal states. this prevents the recognition of interrupt causing events (no IP bits can be set).

6. CIO Technical Manual p2-9, IP Bit section. Note that IP can also be set on Terminal count. (Not mentioned in text.)

7. CIO Technical Manual p6-1. The code listing here is incorrect and will not work; the code does not get the part back to State 0.

8. Note: in the I/O port operation when you link internally, you do NOT go throught the programmable inverter logic. This is not clear in the documentation.

9. CIO Technical Manual p2-4. The top of the second column should read "SETTING" not "CLEARING."

10. Trigger (internal or external).
    Note that if software writes a 1 to trigger, a 0 will be read back (write only bit).

    Technical Manual page 2-15: Trigger Command Bit (first sentence)

    Actual Response after Trigger (internal or external):

    a) nothing happens immediately
    b) first clock edge (event) loads the counter
    c) second clock edge counts down

    The counter is actually a synchronous load.

    Some users may expect the counter to decrement on the first clock edge.

11. Vector Include Status
    Current Vector Register: Bottom 3 bits of vector are status.

    The operation is supposed to be that the status is included if VIS = 1 and the original whole vector is returned if VIS = 0. This function is supposed to be independent of MIE> However, to get the whole original vector returned (no status), MIE must also be 0; if MIE = 1 then the vector with status is returned (VIS has no effect).

12. Power Up
    The CIO takes a long time (about 50 mS) to come out of the power up reset.

13. 8036 Address Strobe.
    AS (Address Strobe) in the 8036 is also used as the internal clock, consequently AS must be constantly applied even though the device is not addressed by the CPU.

14. Writing the Time Constant Register
    Writing in two bytes causes a problem if the time constant value is used by the counter in between the writing of the two bytes. A hold-off is needed.

15. The falling edge of RD unfreezes the CCR. This allows the data being read by the CPU to change during the read process if the counter happens to be clocked while RD is low.

16. Always disable the CPU interrupts before disabling and modifying the interrupts on the CIO. If an interrupt request is received and responded to by the CPU at the same time the CIO interrupts are disabled, the CPU will expect to see a vector (vector mode), but no vector will be provided, and the int req line will go invalid. The CPU will then try to jump to the vector.

17. The IP bit is not updated in State 1 to allow the command registers to be read without updating the bits in mid read. This also affects the CMA control lines, because they are controlled by IP. The DMA request line will stay in the state it was in when state 1 was entered, which means that the req line will remain low until you leave state 1. The DMA may not know how to interpret this, and will probably send excess data.

    Req/Wait logic can become stuck in a previous level when the CIO is in State 1. This is because the req/wait line is dependant in the IP bits, which are frozen during State 1 transaction, so that they will not change while being read. State 1 is intended for reading the control registers and IP bits.

18. the interrupt pending bit is NOT cleared automatically in bidirectional mode. The chip appears to latch up because it does NOT change direction until that bit is cleared.

19. For multiple interrupts on the I/O ports, they must be LEVEL triggered in order to allow the one's catcher to store them. The ones catcher is the only backup to the IP, which can only store one interrupt per port. It is possible to use the latched mode, where an edge will latch the current status, however, this again records only one interrupt. Also, you can get an error message if another interrupt on pattern match occurs before you service the existing interrupt. But asynchronous (real-world) edge triggered interrupts are a real problem if they don't occur one at a time in a friendly fashion.

20. IP and IUS: A race condition can occur if the IP and IUS bits are reset at the same time. If the IUS bit is reset first, the IP bit may immediately set the IUS again! Use a separate command to first reset the IP, then the IUS.

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