



# THE DATASHEET OF XC5VLX30-1FFG324I

## Virtex-5 FPGA Electrical Characteristics

Virtex®-5 FPGAs are available in -3, -2, -1 speed grades, with -3 having the highest performance. Virtex-5 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-5 FPGA data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- Virtex-5 Family Overview
- Virtex-5 FPGA User Guide
- Virtex-5 FPGA Configuration Guide
- Virtex-5 FPGA XtremeDSP™ Design Considerations
- Virtex-5 FPGA Packaging and Pinout Specification
- Embedded Processor Block in Virtex-5 FPGAs Reference Guide
- Virtex-5 FPGA RocketIO™ GTP Transceiver User Guide
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs
- Virtex-5 FPGA System Monitor User Guide
- Virtex-5 FPGA PCB Designer's Guide

All specifications are subject to change without notice.

## Virtex-5 FPGA DC Characteristics

Table 1: Absolute Maximum Ratings

| Symbol                         | Description                                                                                    |                                                                                      | Units |
|--------------------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|-------|
| V <sub>CCINT</sub>             | Internal supply voltage relative to GND                                                        | –0.5 to 1.1                                                                          | V     |
| V <sub>CCAUX</sub>             | Auxiliary supply voltage relative to GND                                                       | –0.5 to 3.0                                                                          | V     |
| V <sub>CCO</sub>               | Output drivers supply voltage relative to GND                                                  | –0.5 to 3.75                                                                         | V     |
| V <sub>BATT</sub>              | Key memory battery backup supply                                                               | –0.5 to 4.05                                                                         | V     |
| V <sub>REF</sub>               | Input reference voltage                                                                        | –0.5 to 3.75                                                                         | V     |
| V <sub>IN</sub> <sup>(3)</sup> | 3.3V I/O input voltage relative to GND <sup>(4)</sup> (user and dedicated I/Os)                | –0.75 to 4.05                                                                        | V     |
|                                | 3.3V I/O input voltage relative to GND (restricted to maximum of 100 user I/Os) <sup>(5)</sup> | –0.95 to 4.4<br>(Commercial Temperature)<br>–0.85 to 4.3<br>(Industrial Temperature) | V     |
|                                | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)                      | –0.75 to V <sub>CCO</sub> + 0.5                                                      | V     |
| I <sub>IN</sub>                | Current applied to an I/O pin, powered or unpowered                                            | ±100                                                                                 | mA    |
|                                | Total current applied to all I/O pins, powered or unpowered                                    | ±100                                                                                 | mA    |
| V <sub>TS</sub>                | Voltage applied to 3-state 3.3V output <sup>(4)</sup> (user and dedicated I/Os)                | –0.75 to 4.05                                                                        | V     |
|                                | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)                      | –0.75 to V <sub>CCO</sub> + 0.5                                                      | V     |
| T <sub>STG</sub>               | Storage temperature (ambient)                                                                  | –65 to 150                                                                           | °C    |
| T <sub>SOL</sub>               | Maximum soldering temperature <sup>(2)</sup>                                                   | +220                                                                                 | °C    |
| T <sub>J</sub>                 | Maximum junction temperature <sup>(2)</sup>                                                    | +125                                                                                 | °C    |

### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines, refer to [UG112: Device Package User Guide](#). For thermal considerations, refer to [UG195: Virtex-5 FPGA Packaging and Pinout Specification](#) on the Xilinx website.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For 3.3V I/O operation, refer to [UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines](#).
5. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal specification for no more than 20% of a data period.

Table 2: Recommended Operating Conditions

| Symbol              | Description                                                                                          | Temperature Range | Min        | Max             | Units |
|---------------------|------------------------------------------------------------------------------------------------------|-------------------|------------|-----------------|-------|
| $V_{CCINT}$         | Internal supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$          | Commercial        | 0.95       | 1.05            | V     |
|                     | Internal supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$       | Industrial        | 0.95       | 1.05            | V     |
| $V_{CCAUX}^{(1)}$   | Auxiliary supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$         | Commercial        | 2.375      | 2.625           | V     |
|                     | Auxiliary supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$      | Industrial        | 2.375      | 2.625           | V     |
| $V_{CCO}^{(2,4,5)}$ | Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$                   | Commercial        | 1.14       | 3.45            | V     |
|                     | Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$                | Industrial        | 1.14       | 3.45            | V     |
| $V_{IN}$            | 3.3V supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$              | Commercial        | GND – 0.20 | 3.45            | V     |
|                     | 3.3V supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$           | Industrial        | GND – 0.20 | 3.45            | V     |
|                     | 2.5V and below supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$    | Commercial        | GND – 0.20 | $V_{CCO} + 0.2$ | V     |
|                     | 2.5V and below supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ | Industrial        | GND – 0.20 | $V_{CCO} + 0.2$ | V     |
| $I_{IN}^{(6)}$      | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode  | Commercial        |            | 10              | mA    |
|                     |                                                                                                      | Industrial        |            | 10              | mA    |
| $V_{BATT}^{(3)}$    | Battery voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$                  | Commercial        | 1.0        | 3.6             | V     |
|                     | Battery voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$               | Industrial        | 1.0        | 3.6             | V     |

**Notes:**

1. Recommended maximum voltage drop for  $V_{CCAUX}$  is 10 mV/ms.
2. Configuration data is retained even if  $V_{CCO}$  drops to 0V.
3.  $V_{BATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{BATT}$  to either ground or  $V_{CCAUX}$ .
4. Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage  $V_{CC\_CONFIG}$  is also known as  $V_{CCO\_0}$ .
6. A total of 100 mA per bank should not be exceeded.

Table 3: DC Characteristics Over Recommended Operating Conditions

| Symbol           | Description                                                                       | Data Rate | Min  | Typ    | Max | Units         |
|------------------|-----------------------------------------------------------------------------------|-----------|------|--------|-----|---------------|
| $V_{DRINT}$      | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) |           | 0.75 |        |     | V             |
| $V_{DRI}$        | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) |           | 2.0  |        |     | V             |
| $I_{REF}$        | $V_{REF}$ leakage current per pin                                                 |           |      |        | 10  | $\mu\text{A}$ |
| $I_L$            | Input or output leakage current per pin (sample-tested)                           |           |      |        | 10  | $\mu\text{A}$ |
| $C_{IN}$         | Input capacitance (sample-tested)                                                 |           |      |        | 8   | pF            |
| $I_{RPU}^{(1)}$  | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 3.3\text{V}$      |           | 20   |        | 150 | $\mu\text{A}$ |
|                  | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 2.5\text{V}$      |           | 10   |        | 90  | $\mu\text{A}$ |
|                  | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.8\text{V}$      |           | 5    |        | 45  | $\mu\text{A}$ |
|                  | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.5\text{V}$      |           | 3    |        | 30  | $\mu\text{A}$ |
|                  | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.2\text{V}$      |           | 2    |        | 15  | $\mu\text{A}$ |
| $I_{RPD}^{(1)}$  | Pad pull-down (when selected) @ $V_{IN} = 2.5\text{V}$                            |           | 5    |        | 110 | $\mu\text{A}$ |
| $I_{BATT}^{(2)}$ | Battery supply current                                                            |           |      |        | 150 | nA            |
| n                | Temperature diode ideality factor                                                 |           |      | 1.0002 |     | n             |
| r                | Series resistance                                                                 |           |      | 5.0    |     | $\Omega$      |

**Notes:**

1. Typical values are specified at nominal voltage,  $25^{\circ}\text{C}$ .
2. Maximum value specified for worst case process at  $25^{\circ}\text{C}$ .

## Important Note

Typical values for quiescent supply current are now specified at nominal voltage, 85°C junction temperatures ( $T_j$ ). Xilinx recommends analyzing static power consumption at  $T_j = 85^\circ\text{C}$  because the majority of designs operate near the high end of the commercial temperature range. Data sheets for older products (e.g., Virtex-4 devices) still specify typical quiescent supply current at  $T_j = 25^\circ\text{C}$ . Quiescent supply current is specified by speed grade for Virtex-5 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: Typical Quiescent Supply Current

| Symbol       | Description                          | Device     | Speed and Temperature Grade |            |            | Units |
|--------------|--------------------------------------|------------|-----------------------------|------------|------------|-------|
|              |                                      |            | -3 (C)                      | -2 (C & I) | -1 (C & I) |       |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC5VLX20T  | N/A                         | 406        | 253        | mA    |
|              |                                      | XC5VLX30   | 480                         | 480        | 300        | mA    |
|              |                                      | XC5VLX30T  | 507                         | 507        | 317        | mA    |
|              |                                      | XC5VLX50   | 651                         | 651        | 449        | mA    |
|              |                                      | XC5VLX50T  | 689                         | 689        | 475        | mA    |
|              |                                      | XC5VLX85   | 1072                        | 1072       | 833        | mA    |
|              |                                      | XC5VLX85T  | 1115                        | 1115       | 866        | mA    |
|              |                                      | XC5VLX110  | 1391                        | 1391       | 1109       | mA    |
|              |                                      | XC5VLX110T | 1448                        | 1448       | 1154       | mA    |
|              |                                      | XC5VLX155  | 2615                        | 2615       | 2141       | mA    |
|              |                                      | XC5VLX155T | 2674                        | 2674       | 2188       | mA    |
|              |                                      | XC5VLX220  | N/A                         | 2783       | 2278       | mA    |
|              |                                      | XC5VLX220T | N/A                         | 2844       | 2328       | mA    |
|              |                                      | XC5VLX330  | N/A                         | 4193       | 3432       | mA    |
|              |                                      | XC5VLX330T | N/A                         | 4267       | 3492       | mA    |
|              |                                      | XC5VSX35T  | 720                         | 720        | 554        | mA    |
|              |                                      | XC5VSX50T  | 1092                        | 1092       | 840        | mA    |
|              |                                      | XC5VSX95T  | N/A                         | 1924       | 1475       | mA    |
|              |                                      | XC5VSX240T | N/A                         | 4137       | 3168       | mA    |
|              |                                      | XC5VTX150T | N/A                         | 2067       | 2067       | mA    |
|              |                                      | XC5VTX240T | N/A                         | 2881       | 2881       | mA    |
|              |                                      | XC5VFX30T  | 1024                        | 1024       | 1024       | mA    |
|              |                                      | XC5VFX70T  | 1658                        | 1658       | 1658       | mA    |
|              |                                      | XC5VFX100T | 2875                        | 2875       | 2875       | mA    |
|              |                                      | XC5VFX130T | 3041                        | 3041       | 3041       | mA    |
|              |                                      | XC5VFX200T | N/A                         | 3755       | 3755       | mA    |

Table 4: Typical Quiescent Supply Current (Cont'd)

| Symbol            | Description                               | Device     | Speed and Temperature Grade |            |            | Units |
|-------------------|-------------------------------------------|------------|-----------------------------|------------|------------|-------|
|                   |                                           |            | -3 (C)                      | -2 (C & I) | -1 (C & I) |       |
| I <sub>CCOQ</sub> | Quiescent V <sub>CCO</sub> supply current | XC5VLX20T  | N/A                         | 2          | 2          | mA    |
|                   |                                           | XC5VLX30   | 1.5                         | 1.5        | 1.5        | mA    |
|                   |                                           | XC5VLX30T  | 1.5                         | 1.5        | 1.5        | mA    |
|                   |                                           | XC5VLX50   | 2                           | 2          | 2          | mA    |
|                   |                                           | XC5VLX50T  | 2                           | 2          | 2          | mA    |
|                   |                                           | XC5VLX85   | 3                           | 3          | 3          | mA    |
|                   |                                           | XC5VLX85T  | 3                           | 3          | 3          | mA    |
|                   |                                           | XC5VLX110  | 4                           | 4          | 4          | mA    |
|                   |                                           | XC5VLX110T | 4                           | 4          | 4          | mA    |
|                   |                                           | XC5VLX155  | 8                           | 8          | 8          | mA    |
|                   |                                           | XC5VLX155T | 8                           | 8          | 8          | mA    |
|                   |                                           | XC5VLX220  | N/A                         | 8          | 8          | mA    |
|                   |                                           | XC5VLX220T | N/A                         | 8          | 8          | mA    |
|                   |                                           | XC5VLX330  | N/A                         | 12         | 12         | mA    |
|                   |                                           | XC5VLX330T | N/A                         | 12         | 12         | mA    |
|                   |                                           | XC5VSX35T  | 1.5                         | 1.5        | 1.5        | mA    |
|                   |                                           | XC5VSX50T  | 2                           | 2          | 2          | mA    |
|                   |                                           | XC5VSX95T  | N/A                         | 4          | 4          | mA    |
|                   |                                           | XC5VSX240T | N/A                         | 12         | 12         | mA    |
|                   |                                           | XC5VTX150T | N/A                         | 7          | 7          | mA    |
|                   |                                           | XC5VTX240T | N/A                         | 7          | 7          | mA    |
|                   |                                           | XC5VFX30T  | 4                           | 4          | 4          | mA    |
|                   |                                           | XC5VFX70T  | 6                           | 6          | 6          | mA    |
|                   |                                           | XC5VFX100T | 7                           | 7          | 7          | mA    |
|                   |                                           | XC5VFX130T | 8                           | 8          | 8          | mA    |
|                   |                                           | XC5VFX200T | N/A                         | 10         | 10         | mA    |

Table 4: Typical Quiescent Supply Current (Cont'd)

| Symbol              | Description                                 | Device     | Speed and Temperature Grade |            |            | Units |
|---------------------|---------------------------------------------|------------|-----------------------------|------------|------------|-------|
|                     |                                             |            | -3 (C)                      | -2 (C & I) | -1 (C & I) |       |
| I <sub>CCAUXQ</sub> | Quiescent V <sub>CCAUX</sub> supply current | XC5VLX20T  | N/A                         | 32         | 32         | mA    |
|                     |                                             | XC5VLX30   | 38                          | 38         | 38         | mA    |
|                     |                                             | XC5VLX30T  | 43                          | 43         | 43         | mA    |
|                     |                                             | XC5VLX50   | 57                          | 57         | 57         | mA    |
|                     |                                             | XC5VLX50T  | 62                          | 62         | 62         | mA    |
|                     |                                             | XC5VLX85   | 93                          | 93         | 93         | mA    |
|                     |                                             | XC5VLX85T  | 98                          | 98         | 98         | mA    |
|                     |                                             | XC5VLX110  | 125                         | 125        | 125        | mA    |
|                     |                                             | XC5VLX110T | 130                         | 130        | 130        | mA    |
|                     |                                             | XC5VLX155  | 172                         | 172        | 172        | mA    |
|                     |                                             | XC5VLX155T | 177                         | 177        | 177        | mA    |
|                     |                                             | XC5VLX220  | N/A                         | 229        | 229        | mA    |
|                     |                                             | XC5VLX220T | N/A                         | 236        | 236        | mA    |
|                     |                                             | XC5VLX330  | N/A                         | 345        | 345        | mA    |
|                     |                                             | XC5VLX330T | N/A                         | 353        | 353        | mA    |
|                     |                                             | XC5VSX35T  | 49                          | 49         | 49         | mA    |
|                     |                                             | XC5VSX50T  | 74                          | 74         | 74         | mA    |
|                     |                                             | XC5VSX95T  | N/A                         | 131        | 131        | mA    |
|                     |                                             | XC5VSX240T | N/A                         | 300        | 300        | mA    |
|                     |                                             | XC5VTX150T | N/A                         | 180        | 180        | mA    |
|                     |                                             | XC5VTX240T | N/A                         | 300        | 300        | mA    |
|                     |                                             | XC5VFX30T  | 60                          | 60         | 60         | mA    |
|                     |                                             | XC5VFX70T  | 110                         | 110        | 110        | mA    |
|                     |                                             | XC5VFX100T | 150                         | 150        | 150        | mA    |
|                     |                                             | XC5VFX130T | 180                         | 180        | 180        | mA    |
|                     |                                             | XC5VFX200T | N/A                         | 250        | 250        | mA    |

**Notes:**

- Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

## Power-On Power Supply Requirements

Xilinx® FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of  $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$ . The I/O will remain 3-stated through power-on if the recommended power-on sequence is followed. Xilinx does not specify the current or I/O behavior for other power-on sequences.

Table 5 shows the minimum current required by Virtex-5 devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after  $V_{CCINT}$  is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-5 Devices

| Device    | $I_{CCINTMIN}$<br>Typ <sup>(1)</sup> | $I_{CCAUXMIN}$<br>Typ <sup>(1)</sup> | $I_{CCOMIN}$<br>Typ <sup>(1)</sup> | Units |
|-----------|--------------------------------------|--------------------------------------|------------------------------------|-------|
| XC5VLX20T | 172                                  | 54                                   | 50                                 | mA    |
| XC5VLX30  | 235                                  | 76                                   | 50                                 | mA    |
| XC5VLX30T | 246                                  | 86                                   | 50                                 | mA    |
| XC5VLX50  | 320                                  | 114                                  | 50                                 | mA    |
| XC5VLX50T | 336                                  | 124                                  | 50                                 | mA    |
| XC5VLX85  | 492                                  | 186                                  | 100                                | mA    |
| XC5VLX85T | 515                                  | 196                                  | 100                                | mA    |

Table 5: Power-On Current for Virtex-5 Devices

| Device     | $I_{CCINTMIN}$<br>Typ <sup>(1)</sup> | $I_{CCAUXMIN}$<br>Typ <sup>(1)</sup> | $I_{CCOMIN}$<br>Typ <sup>(1)</sup> | Units |
|------------|--------------------------------------|--------------------------------------|------------------------------------|-------|
| XC5VLX110  | 623                                  | 250                                  | 100                                | mA    |
| XC5VLX110T | 651                                  | 260                                  | 100                                | mA    |
| XC5VLX155  | 695                                  | 351                                  | 100                                | mA    |
| XC5VLX155T | 728                                  | 368                                  | 100                                | mA    |
| XC5VLX220  | 1023                                 | 458                                  | 150                                | mA    |
| XC5VLX220T | 1056                                 | 472                                  | 150                                | mA    |
| XC5VLX330  | 1470                                 | 690                                  | 150                                | mA    |
| XC5VLX330T | 1509                                 | 706                                  | 150                                | mA    |
| XC5VSX35T  | 307                                  | 98                                   | 50                                 | mA    |
| XC5VSX50T  | 472                                  | 148                                  | 50                                 | mA    |
| XC5VSX95T  | 804                                  | 262                                  | 100                                | mA    |
| XC5VSX240T | 1632                                 | 662                                  | 150                                | mA    |
| XC5VTX150T | 969                                  | 386                                  | 150                                | mA    |
| XC5VTX240T | 1245                                 | 572                                  | 150                                | mA    |
| XC5VFX30T  | 358                                  | 116                                  | 50                                 | mA    |
| XC5VFX70T  | 695                                  | 232                                  | 100                                | mA    |
| XC5VFX100T | 749                                  | 298                                  | 100                                | mA    |
| XC5VFX130T | 1111                                 | 392                                  | 150                                | mA    |
| XC5VFX200T | 1222                                 | 534                                  | 150                                | mA    |

### Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. The maximum startup current can be obtained using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools and adding the quiescent plus dynamic current consumption.

Table 6: Power Supply Ramp Time

| Symbol      | Description                                   | Ramp Time    | Units |
|-------------|-----------------------------------------------|--------------|-------|
| $V_{CCINT}$ | Internal supply voltage relative to GND       | 0.20 to 50.0 | ms    |
| $V_{CCO}$   | Output drivers supply voltage relative to GND | 0.20 to 50.0 | ms    |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND      | 0.20 to 50.0 | ms    |

## SelectIO™ DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 7: SelectIO DC Input and Output Levels

| I/O Standard                | $V_{IL}$ |                       | $V_{IH}$              |                 | $V_{OL}$        | $V_{OH}$         | $I_{OL}$ | $I_{OH}$ |
|-----------------------------|----------|-----------------------|-----------------------|-----------------|-----------------|------------------|----------|----------|
|                             | V, Min   | V, Max                | V, Min                | V, Max          | V, Max          | V, Min           | mA       | mA       |
| LVTTL                       | -0.3     | 0.8                   | 2.0                   | 3.45            | 0.4             | 2.4              | Note(3)  | Note(3)  |
| LVC MOS33,<br>LVDCI33       | -0.3     | 0.8                   | 2.0                   | 3.45            | 0.4             | $V_{CCO} - 0.4$  | Note(3)  | Note(3)  |
| LVC MOS25,<br>LVDCI25       | -0.3     | 0.7                   | 1.7                   | $V_{CCO} + 0.3$ | 0.4             | $V_{CCO} - 0.4$  | Note(3)  | Note(3)  |
| LVC MOS18,<br>LVDCI18       | -0.3     | 35% $V_{CCO}$         | 65% $V_{CCO}$         | $V_{CCO} + 0.3$ | 0.45            | $V_{CCO} - 0.45$ | Note(4)  | Note(4)  |
| LVC MOS15,<br>LVDCI15       | -0.3     | 35% $V_{CCO}$         | 65% $V_{CCO}$         | $V_{CCO} + 0.3$ | 25% $V_{CCO}$   | 75% $V_{CCO}$    | Note(4)  | Note(4)  |
| LVC MOS12                   | -0.3     | 35% $V_{CCO}$         | 65% $V_{CCO}$         | $V_{CCO} + 0.3$ | 25% $V_{CCO}$   | 75% $V_{CCO}$    | Note(6)  | Note(6)  |
| PCI33_3 <sup>(5)</sup>      | -0.2     | 30% $V_{CCO}$         | 50% $V_{CCO}$         | $V_{CCO}$       | 10% $V_{CCO}$   | 90% $V_{CCO}$    | Note(5)  | Note(5)  |
| PCI66_3 <sup>(5)</sup>      | -0.2     | 30% $V_{CCO}$         | 50% $V_{CCO}$         | $V_{CCO}$       | 10% $V_{CCO}$   | 90% $V_{CCO}$    | Note(5)  | Note(5)  |
| PCI-X <sup>(5)</sup>        | -0.2     | 35% $V_{CCO}$         | 50% $V_{CCO}$         | $V_{CCO}$       | 10% $V_{CCO}$   | 90% $V_{CCO}$    | Note(5)  | Note(5)  |
| GTLP                        | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | —               | 0.6             | N/A              | 36       | N/A      |
| GTL                         | -0.3     | $V_{REF} - 0.05$      | $V_{REF} + 0.05$      | —               | 0.4             | N/A              | 32       | N/A      |
| HSTL I <sub>12</sub>        | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | $V_{CCO} + 0.3$ | 25% $V_{CCO}$   | 75% $V_{CCO}$    | 6.3      | 6.3      |
| HSTL I <sup>(2)</sup>       | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | $V_{CCO} + 0.3$ | 0.4             | $V_{CCO} - 0.4$  | 8        | -8       |
| HSTL II <sup>(2)</sup>      | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | $V_{CCO} + 0.3$ | 0.4             | $V_{CCO} - 0.4$  | 16       | -16      |
| HSTL III <sup>(2)</sup>     | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | $V_{CCO} + 0.3$ | 0.4             | $V_{CCO} - 0.4$  | 24       | -8       |
| HSTL IV <sup>(2)</sup>      | -0.3     | $V_{REF} - 0.1$       | $V_{REF} + 0.1$       | $V_{CCO} + 0.3$ | 0.4             | $V_{CCO} - 0.4$  | 48       | -8       |
| DIFF HSTL I <sup>(2)</sup>  | -0.3     | 50% $V_{CCO} - 0.1$   | 50% $V_{CCO} + 0.1$   | $V_{CCO} + 0.3$ | —               | —                | —        | —        |
| DIFF HSTL II <sup>(2)</sup> | -0.3     | 50% $V_{CCO} - 0.1$   | 50% $V_{CCO} + 0.1$   | $V_{CCO} + 0.3$ | —               | —                | —        | —        |
| SSTL2 I                     | -0.3     | $V_{REF} - 0.15$      | $V_{REF} + 0.15$      | $V_{CCO} + 0.3$ | $V_{TT} - 0.61$ | $V_{TT} + 0.61$  | 8.1      | -8.1     |
| SSTL2 II                    | -0.3     | $V_{REF} - 0.15$      | $V_{REF} + 0.15$      | $V_{CCO} + 0.3$ | $V_{TT} - 0.81$ | $V_{TT} + 0.81$  | 16.2     | -16.2    |
| DIFF SSTL2 I                | -0.3     | 50% $V_{CCO} - 0.15$  | 50% $V_{CCO} + 0.15$  | $V_{CCO} + 0.3$ | —               | —                | —        | —        |
| DIFF SSTL2 II               | -0.3     | 50% $V_{CCO} - 0.15$  | 50% $V_{CCO} + 0.15$  | $V_{CCO} + 0.3$ | —               | —                | —        | —        |
| SSTL18 I                    | -0.3     | $V_{REF} - 0.125$     | $V_{REF} + 0.125$     | $V_{CCO} + 0.3$ | $V_{TT} - 0.47$ | $V_{TT} + 0.47$  | 6.7      | -6.7     |
| SSTL18 II                   | -0.3     | $V_{REF} - 0.125$     | $V_{REF} + 0.125$     | $V_{CCO} + 0.3$ | $V_{TT} - 0.60$ | $V_{TT} + 0.60$  | 13.4     | -13.4    |
| DIFF SSTL18 I               | -0.3     | 50% $V_{CCO} - 0.125$ | 50% $V_{CCO} + 0.125$ | $V_{CCO} + 0.3$ | —               | —                | —        | —        |
| DIFF SSTL18 II              | -0.3     | 50% $V_{CCO} - 0.125$ | 50% $V_{CCO} + 0.125$ | $V_{CCO} + 0.3$ | —               | —                | —        | —        |

### Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33\_3, PCI66\_3, and PCI-X, refer to [UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines](#).
6. Supported drive strengths of 2, 4, 6, or 8 mA.

## HT DC Specifications (HT\_25)

Table 8: HT DC Specifications

| Symbol           | DC Parameter                  | Conditions                                              | Min  | Typ | Max  | Units |
|------------------|-------------------------------|---------------------------------------------------------|------|-----|------|-------|
| $V_{CCO}$        | Supply Voltage                |                                                         | 2.38 | 2.5 | 2.63 | V     |
| $V_{OD}$         | Differential Output Voltage   | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 495  | 600 | 715  | mV    |
| $\Delta V_{OD}$  | Change in $V_{OD}$ Magnitude  |                                                         | -15  |     | 15   | mV    |
| $V_{OCM}$        | Output Common Mode Voltage    | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 495  | 600 | 715  | mV    |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ Magnitude |                                                         | -15  |     | 15   | mV    |
| $V_{ID}$         | Input Differential Voltage    |                                                         | 200  | 600 | 1000 | mV    |
| $\Delta V_{ID}$  | Change in $V_{ID}$ Magnitude  |                                                         | -15  |     | 15   | mV    |
| $V_{ICM}$        | Input Common Mode Voltage     |                                                         | 440  | 600 | 780  | mV    |
| $\Delta V_{ICM}$ | Change in $V_{ICM}$ Magnitude |                                                         | -15  |     | 15   | mV    |

## LVDS DC Specifications (LVDS\_25)

Table 9: LVDS DC Specifications

| Symbol      | DC Parameter                                                                                                 | Conditions                                              | Min   | Typ   | Max   | Units |
|-------------|--------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|-------|-------|-------|-------|
| $V_{CCO}$   | Supply Voltage                                                                                               |                                                         | 2.38  | 2.5   | 2.63  | V     |
| $V_{OH}$    | Output High Voltage for Q and $\overline{Q}$                                                                 | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals |       |       | 1.675 | V     |
| $V_{OL}$    | Output Low Voltage for Q and $\overline{Q}$                                                                  | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 0.825 |       |       | V     |
| $V_{ODIFF}$ | Differential Output Voltage (Q - $\overline{Q}$ ),<br>Q = High ( $\overline{Q} - Q$ ), $\overline{Q}$ = High | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 247   | 350   | 600   | mV    |
| $V_{OCM}$   | Output Common-Mode Voltage                                                                                   | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 1.125 | 1.250 | 1.375 | V     |
| $V_{IDIFF}$ | Differential Input Voltage (Q - $\overline{Q}$ ),<br>Q = High ( $\overline{Q} - Q$ ), $\overline{Q}$ = High  |                                                         | 100   | 350   | 600   | mV    |
| $V_{ICM}$   | Input Common-Mode Voltage                                                                                    |                                                         | 0.3   | 1.2   | 2.2   | V     |

## Extended LVDS DC Specifications (LVDS\_EXT\_25)

Table 10: Extended LVDS DC Specifications

| Symbol      | DC Parameter                                                                                                 | Conditions                                              | Min   | Typ   | Max   | Units |
|-------------|--------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|-------|-------|-------|-------|
| $V_{CCO}$   | Supply Voltage                                                                                               |                                                         | 2.38  | 2.5   | 2.63  | V     |
| $V_{OH}$    | Output High Voltage for Q and $\overline{Q}$                                                                 | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals |       | —     | 1.785 | V     |
| $V_{OL}$    | Output Low Voltage for Q and $\overline{Q}$                                                                  | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 0.715 | —     | —     | V     |
| $V_{ODIFF}$ | Differential Output Voltage (Q - $\overline{Q}$ ),<br>Q = High ( $\overline{Q} - Q$ ), $\overline{Q}$ = High | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 350   | —     | 820   | mV    |
| $V_{OCM}$   | Output Common-Mode Voltage                                                                                   | $R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals | 1.125 | 1.250 | 1.375 | V     |
| $V_{IDIFF}$ | Differential Input Voltage (Q - $\overline{Q}$ ),<br>Q = High ( $\overline{Q} - Q$ ), $\overline{Q}$ = High  | Common-mode input voltage = 1.25V                       | 100   | —     | 1000  | mV    |
| $V_{ICM}$   | Input Common-Mode Voltage                                                                                    | Differential input voltage = $\pm 350$ mV               | 0.3   | 1.2   | 2.2   | V     |

## LVPECL DC Specifications (LVPECL\_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The  $V_{OH}$  levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. [Table 11](#) summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see [UG190: Virtex-5 FPGA User Guide, Chapter 6, SelectIO Resources](#).

Table 11: LVPECL DC Specifications

| Symbol      | DC Parameter                                | Min              | Typ   | Max             | Units |
|-------------|---------------------------------------------|------------------|-------|-----------------|-------|
| $V_{OH}$    | Output High Voltage                         | $V_{CC} - 1.025$ | 1.545 | $V_{CC} - 0.88$ | V     |
| $V_{OL}$    | Output Low Voltage                          | $V_{CC} - 1.81$  | 0.795 | $V_{CC} - 1.62$ | V     |
| $V_{ICM}$   | Input Common-Mode Voltage                   | 0.6              |       | 2.2             | V     |
| $V_{IDIFF}$ | Differential Input Voltage <sup>(1,2)</sup> | 0.100            |       | 1.5             | V     |

### Notes:

1. Recommended input maximum voltage not to exceed  $V_{CCO} + 0.2V$ .
2. Recommended input minimum voltage not to go below  $-0.5V$ .

## PowerPC 440 Switching Characteristics

Consult the *Embedded Processor Block in Virtex-5 FPGAs Reference Guide* for further information.

Table 12: Processor Block Switching Characteristics

| Clock Name         | Description                              | Speed Grade |       |       | Units |
|--------------------|------------------------------------------|-------------|-------|-------|-------|
|                    |                                          | -3          | -2    | -1    |       |
| CPMC440CLK         | CPU clock                                | 550         | 475   | 400   | MHz   |
| CPMINTERCONNECTCLK | Xbar clock                               | 366.6       | 316.6 | 266.6 | MHz   |
| CPMPPCS0PLBCLK     | Slave 0 PLB clock <sup>(1)</sup>         | 183.3       | 158.3 | 133.3 | MHz   |
| CPMPPCS1PLBCLK     | Slave 1 PLB clock <sup>(1)</sup>         | 183.3       | 158.3 | 133.3 | MHz   |
| CPMPPCMPLBCLK      | Master PLB clock <sup>(1)</sup>          | 183.3       | 158.3 | 133.3 | MHz   |
| CPMMCCLK           | Memory interface clock <sup>(1)(2)</sup> | 366.6       | 316.6 | 266.6 | MHz   |
| CPMFCMCLK          | FCM clock <sup>(1)</sup>                 | 275         | 237.5 | 200   | MHz   |
| CPMDCRCLK          | FPGA logic DCR clock <sup>(1)</sup>      | 183.3       | 158.3 | 133.3 | MHz   |
| CPMDMA0LLCLK       | DMA0 LL clock <sup>(1)</sup>             | 250         | 250   | 200   | MHz   |
| CPMDMA1LLCLK       | DMA1 LL clock <sup>(1)</sup>             | 250         | 250   | 200   | MHz   |
| CPMDMA2LLCLK       | DMA2 LL clock <sup>(1)</sup>             | 250         | 250   | 200   | MHz   |
| CPMDMA3LLCLK       | DMA3 LL clock <sup>(1)</sup>             | 250         | 250   | 200   | MHz   |
| JTGC440TCK         | JTAG clock                               | 50          | 50    | 50    | MHz   |
| CPMC440TIMERCLOCK  | Timer clock                              | 275         | 237.5 | 200   | MHz   |

### Notes:

1. Typical bus frequencies are provided for reference only, actual frequencies are user-design dependent.
2. Refer to [DS567](#) for maximum clock speed of designs using the DDR2 Memory Controller for PowerPC® 440 Processors.

Table 13: Processor Block MIB Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMMCCLK        | 1.146       | 1.247 | 1.463 | ps    |
| T <sub>CK_ADDRESS</sub>                  |             | CPMMCCLK        | 1.017       | 1.136 | 1.38  | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMMCCLK        | 1.076       | 1.172 | 1.38  | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMMCCLK        | 0.736       | 0.844 | 0.941 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMMCCLK        | 0.834       | 0.95  | 1.058 | ps    |

Table 14: Processor Block PLBM Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMPPCMPLBCLK   | 0.971       | 1.095 | 1.354 | ps    |
| T <sub>CK_ADDRESS</sub>                  |             | CPMPPCMPLBCLK   | 1.215       | 1.372 | 1.673 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMPPCMPLBCLK   | 1.115       | 1.257 | 1.535 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMPPCMPLBCLK   | 1.7         | 1.79  | 1.86  | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMPPCMPLBCLK   | 0.774       | 0.914 | 1.059 | ps    |

Table 15: Processor Block PLBS0 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMPPCS0PLBCLK  | 1.063       | 1.196 | 1.462 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMPPCS0PLBCLK  | 1.052       | 1.189 | 1.461 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMPPCS0PLBCLK  | 1.307       | 1.545 | 1.836 | ps    |
| T <sub>ADDRESS_CK</sub>                  |             | CPMPPCS0PLBCLK  | 1.253       | 1.492 | 1.787 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMPPCS0PLBCLK  | 0.825       | 0.971 | 1.124 | ps    |

Table 16: Processor Block PLBS1 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMPPCS1PLBCLK  | 1.083       | 1.234 | 1.525 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMPPCS1PLBCLK  | 1.146       | 1.298 | 1.615 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMPPCS1PLBCLK  | 1.335       | 1.596 | 1.921 | ps    |
| T <sub>ADDRESS_CK</sub>                  |             | CPMPPCS1PLBCLK  | 1.328       | 1.568 | 1.864 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMPPCS1PLBCLK  | 0.821       | 0.969 | 1.127 | ps    |

Table 17: Processor Block DMA0 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |        |        | Units |
|------------------------------------------|-------------|-----------------|-------------|--------|--------|-------|
|                                          |             |                 | -3          | -2     | -1     |       |
| Clock-to-out and setup relative to clock |             |                 |             |        |        |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMDMA0LLCLK    | 1.256       | 1.42   | 1.665  | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMDMA0LLCLK    | 1.312       | 1.472  | 1.712  | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMDMA0LLCLK    | 0.453       | 0.558  | 0.716  | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMDMA0LLCLK    | −0.105      | −0.105 | −0.104 | ps    |

Table 18: Processor Block DMA1 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMDMA1LLCLK    | 1.127       | 1.266 | 1.474 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMDMA1LLCLK    | 1.266       | 1.418 | 1.645 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMDMA1LLCLK    | 0.447       | 0.555 | 0.717 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMDMA1LLCLK    | −0.014      | 0.01  | 0.046 | ps    |

Table 19: Processor Block DMA2 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMDMA2LLCLK    | 1.101       | 1.235 | 1.437 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMDMA2LLCLK    | 1.127       | 1.262 | 1.463 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMDMA2LLCLK    | 0.771       | 0.924 | 1.155 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMDMA2LLCLK    | 0.135       | 0.142 | 0.168 | ps    |

Table 20: Processor Block DMA3 Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMDMA3LLCLK    | 1.094       | 1.242 | 1.462 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMDMA3LLCLK    | 1.056       | 1.184 | 1.376 | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMDMA3LLCLK    | 0.636       | 0.767 | 0.965 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMDMA3LLCLK    | 0.087       | 0.119 | 0.116 | ps    |

Table 21: Processor Block DCR Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |    |    | Units |
|------------------------------------------|-------------|-----------------|-------------|----|----|-------|
|                                          |             |                 | -3          | -2 | -1 |       |
| Clock-to-out and setup relative to clock |             |                 |             |    |    |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMDCRCLK       |             |    |    |       |
| T <sub>CK_ADDRESS</sub>                  |             | CPMDCRCLK       |             |    |    |       |
| T <sub>CK_DATA</sub>                     |             | CPMDCRCLK       |             |    |    |       |
| T <sub>CONTROL_CK</sub>                  |             | CPMDCRCLK       |             |    |    |       |
| T <sub>ADDRESS_CK</sub>                  |             | CPMDCRCLK       |             |    |    |       |
| T <sub>DATA_CK</sub>                     |             | CPMDCRCLK       |             |    |    |       |

Table 22: Processor Block FCM Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |       |       | Units |
|------------------------------------------|-------------|-----------------|-------------|-------|-------|-------|
|                                          |             |                 | -3          | -2    | -1    |       |
| Clock-to-out and setup relative to clock |             |                 |             |       |       |       |
| T <sub>CK_CONTROL</sub>                  |             | CPMFCMCLK       | 0.967       | 1.084 | 1.324 | ps    |
| T <sub>CK_DATA</sub>                     |             | CPMFCMCLK       | 1.041       | 1.158 | 1.4   | ps    |
| T <sub>CK_INSTRUCTION</sub>              |             | CPMFCMCLK       | 0.701       | 0.818 | 1.06  | ps    |
| T <sub>CONTROL_CK</sub>                  |             | CPMFCMCLK       | 1.057       | 1.218 | 1.395 | ps    |
| T <sub>DATA_CK</sub>                     |             | CPMFCMCLK       | 0.608       | 0.698 | 0.768 | ps    |
| T <sub>RESULT_CK</sub>                   |             | CPMFCMCLK       | 0.608       | 0.698 | 0.768 | ps    |

Table 23: Processor Block MISC Switching Characteristics

| Clock Name                               | Description | Reference Clock | Speed Grade |    |    | Units |
|------------------------------------------|-------------|-----------------|-------------|----|----|-------|
|                                          |             |                 | -3          | -2 | -1 |       |
| Clock-to-out and setup relative to clock |             |                 |             |    |    |       |
| T <sub>CK_CONTROL</sub>                  |             | CLK1            |             |    |    |       |
| T <sub>CK_ADDRESS</sub>                  |             | CLK2            |             |    |    |       |
| T <sub>CK_DATA</sub>                     |             | CLK3            |             |    |    |       |
| T <sub>CONTROL_CK</sub>                  |             | CLK4            |             |    |    |       |
| T <sub>ADDRESS_CK</sub>                  |             | CLK5            |             |    |    |       |
| T <sub>DATA_CK</sub>                     |             | CLK6            |             |    |    |       |

## GTP\_DUAL Tile Specifications

### GTP\_DUAL Tile DC Characteristics

Table 24: Absolute Maximum Ratings for GTP\_DUAL Tiles

| Symbol     | Description                                                                       |              | Units |
|------------|-----------------------------------------------------------------------------------|--------------|-------|
| MGTAVCCPLL | Analog supply voltage for the GTP_DUAL shared PLL relative to GND                 | –0.5 to 1.32 | V     |
| MGTAVTTTX  | Analog supply voltage for the GTP_DUAL transmitters relative to GND               | –0.5 to 1.32 | V     |
| MGTAVTTRX  | Analog supply voltage for the GTP_DUAL receivers relative to GND                  | –0.5 to 1.32 | V     |
| MGTAVCC    | Analog supply voltage for the GTP_DUAL common circuits relative to GND            | –0.5 to 1.1  | V     |
| MGTAVTTRXC | Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column | –0.5 to 1.32 | V     |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 25: Recommended Operating Conditions for GTP\_DUAL Tiles<sup>(1)(2)</sup>

| Symbol                    | Description                                                                       | Min  | Max  | Units |
|---------------------------|-----------------------------------------------------------------------------------|------|------|-------|
| MGTAVCCPLL <sup>(1)</sup> | Analog supply voltage for the GTP_DUAL shared PLL relative to GND                 | 1.14 | 1.26 | V     |
| MGTAVTTTX <sup>(1)</sup>  | Analog supply voltage for the GTP_DUAL transmitters relative to GND               | 1.14 | 1.26 | V     |
| MGTAVTTRX <sup>(1)</sup>  | Analog supply voltage for the GTP_DUAL receivers relative to GND                  | 1.14 | 1.26 | V     |
| MGTAVCC <sup>(1)</sup>    | Analog supply voltage for the GTP_DUAL common circuits relative to GND            | 0.95 | 1.05 | V     |
| MGTAVTTRXC <sup>(1)</sup> | Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column | 1.14 | 1.26 | V     |

**Notes:**

- Each voltage listed requires the filter circuit described in [UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#).
- Voltages are specified for the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ .

Table 26: DC Characteristics Over Recommended Operating Conditions for GTP\_DUAL Tiles<sup>(1)</sup>

| Symbol                     | Description                                                         | Min                      | Typ | Max | Units    |
|----------------------------|---------------------------------------------------------------------|--------------------------|-----|-----|----------|
| $I_{\text{MGTAVTTTX}}$     | GTP_DUAL tile transmitter termination supply current <sup>(2)</sup> |                          | 71  | 90  | mA       |
| $I_{\text{MGTAVCCPLL}}$    | GTP_DUAL tile shared PLL supply current                             |                          | 36  | 60  | mA       |
| $I_{\text{MGTAVTTRXC}}$    | GTP_DUAL tile resistor termination calibration supply current       |                          | 0.1 | 0.5 | mA       |
| $I_{\text{MGTAVTTRX}}$     | GTP_DUAL tile receiver termination supply current <sup>(3)</sup>    |                          | 0.1 | 0.5 | mA       |
| $I_{\text{MGTAVCC}}$       | GTP_DUAL tile internal analog supply current                        |                          | 56  | 110 | mA       |
| $\text{MGTR}_{\text{REF}}$ | Precision reference resistor for internal calibration termination   | $49.9 \pm 1\%$ tolerance |     |     | $\Omega$ |

**Notes:**

- Typical values are specified at nominal voltage,  $25^{\circ}\text{C}$ , with a 3.2 Gb/s line rate.
- ICC numbers are given per GTP\_DUAL tile with both GTP transceivers operating with default settings.
- AC coupled TX/RX link.

Table 27: GTP\_DUAL Tile Quiescent Supply Current

| Symbol         | Description                                                                      | Typ <sup>(1)</sup> | Max | Units |
|----------------|----------------------------------------------------------------------------------|--------------------|-----|-------|
| $I_{AVTTTXQ}$  | Quiescent MGTAVTTTX (transmitter termination) supply current                     | 8.5                | 18  | mA    |
| $I_{AVCCPLLQ}$ | Quiescent MGTAVCCPLL (PLL) supply current                                        | 8                  | 18  | mA    |
| $I_{AVTTRXQ}$  | Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ. | 0.1                | 0.8 | mA    |
| $I_{AVCCQ}$    | Quiescent MGTAVCC (analog) supply current                                        | 2.5                | 11  | mA    |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTP\_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP\_DUAL tiles in the target LXT or SXT device.

**GTP\_DUAL Tile DC Input and Output Levels**

Table 28 summarizes the DC output specifications of the GTP\_DUAL tiles in Virtex-5 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult [UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#) for further details.

Table 28: GTP\_DUAL Tile DC Specifications

| Symbol       | DC Parameter                                              | Conditions                                 | Min                  | Typ | Max                        | Units    |
|--------------|-----------------------------------------------------------|--------------------------------------------|----------------------|-----|----------------------------|----------|
| $DV_{PPIN}$  | Differential peak-to-peak input voltage                   | External AC coupled $\leq 3.2$ Gb/s        | 150                  |     | 2000                       | mV       |
|              |                                                           | External AC coupled $> 3.2$ Gb/s           | 180                  |     | 2000                       | mV       |
| $V_{IN}$     | Absolute input voltage                                    | DC coupled                                 | -400                 |     | MGTAVTTRX + 400 up to 1320 | mV       |
| $V_{CMIN}$   | Common mode input voltage                                 | DC coupled<br>MGTAVTTRX = 1.2V             |                      | 800 |                            | mV       |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage <sup>(1)</sup>   | TXBUFDIFFCTRL = 000,<br>TX_DIFF_BOOST = ON |                      |     | 1400                       | mV       |
| $V_{SEOUT}$  | Single-ended output voltage swing <sup>(1)</sup>          | TXBUFDIFFCTRL = 000,<br>TX_DIFF_BOOST = ON |                      |     | 700                        | mV       |
| $V_{CMOUT}$  | Common mode output voltage                                | Equation based<br>MGTAVTTTX = 1.2V         | $1200 - V_{SEOUT}/2$ |     |                            | mV       |
| $R_{IN}$     | Differential input resistance                             |                                            | 90                   | 100 | 120                        | $\Omega$ |
| $R_{OUT}$    | Differential output resistance                            |                                            | 90                   | 100 | 120                        | $\Omega$ |
| $T_{OSKEW}$  | Transmitter output skew                                   |                                            |                      |     | 15                         | ps       |
| $C_{EXT}$    | Recommended external AC coupling capacitor <sup>(2)</sup> |                                            | 75                   | 100 | 200                        | nF       |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

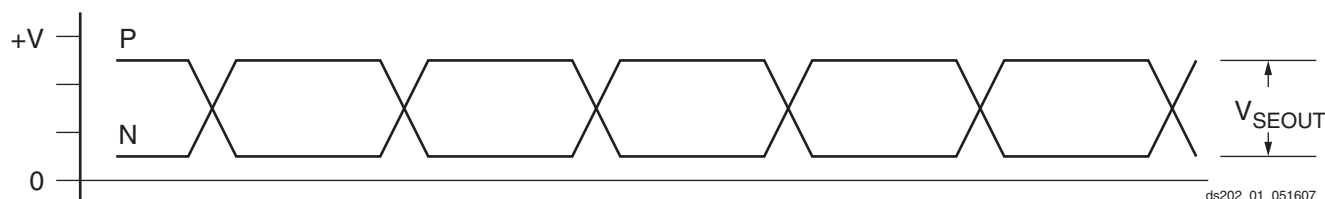


Figure 1: Single-Ended Output Voltage Swing

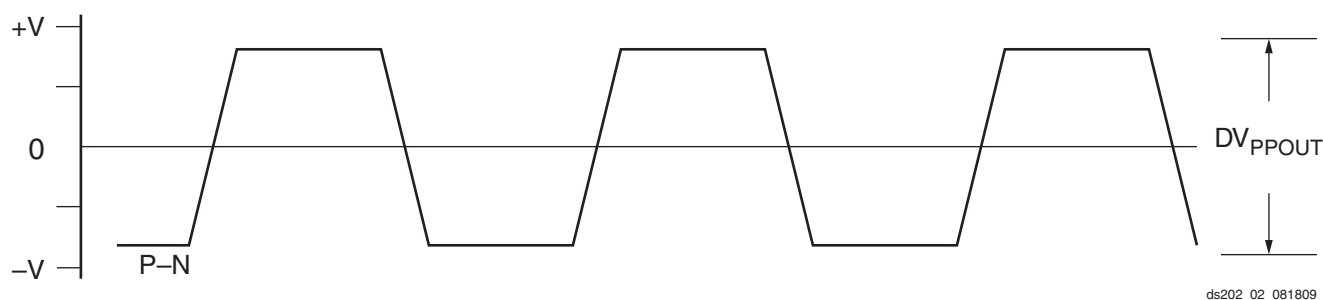


Figure 2: Peak-to-Peak Differential Output Voltage

Table 29 summarizes the DC specifications of the clock input of the GTP\_DUAL tile. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide for further details.

Table 29: GTP\_DUAL Tile Clock DC Input Specifications<sup>(1)</sup>

| Symbol      | DC Parameter                            | Conditions | Min | Typ | Max  | Units    |
|-------------|-----------------------------------------|------------|-----|-----|------|----------|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage |            | 200 | 800 | 2000 | mV       |
| $V_{ISE}$   | Single-ended input voltage              |            | 100 | 400 | 1000 | mV       |
| $R_{IN}$    | Differential input resistance           |            | 80  | 105 | 130  | $\Omega$ |
| $C_{EXT}$   | Required external AC coupling capacitor |            | 75  | 100 | 200  | nF       |

#### Notes:

- $V_{MIN} = 0V$  and  $V_{MAX} = 1200mV$

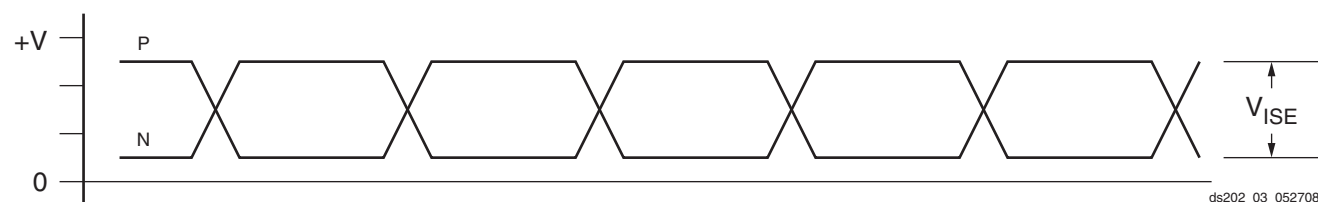


Figure 3: Single-Ended Clock Input Voltage Swing Peak-to-Peak

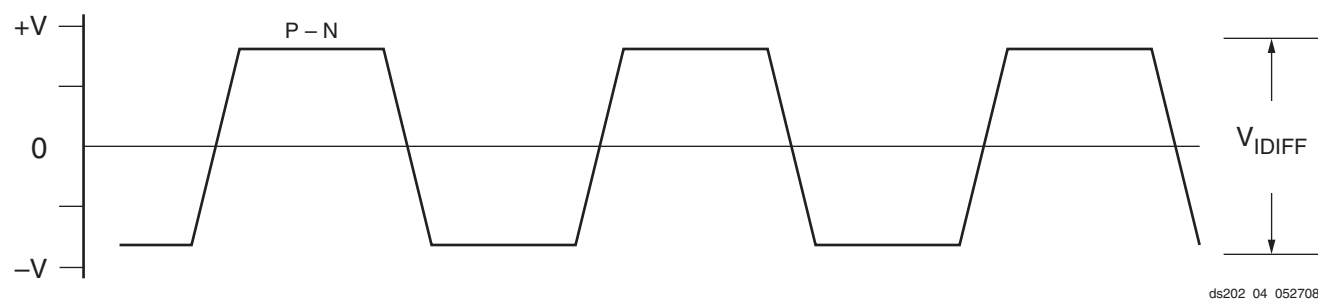


Figure 4: Differential Clock Input Voltage Swing Peak-to-Peak

## GTP\_DUAL Tile Switching Characteristics

Consult [UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#) for further information.

Table 30: GTP\_DUAL Tile Performance

| Symbol        | Description                       | Speed Grade |      |     | Units |
|---------------|-----------------------------------|-------------|------|-----|-------|
|               |                                   | -3          | -2   | -1  |       |
| $F_{GTPMAX}$  | Maximum GTP transceiver data rate | 3.75        | 3.75 | 3.2 | Gb/s  |
| $F_{GPLLMAX}$ | Maximum PLL frequency             | 2.0         | 2.0  | 2.0 | GHz   |
| $F_{GPLLMIN}$ | Minimum PLL frequency             | 1.0         | 1.0  | 1.0 | GHz   |

Table 31: Dynamic Reconfiguration Port (DRP) in the GTP\_DUAL Tile Switching Characteristics

| Symbol         | Description                            | Speed Grade |     |     | Units |
|----------------|----------------------------------------|-------------|-----|-----|-------|
|                |                                        | -3          | -2  | -1  |       |
| $F_{GTPDRCLK}$ | GTP DCLK (DRP clock) maximum frequency | 200         | 175 | 150 | MHz   |

Table 32: GTP\_DUAL Tile Reference Clock Switching Characteristics

| Symbol      | Description                                            | Conditions                                               | All Speed Grades |     |     | Units |
|-------------|--------------------------------------------------------|----------------------------------------------------------|------------------|-----|-----|-------|
|             |                                                        |                                                          | Min              | Typ | Max |       |
| $F_{GCLK}$  | Reference clock frequency range <sup>(1)</sup>         | CLK                                                      | 60               |     | 350 | MHz   |
| $T_{RCLK}$  | Reference clock rise time                              | 20% – 80%                                                |                  | 200 | 400 | ps    |
| $T_{FCLK}$  | Reference clock fall time                              | 80% – 20%                                                |                  | 200 | 400 | ps    |
| $T_{DCREF}$ | Reference clock duty cycle <sup>(2)</sup>              | CLK                                                      | 40               | 50  | 60  | %     |
| $T_{GJTT}$  | Reference clock total jitter, peak-peak <sup>(3)</sup> | CLK                                                      |                  |     | 40  | ps    |
| $T_{LOCK}$  | Clock recovery frequency acquisition time              | Initial PLL lock                                         |                  |     | 1   | ms    |
| $T_{PHASE}$ | Clock recovery phase acquisition time                  | Lock to data after PLL has locked to the reference clock |                  |     | 200 | μs    |

### Notes:

1. The clock from the GTP\_DUAL differential clock pin pair can be used for all serial bit rates. GREFCLK can be used for serial bit rates up to 1 Gb/s.
2. For reference clock rates above 325 MHz, a duty cycle of 45% to 55% must be maintained.
3. Measured at the package pin. GTP\_DUAL jitter characteristics measured using a clock with specification  $T_{GJTT}$ .

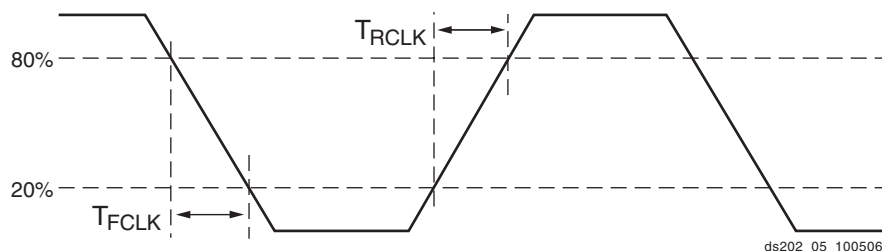


Figure 5: Reference Clock Timing Parameters

Table 33: GTP\_DUAL Tile User Clock Switching Characteristics<sup>(1)</sup>

| Symbol             | Description                 | Conditions      | Speed Grade |       |     | Units |
|--------------------|-----------------------------|-----------------|-------------|-------|-----|-------|
|                    |                             |                 | -3          | -2    | -1  |       |
| F <sub>TXOUT</sub> | TXOUTCLK maximum frequency  |                 | 375         | 375   | 320 | MHz   |
| F <sub>RXREC</sub> | RXRECCLK maximum frequency  |                 | 375         | 375   | 320 | MHz   |
| T <sub>RX</sub>    | RXUSRCLK maximum frequency  |                 | 375         | 375   | 320 | MHz   |
| T <sub>RX2</sub>   | RXUSRCLK2 maximum frequency | RXDATAWIDTH = 0 | 350         | 350   | 320 | MHz   |
|                    |                             | RXDATAWIDTH = 1 | 187.5       | 187.5 | 160 | MHz   |
| T <sub>TX</sub>    | TXUSRCLK maximum frequency  |                 | 375         | 375   | 320 | MHz   |
| T <sub>TX2</sub>   | TXUSRCLK2 maximum frequency | TXDATAWIDTH = 0 | 350         | 350   | 320 | MHz   |
|                    |                             | TXDATAWIDTH = 1 | 187.5       | 187.5 | 160 | MHz   |

**Notes:**

1. Clocking must be implemented as described in [UG196: Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#)

Table 34: GTP\_DUAL Tile Transmitter Switching Characteristics

| Symbol                  | Description                         | Min       | Typ | Max                 | Units |
|-------------------------|-------------------------------------|-----------|-----|---------------------|-------|
| F <sub>GTPTX</sub>      | Serial data rate range              | 0.1       |     | F <sub>GTPMAX</sub> | Gb/s  |
| T <sub>RTX</sub>        | TX Rise time                        |           | 140 |                     | ps    |
| T <sub>FTX</sub>        | TX Fall time                        |           | 120 |                     | ps    |
| T <sub>LLSKEW</sub>     | TX lane-to-lane skew <sup>(1)</sup> |           |     | 855                 | ps    |
| V <sub>TXOVBVDP</sub>   | Electrical idle amplitude           |           |     | 20                  | mV    |
| T <sub>TXOVBTRANS</sub> | Electrical idle transition time     |           |     | 40                  | ns    |
| T <sub>J3.75</sub>      | Total Jitter <sup>(2)</sup>         | 3.75 Gb/s |     | 0.35                | UI    |
| D <sub>J3.75</sub>      | Deterministic Jitter <sup>(2)</sup> |           |     | 0.19                | UI    |
| T <sub>J3.2</sub>       | Total Jitter <sup>(2)</sup>         | 3.20 Gb/s |     | 0.35                | UI    |
| D <sub>J3.2</sub>       | Deterministic Jitter <sup>(2)</sup> |           |     | 0.19                | UI    |
| T <sub>J2.5</sub>       | Total Jitter <sup>(2)</sup>         | 2.50 Gb/s |     | 0.30                | UI    |
| D <sub>J2.5</sub>       | Deterministic Jitter <sup>(2)</sup> |           |     | 0.14                | UI    |
| T <sub>J2.0</sub>       | Total Jitter <sup>(2)</sup>         | 2.00 Gb/s |     | 0.30                | UI    |
| D <sub>J2.0</sub>       | Deterministic Jitter <sup>(2)</sup> |           |     | 0.14                | UI    |
| T <sub>J1.25</sub>      | Total Jitter <sup>(2)</sup>         | 1.25 Gb/s |     | 0.20                | UI    |
| D <sub>J1.25</sub>      | Deterministic Jitter <sup>(2)</sup> |           |     | 0.10                | UI    |
| T <sub>J1.00</sub>      | Total Jitter <sup>(2)</sup>         | 1.00 Gb/s |     | 0.20                | UI    |
| D <sub>J1.00</sub>      | Deterministic Jitter <sup>(2)</sup> |           |     | 0.10                | UI    |
| T <sub>J500</sub>       | Total Jitter <sup>(2)</sup>         | 500 Mb/s  |     | 0.10                | UI    |
| D <sub>J500</sub>       | Deterministic Jitter <sup>(2)</sup> |           |     | 0.04                | UI    |
| T <sub>J100</sub>       | Total Jitter <sup>(2)</sup>         | 100 Mb/s  |     | 0.02                | UI    |
| D <sub>J100</sub>       | Deterministic Jitter <sup>(2)</sup> |           |     | 0.01                | UI    |

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP\_DUAL sites.
2. Using PLL\_DIVSEL\_FB = 2, INTDATAWIDTH = 1.
3. All jitter values are based on a Bit-Error Ratio of 1e<sup>-12</sup>.

Table 35: GTP\_DUAL Tile Receiver Switching Characteristics

| Symbol                                               | Description                                        |                                                                                   | Min   | Typ | Max                 | Units |
|------------------------------------------------------|----------------------------------------------------|-----------------------------------------------------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTPRX</sub>                                   | Serial data rate                                   | RX oversampler not enabled                                                        | 0.5   |     | F <sub>GTPMAX</sub> | Gb/s  |
|                                                      |                                                    | RX oversampler enabled                                                            | 0.1   |     | 0.5                 | Gb/s  |
| R <sub>XOOBVDPP</sub>                                | OOB detect threshold peak-to-peak                  | OOBDETECT_THRESHOLD = 100                                                         | 60    | 105 | 165                 | mV    |
| R <sub>XSST</sub>                                    | Receiver spread-spectrum tracking <sup>(1)</sup>   | Modulated @ 33 KHz                                                                | −5000 |     | 0                   | ppm   |
| R <sub>XRL</sub>                                     | Run length (CID)                                   | Internal AC capacitor bypassed                                                    |       |     | 150                 | UI    |
| R <sub>XPPMTOL</sub>                                 | Data/REFCLK PPM offset tolerance <sup>(2)</sup>    | CDR 2 <sup>nd</sup> -order loop disabled with PLL_RXDIVSEL_OUT = 1 <sup>(3)</sup> | −200  |     | 200                 | ppm   |
|                                                      |                                                    | CDR 2 <sup>nd</sup> -order loop disabled with PLL_RXDIVSEL_OUT = 2 <sup>(3)</sup> | −200  |     | 200                 | ppm   |
|                                                      |                                                    | CDR 2 <sup>nd</sup> -order loop disabled with PLL_RXDIVSEL_OUT = 4 <sup>(3)</sup> | −100  |     | 100                 | ppm   |
|                                                      |                                                    | CDR 2 <sup>nd</sup> -order loop enabled                                           | −1000 |     | 1000                | ppm   |
| SJ Jitter Tolerance <sup>(4)</sup>                   |                                                    |                                                                                   |       |     |                     |       |
| JT_SJ <sub>3.75</sub>                                | Sinusoidal Jitter <sup>(5)</sup>                   | 3.75 Gb/s                                                                         | 0.30  |     |                     | UI    |
| JT_SJ <sub>3.2</sub>                                 | Sinusoidal Jitter <sup>(5)</sup>                   | 3.20 Gb/s                                                                         | 0.40  |     |                     | UI    |
| JT_SJ <sub>2.50</sub>                                | Sinusoidal Jitter <sup>(5)</sup>                   | 2.50 Gb/s                                                                         | 0.40  |     |                     | UI    |
| JT_SJ <sub>2.00</sub>                                | Sinusoidal Jitter <sup>(5)</sup>                   | 2.00 Gb/s                                                                         | 0.40  |     |                     | UI    |
| JT_SJ <sub>1.00</sub>                                | Sinusoidal Jitter <sup>(5)</sup>                   | 1.00 Gb/s                                                                         | 0.30  |     |                     | UI    |
| JT_SJ <sub>500</sub>                                 | Sinusoidal Jitter <sup>(5)</sup>                   | 500 Mb/s                                                                          | 0.30  |     |                     | UI    |
| JT_SJ <sub>500</sub>                                 | Sinusoidal Jitter <sup>(5)</sup>                   | 500 Mb/s OS                                                                       | 0.30  |     |                     | UI    |
| JT_SJ <sub>100</sub>                                 | Sinusoidal Jitter <sup>(5)</sup>                   | 100 Mb/s OS                                                                       | 0.30  |     |                     | UI    |
| SJ Jitter Tolerance with Stressed Eye <sup>(4)</sup> |                                                    |                                                                                   |       |     |                     |       |
| JT_TJSE <sub>3.2</sub>                               | Total Jitter with Stressed Eye <sup>(6)</sup>      | 3.20 Gb/s                                                                         | 0.87  |     |                     | UI    |
| JT_SJSE <sub>3.2</sub>                               | Sinusoidal Jitter with Stressed Eye <sup>(6)</sup> | 3.20 Gb/s                                                                         | 0.30  |     |                     | UI    |

**Notes:**

- Using PLL\_RXDIVSEL\_OUT = 1 only.
- Indicates the maximum offset between the receiver reference clock and the serial data. For example, a reference clock with ±100 ppm resolution results in a maximum offset of 200 ppm between the reference clock and the serial data.
- CDR 1st-order step size set to 2.
- All jitter values are based on a Bit Error Ratio of 1e<sup>–12</sup>.
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Stimulus signal includes 0.4UI of DJ and 0.17UI of RJ. RX equalizer is enabled.

## GTX\_DUAL Tile Specifications

### GTX\_DUAL Tile DC Characteristics

Table 36: Absolute Maximum Ratings for GTX\_DUAL Tiles

| Symbol     | Description                                                                       |              | Units |
|------------|-----------------------------------------------------------------------------------|--------------|-------|
| MGTAVCCPLL | Analog supply voltage for the GTX_DUAL shared PLL relative to GND                 | –0.5 to 1.1  | V     |
| MGTAVTTTX  | Analog supply voltage for the GTX_DUAL transmitters relative to GND               | –0.5 to 1.32 | V     |
| MGTAVTTRX  | Analog supply voltage for the GTX_DUAL receivers relative to GND                  | –0.5 to 1.32 | V     |
| MGTAVCC    | Analog supply voltage for the GTX_DUAL common circuits relative to GND            | –0.5 to 1.1  | V     |
| MGTAVTTRXC | Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column | –0.5 to 1.32 | V     |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 37: Recommended Operating Conditions for GTX\_DUAL Tiles<sup>(1)(2)</sup>

| Symbol                    | Description                                                                       | Min  | Max  | Units |
|---------------------------|-----------------------------------------------------------------------------------|------|------|-------|
| MGTAVCCPLL <sup>(1)</sup> | Analog supply voltage for the GTX_DUAL shared PLL relative to GND                 | 0.95 | 1.05 | V     |
| MGTAVTTTX <sup>(1)</sup>  | Analog supply voltage for the GTX_DUAL transmitters relative to GND               | 1.14 | 1.26 | V     |
| MGTAVTTRX <sup>(1)</sup>  | Analog supply voltage for the GTX_DUAL receivers relative to GND                  | 1.14 | 1.26 | V     |
| MGTAVCC <sup>(1)</sup>    | Analog supply voltage for the GTX_DUAL common circuits relative to GND            | 0.95 | 1.05 | V     |
| MGTAVTTRXC <sup>(1)</sup> | Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column | 1.14 | 1.26 | V     |

**Notes:**

- Each voltage listed requires the filter circuit described in [UG198: Virtex-5 FPGA RocketIO GTX Transceiver User Guide](#).
- Voltages are specified for the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ .

Table 38: DC Characteristics Over Recommended Operating Conditions for GTX\_DUAL Tiles<sup>(1)</sup>

| Symbol                     | Description                                                         | Min                      | Typ  | Max   | Units    |
|----------------------------|---------------------------------------------------------------------|--------------------------|------|-------|----------|
| $I_{\text{MGTAVTTTX}}$     | GTX_DUAL tile transmitter termination supply current <sup>(2)</sup> |                          | 43.3 | 86.3  | mA       |
| $I_{\text{MGTAVCCPLL}}$    | GTX_DUAL tile shared PLL supply current                             |                          | 38.0 | 99.4  | mA       |
| $I_{\text{MGTAVTTRXC}}$    | GTX_DUAL tile resistor termination calibration supply current       |                          | 0.1  | 0.5   | mA       |
| $I_{\text{MGTAVTTRX}}$     | GTX_DUAL tile receiver termination supply current <sup>(3)</sup>    |                          | 40.3 | 56.5  | mA       |
| $I_{\text{MGTAVCC}}$       | GTX_DUAL tile internal analog supply current                        |                          | 80.5 | 179.5 | mA       |
| $\text{MGTR}_{\text{REF}}$ | Precision reference resistor for internal calibration termination   | $59.0 \pm 1\%$ tolerance |      |       | $\Omega$ |

**Notes:**

- Typical values are specified at nominal voltage,  $25^{\circ}\text{C}$ , with a 3.2 Gb/s line rate.
- $I_{\text{CC}}$  numbers are given per GTX\_DUAL tile with both GTX transceivers operating with default settings.
- AC coupled TX/RX link.
- Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 39: GTX\_DUAL Tile Quiescent Supply Current

| Symbol         | Description                                                                      | Typ <sup>(1)</sup> | Max  | Units |
|----------------|----------------------------------------------------------------------------------|--------------------|------|-------|
| $I_{AVTTTXQ}$  | Quiescent MGTAVTTTX (transmitter termination) supply current                     | 8.2                | 21.6 | mA    |
| $I_{AVCCPLLQ}$ | Quiescent MGTAVCCPLL (PLL) supply current                                        | 0.8                | 4.8  | mA    |
| $I_{AVTTRXQ}$  | Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ. | 1.2                | 12.0 | mA    |
| $I_{AVCCQ}$    | Quiescent MGTAVCC (analog) supply current                                        | 9.0                | 50.4 | mA    |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTX\_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX\_DUAL tiles in the target TXT or FXT device.

**GTX\_DUAL Tile DC Input and Output Levels**

Table 40 summarizes the DC output specifications of the GTX\_DUAL tiles in Virtex-5 FPGAs. Figure 6 shows the single-ended output voltage swing. Figure 7 shows the peak-to-peak differential output voltage.

Consult [UG198: Virtex-5 FPGA RocketIO GTX Transceiver User Guide](#) for further details.

Table 40: GTX\_DUAL Tile DC Specifications

| Symbol       | DC Parameter                                              | Conditions                           | Min                   | Typ | Max                          | Units    |
|--------------|-----------------------------------------------------------|--------------------------------------|-----------------------|-----|------------------------------|----------|
| $DV_{PPIN}$  | Differential peak-to-peak input voltage                   | External AC coupled $\leq 4.25$ Gb/s | 125                   |     | 1800                         | mV       |
|              |                                                           | External AC coupled $> 4.25$ Gb/s    | 125                   |     | 1800                         | mV       |
| $V_{IN}$     | Absolute input voltage                                    | DC coupled<br>MGTAVTTRX = 1.2V       | -400                  |     | MGTAVTTRX +400<br>up to 1320 | mV       |
| $V_{CMIN}$   | Common mode input voltage                                 | DC coupled<br>MGTAVTTRX = 1.2V       |                       | 800 |                              | mV       |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage <sup>(1)</sup>   | TXBUFDIFFCTRL = 111                  |                       |     | 1400                         | mV       |
| $V_{SEOUT}$  | Single-ended output voltage swing <sup>(1)</sup>          | TXBUFDIFFCTRL = 111                  |                       |     | 700                          | mV       |
| $V_{CMOUT}$  | Common mode output voltage                                | Equation based<br>MGTAVTTTX = 1.2V   | $1200 - DV_{PPOUT}/4$ |     |                              | mV       |
| $R_{IN}$     | Differential input resistance                             |                                      | 85                    | 100 | 120                          | $\Omega$ |
| $R_{OUT}$    | Differential output resistance                            |                                      | 85                    | 100 | 120                          | $\Omega$ |
| $T_{OSKEW}$  | Transmitter output skew                                   |                                      |                       | 2   | 8                            | ps       |
| $C_{EXT}$    | Recommended external AC coupling capacitor <sup>(2)</sup> |                                      | 75                    | 100 | 200                          | nF       |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG198: Virtex-5 FPGA RocketIO GTX Transceiver User Guide](#) and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

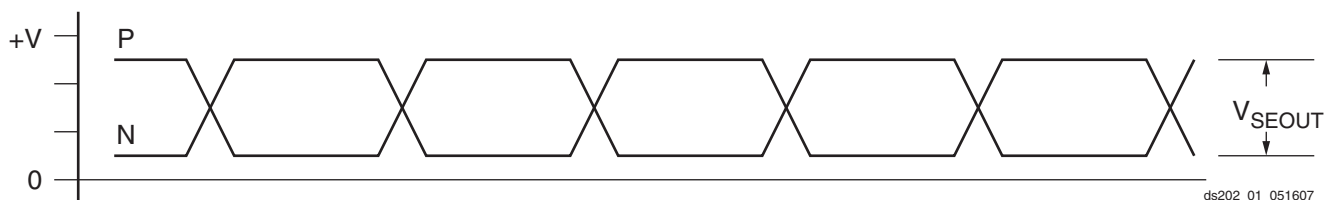


Figure 6: Single-Ended Output Voltage Swing

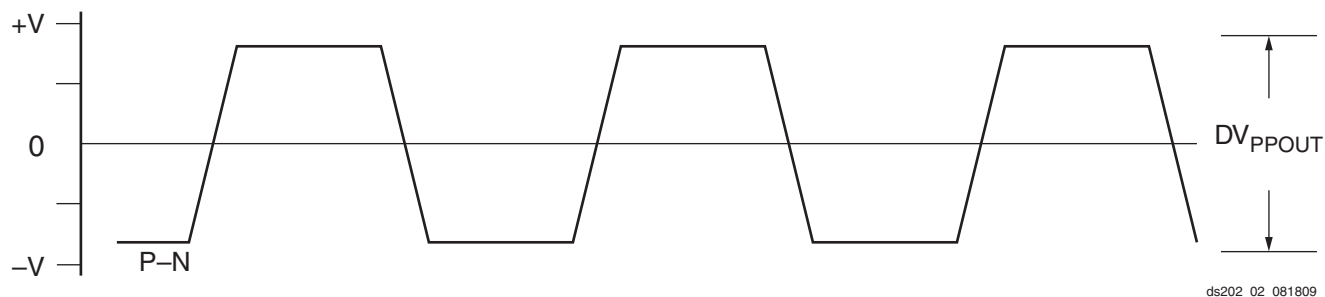


Figure 7: Peak-to-Peak Differential Output Voltage

Table 41 summarizes the DC specifications of the clock input of the GTX\_DUAL tile. Figure 8 shows the single-ended input voltage swing. Figure 9 shows the peak-to-peak differential clock input voltage swing. Consult UG198: Virtex-5 FPGA RocketIO GTX Transceiver User Guide for further details.

Table 41: GTX\_DUAL Tile Clock DC Input Level Specification<sup>(1)</sup>

| Symbol      | DC Parameter                            | Conditions | Min | Typ | Max  | Units    |
|-------------|-----------------------------------------|------------|-----|-----|------|----------|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage |            | 210 | 800 | 2000 | mV       |
| $V_{ISE}$   | Single-ended input voltage              |            | 105 | 400 | 1000 | mV       |
| $R_{IN}$    | Differential input resistance           |            | 90  | 105 | 130  | $\Omega$ |
| $C_{EXT}$   | Required external AC coupling capacitor |            |     | 100 |      | nF       |

**Notes:**

- $V_{MIN} = 0V$  and  $V_{MAX} = 1200mV$

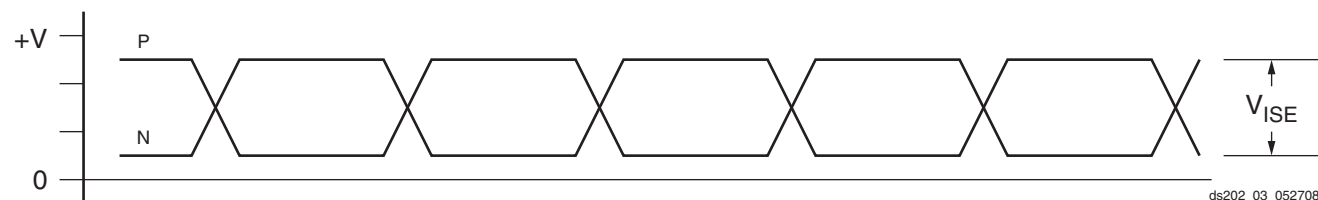


Figure 8: Single-Ended Clock Input Voltage Swing Peak-to-Peak

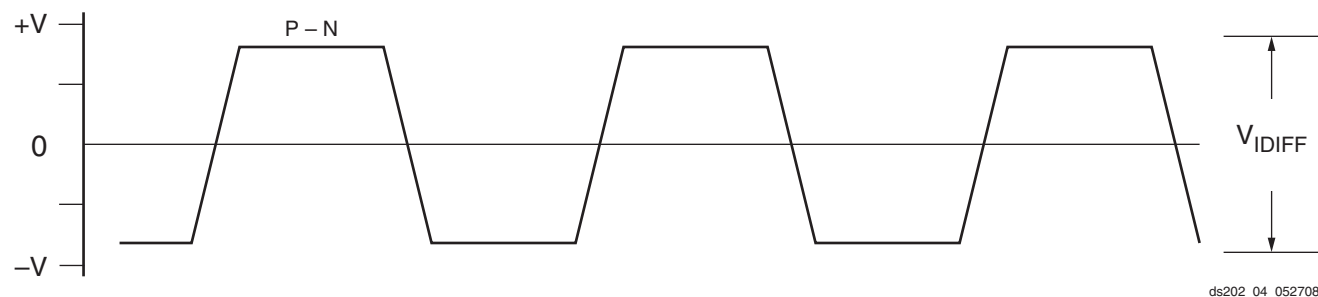


Figure 9: Differential Clock Input Voltage Swing Peak-to-Peak

## GTX\_DUAL Tile Switching Characteristics

Consult [UG198: Virtex-5 FPGA RocketIO GTX Transceiver User Guide](#) for further information.

Table 42: GTX\_DUAL Tile Performance

| Symbol        | Description                       | Speed Grade |      |      | Units |
|---------------|-----------------------------------|-------------|------|------|-------|
|               |                                   | -3          | -2   | -1   |       |
| $F_{GTXMAX}$  | Maximum GTX transceiver data rate | 6.5         | 6.5  | 4.25 | Gb/s  |
| $F_{GPLLMAX}$ | Maximum PLL frequency             | 3.25        | 3.25 | 3.25 | GHz   |
| $F_{GPLLMIN}$ | Minimum PLL frequency             | 1.48        | 1.48 | 1.48 | GHz   |

Table 43: Dynamic Reconfiguration Port (DRP) in the GTX\_DUAL Tile Switching Characteristics

| Symbol          | Description                            | Speed Grade |     |     | Units |
|-----------------|----------------------------------------|-------------|-----|-----|-------|
|                 |                                        | -3          | -2  | -1  |       |
| $F_{GTXDRPCLK}$ | GTX DCLK (DRP clock) maximum frequency | 200         | 175 | 150 | MHz   |

Table 44: GTX\_DUAL Tile Reference Clock Switching Characteristics

| Symbol      | Description                                    | Conditions                                               | All Speed Grades |      |     | Units  |
|-------------|------------------------------------------------|----------------------------------------------------------|------------------|------|-----|--------|
|             |                                                |                                                          | Min              | Typ  | Max |        |
| $F_{GCLK}$  | Reference clock frequency range <sup>(1)</sup> | CLK                                                      | 60               |      | 650 | MHz    |
| $T_{RCLK}$  | Reference clock rise time                      | 20% – 80%                                                |                  | 200  |     | ps     |
| $T_{FCLK}$  | Reference clock fall time                      | 80% – 20%                                                |                  | 200  |     | ps     |
| $T_{DCREF}$ | Reference clock duty cycle                     | CLK                                                      | 40               | 50   | 60  | %      |
| $T_{GJTT}$  | Reference clock total jitter <sup>(2, 3)</sup> | At 100 KHz                                               |                  | –145 |     | dBc/Hz |
|             |                                                | At 1 MHz                                                 |                  | –150 |     | dBc/Hz |
| $T_{LOCK}$  | Clock recovery frequency acquisition time      | Initial PLL lock                                         |                  | 0.25 | 1   | ms     |
| $T_{PHASE}$ | Clock recovery phase acquisition time          | Lock to data after PLL has locked to the reference clock |                  |      | 200 | μs     |

### Notes:

1. GREFCLK can be used for serial bit rates up to 1 Gb/s; however, Jitter Specifications are not guaranteed when using GREFCLK.
2. GTX\_DUAL jitter characteristics measured using a clock with specification  $T_{GJTT}$ . A reference clock with higher phase noise can be used with link margin trade off.
3. The selection of the reference clock is application dependent. This parameter describes the quality of the reference clock used during transceiver jitter characterization - see [Table 46](#) and [Table 47](#).

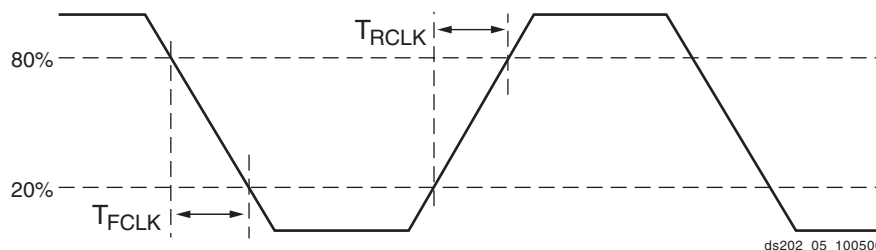


Figure 10: Reference Clock Timing Parameters

Table 45: GTX\_DUAL Tile User Clock Switching Characteristics<sup>(1)</sup>

| Symbol             | Description                 | Conditions               | Device | Speed Grade |         |         | Units |
|--------------------|-----------------------------|--------------------------|--------|-------------|---------|---------|-------|
|                    |                             |                          |        | -3          | -2      | -1      |       |
| F <sub>TXOUT</sub> | TXOUTCLK maximum frequency  | Internal 20-bit datapath | FXT    | 325         | 325     | 212.5   | MHz   |
|                    |                             |                          | TXT    | -           | 325     | 212.5   | MHz   |
|                    |                             | Internal 16-bit datapath | FXT    | 406.25      | 406.25  | 265.625 | MHz   |
|                    |                             |                          | TXT    | -           | 406.25  | 265.625 | MHz   |
| F <sub>RXREC</sub> | RXRECCLK maximum frequency  |                          | FXT    | 406.25      | 406.25  | 265.625 | MHz   |
|                    |                             |                          | TXT    | -           | 406.25  | 265.625 | MHz   |
| T <sub>RX</sub>    | RXUSRCLK maximum frequency  |                          | FXT    | 406.25      | 406.25  | 265.625 | MHz   |
|                    |                             |                          | TXT    | -           | 406.25  | 265.625 | MHz   |
| T <sub>RX2</sub>   | RXUSRCLK2 maximum frequency | 1 byte interface         | FXT    | 375         | 312.5   | 235.625 | MHz   |
|                    |                             | 2 byte interface         |        | 406.25      | 390.625 | 265.625 | MHz   |
|                    |                             | 4 byte interface         |        | 203.125     | 203.125 | 132.813 | MHz   |
|                    |                             | 1 byte interface         | TXT    | -           | 312.5   | 235.625 | MHz   |
|                    |                             | 2 byte interface         |        | -           | 265.625 | 265.625 | MHz   |
|                    |                             | 4 byte interface         |        | -           | 203.125 | 132.813 | MHz   |
| T <sub>TX</sub>    | TXUSRCLK maximum frequency  |                          | FXT    | 406.25      | 406.25  | 265.625 | MHz   |
|                    |                             |                          | TXT    | -           | 406.25  | 265.625 | MHz   |
| T <sub>TX2</sub>   | TXUSRCLK2 maximum frequency | 1 byte interface         | FXT    | 375         | 312.5   | 235.625 | MHz   |
|                    |                             | 2 byte interface         |        | 406.25      | 390.625 | 265.625 | MHz   |
|                    |                             | 4 byte interface         |        | 203.125     | 203.125 | 132.813 | MHz   |
|                    |                             | 1 byte interface         | TXT    | -           | 312.5   | 235.625 | MHz   |
|                    |                             | 2 byte interface         |        | -           | 265.625 | 265.625 | MHz   |
|                    |                             | 4 byte interface         |        | -           | 203.125 | 132.813 | MHz   |

**Notes:**

1. Clocking must be implemented as described in [UG198](#): *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 46: GTX\_DUAL Tile Transmitter Switching Characteristics

| Symbol                       | Description                         | Condition | Min  | Typ | Max                 | Units |
|------------------------------|-------------------------------------|-----------|------|-----|---------------------|-------|
| F <sub>GTXTX</sub>           | Serial data rate range              |           | 0.15 |     | F <sub>GTXMAX</sub> | Gb/s  |
| T <sub>RTX</sub>             | TX Rise time                        | 20%–80%   |      | 120 |                     | ps    |
| T <sub>FTX</sub>             | TX Fall time                        | 80%–20%   |      | 120 |                     | ps    |
| T <sub>LLSKEW</sub>          | TX lane-to-lane skew <sup>(1)</sup> |           |      |     | 350                 | ps    |
| V <sub>TXOOBVDPP</sub>       | Electrical idle amplitude           |           |      |     | 15                  | mV    |
| T <sub>TXOOBTRANSITION</sub> | Electrical idle transition time     |           |      |     | 75                  | ns    |
| T <sub>J6.5</sub>            | Total Jitter <sup>(2)</sup>         | 6.5 Gb/s  |      |     | 0.33                | UI    |
| D <sub>J6.5</sub>            | Deterministic Jitter <sup>(2)</sup> |           |      |     | 0.17                | UI    |
| T <sub>J5.0</sub>            | Total Jitter <sup>(2)</sup>         | 5.0 Gb/s  |      |     | 0.33                | UI    |
| D <sub>J5.0</sub>            | Deterministic Jitter <sup>(2)</sup> |           |      |     | 0.15                | UI    |
| T <sub>J4.25</sub>           | Total Jitter <sup>(2)</sup>         | 4.25 Gb/s |      |     | 0.33                | UI    |
| D <sub>J4.25</sub>           | Deterministic Jitter <sup>(2)</sup> |           |      |     | 0.14                | UI    |

Table 46: GTX\_DUAL Tile Transmitter Switching Characteristics (Cont'd)

| Symbol             | Description                            | Condition               | Min | Typ | Max  | Units |
|--------------------|----------------------------------------|-------------------------|-----|-----|------|-------|
| T <sub>J3.75</sub> | Total Jitter <sup>(2)</sup>            | 3.75 Gb/s               |     |     | 0.34 | UI    |
| D <sub>J3.75</sub> | Deterministic Jitter <sup>(2)</sup>    |                         |     |     | 0.16 | UI    |
| T <sub>J3.2</sub>  | Total Jitter <sup>(2)</sup>            | 3.2 Gb/s                |     |     | 0.20 | UI    |
| D <sub>J3.2</sub>  | Deterministic Jitter <sup>(2)</sup>    |                         |     |     | 0.10 | UI    |
| T <sub>J3.2L</sub> | Total Jitter <sup>(2)</sup>            | 3.2 Gb/s <sup>(3)</sup> |     |     | 0.36 | UI    |
| D <sub>J3.2L</sub> | Deterministic Jitter <sup>(2)</sup>    |                         |     |     | 0.16 | UI    |
| T <sub>J2.5</sub>  | Total Jitter <sup>(2)</sup>            | 2.5 Gb/s                |     |     | 0.20 | UI    |
| D <sub>J2.5</sub>  | Deterministic Jitter <sup>(2)</sup>    |                         |     |     | 0.08 | UI    |
| T <sub>J1.25</sub> | Total Jitter <sup>(2)</sup>            | 1.25 Gb/s               |     |     | 0.15 | UI    |
| D <sub>J1.25</sub> | Deterministic Jitter <sup>(2)</sup>    |                         |     |     | 0.06 | UI    |
| T <sub>J750</sub>  | Total Jitter <sup>(2)(4)</sup>         | 750 Mb/s                |     |     | 0.10 | UI    |
| D <sub>J750</sub>  | Deterministic Jitter <sup>(2)(4)</sup> |                         |     |     | 0.03 | UI    |
| T <sub>J150</sub>  | Total Jitter <sup>(2)(4)</sup>         | 150 Mb/s                |     |     | 0.02 | UI    |
| D <sub>J150</sub>  | Deterministic Jitter <sup>(2)(4)</sup> |                         |     |     | 0.01 | UI    |

**Notes:**

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX\_DUAL sites.
- Using PLL\_DIVSEL\_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.
- PLL frequency at 1.6 GHz and OUTDIV = 1.
- GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.

Table 47: GTX\_DUAL Tile Receiver Switching Characteristics

| Symbol                             | Description                                                   |                                          | Min   | Typ | Max                 | Units |
|------------------------------------|---------------------------------------------------------------|------------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTXRX</sub>                 | Serial data rate                                              | RX oversampler not enabled               | 0.75  |     | F <sub>GTXMAX</sub> | Gb/s  |
|                                    |                                                               | RX oversampler enabled                   | 0.15  |     | 0.75                | Gb/s  |
| T <sub>RXELECIDLE</sub>            | Time for RXELECIDLE to respond to loss or restoration of data | OObDETECT_THRESHOLD = 110                |       |     | 75                  | ns    |
| R <sub>XOObVDPP</sub>              | OOb detect threshold peak-to-peak                             | OObDETECT_THRESHOLD = 110                | 55    |     | 135                 | mV    |
| R <sub>XSST</sub>                  | Receiver spread-spectrum tracking <sup>(1)</sup>              | Modulated @ 33 KHz                       | −5000 |     | 0                   | ppm   |
| R <sub>XRL</sub>                   | Run length (CID)                                              | Internal AC capacitor bypassed           |       |     | 512                 | UI    |
| R <sub>XPMTOL</sub>                | Data/REFCLK PPM offset tolerance <sup>(2)</sup>               | CDR 2 <sup>nd</sup> -order loop disabled | −200  |     | 200                 | ppm   |
|                                    |                                                               | CDR 2 <sup>nd</sup> -order loop enabled  | −2000 |     | 2000                | ppm   |
| SJ Jitter Tolerance <sup>(3)</sup> |                                                               |                                          |       |     |                     |       |
| JT_SJ <sub>6.5</sub>               | Sinusoidal Jitter <sup>(4)</sup>                              | 6.5 Gb/s                                 | 0.44  |     |                     | UI    |
| JT_SJ <sub>5.0</sub>               | Sinusoidal Jitter <sup>(4)</sup>                              | 5.0 Gb/s                                 | 0.44  |     |                     | UI    |
| JT_SJ <sub>4.25</sub>              | Sinusoidal Jitter <sup>(4)</sup>                              | 4.25 Gb/s                                | 0.44  |     |                     | UI    |
| JT_SJ <sub>3.75</sub>              | Sinusoidal Jitter <sup>(4)</sup>                              | 3.75 Gb/s                                | 0.44  |     |                     | UI    |
| JT_SJ <sub>3.2</sub>               | Sinusoidal Jitter <sup>(4)</sup>                              | 3.2 Gb/s                                 | 0.45  |     |                     | UI    |
| JT_SJ <sub>3.2L</sub>              | Sinusoidal Jitter <sup>(4)</sup>                              | 3.2 Gb/s <sup>(5)</sup>                  | 0.45  |     |                     | UI    |
| JT_SJ <sub>2.5</sub>               | Sinusoidal Jitter <sup>(4)</sup>                              | 2.5 Gb/s                                 | 0.50  |     |                     | UI    |
| JT_SJ <sub>1.25</sub>              | Sinusoidal Jitter <sup>(4)</sup>                              | 1.25 Gb/s                                | 0.50  |     |                     | UI    |

Table 47: GTX\_DUAL Tile Receiver Switching Characteristics (Cont'd)

| Symbol                                                     | Description                                        |           | Min  | Typ | Max | Units |
|------------------------------------------------------------|----------------------------------------------------|-----------|------|-----|-----|-------|
| JT_SJ <sub>750</sub>                                       | Sinusoidal Jitter <sup>(4)(6)</sup>                | 750 Mb/s  | 0.57 |     |     | UI    |
| JT_SJ <sub>150</sub>                                       | Sinusoidal Jitter <sup>(4)(6)</sup>                | 150 Mb/s  | 0.57 |     |     | UI    |
| <b>SJ Jitter Tolerance with Stressed Eye<sup>(3)</sup></b> |                                                    |           |      |     |     |       |
| JT_TJSE <sub>4.25</sub>                                    | Total Jitter with Stressed Eye <sup>(7)</sup>      | 4.25 Gb/s | 0.69 |     |     | UI    |
| JT_SJSE <sub>4.25</sub>                                    | Sinusoidal Jitter with Stressed Eye <sup>(7)</sup> | 4.25 Gb/s | 0.1  |     |     | UI    |

**Notes:**

- Using PLL\_RXDIVSEL\_OUT = 1, 2, and 4.
- Indicates the maximum offset between the receiver reference clock and the serial data. For example, a reference clock with  $\pm 100$  ppm resolution results in a maximum offset of 200 ppm between the reference clock and the serial data.
- All jitter values are based on a Bit Error Ratio of  $1e^{-12}$ .
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- PLL frequency at 1.6 GHz and OUTDIV = 1.
- GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.
- Composite jitter with RX equalizer enabled. DFE disabled.

## CRC Block Switching Characteristics

Table 48: CRC Block Switching Characteristics

| Symbol           | Description              | Speed Grade |     |     | Units |
|------------------|--------------------------|-------------|-----|-----|-------|
|                  |                          | -3          | -2  | -1  |       |
| F <sub>CRC</sub> | CRCCLK maximum frequency | 325         | 325 | 270 | MHz   |

## Ethernet MAC Switching Characteristics

Consult [UG194](#): *Virtex-5 FPGA Tri-mode Ethernet Media Access Controller User Guide* for further information.

Table 49: Maximum Ethernet MAC Performance

| Symbol                   | Description                          | Conditions               | Speed Grade |      |      | Units |
|--------------------------|--------------------------------------|--------------------------|-------------|------|------|-------|
|                          |                                      |                          | -3          | -2   | -1   |       |
| F <sub>TEMACCLIENT</sub> | Client interface maximum frequency   | 10 Mb/s – 8-bit width    | 1.25        | 1.25 | 1.25 | MHz   |
|                          |                                      | 100 Mb/s – 8-bit width   | 12.5        | 12.5 | 12.5 | MHz   |
|                          |                                      | 1000 Mb/s – 8-bit width  | 125         | 125  | 125  | MHz   |
|                          |                                      | 2000 Mb/s – 16-bit width | 125         | 125  | 125  | MHz   |
| F <sub>TEMACPHY</sub>    | Physical interface maximum frequency | 10 Mb/s – 4-bit width    | 2.5         | 2.5  | 2.5  | MHz   |
|                          |                                      | 100 Mb/s – 4-bit width   | 25          | 25   | 25   | MHz   |
|                          |                                      | 1000 Mb/s – 8-bit width  | 125         | 125  | 125  | MHz   |
|                          |                                      | 2000 Mb/s – 8-bit width  | 250         | 250  | 250  | MHz   |

## Endpoint Block for PCI Express Designs Switching Characteristics

Consult [UG197](#): *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* for further information.

Table 50: Maximum Performance for PCI Express Designs

| Symbol                | Description                  | Speed Grade |     |     | Units |
|-----------------------|------------------------------|-------------|-----|-----|-------|
|                       |                              | -3          | -2  | -1  |       |
| F <sub>PCIECORE</sub> | Core clock maximum frequency | 250         | 250 | 250 | MHz   |
| F <sub>PCIEUSER</sub> | User clock maximum frequency | 250         | 250 | 250 | MHz   |

# System Monitor Analog-to-Digital Converter Specification

Table 51: Analog-to-Digital Specifications

| Parameter                                                                                                                                                                                          | Symbol             | Comments/Conditions                                                                        | Min   | Typ   | Max   | Units     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------------------------------------------|-------|-------|-------|-----------|
| AV <sub>DD</sub> = 2.5V ± 2%, V <sub>REFP</sub> = 2.5V, V <sub>REFN</sub> = 0V, ADCCLK = 5.2 MHz, T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub> , Typical values at T <sub>A</sub> = +25°C |                    |                                                                                            |       |       |       |           |
| <b>DC Accuracy:</b> All external input channels such as V <sub>P</sub> /V <sub>N</sub> and V <sub>AUXP</sub> [15:0]/V <sub>AUXN</sub> [15:0], Unipolar Mode, and Common Mode = 0V                  |                    |                                                                                            |       |       |       |           |
| Resolution                                                                                                                                                                                         |                    |                                                                                            | 10    |       |       | Bits      |
| Integral Nonlinearity                                                                                                                                                                              | INL                |                                                                                            |       |       | ±2    | LSBs      |
| Differential Nonlinearity                                                                                                                                                                          | DNL                | No missing codes (T <sub>MIN</sub> to T <sub>MAX</sub> )<br>Guaranteed Monotonic           |       |       | ±0.9  | LSBs      |
| Unipolar Offset Error <sup>(1)</sup>                                                                                                                                                               |                    | Uncalibrated                                                                               |       | ±2    | ±30   | LSBs      |
| Bipolar Offset Error <sup>(1)</sup>                                                                                                                                                                |                    | Uncalibrated measured in bipolar mode                                                      |       | ±2    | ±30   | LSBs      |
| Gain Error <sup>(1)</sup>                                                                                                                                                                          |                    | Uncalibrated                                                                               |       | ±0.2  | ±2    | %         |
| Bipolar Gain Error <sup>(1)</sup>                                                                                                                                                                  |                    | Uncalibrated measured in bipolar mode                                                      |       | ±0.2  | ±2    | %         |
| Total Unadjusted Error (Uncalibrated)                                                                                                                                                              | TUE                | Deviation from ideal transfer function.<br>V <sub>REFP</sub> - V <sub>REFN</sub> = 2.5V    |       | ±10   |       | LSBs      |
| Total Unadjusted Error (Calibrated)                                                                                                                                                                | TUE                | Deviation from ideal transfer function.<br>V <sub>REFP</sub> - V <sub>REFN</sub> = 2.5V    |       | ±1    | ±2    | LSBs      |
| Calibrated Gain Temperature Coefficient                                                                                                                                                            |                    | Variation of FS code with temperature                                                      |       | ±0.01 |       | LSB/°C    |
| DC Common-Mode Reject                                                                                                                                                                              | CMRR <sub>DC</sub> | V <sub>N</sub> = V <sub>CM</sub> = 0.5V ± 0.5V,<br>V <sub>P</sub> - V <sub>N</sub> = 100mV |       | 70    |       | dB        |
| <b>Conversion Rate<sup>(2)</sup></b>                                                                                                                                                               |                    |                                                                                            |       |       |       |           |
| Conversion Time - Continuous                                                                                                                                                                       | t <sub>CONV</sub>  | Number of CLK cycles                                                                       | 26    |       | 32    |           |
| Conversion Time - Event                                                                                                                                                                            | t <sub>CONV</sub>  | Number of CLK cycles                                                                       |       |       | 21    |           |
| T/H Acquisition Time                                                                                                                                                                               | t <sub>ACQ</sub>   | Number of CLK cycles                                                                       | 4     |       |       |           |
| DRP Clock Frequency                                                                                                                                                                                | DCLK               | DRP clock frequency                                                                        | 8     |       | 250   | MHz       |
| ADC Clock Frequency                                                                                                                                                                                | ADCCLK             | Derived from DCLK                                                                          | 1     |       | 5.2   | MHz       |
| CLK Duty cycle                                                                                                                                                                                     |                    |                                                                                            | 40    |       | 60    | %         |
| <b>Analog Inputs<sup>(3)</sup></b>                                                                                                                                                                 |                    |                                                                                            |       |       |       |           |
| Dedicated Analog Inputs<br>Input Voltage Range<br>V <sub>P</sub> - V <sub>N</sub>                                                                                                                  |                    | Unipolar Operation                                                                         | 0     |       | 1     | Volts     |
|                                                                                                                                                                                                    |                    | Differential Inputs                                                                        | -0.25 |       | +0.25 |           |
|                                                                                                                                                                                                    |                    | Unipolar Common Mode Range (FS input)                                                      | 0     |       | +0.5  |           |
|                                                                                                                                                                                                    |                    | Differential Common Mode Range (FS input)                                                  | +0.3  |       | +0.7  |           |
|                                                                                                                                                                                                    |                    | Bandwidth                                                                                  |       | 20    |       | MHz       |
| Auxiliary Analog Inputs<br>Input Voltage Range<br>V <sub>AUXP</sub> [0]/V <sub>AUXN</sub> [0] to V <sub>AUXP</sub> [15]/V <sub>AUXN</sub> [15]                                                     |                    | Unipolar Operation                                                                         | 0     |       | 1     | Volts     |
|                                                                                                                                                                                                    |                    | Differential Operation                                                                     | -0.25 |       | +0.25 |           |
|                                                                                                                                                                                                    |                    | Unipolar Common Mode Range (FS input)                                                      | 0     |       | +0.5  |           |
|                                                                                                                                                                                                    |                    | Differential Common Mode Range (FS input)                                                  | +0.3  |       | +0.7  |           |
|                                                                                                                                                                                                    |                    | Bandwidth                                                                                  |       | 10    |       | kHz       |
| Input Leakage Current                                                                                                                                                                              |                    | A/D not converting, ADCCLK stopped                                                         |       | ±1.0  |       | µA        |
| Input Capacitance                                                                                                                                                                                  |                    |                                                                                            |       | 10    |       | pF        |
| On-chip Supply Monitor Error                                                                                                                                                                       |                    | V <sub>CCINT</sub> and V <sub>CCAUX</sub> with calibration enabled                         |       |       | ±1.0  | % Reading |
| On-chip Temperature Monitor Error                                                                                                                                                                  |                    | -40°C to +125°C with calibration enabled                                                   |       |       | ±4    | °C        |

Table 51: Analog-to-Digital Specifications (Cont'd)

| Parameter                                      | Symbol     | Comments/Conditions             | Min  | Typ | Max  | Units   |
|------------------------------------------------|------------|---------------------------------|------|-----|------|---------|
| <b>External Reference Inputs<sup>(4)</sup></b> |            |                                 |      |     |      |         |
| Positive Reference Input Voltage Range         | $V_{REFP}$ | Measured Relative to $V_{REFN}$ | 2.45 | 2.5 | 2.55 | Volts   |
| Negative Reference Input Voltage Range         | $V_{REFN}$ | Measured Relative to AGND       | -50  | 0   | 100  | mV      |
| Input current                                  | $I_{REF}$  | ADCCLK = 5.2 MHz                |      |     | 100  | $\mu$ A |
| <b>Power Requirements</b>                      |            |                                 |      |     |      |         |
| Analog Power Supply                            | $AV_{DD}$  | Measured Relative to $AV_{SS}$  | 2.45 | 2.5 | 2.55 | Volts   |
| Analog Supply Current                          | $AI_{DD}$  | ADCCLK = 5.2 MHz                | 5    |     | 13   | mA      |

**Notes:**

- Offset and gain errors are removed by enabling the System Monitor automatic gain calibration feature. See [UG192: Virtex-5 FPGA System Monitor User Guide](#).
- See "System Monitor Timing" in [UG192: Virtex-5 FPGA System Monitor User Guide](#).
- See "Analog Inputs" in [UG192: Virtex-5 FPGA System Monitor User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal  $V_{REFP} = 2.5V$  and  $V_{REFN} = 0V$  will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing the supply voltage and reference to vary by  $\pm 2\%$  is permitted.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-5 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 30](#). [Table 52](#) shows internal (register-to-register) performance.

Table 52: Register-to-Register Performance

| Description                                      | Register-to-Register (with I/O Delays) |     |     | Units |
|--------------------------------------------------|----------------------------------------|-----|-----|-------|
|                                                  | Speed Grade                            |     |     |       |
|                                                  | -3                                     | -2  | -1  |       |
| Basic Functions                                  |                                        |     |     |       |
| 16:1 Multiplexer                                 | 550                                    | 500 | 450 | MHz   |
| 32:1 Multiplexer                                 | 550                                    | 500 | 450 | MHz   |
| 64:1 Multiplexer                                 | 511                                    | 467 | 407 | MHz   |
| 9 x 9 Logic Multiplier with 4 pipe stages        | 468                                    | 438 | 428 | MHz   |
| 9 x 9 Logic Multiplier with 5 pipe stages        | 550                                    | 500 | 428 | MHz   |
| 16-bit Adder                                     | 550                                    | 500 | 450 | MHz   |
| 32-bit Adder                                     | 550                                    | 500 | 447 | MHz   |
| 64-bit Adder                                     | 423                                    | 377 | 323 | MHz   |
| Register to LUT to Register                      | 550                                    | 500 | 450 | MHz   |
| 16-bit Counter                                   | 550                                    | 500 | 450 | MHz   |
| 32-bit Counter                                   | 550                                    | 500 | 450 | MHz   |
| 64-bit Counter                                   | 428                                    | 381 | 333 | MHz   |
| Memory                                           |                                        |     |     |       |
| Cascaded block RAM (64K)                         | 500                                    | 450 | 400 | MHz   |
| Block RAM Pipelined                              |                                        |     |     |       |
| Single-Port 512 x 36 bits                        | 550                                    | 500 | 450 | MHz   |
| Single-Port 4096 x 4 bits                        | 550                                    | 500 | 450 | MHz   |
| Dual-Port A: 4096 x 4 bits and B: 1024 x 18 bits | 550                                    | 500 | 450 | MHz   |
| Distributed RAM                                  |                                        |     |     |       |
| Single-Port 16 x 8                               | 550                                    | 500 | 450 | MHz   |
| Single-Port 32 x 8                               | 550                                    | 500 | 450 | MHz   |
| Single-Port 64 x 8                               | 550                                    | 500 | 450 | MHz   |
| Dual-Port 16 x 8                                 |                                        |     |     | MHz   |
| Shift Register Chain                             |                                        |     |     |       |
| 16-bit                                           | 550                                    | 500 | 450 | MHz   |
| 32-bit                                           | 550                                    | 500 | 450 | MHz   |
| 64-bit                                           | 550                                    | 500 | 438 | MHz   |

Table 52: Register-to-Register Performance (Cont'd)

| Description                                | Register-to-Register (with I/O Delays) |     |     | Units |
|--------------------------------------------|----------------------------------------|-----|-----|-------|
|                                            | Speed Grade                            |     |     |       |
|                                            | -3                                     | -2  | -1  |       |
| Dedicated Arithmetic Logic                 |                                        |     |     |       |
| DSP48E Quad 12-bit Adder/Subtractor        | 550                                    | 500 | 450 | MHz   |
| DSP48E Dual 24-bit Adder/Subtractor        | 550                                    | 500 | 450 | MHz   |
| DSP48E 48-bit Adder/Subtractor             | 550                                    | 500 | 450 | MHz   |
| DSP48E 48-bit Counter                      | 550                                    | 500 | 450 | MHz   |
| DSP48E 48-bit Comparator                   | 550                                    | 500 | 450 | MHz   |
| DSP48E 25 x 18 bit Pipelined Multiplier    | 550                                    | 500 | 450 | MHz   |
| DSP48E Direct 4-tap FIR Filter Pipelined   | 510                                    | 458 | 397 | MHz   |
| DSP48E Systolic n-tap FIR Filter Pipelined | 550                                    | 500 | 450 | MHz   |

**Notes:**

1. Device used is the XC5VLX50T- FF1136

Table 53: Interface Performances

| Description                                 | Speed Grade |           |          |
|---------------------------------------------|-------------|-----------|----------|
|                                             | -3          | -2        | -1       |
| <b>Networking Applications</b>              |             |           |          |
| SFI-4.1 (SDR LVDS Interface) <sup>(1)</sup> | 710 MHz     | 710 MHz   | 645 MHz  |
| SPI-4.2 (DDR LVDS Interface) <sup>(2)</sup> | 1.25 Gb/s   | 1.25 Gb/s | 1.0 Gb/s |
| <b>Memory Interfaces</b>                    |             |           |          |
| DDR <sup>(3)</sup>                          | 200 MHz     | 200 MHz   | 200 MHz  |
| DDR2 <sup>(4)</sup>                         | 333 MHz     | 300 MHz   | 267 MHz  |
| QDR II SRAM <sup>(5)</sup>                  | 300 MHz     | 300 MHz   | 250 MHz  |
| RLDRAM II <sup>(6)</sup>                    | 333 MHz     | 300 MHz   | 250 MHz  |

**Notes:**

1. Performance defined using design implementation described in application note XAPP856: SFI-4.1 16-Channel SDR Interface with Bus Alignment
2. Performance defined using design implementation described in application note XAPP860: 16-Channel, DDR LVDS Interface with Real-time Window Monitoring
3. Performance defined using design implementation described in application note XAPP851: DDR SDRAM Controller
4. Performance defined using design implementation described in application note XAPP858: High-Performance DDR2 SDRAM Interface Data Capture
5. Performance defined using design implementation described in application note XAPP853: QDR II SRAM Interface
6. Performance defined using design implementation described in application note XAPP852: Synthesizable RLDRAM II Controller

## Switching Characteristics

All values represented in this data sheet are based on speed specification version 1.62. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

[Table 54](#) correlates the current status of each Virtex-5 device on a per speed grade basis.

**Table 54: Virtex-5 Device Speed Grade Designations**

| Device     | Speed Grade Designations |             |            |
|------------|--------------------------|-------------|------------|
|            | Advance                  | Preliminary | Production |
| XC5VLX20T  |                          |             | -2, -1     |
| XC5VLX30   |                          |             | -3, -2, -1 |
| XC5VLX30T  |                          |             | -3, -2, -1 |
| XC5VLX50   |                          |             | -3, -2, -1 |
| XC5VLX50T  |                          |             | -3, -2, -1 |
| XC5VLX85   |                          |             | -3, -2, -1 |
| XC5VLX85T  |                          |             | -3, -2, -1 |
| XC5VLX110  |                          |             | -3, -2, -1 |
| XC5VLX110T |                          |             | -3, -2, -1 |
| XC5VLX155  |                          |             | -3, -2, -1 |
| XC5VLX155T |                          |             | -3, -2, -1 |
| XC5VLX220  |                          |             | -2, -1     |
| XC5VLX220T |                          |             | -2, -1     |
| XC5VLX330  |                          |             | -2, -1     |
| XC5VLX330T |                          |             | -2, -1     |
| XC5VSX35T  |                          |             | -3, -2, -1 |
| XC5VSX50T  |                          |             | -3, -2, -1 |
| XC5VSX95T  |                          |             | -2, -1     |
| XC5VSX240T |                          |             | -2, -1     |
| XC5VTX150T |                          |             | -2, -1     |
| XC5VTX240T |                          |             | -2, -1     |
| XC5VFX30T  |                          |             | -3, -2, -1 |
| XC5VFX70T  |                          |             | -3, -2, -1 |
| XC5VFX100T |                          |             | -3, -2, -1 |
| XC5VFX130T |                          |             | -3, -2, -1 |
| XC5VFX200T |                          |             | -2, -1     |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-5 devices.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. [Table 55](#) lists the production released Virtex-5 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

**Table 55: Virtex-5 Device Production Software and Speed Specification Release**

| Device     | Speed Grade Designations |                    |    |
|------------|--------------------------|--------------------|----|
|            | -3                       | -2                 | -1 |
| XC5VLX20T  | N/A                      | ISE 10.1 SP2 v1.61 |    |
| XC5VLX30   | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX30T  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX50   | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX50T  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX85   | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX85T  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX110  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX110T | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VLX155  | ISE 10.1 SP2 v1.61       |                    |    |
| XC5VLX155T | ISE 10.1 SP2 v1.61       |                    |    |
| XC5VLX220  | N/A                      | ISE 9.2i SP4 v1.58 |    |
| XC5VLX220T | N/A                      | ISE 9.2i SP4 v1.58 |    |
| XC5VLX330  | N/A                      | ISE 9.2i SP4 v1.58 |    |
| XC5VLX330T | N/A                      | ISE 9.2i SP4 v1.58 |    |
| XC5VSX35T  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VSX50T  | ISE 9.2i SP4 v1.58       |                    |    |
| XC5VSX95T  | N/A                      | ISE 9.2i SP4 v1.58 |    |
| XC5VSX240T | N/A                      | ISE 10.1 SP3 v1.63 |    |
| XC5VTX150T | N/A                      | ISE 10.1 SP3 v1.63 |    |
| XC5VTX240T | N/A                      | ISE 10.1 SP3 v1.63 |    |
| XC5VFX30T  | ISE 10.1 SP3 v1.63       |                    |    |
| XC5VFX70T  | ISE 10.1 SP3 v1.63       |                    |    |
| XC5VFX100T | ISE 10.1 SP3 v1.63       |                    |    |
| XC5VFX130T | ISE 10.1 SP3 v1.63       |                    |    |
| XC5VFX200T | N/A                      | ISE 10.1 SP3 v1.63 |    |

### Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

## IOB Pad Input/Output/3-State Switching Characteristics

Table 56 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 57 summarizes the value of  $T_{IOTPHZ}$ .  $T_{IOTPHZ}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 56: IOB Switching Characteristics

| I/O Standard             | T <sub>IOPI</sub> |      |      | T <sub>IOOP</sub> |      |      | T <sub>IOTP</sub> |      |      | Units |
|--------------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
|                          | Speed Grade       |      |      | Speed Grade       |      |      | Speed Grade       |      |      |       |
|                          | -3                | -2   | -1   | -3                | -2   | -1   | -3                | -2   | -1   |       |
| LVDS_25                  | 0.80              | 0.90 | 1.06 | 1.13              | 1.29 | 1.44 | 1.13              | 1.29 | 1.44 | ns    |
| LVDSEXT_25               | 1.01              | 1.16 | 1.30 | 1.17              | 1.34 | 1.49 | 1.17              | 1.34 | 1.49 | ns    |
| HT_25                    | 0.80              | 0.90 | 1.06 | 1.10              | 1.26 | 1.40 | 1.10              | 1.26 | 1.40 | ns    |
| BLVDS_25                 | 0.80              | 0.90 | 1.06 | 1.24              | 1.38 | 1.58 | 1.24              | 1.38 | 1.58 | ns    |
| RSDS_25 (point to point) | 0.80              | 0.90 | 1.06 | 1.13              | 1.29 | 1.44 | 1.13              | 1.29 | 1.44 | ns    |
| ULVDS_25                 | 0.80              | 0.90 | 1.06 | 1.10              | 1.27 | 1.41 | 1.10              | 1.27 | 1.41 | ns    |
| PCI33_3                  | 0.62              | 0.70 | 0.82 | 1.85              | 2.06 | 2.38 | 1.85              | 2.06 | 2.38 | ns    |
| PCI66_3                  | 0.62              | 0.70 | 0.82 | 1.85              | 2.06 | 2.38 | 1.85              | 2.06 | 2.38 | ns    |
| PCI-X                    | 0.62              | 0.70 | 0.82 | 1.40              | 1.56 | 1.80 | 1.40              | 1.56 | 1.80 | ns    |
| GTL                      | 0.76              | 0.85 | 1.00 | 1.47              | 1.63 | 1.86 | 1.47              | 1.63 | 1.86 | ns    |
| GTLP                     | 0.76              | 0.85 | 1.00 | 1.51              | 1.68 | 1.93 | 1.51              | 1.68 | 1.93 | ns    |
| HSTL_I                   | 0.76              | 0.85 | 1.00 | 1.42              | 1.57 | 1.79 | 1.42              | 1.57 | 1.79 | ns    |
| HSTL_II                  | 0.76              | 0.85 | 1.00 | 1.39              | 1.53 | 1.74 | 1.39              | 1.53 | 1.74 | ns    |
| HSTL_III                 | 0.76              | 0.85 | 1.00 | 1.44              | 1.60 | 1.85 | 1.44              | 1.60 | 1.85 | ns    |
| HSTL_IV                  | 0.76              | 0.85 | 1.00 | 1.44              | 1.60 | 1.83 | 1.44              | 1.60 | 1.83 | ns    |
| HSTL_I_18                | 0.76              | 0.85 | 1.00 | 1.40              | 1.55 | 1.77 | 1.40              | 1.55 | 1.77 | ns    |
| HSTL_II_18               | 0.76              | 0.85 | 1.00 | 1.36              | 1.51 | 1.72 | 1.36              | 1.51 | 1.72 | ns    |
| HSTL_III_18              | 0.76              | 0.85 | 1.00 | 1.45              | 1.61 | 1.85 | 1.45              | 1.61 | 1.85 | ns    |
| HSTL_IV_18               | 0.76              | 0.85 | 1.00 | 1.41              | 1.57 | 1.81 | 1.41              | 1.57 | 1.81 | ns    |
| SSTL2_I                  | 0.76              | 0.85 | 1.00 | 1.48              | 1.64 | 1.87 | 1.48              | 1.64 | 1.87 | ns    |
| SSTL2_II                 | 0.76              | 0.85 | 1.00 | 1.40              | 1.55 | 1.76 | 1.40              | 1.55 | 1.76 | ns    |
| LVTTL, Slow, 2 mA        | 0.62              | 0.70 | 0.82 | 4.10              | 4.47 | 5.01 | 4.10              | 4.47 | 5.01 | ns    |
| LVTTL, Slow, 4 mA        | 0.62              | 0.70 | 0.82 | 2.87              | 3.09 | 3.41 | 2.87              | 3.09 | 3.41 | ns    |
| LVTTL, Slow, 6 mA        | 0.62              | 0.70 | 0.82 | 2.66              | 2.91 | 3.29 | 2.66              | 2.91 | 3.29 | ns    |
| LVTTL, Slow, 8 mA        | 0.62              | 0.70 | 0.82 | 2.09              | 2.30 | 2.61 | 2.09              | 2.30 | 2.61 | ns    |
| LVTTL, Slow, 12 mA       | 0.62              | 0.70 | 0.82 | 1.94              | 2.15 | 2.46 | 1.94              | 2.15 | 2.46 | ns    |
| LVTTL, Slow, 16 mA       | 0.62              | 0.70 | 0.82 | 1.84              | 2.04 | 2.34 | 1.84              | 2.04 | 2.34 | ns    |
| LVTTL, Slow, 24 mA       | 0.62              | 0.70 | 0.82 | 1.87              | 2.07 | 2.38 | 1.87              | 2.07 | 2.38 | ns    |

Table 56: IOB Switching Characteristics (Cont'd)

| I/O Standard           | T <sub>IOPI</sub> |      |      | T <sub>IOOP</sub> |      |      | T <sub>IOTP</sub> |      |      | Units |
|------------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
|                        | Speed Grade       |      |      | Speed Grade       |      |      | Speed Grade       |      |      |       |
|                        | -3                | -2   | -1   | -3                | -2   | -1   | -3                | -2   | -1   |       |
| LVTTL, Fast, 2 mA      | 0.62              | 0.70 | 0.82 | 3.32              | 3.61 | 4.05 | 3.32              | 3.61 | 4.05 | ns    |
| LVTTL, Fast, 4 mA      | 0.62              | 0.70 | 0.82 | 2.32              | 2.55 | 2.90 | 2.32              | 2.55 | 2.90 | ns    |
| LVTTL, Fast, 6 mA      | 0.62              | 0.70 | 0.82 | 2.10              | 2.31 | 2.63 | 2.10              | 2.31 | 2.63 | ns    |
| LVTTL, Fast, 8 mA      | 0.62              | 0.70 | 0.82 | 1.65              | 1.82 | 2.09 | 1.65              | 1.82 | 2.09 | ns    |
| LVTTL, Fast, 12 mA     | 0.62              | 0.70 | 0.82 | 1.47              | 1.63 | 1.89 | 1.47              | 1.63 | 1.89 | ns    |
| LVTTL, Fast, 16 mA     | 0.62              | 0.70 | 0.82 | 1.41              | 1.57 | 1.81 | 1.41              | 1.57 | 1.81 | ns    |
| LVTTL, Fast, 24 mA     | 0.62              | 0.70 | 0.82 | 1.36              | 1.52 | 1.74 | 1.36              | 1.52 | 1.74 | ns    |
| LVC MOS33, Slow, 2 mA  | 0.62              | 0.70 | 0.82 | 3.63              | 3.96 | 4.44 | 3.63              | 3.96 | 4.44 | ns    |
| LVC MOS33, Slow, 4 mA  | 0.62              | 0.70 | 0.82 | 2.82              | 3.09 | 3.49 | 2.82              | 3.09 | 3.49 | ns    |
| LVC MOS33, Slow, 6 mA  | 0.62              | 0.70 | 0.82 | 2.61              | 2.86 | 3.24 | 2.61              | 2.86 | 3.24 | ns    |
| LVC MOS33, Slow, 8 mA  | 0.62              | 0.70 | 0.82 | 2.06              | 2.26 | 2.57 | 2.06              | 2.26 | 2.57 | ns    |
| LVC MOS33, Slow, 12 mA | 0.62              | 0.70 | 0.82 | 1.95              | 2.14 | 2.42 | 1.95              | 2.14 | 2.42 | ns    |
| LVC MOS33, Slow, 16 mA | 0.62              | 0.70 | 0.82 | 1.86              | 2.04 | 2.31 | 1.86              | 2.04 | 2.31 | ns    |
| LVC MOS33, Slow, 24 mA | 0.62              | 0.70 | 0.82 | 1.87              | 2.07 | 2.35 | 1.87              | 2.07 | 2.35 | ns    |
| LVC MOS33, Fast, 2 mA  | 0.62              | 0.70 | 0.82 | 2.94              | 3.20 | 3.59 | 2.94              | 3.20 | 3.59 | ns    |
| LVC MOS33, Fast, 4 mA  | 0.62              | 0.70 | 0.82 | 2.27              | 2.50 | 2.84 | 2.27              | 2.50 | 2.84 | ns    |
| LVC MOS33, Fast, 6 mA  | 0.62              | 0.70 | 0.82 | 2.06              | 2.27 | 2.59 | 2.06              | 2.27 | 2.59 | ns    |
| LVC MOS33, Fast, 8 mA  | 0.62              | 0.70 | 0.82 | 1.61              | 1.79 | 2.05 | 1.61              | 1.79 | 2.05 | ns    |
| LVC MOS33, Fast, 12 mA | 0.62              | 0.70 | 0.82 | 1.45              | 1.61 | 1.86 | 1.45              | 1.61 | 1.86 | ns    |
| LVC MOS33, Fast, 16 mA | 0.62              | 0.70 | 0.82 | 1.40              | 1.56 | 1.80 | 1.40              | 1.56 | 1.80 | ns    |
| LVC MOS33, Fast, 24 mA | 0.62              | 0.70 | 0.82 | 1.35              | 1.51 | 1.74 | 1.35              | 1.51 | 1.74 | ns    |
| LVC MOS25, Slow, 2 mA  | 0.61              | 0.70 | 0.82 | 3.67              | 3.97 | 4.42 | 3.67              | 3.97 | 4.42 | ns    |
| LVC MOS25, Slow, 4 mA  | 0.61              | 0.70 | 0.82 | 2.37              | 2.60 | 2.94 | 2.37              | 2.60 | 2.94 | ns    |
| LVC MOS25, Slow, 6 mA  | 0.61              | 0.70 | 0.82 | 2.19              | 2.41 | 2.74 | 2.19              | 2.41 | 2.74 | ns    |
| LVC MOS25, Slow, 8 mA  | 0.61              | 0.70 | 0.82 | 2.05              | 2.26 | 2.56 | 2.05              | 2.26 | 2.56 | ns    |
| LVC MOS25, Slow, 12 mA | 0.61              | 0.70 | 0.82 | 2.10              | 2.31 | 2.63 | 2.10              | 2.31 | 2.63 | ns    |
| LVC MOS25, Slow, 16 mA | 0.61              | 0.70 | 0.82 | 1.84              | 2.02 | 2.30 | 1.84              | 2.02 | 2.30 | ns    |
| LVC MOS25, Slow, 24 mA | 0.61              | 0.70 | 0.82 | 1.83              | 2.04 | 2.34 | 1.83              | 2.04 | 2.34 | ns    |
| LVC MOS25, Fast, 2 mA  | 0.61              | 0.70 | 0.82 | 3.14              | 3.41 | 3.82 | 3.14              | 3.41 | 3.82 | ns    |
| LVC MOS25, Fast, 4 mA  | 0.61              | 0.70 | 0.82 | 1.89              | 2.08 | 2.37 | 1.89              | 2.08 | 2.37 | ns    |
| LVC MOS25, Fast, 6 mA  | 0.61              | 0.70 | 0.82 | 1.74              | 1.92 | 2.20 | 1.74              | 1.92 | 2.20 | ns    |
| LVC MOS25, Fast, 8 mA  | 0.61              | 0.70 | 0.82 | 1.66              | 1.83 | 2.09 | 1.66              | 1.83 | 2.09 | ns    |
| LVC MOS25, Fast, 12 mA | 0.61              | 0.70 | 0.82 | 1.52              | 1.69 | 1.94 | 1.52              | 1.69 | 1.94 | ns    |
| LVC MOS25, Fast, 16 mA | 0.61              | 0.70 | 0.82 | 1.43              | 1.60 | 1.85 | 1.43              | 1.60 | 1.85 | ns    |
| LVC MOS25, Fast, 24 mA | 0.61              | 0.70 | 0.82 | 1.40              | 1.54 | 1.76 | 1.40              | 1.54 | 1.76 | ns    |

Table 56: IOB Switching Characteristics (Cont'd)

| I/O Standard           | T <sub>IOP1</sub> |      |      | T <sub>IOP</sub> |      |      | T <sub>IOTP</sub> |      |      | Units |
|------------------------|-------------------|------|------|------------------|------|------|-------------------|------|------|-------|
|                        | Speed Grade       |      |      | Speed Grade      |      |      | Speed Grade       |      |      |       |
|                        | -3                | -2   | -1   | -3               | -2   | -1   | -3                | -2   | -1   |       |
| LVC MOS18, Slow, 2 mA  | 0.67              | 0.76 | 0.89 | 4.20             | 4.56 | 5.09 | 4.20              | 4.56 | 5.09 | ns    |
| LVC MOS18, Slow, 4 mA  | 0.67              | 0.76 | 0.89 | 3.03             | 3.32 | 3.75 | 3.03              | 3.32 | 3.75 | ns    |
| LVC MOS18, Slow, 6 mA  | 0.67              | 0.76 | 0.89 | 2.37             | 2.61 | 2.97 | 2.37              | 2.61 | 2.97 | ns    |
| LVC MOS18, Slow, 8 mA  | 0.67              | 0.76 | 0.89 | 2.15             | 2.37 | 2.69 | 2.15              | 2.37 | 2.69 | ns    |
| LVC MOS18, Slow, 12 mA | 0.67              | 0.76 | 0.89 | 1.95             | 2.16 | 2.47 | 1.95              | 2.16 | 2.47 | ns    |
| LVC MOS18, Slow, 16 mA | 0.67              | 0.76 | 0.89 | 1.93             | 2.14 | 2.45 | 1.93              | 2.14 | 2.45 | ns    |
| LVC MOS18, Fast, 2 mA  | 0.67              | 0.76 | 0.89 | 3.41             | 3.71 | 4.16 | 3.41              | 3.71 | 4.16 | ns    |
| LVC MOS18, Fast, 4 mA  | 0.67              | 0.76 | 0.89 | 2.36             | 2.61 | 2.98 | 2.36              | 2.61 | 2.98 | ns    |
| LVC MOS18, Fast, 6 mA  | 0.67              | 0.76 | 0.89 | 1.87             | 2.06 | 2.35 | 1.87              | 2.06 | 2.35 | ns    |
| LVC MOS18, Fast, 8 mA  | 0.67              | 0.76 | 0.89 | 1.69             | 1.87 | 2.13 | 1.69              | 1.87 | 2.13 | ns    |
| LVC MOS18, Fast, 12 mA | 0.67              | 0.76 | 0.89 | 1.51             | 1.68 | 1.93 | 1.51              | 1.68 | 1.93 | ns    |
| LVC MOS18, Fast, 16 mA | 0.67              | 0.76 | 0.89 | 1.44             | 1.61 | 1.86 | 1.44              | 1.61 | 1.86 | ns    |
| LVC MOS15, Slow, 2 mA  | 0.73              | 0.83 | 0.98 | 3.50             | 3.84 | 4.34 | 3.50              | 3.84 | 4.34 | ns    |
| LVC MOS15, Slow, 4 mA  | 0.73              | 0.83 | 0.98 | 2.17             | 2.40 | 2.74 | 2.17              | 2.40 | 2.74 | ns    |
| LVC MOS15, Slow, 6 mA  | 0.73              | 0.83 | 0.98 | 1.99             | 2.20 | 2.52 | 1.99              | 2.20 | 2.52 | ns    |
| LVC MOS15, Slow, 8 mA  | 0.73              | 0.83 | 0.98 | 1.91             | 2.12 | 2.43 | 1.91              | 2.12 | 2.43 | ns    |
| LVC MOS15, Slow, 12 mA | 0.73              | 0.83 | 0.98 | 1.74             | 1.95 | 2.25 | 1.74              | 1.95 | 2.25 | ns    |
| LVC MOS15, Slow, 16 mA | 0.73              | 0.83 | 0.98 | 1.71             | 1.91 | 2.20 | 1.71              | 1.91 | 2.20 | ns    |
| LVC MOS15, Fast, 2 mA  | 0.73              | 0.83 | 0.98 | 2.80             | 3.07 | 3.48 | 2.80              | 3.07 | 3.48 | ns    |
| LVC MOS15, Fast, 4 mA  | 0.73              | 0.83 | 0.98 | 1.76             | 1.95 | 2.23 | 1.76              | 1.95 | 2.23 | ns    |
| LVC MOS15, Fast, 6 mA  | 0.73              | 0.83 | 0.98 | 1.62             | 1.80 | 2.06 | 1.62              | 1.80 | 2.06 | ns    |
| LVC MOS15, Fast, 8 mA  | 0.73              | 0.83 | 0.98 | 1.57             | 1.74 | 2.00 | 1.57              | 1.74 | 2.00 | ns    |
| LVC MOS15, Fast, 12 mA | 0.73              | 0.83 | 0.98 | 1.43             | 1.60 | 1.86 | 1.43              | 1.60 | 1.86 | ns    |
| LVC MOS15, Fast, 16 mA | 0.73              | 0.83 | 0.98 | 1.37             | 1.53 | 1.77 | 1.37              | 1.53 | 1.77 | ns    |
| LVC MOS12, Slow, 2 mA  | 0.84              | 0.96 | 1.14 | 3.58             | 3.98 | 4.58 | 3.58              | 3.98 | 4.58 | ns    |
| LVC MOS12, Slow, 4 mA  | 0.84              | 0.96 | 1.14 | 2.10             | 2.33 | 2.66 | 2.10              | 2.33 | 2.66 | ns    |
| LVC MOS12, Slow, 6 mA  | 0.84              | 0.96 | 1.14 | 2.00             | 2.18 | 2.45 | 2.00              | 2.18 | 2.45 | ns    |
| LVC MOS12, Slow, 8 mA  | 0.84              | 0.96 | 1.14 | 1.91             | 2.14 | 2.48 | 1.91              | 2.14 | 2.48 | ns    |
| LVC MOS12, Fast, 2 mA  | 0.84              | 0.96 | 1.14 | 3.05             | 3.38 | 3.87 | 3.05              | 3.38 | 3.87 | ns    |
| LVC MOS12, Fast, 4 mA  | 0.84              | 0.96 | 1.14 | 1.71             | 1.91 | 2.20 | 1.71              | 1.91 | 2.20 | ns    |
| LVC MOS12, Fast, 6 mA  | 0.84              | 0.96 | 1.14 | 1.58             | 1.78 | 2.08 | 1.58              | 1.78 | 2.08 | ns    |
| LVC MOS12, Fast, 8 mA  | 0.84              | 0.96 | 1.14 | 1.52             | 1.70 | 1.97 | 1.52              | 1.70 | 1.97 | ns    |
| LVDCI_33               | 0.62              | 0.70 | 0.82 | 1.50             | 1.66 | 1.90 | 1.50              | 1.66 | 1.90 | ns    |
| LVDCI_25               | 0.61              | 0.70 | 0.82 | 1.55             | 1.71 | 1.93 | 1.55              | 1.71 | 1.93 | ns    |
| LVDCI_18               | 0.67              | 0.76 | 0.89 | 1.65             | 1.78 | 1.99 | 1.65              | 1.78 | 1.99 | ns    |
| LVDCI_15               | 0.73              | 0.83 | 0.98 | 1.58             | 1.75 | 2.02 | 1.58              | 1.75 | 2.02 | ns    |

Table 56: IOB Switching Characteristics (Cont'd)

| I/O Standard        | T <sub>IOPI</sub> |      |      | T <sub>IOOP</sub> |      |      | T <sub>IOTP</sub> |      |      | Units |
|---------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
|                     | Speed Grade       |      |      | Speed Grade       |      |      | Speed Grade       |      |      |       |
|                     | -3                | -2   | -1   | -3                | -2   | -1   | -3                | -2   | -1   |       |
| LVDCI_DV2_25        | 0.61              | 0.70 | 0.82 | 1.36              | 1.51 | 1.74 | 1.36              | 1.51 | 1.74 | ns    |
| LVDCI_DV2_18        | 0.67              | 0.76 | 0.89 | 1.43              | 1.60 | 1.85 | 1.43              | 1.60 | 1.85 | ns    |
| LVDCI_DV2_15        | 0.73              | 0.83 | 0.98 | 1.48              | 1.65 | 1.91 | 1.48              | 1.65 | 1.91 | ns    |
| GTL_DCI             | 0.76              | 0.85 | 1.00 | 1.36              | 1.47 | 1.65 | 1.36              | 1.47 | 1.65 | ns    |
| GTL_P_DCI           | 0.76              | 0.85 | 1.00 | 1.37              | 1.52 | 1.76 | 1.37              | 1.52 | 1.76 | ns    |
| LVPECL_25           | 0.80              | 0.90 | 1.06 | 1.28              | 1.42 | 1.62 | 1.28              | 1.42 | 1.62 | ns    |
| HSTL_I_12           | 0.76              | 0.85 | 1.00 | 1.45              | 1.61 | 1.85 | 1.45              | 1.61 | 1.85 | ns    |
| HSTL_I_DCI          | 0.76              | 0.85 | 1.00 | 1.41              | 1.56 | 1.77 | 1.41              | 1.56 | 1.77 | ns    |
| HSTL_II_DCI         | 0.76              | 0.85 | 1.00 | 1.34              | 1.48 | 1.69 | 1.34              | 1.48 | 1.69 | ns    |
| HSTL_II_T_DCI       | 0.76              | 0.85 | 1.00 | 1.41              | 1.56 | 1.77 | 1.41              | 1.56 | 1.77 | ns    |
| HSTL_III_DCI        | 0.76              | 0.85 | 1.00 | 1.57              | 1.72 | 1.95 | 1.57              | 1.72 | 1.95 | ns    |
| HSTL_IV_DCI         | 0.76              | 0.85 | 1.00 | 1.34              | 1.46 | 1.64 | 1.34              | 1.46 | 1.64 | ns    |
| HSTL_I_DCI_18       | 0.76              | 0.85 | 1.00 | 1.36              | 1.50 | 1.70 | 1.36              | 1.50 | 1.70 | ns    |
| HSTL_II_DCI_18      | 0.76              | 0.85 | 1.00 | 1.30              | 1.43 | 1.64 | 1.30              | 1.43 | 1.64 | ns    |
| HSTL_II_T_DCI_18    | 0.76              | 0.85 | 1.00 | 1.36              | 1.50 | 1.70 | 1.36              | 1.50 | 1.70 | ns    |
| HSTL_III_DCI_18     | 0.76              | 0.85 | 1.00 | 1.55              | 1.69 | 1.91 | 1.55              | 1.69 | 1.91 | ns    |
| HSTL_IV_DCI_18      | 0.76              | 0.85 | 1.00 | 1.31              | 1.44 | 1.62 | 1.31              | 1.44 | 1.62 | ns    |
| DIFF_HSTL_I_18      | 0.80              | 0.90 | 1.06 | 1.40              | 1.55 | 1.77 | 1.40              | 1.55 | 1.77 | ns    |
| DIFF_HSTL_I_DCI_18  | 0.80              | 0.90 | 1.06 | 1.36              | 1.50 | 1.70 | 1.36              | 1.50 | 1.70 | ns    |
| DIFF_HSTL_I         | 0.80              | 0.90 | 1.06 | 1.42              | 1.57 | 1.79 | 1.42              | 1.57 | 1.79 | ns    |
| DIFF_HSTL_I_DCI     | 0.80              | 0.90 | 1.06 | 1.41              | 1.56 | 1.77 | 1.41              | 1.56 | 1.77 | ns    |
| DIFF_HSTL_II_18     | 0.80              | 0.90 | 1.06 | 1.36              | 1.51 | 1.72 | 1.36              | 1.51 | 1.72 | ns    |
| DIFF_HSTL_II_DCI_18 | 0.80              | 0.90 | 1.06 | 1.30              | 1.43 | 1.64 | 1.30              | 1.43 | 1.64 | ns    |
| DIFF_HSTL_II        | 0.80              | 0.90 | 1.06 | 1.39              | 1.53 | 1.74 | 1.39              | 1.53 | 1.74 | ns    |
| DIFF_HSTL_II_DCI    | 0.80              | 0.90 | 1.06 | 1.34              | 1.48 | 1.69 | 1.34              | 1.48 | 1.69 | ns    |
| SSTL2_I_DCI         | 0.76              | 0.85 | 1.00 | 1.42              | 1.56 | 1.78 | 1.42              | 1.56 | 1.78 | ns    |
| SSTL2_II_DCI        | 0.76              | 0.85 | 1.00 | 1.34              | 1.48 | 1.70 | 1.34              | 1.48 | 1.70 | ns    |
| SSTL2_II_T_DCI      | 0.76              | 0.85 | 1.00 | 1.42              | 1.56 | 1.78 | 1.42              | 1.56 | 1.78 | ns    |
| SSTL18_I            | 0.76              | 0.85 | 1.00 | 1.46              | 1.61 | 1.84 | 1.46              | 1.61 | 1.84 | ns    |
| SSTL18_II           | 0.76              | 0.85 | 1.00 | 1.39              | 1.53 | 1.75 | 1.39              | 1.53 | 1.75 | ns    |
| SSTL18_I_DCI        | 0.76              | 0.85 | 1.00 | 1.39              | 1.53 | 1.74 | 1.39              | 1.53 | 1.74 | ns    |
| SSTL18_II_DCI       | 0.76              | 0.85 | 1.00 | 1.30              | 1.44 | 1.64 | 1.30              | 1.44 | 1.64 | ns    |
| SSTL18_II_T_DCI     | 0.76              | 0.85 | 1.00 | 1.39              | 1.53 | 1.74 | 1.39              | 1.53 | 1.74 | ns    |

Table 56: IOB Switching Characteristics (Cont'd)

| I/O Standard       | T <sub>IOPI</sub> |      |      | T <sub>IOOP</sub> |      |      | T <sub>IOTP</sub> |      |      | Units |
|--------------------|-------------------|------|------|-------------------|------|------|-------------------|------|------|-------|
|                    | Speed Grade       |      |      | Speed Grade       |      |      | Speed Grade       |      |      |       |
|                    | -3                | -2   | -1   | -3                | -2   | -1   | -3                | -2   | -1   |       |
| DIFF_SSTL2_I       | 0.80              | 0.90 | 1.06 | 1.48              | 1.64 | 1.87 | 1.48              | 1.64 | 1.87 | ns    |
| DIFF_SSTL2_I_DCI   | 0.80              | 0.90 | 1.06 | 1.42              | 1.56 | 1.78 | 1.42              | 1.56 | 1.78 | ns    |
| DIFF_SSTL18_I      | 0.80              | 0.90 | 1.06 | 1.46              | 1.61 | 1.84 | 1.46              | 1.61 | 1.84 | ns    |
| DIFF_SSTL18_I_DCI  | 0.80              | 0.90 | 1.06 | 1.39              | 1.53 | 1.74 | 1.39              | 1.53 | 1.74 | ns    |
| DIFF_SSTL2_II      | 0.80              | 0.90 | 1.06 | 1.40              | 1.55 | 1.76 | 1.40              | 1.55 | 1.76 | ns    |
| DIFF_SSTL2_II_DCI  | 0.80              | 0.90 | 1.06 | 1.34              | 1.48 | 1.70 | 1.34              | 1.48 | 1.70 | ns    |
| DIFF_SSTL18_II     | 0.80              | 0.90 | 1.06 | 1.39              | 1.53 | 1.75 | 1.39              | 1.53 | 1.75 | ns    |
| DIFF_SSTL18_II_DCI | 0.80              | 0.90 | 1.06 | 1.30              | 1.44 | 1.64 | 1.30              | 1.44 | 1.64 | ns    |

Table 57: IOB 3-state ON Output Switching Characteristics ( $T_{IOTPHZ}$ )

| Symbol       | Description                   | Speed Grade |      |      | Units |
|--------------|-------------------------------|-------------|------|------|-------|
|              |                               | -3          | -2   | -1   |       |
| $T_{IOTPHZ}$ | T input to Pad high-impedance | 0.88        | 1.01 | 1.12 | ns    |

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 58 shows the test setup parameters used for measuring input delay.

Table 58: Input Delay Measurement Methodology

| Description                                                  | I/O Standard Attribute  | $V_L^{(1,2)}$                    | $V_H^{(1,2)}$                    | $V_{MEAS}^{(1,4,5)}$ | $V_{REF}^{(1,3,5)}$ |
|--------------------------------------------------------------|-------------------------|----------------------------------|----------------------------------|----------------------|---------------------|
| LVTTL (Low-Voltage Transistor-Transistor Logic)              | LVTTL                   | 0                                | 3.0                              | 1.4                  | —                   |
| LVC MOS (Low-Voltage CMOS), 3.3V                             | LVC MOS33               | 0                                | 3.3                              | 1.65                 | —                   |
| LVC MOS, 2.5V                                                | LVC MOS25               | 0                                | 2.5                              | 1.25                 | —                   |
| LVC MOS, 1.8V                                                | LVC MOS18               | 0                                | 1.8                              | 0.9                  | —                   |
| LVC MOS, 1.5V                                                | LVC MOS15               | 0                                | 1.5                              | 0.75                 | —                   |
| LVC MOS, 1.2V                                                | LVC MOS12               | 0                                | 1.2                              | 0.6                  | —                   |
| PCI (Peripheral Component Interconnect), 33 MHz, 3.3V        | PCI33_3                 | Per PCI™ Specification           |                                  |                      | —                   |
| PCI, 66 MHz, 3.3V                                            | PCI66_3                 | Per PCI Specification            |                                  |                      | —                   |
| PCI-X, 133 MHz, 3.3V                                         | PCIX                    | Per PCI-X™ Specification         |                                  |                      | —                   |
| GTL (Gunning Transceiver Logic)                              | GTL                     | $V_{REF} - 0.2$                  | $V_{REF} + 0.2$                  | $V_{REF}$            | 0.80                |
| GTL Plus                                                     | GTLP                    | $V_{REF} - 0.2$                  | $V_{REF} + 0.2$                  | $V_{REF}$            | 1.0                 |
| HSTL (High-Speed Transceiver Logic), Class I & II            | HSTL_I, HSTL_II         | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$            | 0.75                |
| HSTL, Class III & IV                                         | HSTL_III, HSTL_IV       | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$            | 0.90                |
| HSTL, Class I & II, 1.8V                                     | HSTL_I_18, HSTL_II_18   | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$            | 0.90                |
| HSTL, Class III & IV, 1.8V                                   | HSTL_III_18, HSTL_IV_18 | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$            | 1.08                |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II       | $V_{REF} - 1.00$                 | $V_{REF} + 1.00$                 | $V_{REF}$            | 1.5                 |
| SSTL, Class I & II, 2.5V                                     | SSTL2_I, SSTL2_II       | $V_{REF} - 0.75$                 | $V_{REF} + 0.75$                 | $V_{REF}$            | 1.25                |
| SSTL, Class I & II, 1.8V                                     | SSTL18_I, SSTL18_II     | $V_{REF} - 0.5$                  | $V_{REF} + 0.5$                  | $V_{REF}$            | 0.90                |
| AGP-2X/AGP (Accelerated Graphics Port)                       | AGP                     | $V_{REF} - (0.2 \times V_{CCO})$ | $V_{REF} + (0.2 \times V_{CCO})$ | $V_{REF}$            | AGP Spec            |
| LVDS (Low-Voltage Differential Signaling), 2.5V              | LVDS_25                 | $1.2 - 0.125$                    | $1.2 + 0.125$                    | 0 <sup>(6)</sup>     |                     |
| LVDS EXT (LVDS Extended Mode), 2.5V                          | LVDS EXT_25             | $1.2 - 0.125$                    | $1.2 + 0.125$                    | 0 <sup>(6)</sup>     |                     |
| LDT (HyperTransport), 2.5V                                   | LDT_25                  | $0.6 - 0.125$                    | $0.6 + 0.125$                    | 0 <sup>(6)</sup>     |                     |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V    | LVPECL_25               | $1.15 - 0.3$                     | $1.15 - 0.3$                     | 0 <sup>(6)</sup>     |                     |

#### Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL\_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between  $V_L$  and  $V_H$ .
3. Measurements are made at typical, minimum, and maximum  $V_{REF}$  values. Reported delays reflect worst case of these measurements.  $V_{REF}$  values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the  $V_{REF} / V_{MEAS}$  parameters found in IBIS models and/or noted in Figure 11.
6. The value given is the differential input voltage.

## Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe ( $< 1$  pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 11 and Figure 12.

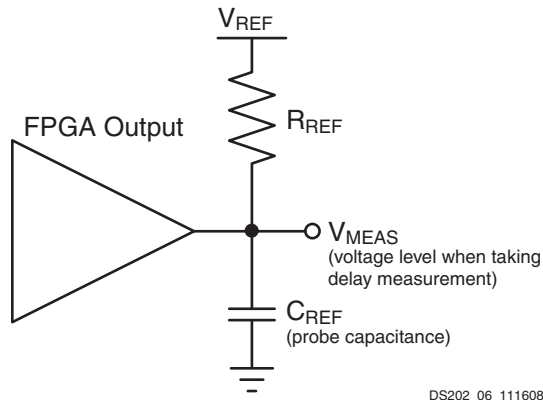
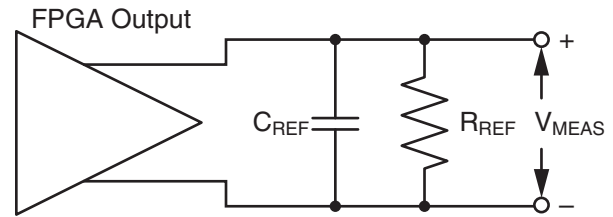


Figure 11: Single Ended Test Setup



ds202\_12\_042808

Figure 12: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 59.
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 59: Output Delay Measurement Methodology

| Description                                        | I/O Standard Attribute | $R_{REF}$ ( $\Omega$ ) | $C_{REF}^{(1)}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|----------------------------------------------------|------------------------|------------------------|----------------------|----------------|---------------|
| LVTTTL (Low-Voltage Transistor-Transistor Logic)   | LVTTTL (all)           | 1M                     | 0                    | 1.4            | 0             |
| LVC MOS (Low-Voltage CMOS), 3.3V                   | LVC MOS33              | 1M                     | 0                    | 1.65           | 0             |
| LVC MOS, 2.5V                                      | LVC MOS25              | 1M                     | 0                    | 1.25           | 0             |
| LVC MOS, 1.8V                                      | LVC MOS18              | 1M                     | 0                    | 0.9            | 0             |
| LVC MOS, 1.5V                                      | LVC MOS15              | 1M                     | 0                    | 0.75           | 0             |
| LVC MOS, 1.2V                                      | LVC MOS12              | 1M                     | 0                    | 0.6            | 0             |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 (rising edge)  | 25                     | $10^{(2)}$           | 0.94           | 0             |
|                                                    | PCI33_3 (falling edge) | 25                     | $10^{(2)}$           | 2.03           | 3.3           |
| PCI, 66 MHz, 3.3V                                  | PCI66_3 (rising edge)  | 25                     | $10^{(2)}$           | 0.94           | 0             |
|                                                    | PCI66_3 (falling edge) | 25                     | $10^{(2)}$           | 2.03           | 3.3           |
| PCI-X, 133 MHz, 3.3V                               | PCIX (rising edge)     | 25                     | $10^{(3)}$           | 0.94           |               |
|                                                    | PCIX (falling edge)    | 25                     | $10^{(3)}$           | 2.03           | 3.3           |
| GTL (Gunning Transceiver Logic)                    | GTL                    | 25                     | 0                    | 0.8            | 1.2           |
| GTL Plus                                           | GTLP                   | 25                     | 0                    | 1.0            | 1.5           |
| HSTL (High-Speed Transceiver Logic), Class I       | HSTL_I                 | 50                     | 0                    | $V_{REF}$      | 0.75          |
| HSTL, Class II                                     | HSTL_II                | 25                     | 0                    | $V_{REF}$      | 0.75          |
| HSTL, Class III                                    | HSTL_III               | 50                     | 0                    | 0.9            | 1.5           |

Table 59: Output Delay Measurement Methodology (Cont'd)

| Description                                                      | I/O Standard Attribute          | $R_{REF}$<br>( $\Omega$ ) | $C_{REF}^{(1)}$<br>(pF) | $V_{MEAS}$<br>(V) | $V_{REF}$<br>(V) |
|------------------------------------------------------------------|---------------------------------|---------------------------|-------------------------|-------------------|------------------|
| HSTL, Class IV                                                   | HSTL_IV                         | 25                        | 0                       | 0.9               | 1.5              |
| HSTL, Class I, 1.8V                                              | HSTL_I_18                       | 50                        | 0                       | $V_{REF}$         | 0.9              |
| HSTL, Class II, 1.8V                                             | HSTL_II_18                      | 25                        | 0                       | $V_{REF}$         | 0.9              |
| HSTL, Class III, 1.8V                                            | HSTL_III_18                     | 50                        | 0                       | 1.1               | 1.8              |
| HSTL, Class IV, 1.8V                                             | HSTL_IV_18                      | 25                        | 0                       | 1.1               | 1.8              |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V               | SSTL18_I                        | 50                        | 0                       | $V_{REF}$         | 0.9              |
| SSTL, Class II, 1.8V                                             | SSTL18_II                       | 25                        | 0                       | $V_{REF}$         | 0.9              |
| SSTL, Class I, 2.5V                                              | SSTL2_I                         | 50                        | 0                       | $V_{REF}$         | 1.25             |
| SSTL, Class II, 2.5V                                             | SSTL2_II                        | 25                        | 0                       | $V_{REF}$         | 1.25             |
| LVDS (Low-Voltage Differential Signaling), 2.5V                  | LVDS_25                         | 100                       | 0                       | 0 <sup>(4)</sup>  | 1.2              |
| LVDS (Low-Voltage Differential Signaling), 2.5V                  | LVDS_25                         | 100                       | 0                       | 0 <sup>(4)</sup>  | 1.2              |
| BLVDS (Bus LVDS), 2.5V                                           | BLVDS_25                        | 100                       | 0                       | 0 <sup>(4)</sup>  | 0                |
| LDT (HyperTransport), 2.5V                                       | LDT_25                          | 100                       | 0                       | 0 <sup>(4)</sup>  | 0.6              |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V        | LVPECL_25                       | 100                       | 0                       | 0 <sup>(4)</sup>  | 0                |
| LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33, HSLVDCI_33            | 1M                        | 0                       | 1.65              | 0                |
| LVDCI/HSLVDCI, 2.5V                                              | LVDCI_25, HSLVDCI_25            | 1M                        | 0                       | 1.25              | 0                |
| LVDCI/HSLVDCI, 1.8V                                              | LVDCI_18, HSLVDCI_18            | 1M                        | 0                       | 0.9               | 0                |
| LVDCI/HSLVDCI, 1.5V                                              | LVDCI_15, HSLVDCI_15            | 1M                        | 0                       | 0.75              | 0                |
| HSTL (High-Speed Transceiver Logic), Class I & II, with DCI      | HSTL_I_DCI, HSTL_II_DCI         | 50                        | 0                       | $V_{REF}$         | 0.75             |
| HSTL, Class III & IV, with DCI                                   | HSTL_III_DCI, HSTL_IV_DCI       | 50                        | 0                       | 0.9               | 1.5              |
| HSTL, Class I & II, 1.8V, with DCI                               | HSTL_I_DCI_18, HSTL_II_DCI_18   | 50                        | 0                       | $V_{REF}$         | 0.9              |
| HSTL, Class III & IV, 1.8V, with DCI                             | HSTL_III_DCI_18, HSTL_IV_DCI_18 | 50                        | 0                       | 1.1               | 1.8              |
| SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI   | SSTL18_I_DCI, SSTL18_II_DCI     | 50                        | 0                       | $V_{REF}$         | 0.9              |
| SSTL, Class I & II, 2.5V, with DCI                               | SSTL2_I_DCI, SSTL2_II_DCI       | 50                        | 0                       | $V_{REF}$         | 1.25             |
| GTL (Gunning Transceiver Logic) with DCI                         | GTL_DCI                         | 50                        | 0                       | 0.8               | 1.2              |
| GTL Plus with DCI                                                | GTLP_DCI                        | 50                        | 0                       | 1.0               | 1.5              |

**Notes:**

1.  $C_{REF}$  is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.
4. The value given is the differential input voltage.

## Input/Output Logic Switching Characteristics

Table 60: ILOGIC Switching Characteristics

| Symbol                                   | Description                                                               | Speed Grade   |               |               | Units   |
|------------------------------------------|---------------------------------------------------------------------------|---------------|---------------|---------------|---------|
|                                          |                                                                           | -3            | -2            | -1            |         |
| Setup/Hold                               |                                                                           |               |               |               |         |
| T <sub>ICE1CK</sub> /T <sub>ICKCE1</sub> | CE1 pin Setup/Hold with respect to CLK                                    | 0.43<br>−0.24 | 0.49<br>−0.24 | 0.59<br>−0.24 | ns      |
| T <sub>ISRCK</sub> /T <sub>ICKSR</sub>   | SR/REV pin Setup/Hold with respect to CLK                                 | 0.85<br>−0.20 | 1.00<br>−0.20 | 1.22<br>−0.20 | ns      |
| T <sub>IDOCK</sub> /T <sub>IOCKD</sub>   | D pin Setup/Hold with respect to CLK without Delay                        | 0.34<br>−0.12 | 0.37<br>−0.12 | 0.39<br>−0.12 | ns      |
| T <sub>IDOCKD</sub> /T <sub>IOCKDD</sub> | DDL <sub>Y</sub> pin Setup/Hold with respect to CLK (using IODELAY)       | 0.31<br>−0.09 | 0.33<br>−0.09 | 0.36<br>−0.08 | ns      |
| Combinatorial                            |                                                                           |               |               |               |         |
| T <sub>IDI</sub>                         | D pin to O pin propagation delay, no Delay                                | 0.24          | 0.26          | 0.30          | ns      |
| T <sub>IDID</sub>                        | DDL <sub>Y</sub> pin to O pin propagation delay (using IODELAY)           | 0.20          | 0.22          | 0.26          | ns      |
| Sequential Delays                        |                                                                           |               |               |               |         |
| T <sub>IDLO</sub>                        | D pin to Q1 pin using flip-flop as a latch without Delay                  | 0.44          | 0.50          | 0.58          | ns      |
| T <sub>IDLOD</sub>                       | DDL <sub>Y</sub> pin to Q1 pin using flip-flop as a latch (using IODELAY) | 0.41          | 0.46          | 0.55          | ns      |
| T <sub>ICKQ</sub>                        | CLK to Q outputs                                                          | 0.47          | 0.52          | 0.60          | ns      |
| T <sub>RQ</sub>                          | SR/REV pin to OQ/TQ out                                                   | 1.12          | 1.28          | 1.53          | ns      |
| T <sub>GSRQ</sub>                        | Global Set/Reset to Q outputs                                             | 7.30          | 7.30          | 10.10         | ns      |
| Set/Reset                                |                                                                           |               |               |               |         |
| T <sub>RPW</sub>                         | Minimum Pulse Width, SR/REV inputs                                        | 0.78          | 0.95          | 1.20          | ns, Min |

Table 61: OLOGIC Switching Characteristics

| Symbol                                   | Description                               | Speed Grade   |               |                | Units   |
|------------------------------------------|-------------------------------------------|---------------|---------------|----------------|---------|
|                                          |                                           | -3            | -2            | -1             |         |
| Setup/Hold                               |                                           |               |               |                |         |
| T <sub>ODCK</sub> /T <sub>OCKD</sub>     | D1/D2 pins Setup/Hold with respect to CLK | 0.30<br>−0.21 | 0.36<br>−0.21 | 0.44<br>−0.21  | ns      |
| T <sub>OOCECK</sub> /T <sub>OCKOCE</sub> | OCE pin Setup/Hold with respect to CLK    | 0.16<br>−0.07 | 0.19<br>−0.07 | 0.23<br>−0.07  | ns      |
| T <sub>OSRCK</sub> /T <sub>OCKSR</sub>   | SR/REV pin Setup/Hold with respect to CLK | 0.93<br>−0.20 | 1.02<br>−0.20 | 1.16<br>−0.20  | ns      |
| T <sub>OTCK</sub> /T <sub>OCKT</sub>     | T1/T2 pins Setup/Hold with respect to CLK | 0.28<br>−0.18 | 0.34<br>−0.18 | 0.41<br>−0.18  | ns      |
| T <sub>OTCECK</sub> /T <sub>OCKTCE</sub> | TCE pin Setup/Hold with respect to CLK    | 0.20<br>−0.06 | 0.23<br>−0.06 | 0.29 –<br>0.06 | ns      |
| Combinatorial                            |                                           |               |               |                |         |
| T <sub>DOQ</sub>                         | D1 to OQ out or T1 to TQ out              | 0.62          | 0.70          | 0.83           | ns      |
| Sequential Delays                        |                                           |               |               |                |         |
| T <sub>OCKQ</sub>                        | CLK to OQ/TQ out                          | 0.61          | 0.62          | 0.62           | ns      |
| T <sub>RQ</sub>                          | SR/REV pin to OQ/TQ out                   | 1.63          | 1.89          | 2.27           | ns      |
| T <sub>GSRQ</sub>                        | Global Set/Reset to Q outputs             | 7.30          | 7.30          | 10.10          | ns      |
| Set/Reset                                |                                           |               |               |                |         |
| T <sub>RPW</sub>                         | Minimum Pulse Width, SR/REV inputs        | 0.80          | 0.98          | 1.25           | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

Table 62: ISERDES Switching Characteristics

| Symbol                                                                        | Description                                                      | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------|------------------------------------------------------------------|---------------|---------------|---------------|-------|
|                                                                               |                                                                  | -3            | -2            | -1            |       |
| Setup/Hold for Control Lines                                                  |                                                                  |               |               |               |       |
| T <sub>ISCKK_BITS<sub>LIP</sub></sub> / T <sub>ISCKC_BITS<sub>LIP</sub></sub> | BITS <sub>LIP</sub> pin Setup/Hold with respect to CLKDIV        | 0.10<br>0.00  | 0.11<br>0.00  | 0.12<br>0.00  | ns    |
| T <sub>ISCKK_CE</sub> / T <sub>ISCKC_CE</sub> <sup>(2)</sup>                  | CE pin Setup/Hold with respect to CLK (for CE1)                  | 0.43<br>−0.24 | 0.49<br>−0.24 | 0.59<br>−0.24 | ns    |
| T <sub>ISCKK_CE2</sub> / T <sub>ISCKC_CE2</sub> <sup>(2)</sup>                | CE pin Setup/Hold with respect to CLKDIV (for CE2)               | 0.03<br>0.11  | 0.04<br>0.13  | 0.06<br>0.15  | ns    |
| Setup/Hold for Data Lines                                                     |                                                                  |               |               |               |       |
| T <sub>ISDCK_D</sub> / T <sub>ISCKD_D</sub>                                   | D pin Setup/Hold with respect to CLK                             | 0.34<br>−0.12 | 0.37<br>−0.12 | 0.39<br>−0.12 | ns    |
| T <sub>ISDCK_DDLY</sub> / T <sub>ISCKD_DDLY</sub>                             | DDLY pin Setup/Hold with respect to CLK (using IODELAY)          | 0.31<br>−0.09 | 0.33<br>−0.09 | 0.36<br>−0.08 | ns    |
| T <sub>ISDCK_DDR</sub> / T <sub>ISCKD_DDR</sub>                               | D pin Setup/Hold with respect to CLK at DDR mode                 | 0.34<br>−0.12 | 0.37<br>−0.12 | 0.39<br>−0.12 | ns    |
| T <sub>ISDCK_DDLY_DDR</sub><br>T <sub>ISCKD_DDLY_DDR</sub>                    | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) | 0.31<br>−0.09 | 0.33<br>−0.09 | 0.36<br>−0.08 | ns    |
| Sequential Delays                                                             |                                                                  |               |               |               |       |
| T <sub>ISCKO_Q</sub>                                                          | CLKDIV to out at Q pin                                           | 0.46          | 0.51          | 0.60          | ns    |
| Propagation Delays                                                            |                                                                  |               |               |               |       |
| T <sub>ISDO_DO</sub>                                                          | D input to DO output pin                                         | 0.20          | 0.22          | 0.26          | ns    |

### Notes:

- Recorded at 0 tap value.
- $T_{ISCK\_CE2}$  and  $T_{ISCKC\_CE2}$  are reported as  $T_{ISCK\_CE} / T_{ISCKC\_CE}$  in TRACE report.

## Output Serializer/Deserializer Switching Characteristics

Table 63: OSERDES Switching Characteristics

| Symbol                                                      | Description                                   | Speed Grade   |               |               | Units |
|-------------------------------------------------------------|-----------------------------------------------|---------------|---------------|---------------|-------|
|                                                             |                                               | -3            | -2            | -1            |       |
| Setup/Hold                                                  |                                               |               |               |               |       |
| T <sub>OSDCK_D</sub> /T <sub>OSCKD_D</sub>                  | D input Setup/Hold with respect to CLKDIV     | 0.21<br>−0.02 | 0.24<br>−0.02 | 0.30<br>−0.02 | ns    |
| T <sub>OSDCK_T</sub> /T <sub>OSCKD_T</sub> <sup>(1)</sup>   | T input Setup/Hold with respect to CLK        | 0.28<br>−0.18 | 0.34<br>−0.18 | 0.41<br>−0.18 | ns    |
| T <sub>OSDCK_T2</sub> /T <sub>OSCKD_T2</sub> <sup>(1)</sup> | T input Setup/Hold with respect to CLKDIV     | 0.21<br>−0.03 | 0.24<br>−0.03 | 0.28<br>−0.03 | ns    |
| T <sub>OSCCK_OCE</sub> /T <sub>OSCKC_OCE</sub>              | OCE input Setup/Hold with respect to CLK      | 0.16<br>−0.07 | 0.19<br>−0.07 | 0.23<br>−0.07 | ns    |
| T <sub>OSCCK_S</sub>                                        | SR (Reset) input Setup with respect to CLKDIV | 0.52          | 0.58          | 0.70          | ns    |
| T <sub>OSCCK_TCE</sub> /T <sub>OSCKC_TCE</sub>              | TCE input Setup/Hold with respect to CLK      | 0.20<br>−0.06 | 0.23<br>−0.06 | 0.29<br>−0.06 | ns    |
| Sequential Delays                                           |                                               |               |               |               |       |
| T <sub>OSCKO_OQ</sub>                                       | Clock to out from CLK to OQ                   | 0.59          | 0.60          | 0.61          | ns    |
| T <sub>OSCKO_TQ</sub>                                       | Clock to out from CLK to TQ                   | 0.61          | 0.62          | 0.62          | ns    |
| Combinatorial                                               |                                               |               |               |               |       |
| T <sub>OSDO_TTQ</sub>                                       | T input to TQ Out                             | 0.62          | 0.70          | 0.83          | ns    |
| T <sub>OSCO_OQ</sub>                                        | Asynchronous Reset to OQ                      | 1.57          | 1.82          | 2.19          | ns    |
| T <sub>OSCO_TQ</sub>                                        | Asynchronous Reset to TQ                      | 1.63          | 1.89          | 2.27          | ns    |

**Notes:**

1.  $T_{OSDCK\_T2}$  and  $T_{OSCKD\_T2}$  are reported as  $T_{OSDCK\_T}/T_{OSCKD\_T}$  in TRACE report.

## Input/Output Delay Switching Characteristics

Table 64: Input/Output Delay Switching Characteristics

| Symbol                     | Description                                                                      | Speed Grade                                                 |               |               | Units  |
|----------------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------|---------------|---------------|--------|
|                            |                                                                                  | -3                                                          | -2            | -1            |        |
| IDELAYCTRL                 |                                                                                  |                                                             |               |               |        |
| T_IDELAYCTRLCO_RDY         | Reset to Ready for IDELAYCTRL                                                    | 3.00                                                        | 3.00          | 3.00          | μs     |
| F_IDELAYCTRL_REF           | REFCLK frequency                                                                 | 200.00                                                      | 200.00        | 200.00        | MHz    |
| IDELAYCTRL_REF_PRECISION   | REFCLK precision                                                                 | ±10                                                         | ±10           | ±10           | MHz    |
| T_IDELAYCTRL_RPW           | Minimum Reset pulse width                                                        | 50.00                                                       | 50.00         | 50.00         | ns     |
| IODELAY                    |                                                                                  |                                                             |               |               |        |
| T_IDELAYRESOLUTION         | IODELAY Chain Delay Resolution                                                   | 1/(64 x F <sub>REF</sub> x 1e <sup>6</sup> ) <sup>(1)</sup> |               |               | ps     |
| T_IDELAYPAT_JIT            | Pattern dependent period jitter in delay chain for clock pattern                 | 0                                                           | 0             | 0             | Note 2 |
|                            | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) | ±5                                                          | ±5            | ±5            | Note 2 |
| T_IODELAY_CLK_MAX          | Maximum frequency of CLK input to IODELAY                                        | 300                                                         | 250           | 250           | MHz    |
| T_IODCKCK_CE / T_IODCKC_CE | CE pin Setup/Hold with respect to CK                                             | 0.29<br>−0.06                                               | 0.34<br>−0.06 | 0.42<br>−0.06 | ns     |
| T_IODCK_INC/ T_IODCKC_INC  | INC pin Setup/Hold with respect to CK                                            | 0.18<br>0.02                                                | 0.20<br>0.04  | 0.24<br>0.06  | ns     |
| T_IODCK_RST/ T_IODCKC_RST  | RST pin Setup/Hold with respect to CK                                            | 0.25<br>−0.12                                               | 0.28<br>−0.12 | 0.33<br>−0.12 | ns     |
| T_IODDO_T                  | TSCONTROL delay to MUXE/MUXF switching and through IODELAY                       | Note 3                                                      | Note 3        | Note 3        |        |
| T_IODDO_IDATAIN            | Propagation delay through IODELAY                                                | Note 3                                                      | Note 3        | Note 3        |        |
| T_IODDO_ODATAIN            | Propagation delay through IODELAY                                                | Note 3                                                      | Note 3        | Note 3        |        |

### Notes:

1. Average Tap Delay at 200 MHz = 78 ps.
2. Units in ps, peak-to-peak per tap, in High Performance mode.
3. Delay depends on IODELAY tap setting. See TRACE report for actual values.

## CLB Switching Characteristics

Table 65: CLB Switching Characteristics

| Symbol               | Description                       | Speed Grade |      |      | Units   |
|----------------------|-----------------------------------|-------------|------|------|---------|
|                      |                                   | -3          | -2   | -1   |         |
| Combinatorial Delays |                                   |             |      |      |         |
| T <sub>ILO</sub>     | An – Dn LUT address to A          | 0.08        | 0.09 | 0.10 | ns, Max |
|                      | An – Dn LUT address to AMUX/CMUX  | 0.20        | 0.22 | 0.25 | ns, Max |
|                      | An – Dn LUT address to BMUX_A     | 0.31        | 0.35 | 0.40 | ns, Max |
| T <sub>ITO</sub>     | An – Dn inputs to A – D Q outputs | 0.67        | 0.77 | 0.90 | ns, Max |
| T <sub>AXA</sub>     | AX inputs to AMUX output          | 0.39        | 0.44 | 0.53 | ns, Max |
| T <sub>AXB</sub>     | AX inputs to BMUX output          | 0.46        | 0.52 | 0.61 | ns, Max |
| T <sub>AXC</sub>     | AX inputs to CMUX output          | 0.31        | 0.36 | 0.42 | ns, Max |
| T <sub>AXD</sub>     | AX inputs to DMUX output          | 0.55        | 0.62 | 0.73 | ns, Max |
| T <sub>BXB</sub>     | BX inputs to BMUX output          | 0.36        | 0.41 | 0.48 | ns, Max |
| T <sub>BXD</sub>     | BX inputs to DMUX output          | 0.45        | 0.51 | 0.59 | ns, Max |

Table 65: CLB Switching Characteristics (Cont'd)

| Symbol                                                               | Description                                      | Speed Grade   |               |               | Units   |
|----------------------------------------------------------------------|--------------------------------------------------|---------------|---------------|---------------|---------|
|                                                                      |                                                  | -3            | -2            | -1            |         |
| $T_{CXB}$                                                            | CX inputs to CMUX output                         | 0.33          | 0.36          | 0.42          | ns, Max |
| $T_{CXD}$                                                            | CX inputs to DMUX output                         | 0.37          | 0.42          | 0.49          | ns, Max |
| $T_{DXD}$                                                            | DX inputs to DMUX output                         | 0.38          | 0.42          | 0.49          | ns, Max |
| $T_{OPCYA}$                                                          | An input to COUT output                          | 0.43          | 0.50          | 0.59          | ns, Max |
| $T_{OPCYB}$                                                          | Bn input to COUT output                          | 0.39          | 0.44          | 0.51          | ns, Max |
| $T_{OPCYC}$                                                          | Cn input to COUT output                          | 0.33          | 0.37          | 0.43          | ns, Max |
| $T_{OPCYD}$                                                          | Dn input to COUT output                          | 0.30          | 0.34          | 0.40          | ns, Max |
| $T_{AXCY}$                                                           | AX input to COUT output                          | 0.36          | 0.42          | 0.50          | ns, Max |
| $T_{BXCy}$                                                           | BX input to COUT output                          | 0.26          | 0.30          | 0.37          | ns, Max |
| $T_{CXCy}$                                                           | CX input to COUT output                          | 0.20          | 0.22          | 0.26          | ns, Max |
| $T_{DxCy}$                                                           | DX input to COUT output                          | 0.20          | 0.22          | 0.26          | ns, Max |
| $T_{BYP}$                                                            | CIN input to COUT output                         | 0.09          | 0.10          | 0.11          | ns, Max |
| $T_{CINA}$                                                           | CIN input to AMUX output                         | 0.24          | 0.27          | 0.31          | ns, Max |
| $T_{CINB}$                                                           | CIN input to BMUX output                         | 0.27          | 0.30          | 0.35          | ns, Max |
| $T_{CINC}$                                                           | CIN input to CMUX output                         | 0.29          | 0.32          | 0.36          | ns, Max |
| $T_{CIND}$                                                           | CIN input to DMUX output                         | 0.31          | 0.35          | 0.41          | ns, Max |
| <b>Sequential Delays</b>                                             |                                                  |               |               |               |         |
| $T_{CKO}$                                                            | Clock to AQ – DQ outputs                         | 0.35          | 0.40          | 0.47          | ns, Max |
| <b>Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK</b> |                                                  |               |               |               |         |
| $T_{DICK}/T_{CKDI}$                                                  | AX – DX input to CLK on A – D Flip Flops         | 0.36<br>0.19  | 0.41<br>0.21  | 0.49<br>0.24  | ns, Min |
| $T_{RCK}$                                                            | DX input to CLK when used as REV                 | 0.37          | 0.42          | 0.51          | ns, Min |
| $T_{CECK}/T_{CKCE}$                                                  | CE input to CLK on A – D Flip Flops              | 0.18<br>–0.04 | 0.20<br>–0.04 | 0.23<br>–0.04 | ns, Min |
| $T_{SRCK}/T_{CKSR}$                                                  | SR input to CLK on A – D Flip Flops              | 0.41<br>–0.19 | 0.49<br>–0.19 | 0.59<br>–0.19 | ns, Min |
| $T_{CINCK}/T_{CKCIN}$                                                | CIN input to CLK on A – D Flip Flops             | 0.14<br>0.14  | 0.16<br>0.16  | 0.18<br>0.19  | ns, Min |
| <b>Set/Reset</b>                                                     |                                                  |               |               |               |         |
| $T_{SRMIN}$                                                          | SR input minimum pulse width                     | 0.90          | 0.90          | 0.90          | ns, Min |
| $T_{RQ}$                                                             | Delay from SR or REV input to AQ – DQ flip-flops | 0.74          | 0.86          | 1.03          | ns, Max |
| $T_{CEO}$                                                            | Delay from CE input to AQ – DQ flip-flops        | 0.46          | 0.52          | 0.63          | ns, Max |
| $F_{TOG}$                                                            | Toggle frequency (for export control)            | 1412          | 1265          | 1098          | MHz     |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 66: CLB Distributed RAM Switching Characteristics

| Symbol                                      | Description                  | Speed Grade   |               |               | Units   |
|---------------------------------------------|------------------------------|---------------|---------------|---------------|---------|
|                                             |                              | -3            | -2            | -1            |         |
| Sequential Delays                           |                              |               |               |               |         |
| T <sub>SHCKO</sub>                          | Clock to A – B outputs       | 1.08          | 1.26          | 1.54          | ns, Max |
| T <sub>SHCKO_1</sub>                        | Clock to AMUX – BMUX outputs | 1.19          | 1.38          | 1.68          | ns, Max |
| Setup and Hold Times Before/After Clock CLK |                              |               |               |               |         |
| T <sub>DS</sub> /T <sub>DH</sub>            | A – D inputs to CLK          | 0.72<br>0.20  | 0.84<br>0.22  | 1.03<br>0.26  | ns, Min |
| T <sub>AS</sub> /T <sub>AH</sub>            | Address An inputs to clock   | 0.41<br>0.20  | 0.46<br>0.22  | 0.54<br>0.27  | ns, Min |
| T <sub>WS</sub> /T <sub>WH</sub>            | WE input to clock            | 0.34<br>–0.06 | 0.39<br>–0.04 | 0.46<br>–0.02 | ns, Min |
| T <sub>CECK</sub> /T <sub>CKCE</sub>        | CE input to CLK              | 0.36<br>–0.08 | 0.42<br>–0.07 | 0.51<br>–0.06 | ns, Min |
| Clock CLK                                   |                              |               |               |               |         |
| T <sub>MPW</sub>                            | Minimum pulse width          | 0.70          | 0.82          | 1.00          | ns, Min |
| T <sub>MCP</sub>                            | Minimum clock period         | 1.40          | 1.64          | 2.00          | ns, Min |

### Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. TSHCKO also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

Table 67: CLB Shift Register Switching Characteristics

| Symbol                                      | Description                         | Speed Grade   |               |               | Units   |
|---------------------------------------------|-------------------------------------|---------------|---------------|---------------|---------|
|                                             |                                     | -3            | -2            | -1            |         |
| Sequential Delays                           |                                     |               |               |               |         |
| T <sub>REG</sub>                            | Clock to A – D outputs              | 1.23          | 1.43          | 1.73          | ns, Max |
| T <sub>REG_MUX</sub>                        | Clock to AMUX – DMUX output         | 1.33          | 1.55          | 1.87          | ns, Max |
| T <sub>REG_M31</sub>                        | Clock to DMUX output via M31 output | 0.99          | 1.15          | 1.38          | ns, Max |
| Setup and Hold Times Before/After Clock CLK |                                     |               |               |               |         |
| T <sub>WS</sub> /T <sub>WH</sub>            | WE input                            | 0.21<br>–0.06 | 0.24<br>–0.04 | 0.29<br>–0.02 | ns, Min |
| T <sub>CECK</sub> /T <sub>CKCE</sub>        | CE input to CLK                     | 0.23<br>–0.08 | 0.27<br>–0.07 | 0.33<br>–0.06 | ns, Min |
| T <sub>DS</sub> /T <sub>DH</sub>            | A – D inputs to CLK                 | 0.57<br>0.07  | 0.66<br>0.09  | 0.78<br>0.11  | ns, Min |
| Clock CLK                                   |                                     |               |               |               |         |
| T <sub>MPW</sub>                            | Minimum pulse width                 | 0.60          | 0.70          | 0.85          | ns, Min |

### Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

## Block RAM and FIFO Switching Characteristics

Table 68: Block RAM and FIFO Switching Characteristics

| Symbol                                                        | Description                                                                    | Speed Grade  |              |              | Units   |
|---------------------------------------------------------------|--------------------------------------------------------------------------------|--------------|--------------|--------------|---------|
|                                                               |                                                                                | -3           | -2           | -1           |         |
| Block RAM and FIFO Clock to Out Delays                        |                                                                                |              |              |              |         |
| T <sub>RCKO_DO</sub> and T <sub>RCKO_DOR</sub> <sup>(1)</sup> | Clock CLK to DOUT output (without output register) <sup>(2,3)</sup>            | 1.79         | 1.92         | 2.19         | ns, Max |
|                                                               | Clock CLK to DOUT output (with output register) <sup>(4,5)</sup>               | 0.61         | 0.69         | 0.82         | ns, Max |
|                                                               | Clock CLK to DOUT output with ECC (without output register) <sup>(2,3)</sup>   | 2.64         | 3.03         | 3.61         | ns, Max |
|                                                               | Clock CLK to DOUT output with ECC (with output register) <sup>(4,5)</sup>      | 0.66         | 0.77         | 0.93         | ns, Max |
|                                                               | Clock CLK to DOUT output with Cascade (without output register) <sup>(2)</sup> | 2.10         | 2.44         | 2.94         | ns, Max |
|                                                               | Clock CLK to DOUT output with Cascade (with output register) <sup>(4)</sup>    | 0.91         | 1.07         | 1.30         | ns, Max |
| T <sub>RCKO_FLAGS</sub>                                       | Clock CLK to FIFO flags outputs <sup>(6)</sup>                                 | 0.76         | 0.87         | 1.02         | ns, Max |
| T <sub>RCKO_POINTERS</sub>                                    | Clock CLK to FIFO pointer outputs <sup>(7)</sup>                               | 1.10         | 1.26         | 1.48         | ns, Max |
| T <sub>RCKO_ECCR</sub>                                        | Clock CLK to BITERR (with output register)                                     | 0.66         | 0.77         | 0.93         | ns, Max |
| T <sub>RCKO_ECC</sub>                                         | Clock CLK to BITERR (without output register)                                  | 2.48         | 2.85         | 3.41         | ns, Max |
|                                                               | Clock CLK to ECCPARITY in standard ECC mode                                    | 1.29         | 1.47         | 1.74         | ns, Max |
|                                                               | Clock CLK to ECCPARITY in ECC encode only mode                                 | 0.77         | 0.89         | 1.05         | ns, Max |
| Setup and Hold Times Before/After Clock CLK                   |                                                                                |              |              |              |         |
| T <sub>RCKK_ADDR</sub> /T <sub>RCKC_ADDR</sub>                | ADDR inputs <sup>(8)</sup>                                                     | 0.34<br>0.30 | 0.40<br>0.32 | 0.48<br>0.36 | ns, Min |
| T <sub>RDCK_DI</sub> /T <sub>RCKD_DI</sub>                    | DIN inputs <sup>(9)</sup>                                                      | 0.27<br>0.28 | 0.30<br>0.28 | 0.35<br>0.29 | ns, Min |
| T <sub>RDCK_DI_ECC</sub> /T <sub>RCKD_DI_ECC</sub>            | DIN inputs with ECC in standard mode <sup>(9)</sup>                            | 0.33<br>0.32 | 0.37<br>0.33 | 0.42<br>0.36 | ns, Min |
|                                                               | DIN inputs with ECC encode only <sup>(9)</sup>                                 | 0.68<br>0.32 | 0.72<br>0.33 | 0.77<br>0.36 | ns, Min |
| T <sub>RCKK_EN</sub> /T <sub>RCKC_EN</sub>                    | Block RAM Enable (EN) input                                                    | 0.32<br>0.15 | 0.36<br>0.15 | 0.42<br>0.15 | ns, Min |
| T <sub>RCKK_REGCE</sub> /T <sub>RCKC_REGCE</sub>              | CE input of output register                                                    | 0.15<br>0.22 | 0.16<br>0.24 | 0.18<br>0.27 | ns, Min |
| T <sub>RCKK_SSR</sub> /T <sub>RCKC_SSR</sub>                  | Synchronous Set/ Reset (SSR) input                                             | 0.17<br>0.23 | 0.21<br>0.25 | 0.26<br>0.28 | ns, Min |
| T <sub>RCKK_WE</sub> /T <sub>RCKC_WE</sub>                    | Write Enable (WE) input                                                        | 0.44<br>0.16 | 0.51<br>0.17 | 0.63<br>0.18 | ns, Min |
| T <sub>RCKK_WREN</sub> /T <sub>RCKC_WREN</sub>                | WREN/RDEN FIFO inputs <sup>(10)</sup>                                          | 0.36<br>0.30 | 0.41<br>0.34 | 0.48<br>0.40 | ns, Min |

Table 68: Block RAM and FIFO Switching Characteristics (Cont'd)

| Symbol                   | Description                                      | Speed Grade |      |      | Units   |
|--------------------------|--------------------------------------------------|-------------|------|------|---------|
|                          |                                                  | -3          | -2   | -1   |         |
| Reset Delays             |                                                  |             |      |      |         |
| T <sub>RCO_FLAGS</sub>   | Reset RST to FIFO Flags/Pointers <sup>(11)</sup> | 1.10        | 1.26 | 1.48 | ns, Max |
| Maximum Frequency        |                                                  |             |      |      |         |
| F <sub>MAX</sub>         | Block RAM in all modes                           | 550         | 500  | 450  | MHz     |
| F <sub>MAX_CASCADE</sub> | Block RAM in cascade configuration               | 500         | 450  | 400  | MHz     |
| F <sub>MAX_FIFO</sub>    | FIFO in all modes                                | 550         | 500  | 450  | MHz     |
| F <sub>MAX_ECC</sub>     | Block RAM and FIFO in ECC configuration          | 415         | 375  | 325  | MHz     |

**Notes:**

- TRACE will report all of these parameters as T<sub>RCKO\_DO</sub>.
- T<sub>RCKO\_DOR</sub> includes T<sub>RCKO\_DOW</sub>, T<sub>RCKO\_DOPR</sub>, and T<sub>RCKO\_DOPW</sub> as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with DO\_REG = 0.
- T<sub>RCKO\_DO</sub> includes T<sub>RCKO\_DOP</sub> as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO\_REG = 1.
- T<sub>RCKO\_FLAGS</sub> includes the following parameters: T<sub>RCKO\_AEMPTY</sub>, T<sub>RCKO\_AFULL</sub>, T<sub>RCKO\_EMPTY</sub>, T<sub>RCKO\_FULL</sub>, T<sub>RCKO\_RDERR</sub>, T<sub>RCKO\_WRERR</sub>.
- T<sub>RCKO\_POINTERS</sub> includes both T<sub>RCKO\_RDCOUNT</sub> and T<sub>RCKO\_WRCOUNT</sub>.
- The ADDR setup and hold must be met when EN is asserted even though WE is deasserted. Otherwise, block RAM data corruption is possible.
- T<sub>RCKO\_DI</sub> includes both A and B inputs as well as the parity inputs of A and B.
- These parameters also apply to RDEN.
- T<sub>RCKO\_FLAGS</sub> includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

## DSP48E Switching Characteristics

Table 69: DSP48E Switching Characteristics

| Symbol                                                                          | Description                                                     | Speed         |               |               | Units |
|---------------------------------------------------------------------------------|-----------------------------------------------------------------|---------------|---------------|---------------|-------|
|                                                                                 |                                                                 | -3            | -2            | -1            |       |
| Setup and Hold Times of Data/Control Pins to the Input Register Clock           |                                                                 |               |               |               |       |
| TDSPDCK_{AA, BB, ACINA, BCINB}/<br>TDSPCKD_{AA, BB, ACINA, BCINB}               | {A, B, ACIN, BCIN} input to {A, B} register CLK                 | 0.17<br>0.17  | 0.21<br>0.23  | 0.26<br>0.30  | ns    |
| TDSPDCK_CC/TDSPCKD_CC                                                           | C input to C register CLK                                       | 0.14<br>0.26  | 0.16<br>0.31  | 0.20<br>0.37  | ns    |
| Setup and Hold Times of Data Pins to the Pipeline Register Clock                |                                                                 |               |               |               |       |
| TDSPDCK_{AM, BM, ACINM, BCINM}/<br>TDSPCKD_{AM, BM, ACINM, BCINM}               | {A, B, ACIN, BCIN} input to M register CLK                      | 1.30<br>0.19  | 1.44<br>0.19  | 1.71<br>0.19  | ns    |
| Setup and Hold Times of Data/Control Pins to the Output Register Clock          |                                                                 |               |               |               |       |
| TDSPDCK_{AP, BP, ACINP, BCINP}_M/<br>TDSPCKD_{AP, BP, ACINP, BCINP}_M           | {A, B, ACIN, BCIN} input to P register CLK using multiplier     | 2.39<br>−0.30 | 2.74<br>−0.30 | 3.25<br>−0.30 | ns    |
| TDSPDCK_{AP, BP, ACINP, BCINP}_NM/<br>TDSPCKD_{AP, BP, ACINP, BCINP}_NM         | {A, B, ACIN, BCIN} input to P register CLK not using multiplier | 1.35<br>−0.10 | 1.54<br>−0.10 | 1.83<br>−0.10 | ns    |
| TDSPDCK_CP/TDSPCKD_CP                                                           | C input to P register CLK                                       | 1.30<br>−0.13 | 1.42<br>−0.13 | 1.70<br>−0.13 | ns    |
| TDSPDCK_{PCINP, CRYCINP, MULTSIGNINP}/<br>TDSPCKD_{PCINP, CRYCINP, MULTSIGNINP} | {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK         | 1.06<br>0.11  | 1.17<br>0.11  | 1.31<br>0.11  | ns    |
| Setup and Hold Times of the CE Pins                                             |                                                                 |               |               |               |       |
| TDSPCCK_{CEA1A, CEA2A, CEB1B, CEB2B}/<br>TDSPCKC_{CEA1A, CEA2A, CEB1A, CEB2B}   | {CEA1, CEA2A, CEB1B, CEB2B} input to {A, B} register CLK        | 0.24<br>0.21  | 0.28<br>0.25  | 0.33<br>0.31  | ns    |
| TDSPCCK_CECC/TDSPCKC_CECC                                                       | CEC input to C register CLK                                     | 0.19<br>0.17  | 0.21<br>0.21  | 0.26<br>0.28  | ns    |

Table 69: DSP48E Switching Characteristics (Cont'd)

| Symbol                                                                                       | Description                                                                          | Speed        |              |              | Units |
|----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|--------------|--------------|--------------|-------|
|                                                                                              |                                                                                      | -3           | -2           | -1           |       |
| TDSPCCK_CEMM/TDSPCKC_CEMM                                                                    | CEM input to M register CLK                                                          | 0.25<br>0.18 | 0.29<br>0.21 | 0.36<br>0.26 | ns    |
| TDSPCCK_CEPP/TDSPCKC_CEPP                                                                    | CEP input to P register CLK                                                          | 0.56<br>0.01 | 0.63<br>0.01 | 0.73<br>0.01 | ns    |
| <b>Setup and Hold Times of the RST Pins</b>                                                  |                                                                                      |              |              |              |       |
| TDSPCCK_{RSTAA, RSTBB}/<br>TDSPCKC_{RSTAA, RSTBB}                                            | {RSTA, RSTB} input to {A, B} register CLK                                            | 0.24<br>0.23 | 0.28<br>0.26 | 0.33<br>0.31 | ns    |
| TDSPCCK_RSTCC/TDSPCKC_RSTCC                                                                  | RSTC input to C register CLK                                                         | 0.19<br>0.17 | 0.21<br>0.21 | 0.26<br>0.28 | ns    |
| TDSPCCK_RSTMM/TDSPCKC_RSTMM                                                                  | RSTM input to M register CLK                                                         | 0.25<br>0.18 | 0.29<br>0.21 | 0.36<br>0.26 | ns    |
| TDSPCCK_RSTPP/TDSPCKC_RSTPP                                                                  | RSTP input to P register CLK                                                         | 0.56<br>0.01 | 0.63<br>0.01 | 0.73<br>0.01 | ns    |
| <b>Combinatorial Delays from Input Pins to Output Pins</b>                                   |                                                                                      |              |              |              |       |
| TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_M                                                          | {A, B} input to {P, CARRYOUT} output using multiplier                                | 2.78         | 3.22         | 3.84         | ns    |
| TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_NM                                                         | {A, B} input to {P, CARRYOUT} output not using multiplier                            | 1.59         | 1.77         | 2.22         | ns    |
| TDSPDO_{CP, CCRYOUT, CRYINP, CRYINCRYOUT}                                                    | {C, CARRYIN} input to {P, CARRYOUT} output                                           | 1.50         | 1.67         | 2.08         | ns    |
| <b>Combinatorial Delays from Input Pins to Cascading Output Pins</b>                         |                                                                                      |              |              |              |       |
| TDSPDO_{AACOUT, BBCOUT}                                                                      | {A, B} input to {ACOUT, BCOUT} output                                                | 1.00         | 1.12         | 1.31         | ns    |
| TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_M                    | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier           | 2.78         | 3.22         | 3.84         | ns    |
| TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_NM                   | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier       | 1.72         | 1.92         | 2.42         | ns    |
| TDSPDO_{CPCOUT, CCRYCOUT, CMULTSIGNOUT, CRYINPCOUT, CRYINCRYCOUT, CRYINMULTSIGNOUT}          | {C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output                      | 1.63         | 1.82         | 2.28         | ns    |
| <b>Combinatorial Delays from Cascading Input Pins to All Output Pins</b>                     |                                                                                      |              |              |              |       |
| TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_M                                              | {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier                          | 2.78         | 3.22         | 3.84         | ns    |
| TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_NM                                             | {ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier                      | 1.59         | 1.77         | 2.22         | ns    |
| TDSPDO_{ACINACOUT, BCINBCOUT}                                                                | {ACIN, BCIN} input to {ACOUT, BCOUT} output                                          | 1.00         | 1.12         | 1.31         | ns    |
| TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_M  | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier     | 2.78         | 3.22         | 3.84         | ns    |
| TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_NM | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.72         | 1.92         | 2.42         | ns    |
| TDSPDO_{PCINP, CRYCINP, MULTSIGNINP, PCINCRYOUT, CRYCINCRYOUT, MULTSIGNINCRYOUT}             | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output                        | 1.30         | 1.45         | 1.82         | ns    |

Table 69: DSP48E Switching Characteristics (Cont'd)

| Symbol                                                                                                                                                     | Description                                                                        | Speed |      |      | Units |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-------|------|------|-------|
|                                                                                                                                                            |                                                                                    | -3    | -2   | -1   |       |
| TDSPDO_{PCINPCOUT, CRYCINPCOUT, MULTSIGNINPCOUT, PCINCRYCOUT, CRYCINCRYCOUT, MULTSIGNINCRYCOUT, PCINMULTSIGNOUT, CRYCINMULTSIGNOUT, MULTSIGNINMULTSIGNOUT} | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.43  | 1.60 | 2.02 | ns    |
| <b>Clock to Outs from Output Register Clock to Output Pins</b>                                                                                             |                                                                                    |       |      |      |       |
| TDSPCKO_{PP, CRYOUTP}                                                                                                                                      | CLK (PREG) to {P, CARRYOUT} output                                                 | 0.45  | 0.48 | 0.56 | ns    |
| TDSPCKO_{CRYCOUTP, PCOUTP, MULTSIGNOUTP}                                                                                                                   | CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output                            | 0.48  | 0.53 | 0.62 | ns    |
| <b>Clock to Outs from Pipeline Register Clock to Output Pins</b>                                                                                           |                                                                                    |       |      |      |       |
| TDSPCKO_{PM, CRYOUTM}                                                                                                                                      | CLK (MREG) to {P, CARRYOUT} output                                                 | 1.81  | 2.10 | 2.47 | ns    |
| TDSPCKO_{PCOUTM, CRYCOUTM, MULTSIGNOUTM}                                                                                                                   | CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output                            | 1.91  | 2.13 | 2.66 | ns    |
| <b>Clock to Outs from Input Register Clock to Output Pins</b>                                                                                              |                                                                                    |       |      |      |       |
| TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_M                                                                                                                       | CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier                          | 3.09  | 3.57 | 4.23 | ns    |
| TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_NM                                                                                                                      | CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier                      | 1.90  | 2.11 | 2.63 | ns    |
| TDSPCKO_{PC, CRYOUTC}                                                                                                                                      | CLK (CREG) to {P, CARRYOUT} output                                                 | 1.89  | 2.11 | 2.62 | ns    |
| <b>Clock to Outs from Input Register Clock to Cascading Output Pins</b>                                                                                    |                                                                                    |       |      |      |       |
| TDSPCKO_{ACOUTA, BCOUTB}                                                                                                                                   | CLK (AREG, BREG) to {ACOUT, BCOUT}                                                 | 0.61  | 0.68 | 0.79 | ns    |
| TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_M                                                                                 | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier     | 3.09  | 3.57 | 4.23 | ns    |
| TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_NM                                                                                | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 2.03  | 2.27 | 2.82 | ns    |
| TDSPCKO_{PCOUTC, CRYCOUTC, MULTSIGNOUTC}                                                                                                                   | CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output                            | 2.03  | 2.26 | 2.82 | ns    |
| <b>Maximum Frequency</b>                                                                                                                                   |                                                                                    |       |      |      |       |
| F <sub>MAX</sub>                                                                                                                                           | With all registers used                                                            | 550   | 500  | 450  | MHz   |
| F <sub>MAX_PATDET</sub>                                                                                                                                    | With pattern detector                                                              | 515   | 465  | 410  | MHz   |
| F <sub>MAX_MULT_NOMREG</sub>                                                                                                                               | Two register multiply without MREG                                                 | 374   | 324  | 275  | MHz   |
| F <sub>MAX_MULT_NOMREG_PATDET</sub>                                                                                                                        | Two register multiply without MREG with pattern detect                             | 345   | 300  | 254  | MHz   |

## Configuration Switching Characteristics

Table 70: Configuration Switching Characteristics

| Symbol                                                        | Description                                                    | Speed Grade |            |            | Units       |
|---------------------------------------------------------------|----------------------------------------------------------------|-------------|------------|------------|-------------|
|                                                               |                                                                | -3          | -2         | -1         |             |
| Power-up Timing Characteristics                               |                                                                |             |            |            |             |
| T <sub>PL</sub>                                               | Program Latency                                                | 3           | 3          | 3          | ms, Max     |
| T <sub>POR</sub>                                              | Power-on-Reset                                                 | 10<br>50    | 10<br>50   | 10<br>50   | ms, Min/Max |
| T <sub>ICCK</sub>                                             | CCLK (output) delay                                            | 400         | 400        | 400        | ns, Min     |
| T <sub>PROGRAM</sub>                                          | Program Pulse Width                                            | 250         | 250        | 250        | ns, Min     |
| Master/Slave Serial Mode Programming Switching <sup>(1)</sup> |                                                                |             |            |            |             |
| T <sub>DCCK</sub> /T <sub>CCKD</sub>                          | DIN Setup/Hold, slave mode                                     | 4.0<br>0.0  | 4.0<br>0.0 | 4.0<br>0.0 | ns, Min     |
| T <sub>DSCCK</sub> /T <sub>SCCKD</sub>                        | DIN Setup/Hold, master mode                                    | 4.0<br>0.0  | 4.0<br>0.0 | 4.0<br>0.0 | ns, Min     |
| T <sub>CCO</sub>                                              | DOUT                                                           | 7.5         | 7.5        | 7.5        | ns, Max     |
| F <sub>MCCK</sub>                                             | Maximum Frequency, master mode with respect to nominal CCLK.   | 100         | 100        | 100        | MHz, Max    |
| F <sub>MCCKTOL</sub>                                          | Frequency Tolerance, master mode with respect to nominal CCLK. | ±50         | ±50        | ±50        | %           |
| F <sub>MSCCK</sub>                                            | Slave mode external CCLK                                       | 100         | 100        | 100        | MHz         |
| SelectMAP Mode Programming Switching <sup>(1)</sup>           |                                                                |             |            |            |             |
| T <sub>SMDCK</sub> /T <sub>SMCKD</sub>                        | SelectMAP Data Setup/Hold                                      | 3.0<br>0.5  | 3.0<br>0.5 | 3.0<br>0.5 | ns, Min     |
| T <sub>SMCSCCK</sub> /T <sub>SMCKCS</sub>                     | CS_B Setup/Hold                                                | 3.0<br>0.5  | 3.0<br>0.5 | 3.0<br>0.5 | ns, Min     |
| T <sub>SMCKKW</sub> /T <sub>SMWCKK</sub>                      | RDWR_B Setup/Hold                                              | 8.0<br>0.5  | 8.0<br>0.5 | 8.0<br>0.5 | ns, Min     |
| T <sub>SMCKCSO</sub>                                          | CSO_B clock to out (330 Ω pull-up resistor required)           | 10          | 10         | 10         | ns, Min     |
| T <sub>SMCO</sub>                                             | CCLK to DATA out in readback                                   | 9.0         | 9.0        | 9.0        | ns, Max     |
| T <sub>SMCKBY</sub>                                           | CCLK to BUSY out in readback                                   | 7.5         | 7.5        | 7.5        | ns, Max     |
| F <sub>SMCKK</sub>                                            | Maximum Frequency with respect to nominal CCLK.                | 100         | 100        | 100        | MHz, Max    |
| F <sub>RBCKK</sub>                                            | Maximum Readback Frequency with respect to nominal CCLK        | 60          | 60         | 60         | MHz, Max    |
| F <sub>MCCKTOL</sub>                                          | Frequency Tolerance with respect to nominal CCLK.              | ±50         | ±50        | ±50        | %           |
| Boundary-Scan Port Timing Specifications                      |                                                                |             |            |            |             |
| T <sub>TAPTCK</sub>                                           | TMS and TDI Setup time before TCK                              | 1.0         | 1.0        | 1.0        | ns, Min     |
| T <sub>TCKTAP</sub>                                           | TMS and TDI Hold time after TCK                                | 2.0         | 2.0        | 2.0        | ns, Min     |
| T <sub>TCKTDO</sub>                                           | TCK falling edge to TDO output valid                           | 6           | 6          | 6          | ns, Max     |
| F <sub>TCK</sub>                                              | Maximum configuration TCK clock frequency                      | 66          | 66         | 66         | MHz, Max    |
| F <sub>TCKB</sub>                                             | Maximum boundary-scan TCK clock frequency                      | 66          | 66         | 66         | MHz, Max    |

Table 70: Configuration Switching Characteristics (Cont'd)

| Symbol                                                                   | Description                                                                   | Speed Grade |             |             | Units       |
|--------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------|-------------|-------------|-------------|
|                                                                          |                                                                               | -3          | -2          | -1          |             |
| BPI Master Flash Mode Programming Switching                              |                                                                               |             |             |             |             |
| T <sub>BPICCO</sub> <sup>(4)</sup>                                       | ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge | 10          | 10          | 10          | ns          |
| T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>                                 | Setup/Hold on D[15:0] data input pins                                         | 3.0<br>0.5  | 3.0<br>0.5  | 3.0<br>0.5  | ns          |
| T <sub>INITADDR</sub>                                                    | Minimum period of initial ADDR[25:0] address cycles                           | 3.0         | 3.0         | 3.0         | CCLK cycles |
| SPI Master Flash Mode Programming Switching                              |                                                                               |             |             |             |             |
| T <sub>SPIDCC</sub> /T <sub>SPIDCCD</sub>                                | DIN Setup/Hold before/after the rising CCLK edge                              | 4.0<br>0.0  | 4.0<br>0.0  | 4.0<br>0.0  | ns          |
| T <sub>SPICCM</sub>                                                      | MOSI clock to out                                                             | 10          | 10          | 10          | ns          |
| T <sub>SPICCF</sub>                                                      | FCS_B clock to out                                                            | 10          | 10          | 10          | ns          |
| T <sub>FSINIT</sub> /T <sub>FSINITH</sub>                                | FS[2:0] to INIT_B rising edge Setup and Hold                                  | 2           | 2           | 2           | μs          |
| CCLK Output (Master Modes)                                               |                                                                               |             |             |             |             |
| T <sub>MCCKL</sub>                                                       | Master CCLK clock minimum Low time                                            | 3.0         | 3.0         | 3.0         | ns, Min     |
| T <sub>MCCKH</sub>                                                       | Master CCLK clock minimum High time                                           | 3.0         | 3.0         | 3.0         | ns, Min     |
| CCLK Input (Slave Modes)                                                 |                                                                               |             |             |             |             |
| T <sub>SCCKL</sub>                                                       | Slave CCLK clock minimum Low time                                             | 2.0         | 2.0         | 2.0         | ns, Min     |
| T <sub>SCCKH</sub>                                                       | Slave CCLK clock minimum High time                                            | 2.0         | 2.0         | 2.0         | ns, Min     |
| Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK |                                                                               |             |             |             |             |
| F <sub>DCK</sub>                                                         | Maximum frequency for DCLK                                                    | 500         | 450         | 400         | MHz         |
| T <sub>DMCKC_DADDR</sub> /T <sub>DMCKC_DADDR</sub>                       | DADDR Setup/Hold                                                              | 1.2<br>0.0  | 1.35<br>0.0 | 1.56<br>0.0 | ns          |
| T <sub>DMCKC_DI</sub> /T <sub>DMCKC_DI</sub>                             | DI Setup/Hold                                                                 | 1.2<br>0.0  | 1.35<br>0.0 | 1.56<br>0.0 | ns          |
| T <sub>DMCKC_DEN</sub> /T <sub>DMCKC_DEN</sub>                           | DEN Setup/Hold time                                                           | 1.2<br>0.0  | 1.35<br>0.0 | 1.56<br>0.0 | ns          |
| T <sub>DMCKC_DWE</sub> /T <sub>DMCKC_DWE</sub>                           | DWE Setup/Hold time                                                           | 1.2<br>0.0  | 1.35<br>0.0 | 1.56<br>0.0 | ns          |
| T <sub>DMCKO_DO</sub>                                                    | CLK to out of DO <sup>(3)</sup>                                               | 1.0         | 1.12        | 1.3         | ns          |
| T <sub>DMCKO_DRDY</sub>                                                  | CLK to out of DRDY                                                            | 1.0         | 1.12        | 1.3         | ns          |

**Notes:**

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG190: Virtex-5 FPGA User Guide](#).
- DO will hold until next DRP operation.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## Clock Buffers and Networks

Table 71: Global Clock Switching Characteristics (Including BUFGCTRL)

| Symbol                                                      | Description                    | Devices                                                                                       | Speed Grade  |              |              | Units |
|-------------------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------|--------------|--------------|--------------|-------|
|                                                             |                                |                                                                                               | -3           | -2           | -1           |       |
| T <sub>BCCCK_CE</sub> /T <sub>BCCCK_CE</sub> <sup>(1)</sup> | CE pins Setup/Hold             | All                                                                                           | 0.27<br>0.00 | 0.27<br>0.00 | 0.31<br>0.00 | ns    |
| T <sub>BCCCK_S</sub> /T <sub>BCCCK_S</sub> <sup>(1)</sup>   | S pins Setup/Hold              | All                                                                                           | 0.27<br>0.00 | 0.27<br>0.00 | 0.31<br>0.00 | ns    |
| T <sub>BCCCK_O</sub> <sup>(2)</sup>                         | BUFGCTRL delay from I0/I1 to O | LX20T                                                                                         | N/A          | 0.24         | 0.30         | ns    |
|                                                             |                                | LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, SX50T, FX70T, FX100T, and FX130T | 0.19         | 0.22         | 0.25         | ns    |
|                                                             |                                | FX30T                                                                                         | 0.23         | 0.23         | 0.25         | ns    |
|                                                             |                                | LX155 and LX155T                                                                              | 0.12         | 0.14         | 0.30         | ns    |
|                                                             |                                | LX220, LX220T, LX330, LX330T, SX95T, SX240T, TX150T, TX240T, and FX200T                       | N/A          | 0.22         | 0.25         | ns    |
| Maximum Frequency                                           |                                |                                                                                               |              |              |              |       |
| F <sub>MAX</sub>                                            | Global clock tree (BUFG)       | LX20T                                                                                         | N/A          | 667          | 600          | MHz   |
|                                                             |                                | LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, SX50T, FX30T, and FX70T          | 710          | 667          | 600          | MHz   |
|                                                             |                                | LX155, LX155T, and FX100T                                                                     | 650          | 600          | 550          | MHz   |
|                                                             |                                | FX130T                                                                                        | 550          | 500          | 450          | MHz   |
|                                                             |                                | LX220, LX220T, LX330, LX330T, SX95T, SX240T, TX150T, TX240T, and FX200T                       | N/A          | 500          | 450          | MHz   |

### Notes:

- $T_{BCCCK\_CE}$  and  $T_{BCKCK\_CE}$  must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX\_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- $T_{BGCKO\_O}$  (BUFG delay from I0 to O) values are the same as  $T_{BCKCK\_O}$  values.

Table 72: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol                   | Description                    | Speed Grade |      |      | Units |
|--------------------------|--------------------------------|-------------|------|------|-------|
|                          |                                | -3          | -2   | -1   |       |
| $T_{BUFIOCKO\_O}$        | Clock to out delay from I to O | 1.08        | 1.16 | 1.29 | ns    |
| <b>Maximum Frequency</b> |                                |             |      |      |       |
| $F_{MAX}$                | I/O clock tree (BUFIO)         | 710         | 710  | 644  | MHz   |

Table 73: Regional Clock Switching Characteristics (BUFR)

| Symbol                   | Description                                                     | Devices                                                                                              | Speed Grade |      |      | Units |
|--------------------------|-----------------------------------------------------------------|------------------------------------------------------------------------------------------------------|-------------|------|------|-------|
|                          |                                                                 |                                                                                                      | -3          | -2   | -1   |       |
| $T_{BRCKO\_O}$           | Clock to out delay from I to O                                  | LX20T                                                                                                | N/A         | 0.79 | 0.90 | ns    |
|                          |                                                                 | LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, SX50T, FX100T, and FX130T               | 0.56        | 0.59 | 0.67 | ns    |
|                          |                                                                 | FX30T                                                                                                | 0.72        | 0.78 | 0.86 | ns    |
|                          |                                                                 | FX70T                                                                                                | 0.69        | 0.74 | 0.83 | ns    |
|                          |                                                                 | LX155 and LX155T                                                                                     | 0.73        | 0.80 | 0.90 | ns    |
|                          |                                                                 | LX220, LX220T, LX330, LX330T, SX95T, SX240T, TX150T, TX240T, and FX200T                              | N/A         | 0.59 | 0.67 | ns    |
| $T_{BRCKO\_O\_BYP}$      | Clock to out delay from I to O with Divide Bypass attribute set | LX20T                                                                                                | N/A         | 0.29 | 0.30 | ns    |
|                          |                                                                 | LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, SX50T, FX30T, FX70T, FX100T, and FX130T | 0.23        | 0.24 | 0.26 | ns    |
|                          |                                                                 | LX155 and LX155T                                                                                     | 0.24        | 0.26 | 0.30 | ns    |
|                          |                                                                 | LX220, LX220T, LX330, LX330T, SX95T, SX240T, TX150T, TX240T, and FX200T                              | N/A         | 0.24 | 0.26 | ns    |
| $T_{BRDO\_CLRO}$         | Propagation delay from CLR to O                                 | All                                                                                                  | 0.61        | 0.70 | 0.82 | ns    |
| <b>Maximum Frequency</b> |                                                                 |                                                                                                      |             |      |      |       |
| $F_{MAX}$                | Regional clock tree (BUFR)                                      | All                                                                                                  | 300         | 250  | 250  | MHz   |

## PLL Switching Characteristics

Table 74: PLL Specification

| Symbol             | Description                                                                                                                   | Speed Grade                             |       |       | Units |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|-------|-------|-------|
|                    |                                                                                                                               | -3                                      | -2    | -1    |       |
| $F_{INMAX}$        | Maximum Input Clock Frequency                                                                                                 | 710                                     | 710   | 645   | MHz   |
| $F_{INMIN}$        | Minimum Input Clock Frequency                                                                                                 | 19                                      | 19    | 19    | MHz   |
| $F_{INJITTER}$     | Maximum Input Clock Period Jitter                                                                                             | <20% of clock input period or 1 ns Max  |       |       |       |
| $F_{INDUTY}$       | Allowable Input Duty Cycle: 19—49 MHz                                                                                         | 25/75                                   |       |       | %     |
|                    | Allowable Input Duty Cycle: 50—199 MHz                                                                                        | 30/70                                   |       |       | %     |
|                    | Allowable Input Duty Cycle: 200—399 MHz                                                                                       | 35/65                                   |       |       | %     |
|                    | Allowable Input Duty Cycle: 400—499 MHz                                                                                       | 40/60                                   |       |       | %     |
|                    | Allowable Input Duty Cycle: >500 MHz                                                                                          | 45/55                                   |       |       | %     |
| $F_{VCOMIN}$       | Minimum PLL VCO Frequency                                                                                                     | 400                                     | 400   | 400   | MHz   |
| $F_{VCOMAX}$       | Maximum PLL VCO Frequency                                                                                                     | 1440                                    | 1200  | 1000  | MHz   |
| $F_{BANDWIDTH}$    | Low PLL Bandwidth at Typical <sup>(1)</sup>                                                                                   | 1                                       | 1     | 1     | MHz   |
|                    | High PLL Bandwidth at Typical <sup>(1)</sup>                                                                                  | 4                                       | 4     | 4     | MHz   |
| $T_{STAPHAOFFSET}$ | Static Phase Offset of the PLL Outputs                                                                                        | 120                                     | 120   | 120   | ps    |
| $T_{OUTJITTER}$    | PLL Output Jitter <sup>(2)</sup>                                                                                              | Note 1                                  |       |       |       |
| $T_{OUTDUTY}$      | PLL Output Clock Duty Cycle Precision <sup>(3)</sup>                                                                          | ±150                                    | ±200  | ±200  | ps    |
| $T_{LOCKMAX}$      | PLL Maximum Lock Time <sup>(4)</sup>                                                                                          | 100                                     | 100   | 100   | µs    |
| $F_{OUTMAX}$       | PLL Maximum Output Frequency for LX20T devices                                                                                | N/A                                     | 667   | 600   | MHz   |
|                    | PLL Maximum Output Frequency for LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, SX50T, FX30T, and FX70T devices | 710                                     | 667   | 600   | MHz   |
|                    | PLL Maximum Output Frequency for LX155, LX155T, and FX100T devices                                                            | 650                                     | 600   | 550   | MHz   |
|                    | PLL Maximum Output Frequency for FX130T devices                                                                               | 550                                     | 500   | 450   | MHz   |
|                    | PLL Maximum Output Frequency for LX220, LX220T, LX330, LX330T, SX95T, SX240T, TX150T, TX240T, and FX200T devices              | N/A                                     | 500   | 450   | MHz   |
| $F_{OUTMIN}$       | PLL Minimum Output Frequency <sup>(5)</sup>                                                                                   | 3.125                                   | 3.125 | 3.125 | MHz   |
| $T_{EXTFDVAR}$     | External Clock Feedback Variation                                                                                             | < 20% of clock input period or 1 ns Max |       |       |       |
| $RST_{MINPULSE}$   | Minimum Reset Pulse Width                                                                                                     | 5                                       | 5     | 5     | ns    |
| $F_{PFDMAX}$       | Maximum Frequency at the Phase Frequency Detector                                                                             | 550                                     | 500   | 450   | MHz   |
| $F_{PFDMIN}$       | Minimum Frequency at the Phase Frequency Detector                                                                             | 19                                      | 19    | 19    | MHz   |
| $T_{FBDELAY}$      | Maximum External Delay in the Feedback Path                                                                                   | 3 ns Max or one CLKIN cycle             |       |       |       |

### Notes:

1. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. Values for this parameter are available in the Architecture Wizard.
3. Includes global clock buffer.
4. The LOCK signal must be sampled after  $T_{LOCKMAX}$ . The LOCK signal is invalid after configuration or reset until the  $T_{LOCKMAX}$  time has expired.
5. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.

Table 75: PLL in PMCD Mode Switching Characteristics

| Symbol                           | Description                             | Speed Grade  |              |              | Units |
|----------------------------------|-----------------------------------------|--------------|--------------|--------------|-------|
|                                  |                                         | -3           | -2           | -1           |       |
| $T_{PLLCK\_REL}/T_{PLLCKC\_REL}$ | REL Setup and Hold for all Outputs      | 0.00<br>0.60 | 0.00<br>0.60 | 0.00<br>0.60 | ns    |
| $T_{PLLCKO}$                     | Maximum Clock Propagation Delay         | 4.6          | 4.6          | 5.2          | ns    |
| CLKIN_FREQ_MAX                   | Maximum Input Frequency                 | 710          | 710          | 645          | MHz   |
| CLKIN_FREQ_MIN                   | Minimum Input Frequency                 | 1            | 1            | 1            | MHz   |
| CLKIN_DUTY_CYCLE                 | Allowable Input Duty Cycle: 1—49 MHz    | 25/75        |              |              | %     |
|                                  | Allowable Input Duty Cycle: 50—199 MHz  | 30/70        |              |              | %     |
|                                  | Allowable Input Duty Cycle: 200—399 MHz | 35/65        |              |              | %     |
|                                  | Allowable Input Duty Cycle: 400—499 MHz | 40/60        |              |              | %     |
|                                  | Allowable Input Duty Cycle: >500 MHz    | 45/55        |              |              | %     |
| RES_REL_PULSE_MIN                | Minimum Pulse Width for RST and REL     | 5            | 5            | 5            | ns    |

## DCM Switching Characteristics

Table 76: Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode

| Symbol                               | Description                                         | Speed Grade |        |        | Units |  |
|--------------------------------------|-----------------------------------------------------|-------------|--------|--------|-------|--|
|                                      |                                                     | -3          | -2     | -1     |       |  |
| Outputs Clocks (Low Frequency Mode)  |                                                     |             |        |        |       |  |
| F <sub>1XLFMSMIN</sub>               | CLK0, CLK90, CLK180, CLK270                         | 32.00       | 32.00  | 32.00  | MHz   |  |
| F <sub>1XLFMSMAX</sub>               |                                                     | 150.00      | 135.00 | 120.00 | MHz   |  |
| F <sub>2XLFMSMIN</sub>               | CLK2X, CLK2X180                                     | 64.00       | 64.00  | 64.00  | MHz   |  |
| F <sub>2XLFMSMAX</sub>               |                                                     | 300.00      | 270.00 | 240.00 | MHz   |  |
| F <sub>DVLFMSMIN</sub>               | CLKDV                                               | 2.0         | 2.0    | 2.0    | MHz   |  |
| F <sub>DVLFMSMAX</sub>               |                                                     | 100.00      | 90.00  | 80.00  | MHz   |  |
| F <sub>FXLFMSMIN</sub>               | CLKFX, CLKFX180                                     | 32.00       | 32.00  | 32.00  | MHz   |  |
| F <sub>FXLFMSMAX</sub>               |                                                     | 180.00      | 160.00 | 140.00 | MHz   |  |
| Input Clocks (Low Frequency Mode)    |                                                     |             |        |        |       |  |
| F <sub>DLLLFMSMIN</sub>              | CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>      | 32.00       | 32.00  | 32.00  | MHz   |  |
| F <sub>DLLLFMSMAX</sub>              |                                                     | 150.00      | 135.00 | 120.00 | MHz   |  |
| F <sub>CLKINLFFXMSMIN</sub>          | CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup> | 1.00        | 1.00   | 1.00   | MHz   |  |
| F <sub>CLKINLFFXMSMAX</sub>          |                                                     | 180.00      | 160.00 | 140.00 | MHz   |  |
| F <sub>PSCLKLFMSMIN</sub>            | PSCLK                                               | 1.00        | 1.00   | 1.00   | KHz   |  |
| F <sub>PSCLKLFMSMAX</sub>            |                                                     | 550.00      | 500.00 | 450.00 | MHz   |  |
| Outputs Clocks (High Frequency Mode) |                                                     |             |        |        |       |  |
| F <sub>1XHFMSMIN</sub>               | CLK0, CLK90, CLK180, CLK270                         | 120.00      | 120.00 | 120.00 | MHz   |  |
| F <sub>1XHFMSMAX</sub>               |                                                     | 550.00      | 500.00 | 450.00 | MHz   |  |
| F <sub>2XHFMSMIN</sub>               | CLK2X, CLK2X180                                     | 240.00      | 240.00 | 240.00 | MHz   |  |
| F <sub>2XHFMSMAX</sub>               |                                                     | 550.00      | 500.00 | 450.00 | MHz   |  |
| F <sub>DVHFMSMIN</sub>               | CLKDV                                               | 7.5         | 7.5    | 7.5    | MHz   |  |
| F <sub>DVHFMSMAX</sub>               |                                                     | 366.67      | 333.34 | 300.00 | MHz   |  |
| F <sub>FXHFMSMIN</sub>               | CLKFX, CLKFX180                                     | 140.00      | 140.00 | 140.00 | MHz   |  |
| F <sub>FXHFMSMAX</sub>               |                                                     | 400.00      | 375.00 | 350.00 | MHz   |  |
| Input Clocks (High Frequency Mode)   |                                                     |             |        |        |       |  |
| F <sub>DLLHFMSMIN</sub>              | CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>      | 120.00      | 120.00 | 120.00 | MHz   |  |
| F <sub>DLLHFMSMAX</sub>              |                                                     | 550.00      | 500.00 | 450.00 | MHz   |  |
| F <sub>CLKINHFFXMSMIN</sub>          | CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup> | 25.00       | 25.00  | 25.00  | MHz   |  |
| F <sub>CLKINHFFXMSMAX</sub>          |                                                     | 400.00      | 375.00 | 350.00 | MHz   |  |
| F <sub>PSCLKHFMSMIN</sub>            | PSCLK                                               | 1.00        | 1.00   | 1.00   | KHz   |  |
| F <sub>PSCLKHFMSMAX</sub>            |                                                     | 550.00      | 500.00 | 450.00 | MHz   |  |

### Notes:

1. DLL outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN\_DIVIDE\_BY\_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN\_DIVIDE\_BY\_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 77: Operating Frequency Ranges for DCM in Maximum Range (MR) Mode

| Symbol                              | Description                                         | Speed Grade |        |        | Units |  |
|-------------------------------------|-----------------------------------------------------|-------------|--------|--------|-------|--|
|                                     |                                                     | -3          | -2     | -1     |       |  |
| Outputs Clocks (Low Frequency Mode) |                                                     |             |        |        |       |  |
| F <sub>1XMRMIN</sub>                | CLK0, CLK90, CLK180, CLK270                         | 19.00       | 19.00  | 19.00  | MHz   |  |
| F <sub>1XMRMAX</sub>                |                                                     | 32.00       | 32.00  | 32.00  | MHz   |  |
| F <sub>2XMRMIN</sub>                | CLK2X, CLK2X180                                     | 38.00       | 38.00  | 38.00  | MHz   |  |
| F <sub>2XMRMAX</sub>                |                                                     | 64.00       | 64.00  | 64.00  | MHz   |  |
| F <sub>DLLMRMIN</sub>               | CLKDV                                               | 1.19        | 1.19   | 1.19   | MHz   |  |
| F <sub>DLLMRMAX</sub>               |                                                     | 21.34       | 21.34  | 21.34  | MHz   |  |
| F <sub>FXMRMIN</sub>                | CLKFX, CLKFX180                                     | 19.00       | 19.00  | 19.00  | MHz   |  |
| F <sub>FXMRMAX</sub>                |                                                     | 40.00       | 40.00  | 40.00  | MHz   |  |
| Input Clocks (Low Frequency Mode)   |                                                     |             |        |        |       |  |
| F <sub>CLKINDLLMRMIN</sub>          | CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>      | 19.00       | 19.00  | 19.00  | MHz   |  |
| F <sub>CLKINDLLMRMAX</sub>          |                                                     | 32.00       | 32.00  | 32.00  | MHz   |  |
| F <sub>CLKINFXMRMIN</sub>           | CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup> | 1.00        | 1.00   | 1.00   | MHz   |  |
| F <sub>CLKINFXMRMAX</sub>           |                                                     | 40.00       | 40.00  | 40.00  | MHz   |  |
| F <sub>PSCLKMRMIN</sub>             | PSCLK                                               | 1.00        | 1.00   | 1.00   | KHz   |  |
| F <sub>PSCLKMRMAX</sub>             |                                                     | 300.00      | 270.00 | 240.00 | MHz   |  |

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN\_DIVIDE\_BY\_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN\_DIVIDE\_BY\_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 78: Input Clock Tolerances

| Symbol                                               | Description                              | Frequency Range              |        | Value   | Units |
|------------------------------------------------------|------------------------------------------|------------------------------|--------|---------|-------|
| Duty Cycle Input Tolerance (in %)                    |                                          |                              |        |         |       |
| T <sub>DUTYCYCRANGE_1</sub>                          | PSCLK only                               | < 1 MHz                      |        | 25 - 75 | %     |
| T <sub>DUTYCYCRANGE_1_50</sub>                       | PSCLK and CLKIN                          | 1 - 50 MHz                   |        | 25 - 75 | %     |
| T <sub>DUTYCYCRANGE_50_100</sub>                     |                                          | 50 - 100 MHz                 |        | 30 - 70 | %     |
| T <sub>DUTYCYCRANGE_100_200</sub>                    |                                          | 100 - 200 MHz                |        | 40 - 60 | %     |
| T <sub>DUTYCYCRANGE_200_400</sub>                    |                                          | 200 - 400 MHz <sup>(4)</sup> |        | 45 - 55 | %     |
| T <sub>DUTYCYCRANGE_400</sub>                        |                                          | > 400 MHz                    |        | 45 - 55 | %     |
| Input Clock Cycle-Cycle Jitter (Low Frequency Mode)  |                                          | Speed Grade                  |        |         | Units |
|                                                      |                                          | -3                           | -2     | -1      |       |
| T <sub>CYCLFDLL</sub>                                | CLKIN (using DLL outputs) <sup>(1)</sup> | 300.00                       | 300.00 | 345.00  | ps    |
| T <sub>CYCLFFX</sub>                                 | CLKIN (using DFS outputs) <sup>(2)</sup> | 300.00                       | 300.00 | 345.00  | ps    |
| Input Clock Cycle-Cycle Jitter (High Frequency Mode) |                                          |                              |        |         |       |
| T <sub>CYCHFDLL</sub>                                | CLKIN (using DLL outputs) <sup>(1)</sup> | 150.00                       | 150.00 | 173.00  | ps    |
| T <sub>CYCHFFX</sub>                                 | CLKIN (using DFS outputs) <sup>(2)</sup> | 150.00                       | 150.00 | 173.00  | ps    |
| Input Clock Period Jitter (Low Frequency Mode)       |                                          |                              |        |         |       |
| T <sub>PERLFDLL</sub>                                | CLKIN (using DLL outputs) <sup>(1)</sup> | 1.00                         | 1.00   | 1.15    | ns    |
| T <sub>PERLFFX</sub>                                 | CLKIN (using DFS outputs) <sup>(2)</sup> | 1.00                         | 1.00   | 1.15    | ns    |
| Input Clock Period Jitter (High Frequency Mode)      |                                          |                              |        |         |       |
| T <sub>PERHFDLL</sub>                                | CLKIN (using DLL outputs) <sup>(1)</sup> | 1.00                         | 1.00   | 1.15    | ns    |
| T <sub>PERHFFX</sub>                                 | CLKIN (using DFS outputs) <sup>(2)</sup> | 1.00                         | 1.00   | 1.15    | ns    |
| Feedback Clock Path Delay Variation                  |                                          |                              |        |         |       |
| T <sub>CLKFB_DELAY_VAR</sub>                         | CLKFB off-chip feedback                  | 1.00                         | 1.00   | 1.15    | ns    |

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.
4. This duty cycle specification does not apply to the GTP\_DUAL to DCM or GTX\_DUAL to DCM connection. The GTP transceivers drive the DCMs at the following frequencies: 320 MHz for -1 speed grade devices, 375 MHz for -2 speed grade devices, or 375 MHz for -3 speed grade devices. The GTX transceivers drive the DCMs at the following frequencies: 450 MHz for -1 speed grade devices or 500 MHz for -2 speed grade devices.

## Output Clock Jitter

Table 79: Output Clock Jitter

| Symbol                        | Description                  | Constraints | Speed Grade |        |        | Units |
|-------------------------------|------------------------------|-------------|-------------|--------|--------|-------|
|                               |                              |             | -3          | -2     | -1     |       |
| Clock Synthesis Period Jitter |                              |             |             |        |        |       |
| T <sub>PERJITT_0</sub>        | CLK0                         |             | ±120        | ±120   | ±120   | ps    |
| T <sub>PERJITT_90</sub>       | CLK90                        |             | ±120        | ±120   | ±120   | ps    |
| T <sub>PERJITT_180</sub>      | CLK180                       |             | ±120        | ±120   | ±120   | ps    |
| T <sub>PERJITT_270</sub>      | CLK270                       |             | ±120        | ±120   | ±120   | ps    |
| T <sub>PERJITT_2X</sub>       | CLK2X, CLK2X180              |             | ±200        | ±200   | ±230   | ps    |
| T <sub>PERJITT_DV1</sub>      | CLKDV (integer division)     |             | ±150        | ±150   | ±180   | ps    |
| T <sub>PERJITT_DV2</sub>      | CLKDV (non-integer division) |             | ±300        | ±300   | ±345   | ps    |
| T <sub>PERJITT_FX</sub>       | CLKFX, CLKFX180              |             | Note 1      | Note 1 | Note 1 | ps    |

### Notes:

- Values for this parameter are available in the Architecture Wizard.

## Output Clock Phase Alignment

Table 80: Output Clock Phase Alignment

| Symbol                                              | Description                 | Constraints | Speed Grade |      |      | Units |
|-----------------------------------------------------|-----------------------------|-------------|-------------|------|------|-------|
|                                                     |                             |             | -3          | -2   | -1   |       |
| Phase Offset Between CLKIN and CLKFB                |                             |             |             |      |      |       |
| T <sub>IN_FB_OFFSET</sub>                           | CLKIN/CLKFB                 |             | ±50         | ±50  | ±60  | ps    |
| Phase Offset Between Any DCM Outputs <sup>(1)</sup> |                             |             |             |      |      |       |
| T <sub>OUT_OFFSET_1X</sub>                          | CLK0, CLK90, CLK180, CLK270 |             | ±140        | ±140 | ±160 | ps    |
| T <sub>OUT_OFFSET_2X</sub>                          | CLK2X, CLK2X180, CLKDV      |             | ±150        | ±150 | ±200 | ps    |
| T <sub>OUT_OFFSET_FX</sub>                          | CLKFX, CLKFX180             |             | ±160        | ±160 | ±220 | ps    |
| Duty Cycle Precision <sup>(2)</sup>                 |                             |             |             |      |      |       |
| T <sub>DUTY_CYC_DLL</sub>                           | DLL outputs <sup>(3)</sup>  |             | ±150        | ±150 | ±180 | ps    |
| T <sub>DUTY_CYC_FX</sub>                            | DFS outputs <sup>(4)</sup>  |             | ±150        | ±150 | ±180 | ps    |

### Notes:

- All phase offsets are in respect to group CLK1X.
- CLKOUT\_DUTY\_CYCLE\_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY\_CYCLE\_CORRECTION = TRUE. The duty cycle distortion includes the global clock tree (BUFG).
- DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 81: Miscellaneous Timing Parameters

| Symbol                        | Description                                               | Speed Grade |         |         | Units |
|-------------------------------|-----------------------------------------------------------|-------------|---------|---------|-------|
|                               |                                                           | -3          | -2      | -1      |       |
| Time Required to Achieve LOCK |                                                           |             |         |         |       |
| T <sub>DLL_240</sub>          | DLL output – Frequency range > 240 MHz <sup>(1)</sup>     | 80.00       | 80.00   | 80.00   | μs    |
| T <sub>DLL_120_240</sub>      | DLL output – Frequency range 120 - 240 MHz <sup>(1)</sup> | 250.00      | 250.00  | 250.00  | μs    |
| T <sub>DLL_60_120</sub>       | DLL output – Frequency range 60 - 120 MHz <sup>(1)</sup>  | 900.00      | 900.00  | 900.00  | μs    |
| T <sub>DLL_50_60</sub>        | DLL output – Frequency range 50 - 60 MHz <sup>(1)</sup>   | 1300.00     | 1300.00 | 1300.00 | μs    |
| T <sub>DLL_40_50</sub>        | DLL output – Frequency range 40 - 50 MHz <sup>(1)</sup>   | 2000.00     | 2000.00 | 2000.00 | μs    |
| T <sub>DLL_30_40</sub>        | DLL output – Frequency range 30 - 40 MHz <sup>(1)</sup>   | 3600.00     | 3600.00 | 3600.00 | μs    |
| T <sub>DLL_24_30</sub>        | DLL output – Frequency range 24 - 30 MHz <sup>(1)</sup>   | 5000.00     | 5000.00 | 5000.00 | μs    |
| T <sub>DLL_30</sub>           | DLL output – Frequency range < 30 MHz <sup>(1)</sup>      | 5000.00     | 5000.00 | 5000.00 | μs    |
| T <sub>FX_MIN</sub>           | DFS outputs <sup>(2)</sup>                                | 10.00       | 10.00   | 10.00   | ms    |
| T <sub>FX_MAX</sub>           |                                                           | 10.00       | 10.00   | 10.00   | ms    |
| T <sub>DLL_FINE_SHIFT</sub>   | Multiplication factor for DLL lock time with Fine Shift   | 2.00        | 2.00    | 2.00    |       |
| Fine Phase Shifting           |                                                           |             |         |         |       |
| T <sub>RANGE_MS</sub>         | Absolute shifting range in maximum speed mode             | 7.00        | 7.00    | 7.00    | ns    |
| T <sub>RANGE_MR</sub>         | Absolute shifting range in maximum range mode             | 10.00       | 10.00   | 10.00   | ns    |
| Delay Lines                   |                                                           |             |         |         |       |
| T <sub>TAP_MS_MIN</sub>       | Tap delay resolution (Min) in maximum speed mode          | 7.00        | 7.00    | 7.00    | ps    |
| T <sub>TAP_MS_MAX</sub>       | Tap delay resolution (Max) in maximum speed mode          | 30.00       | 30.00   | 30.00   | ps    |
| T <sub>TAP_MR_MIN</sub>       | Tap delay resolution (Min) in maximum range mode          | 10.00       | 10.00   | 10.00   | ps    |
| T <sub>TAP_MR_MAX</sub>       | Tap delay resolution (Max) in maximum range mode          | 40.00       | 40.00   | 40.00   | ps    |

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 82: Frequency Synthesis

| Attribute      | Min | Max |
|----------------|-----|-----|
| CLKFX_MULTIPLY | 2   | 33  |
| CLKFX_DIVIDE   | 1   | 32  |

Table 83: DCM Switching Characteristics

| Symbol                                     | Description            | Speed Grade  |              |              | Units |
|--------------------------------------------|------------------------|--------------|--------------|--------------|-------|
|                                            |                        | -3           | -2           | -1           |       |
| $T_{DMCK\_PSEN} / T_{DMCKC\_PSEN}$         | PSEN Setup/Hold        | 1.20<br>0.00 | 1.35<br>0.00 | 1.56<br>0.00 | ns    |
| $T_{DMCK\_PSINCDEC} / T_{DMCKC\_PSINCDEC}$ | PSINCDEC Setup/Hold    | 1.20<br>0.00 | 1.35<br>0.00 | 1.56<br>0.00 | ns    |
| $T_{DMCKO\_PSDONE}$                        | Clock to out of PSDONE | 1.00         | 1.12         | 1.30         | ns    |

## Virtex-5 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 84. Values are expressed in nanoseconds unless otherwise noted.

Table 84: Global Clock Input to Output Delay Without DCM or PLL

| Symbol                                                                                                              | Description                                      | Device     | Speed Grade |      |      | Units |
|---------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                     |                                                  |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL |                                                  |            |             |      |      |       |
| T <sub>ICKOF</sub>                                                                                                  | Global Clock and OUTFF <i>without</i> DCM or PLL | XC5VLX20T  | N/A         | 5.98 | 6.69 | ns    |
|                                                                                                                     |                                                  | XC5VLX30   | 5.54        | 6.04 | 6.73 | ns    |
|                                                                                                                     |                                                  | XC5VLX30T  | 5.54        | 6.04 | 6.73 | ns    |
|                                                                                                                     |                                                  | XC5VLX50   | 5.59        | 6.09 | 6.79 | ns    |
|                                                                                                                     |                                                  | XC5VLX50T  | 5.59        | 6.09 | 6.79 | ns    |
|                                                                                                                     |                                                  | XC5VLX85   | 5.78        | 6.28 | 6.99 | ns    |
|                                                                                                                     |                                                  | XC5VLX85T  | 5.78        | 6.28 | 6.99 | ns    |
|                                                                                                                     |                                                  | XC5VLX110  | 5.84        | 6.35 | 7.06 | ns    |
|                                                                                                                     |                                                  | XC5VLX110T | 5.84        | 6.35 | 7.06 | ns    |
|                                                                                                                     |                                                  | XC5VLX155  | 6.16        | 6.68 | 7.52 | ns    |
|                                                                                                                     |                                                  | XC5VLX155T | 6.16        | 6.68 | 7.52 | ns    |
|                                                                                                                     |                                                  | XC5VLX220  | N/A         | 6.99 | 7.71 | ns    |
|                                                                                                                     |                                                  | XC5VLX220T | N/A         | 6.99 | 7.71 | ns    |
|                                                                                                                     |                                                  | XC5VLX330  | N/A         | 7.17 | 7.91 | ns    |
|                                                                                                                     |                                                  | XC5VLX330T | N/A         | 7.17 | 7.91 | ns    |
|                                                                                                                     |                                                  | XC5VSX35T  | 5.72        | 6.22 | 6.92 | ns    |
|                                                                                                                     |                                                  | XC5VSX50T  | 5.77        | 6.27 | 6.97 | ns    |
|                                                                                                                     |                                                  | XC5VSX95T  | N/A         | 6.59 | 7.30 | ns    |
|                                                                                                                     |                                                  | XC5VSX240T | N/A         | 7.24 | 7.98 | ns    |
|                                                                                                                     |                                                  | XC5VTX150T | N/A         | 6.58 | 7.30 | ns    |
|                                                                                                                     |                                                  | XC5VTX240T | N/A         | 6.88 | 7.61 | ns    |
|                                                                                                                     |                                                  | XC5VFX30T  | 5.73        | 6.21 | 6.89 | ns    |
|                                                                                                                     |                                                  | XC5VFX70T  | 5.82        | 6.33 | 7.04 | ns    |
|                                                                                                                     |                                                  | XC5VFX100T | 6.21        | 6.73 | 7.44 | ns    |
|                                                                                                                     |                                                  | XC5VFX130T | 6.28        | 6.80 | 7.52 | ns    |
|                                                                                                                     |                                                  | XC5VFX200T | N/A         | 7.17 | 7.91 | ns    |

### Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 85: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

| Symbol                                                                                                                               | Description                            | Device     | Speed Grade |      |      | Units |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                      |                                        |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode |                                        |            |             |      |      |       |
| T <sub>ICKOFDCM</sub>                                                                                                                | Global Clock and OUTFF <i>with</i> DCM | XC5VLX20T  | N/A         | 2.53 | 2.93 | ns    |
|                                                                                                                                      |                                        | XC5VLX30   | 2.33        | 2.56 | 2.93 | ns    |
|                                                                                                                                      |                                        | XC5VLX30T  | 2.33        | 2.56 | 2.93 | ns    |
|                                                                                                                                      |                                        | XC5VLX50   | 2.35        | 2.58 | 2.95 | ns    |
|                                                                                                                                      |                                        | XC5VLX50T  | 2.35        | 2.58 | 2.95 | ns    |
|                                                                                                                                      |                                        | XC5VLX85   | 2.41        | 2.63 | 3.00 | ns    |
|                                                                                                                                      |                                        | XC5VLX85T  | 2.41        | 2.63 | 3.00 | ns    |
|                                                                                                                                      |                                        | XC5VLX110  | 2.46        | 2.69 | 3.06 | ns    |
|                                                                                                                                      |                                        | XC5VLX110T | 2.46        | 2.69 | 3.06 | ns    |
|                                                                                                                                      |                                        | XC5VLX155  | 2.51        | 2.74 | 3.10 | ns    |
|                                                                                                                                      |                                        | XC5VLX155T | 2.51        | 2.74 | 3.10 | ns    |
|                                                                                                                                      |                                        | XC5VLX220  | N/A         | 2.83 | 3.18 | ns    |
|                                                                                                                                      |                                        | XC5VLX220T | N/A         | 2.83 | 3.18 | ns    |
|                                                                                                                                      |                                        | XC5VLX330  | N/A         | 3.00 | 3.37 | ns    |
|                                                                                                                                      |                                        | XC5VLX330T | N/A         | 3.00 | 3.37 | ns    |
|                                                                                                                                      |                                        | XC5VSX35T  | 2.44        | 2.67 | 3.03 | ns    |
|                                                                                                                                      |                                        | XC5VSX50T  | 2.46        | 2.69 | 3.05 | ns    |
|                                                                                                                                      |                                        | XC5VSX95T  | N/A         | 2.64 | 3.00 | ns    |
|                                                                                                                                      |                                        | XC5VSX240T | N/A         | 3.00 | 3.36 | ns    |
|                                                                                                                                      |                                        | XC5VTX150T | N/A         | 2.77 | 3.15 | ns    |
|                                                                                                                                      |                                        | XC5VTX240T | N/A         | 2.78 | 3.15 | ns    |
|                                                                                                                                      |                                        | XC5VFX30T  | 2.55        | 2.82 | 3.20 | ns    |
|                                                                                                                                      |                                        | XC5VFX70T  | 2.48        | 2.74 | 3.12 | ns    |
|                                                                                                                                      |                                        | XC5VFX100T | 2.33        | 2.59 | 3.00 | ns    |
|                                                                                                                                      |                                        | XC5VFX130T | 2.40        | 2.67 | 3.07 | ns    |
|                                                                                                                                      |                                        | XC5VFX200T | N/A         | 2.87 | 3.27 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 86: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

| Symbol                                                                                                                               | Description                            | Device     | Speed Grade |      |      | Units |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                      |                                        |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode |                                        |            |             |      |      |       |
| T <sub>ICKOFDCM_0</sub>                                                                                                              | Global Clock and OUTFF <i>with</i> DCM | XC5VLX20T  | N/A         | 3.74 | 4.20 | ns    |
|                                                                                                                                      |                                        | XC5VLX30   | 3.45        | 3.71 | 4.15 | ns    |
|                                                                                                                                      |                                        | XC5VLX30T  | 3.45        | 3.71 | 4.15 | ns    |
|                                                                                                                                      |                                        | XC5VLX50   | 3.47        | 3.73 | 4.17 | ns    |
|                                                                                                                                      |                                        | XC5VLX50T  | 3.47        | 3.73 | 4.17 | ns    |
|                                                                                                                                      |                                        | XC5VLX85   | 3.60        | 3.86 | 4.29 | ns    |
|                                                                                                                                      |                                        | XC5VLX85T  | 3.60        | 3.86 | 4.29 | ns    |
|                                                                                                                                      |                                        | XC5VLX110  | 3.65        | 3.92 | 4.36 | ns    |
|                                                                                                                                      |                                        | XC5VLX110T | 3.65        | 3.92 | 4.36 | ns    |
|                                                                                                                                      |                                        | XC5VLX155  | 3.91        | 4.18 | 4.62 | ns    |
|                                                                                                                                      |                                        | XC5VLX155T | 3.91        | 4.18 | 4.62 | ns    |
|                                                                                                                                      |                                        | XC5VLX220  | N/A         | 4.41 | 4.85 | ns    |
|                                                                                                                                      |                                        | XC5VLX220T | N/A         | 4.41 | 4.85 | ns    |
|                                                                                                                                      |                                        | XC5VLX330  | N/A         | 4.58 | 5.04 | ns    |
|                                                                                                                                      |                                        | XC5VLX330T | N/A         | 4.58 | 5.04 | ns    |
|                                                                                                                                      |                                        | XC5VSX35T  | 3.63        | 3.89 | 4.33 | ns    |
|                                                                                                                                      |                                        | XC5VSX50T  | 3.65        | 3.91 | 4.35 | ns    |
|                                                                                                                                      |                                        | XC5VSX95T  | N/A         | 4.16 | 4.59 | ns    |
|                                                                                                                                      |                                        | XC5VSX240T | N/A         | 4.65 | 5.11 | ns    |
|                                                                                                                                      |                                        | XC5VTX150T | N/A         | 4.07 | 4.51 | ns    |
|                                                                                                                                      |                                        | XC5VTX240T | N/A         | 4.30 | 4.74 | ns    |
|                                                                                                                                      |                                        | XC5VFX30T  | 3.74        | 4.05 | 4.50 | ns    |
|                                                                                                                                      |                                        | XC5VFX70T  | 3.67        | 3.96 | 4.41 | ns    |
|                                                                                                                                      |                                        | XC5VFX100T | 3.82        | 4.10 | 4.53 | ns    |
|                                                                                                                                      |                                        | XC5VFX130T | 3.99        | 4.29 | 4.74 | ns    |
|                                                                                                                                      |                                        | XC5VFX200T | N/A         | 4.60 | 5.03 | ns    |

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 87: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

| Symbol                                                                                                                               | Description                            | Device     | Speed Grade |      |      | Units |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                      |                                        |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode |                                        |            |             |      |      |       |
| T <sub>ICKOFFPLL</sub>                                                                                                               | Global Clock and OUTFF <i>with</i> PLL | XC5VLX20T  | N/A         | 2.36 | 2.73 | ns    |
|                                                                                                                                      |                                        | XC5VLX30   | 2.03        | 2.30 | 2.70 | ns    |
|                                                                                                                                      |                                        | XC5VLX30T  | 2.03        | 2.30 | 2.70 | ns    |
|                                                                                                                                      |                                        | XC5VLX50   | 2.20        | 2.47 | 2.86 | ns    |
|                                                                                                                                      |                                        | XC5VLX50T  | 2.20        | 2.47 | 2.86 | ns    |
|                                                                                                                                      |                                        | XC5VLX85   | 2.21        | 2.49 | 2.88 | ns    |
|                                                                                                                                      |                                        | XC5VLX85T  | 2.21        | 2.49 | 2.88 | ns    |
|                                                                                                                                      |                                        | XC5VLX110  | 2.25        | 2.53 | 2.92 | ns    |
|                                                                                                                                      |                                        | XC5VLX110T | 2.25        | 2.53 | 2.92 | ns    |
|                                                                                                                                      |                                        | XC5VLX155  | 2.34        | 2.60 | 3.01 | ns    |
|                                                                                                                                      |                                        | XC5VLX155T | 2.34        | 2.60 | 3.01 | ns    |
|                                                                                                                                      |                                        | XC5VLX220  | N/A         | 2.74 | 3.12 | ns    |
|                                                                                                                                      |                                        | XC5VLX220T | N/A         | 2.74 | 3.12 | ns    |
|                                                                                                                                      |                                        | XC5VLX330  | N/A         | 2.89 | 3.27 | ns    |
|                                                                                                                                      |                                        | XC5VLX330T | N/A         | 2.89 | 3.27 | ns    |
|                                                                                                                                      |                                        | XC5VSX35T  | 2.02        | 2.28 | 2.62 | ns    |
|                                                                                                                                      |                                        | XC5VSX50T  | 2.12        | 2.36 | 2.76 | ns    |
|                                                                                                                                      |                                        | XC5VSX95T  | N/A         | 2.29 | 2.69 | ns    |
|                                                                                                                                      |                                        | XC5VSX240T | N/A         | 2.96 | 3.34 | ns    |
|                                                                                                                                      |                                        | XC5VTX150T | N/A         | 2.54 | 2.92 | ns    |
|                                                                                                                                      |                                        | XC5VTX240T | N/A         | 2.67 | 3.04 | ns    |
|                                                                                                                                      |                                        | XC5VFX30T  | 2.44        | 2.67 | 3.06 | ns    |
|                                                                                                                                      |                                        | XC5VFX70T  | 2.48        | 2.71 | 3.10 | ns    |
|                                                                                                                                      |                                        | XC5VFX100T | 2.41        | 2.70 | 3.10 | ns    |
|                                                                                                                                      |                                        | XC5VFX130T | 2.48        | 2.75 | 3.17 | ns    |
|                                                                                                                                      |                                        | XC5VFX200T | N/A         | 2.96 | 3.35 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 88: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode

| Symbol                                                                                                                               | Description                            | Device     | Speed Grade |      |      | Units |
|--------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                      |                                        |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode |                                        |            |             |      |      |       |
| T <sub>ICKOFFLL_0</sub>                                                                                                              | Global Clock and OUTFF <i>with</i> PLL | XC5VLX20T  | N/A         | 4.31 | 4.88 | ns    |
|                                                                                                                                      |                                        | XC5VLX30   | 3.96        | 4.32 | 4.82 | ns    |
|                                                                                                                                      |                                        | XC5VLX30T  | 3.96        | 4.32 | 4.82 | ns    |
|                                                                                                                                      |                                        | XC5VLX50   | 4.05        | 4.40 | 4.91 | ns    |
|                                                                                                                                      |                                        | XC5VLX50T  | 4.05        | 4.40 | 4.91 | ns    |
|                                                                                                                                      |                                        | XC5VLX85   | 4.07        | 4.40 | 4.88 | ns    |
|                                                                                                                                      |                                        | XC5VLX85T  | 4.07        | 4.40 | 4.88 | ns    |
|                                                                                                                                      |                                        | XC5VLX110  | 4.11        | 4.44 | 4.92 | ns    |
|                                                                                                                                      |                                        | XC5VLX110T | 4.11        | 4.44 | 4.92 | ns    |
|                                                                                                                                      |                                        | XC5VLX155  | 4.31        | 4.66 | 5.16 | ns    |
|                                                                                                                                      |                                        | XC5VLX155T | 4.31        | 4.66 | 5.16 | ns    |
|                                                                                                                                      |                                        | XC5VLX220  | N/A         | 4.85 | 5.29 | ns    |
|                                                                                                                                      |                                        | XC5VLX220T | N/A         | 4.85 | 5.29 | ns    |
|                                                                                                                                      |                                        | XC5VLX330  | N/A         | 5.00 | 5.44 | ns    |
|                                                                                                                                      |                                        | XC5VLX330T | N/A         | 5.00 | 5.44 | ns    |
|                                                                                                                                      |                                        | XC5VSX35T  | 4.19        | 4.54 | 5.03 | ns    |
|                                                                                                                                      |                                        | XC5VSX50T  | 4.20        | 4.54 | 5.02 | ns    |
|                                                                                                                                      |                                        | XC5VSX95T  | N/A         | 4.68 | 5.14 | ns    |
|                                                                                                                                      |                                        | XC5VSX240T | N/A         | 5.07 | 5.51 | ns    |
|                                                                                                                                      |                                        | XC5VTX150T | N/A         | 4.51 | 4.95 | ns    |
|                                                                                                                                      |                                        | XC5VTX240T | N/A         | 4.71 | 5.14 | ns    |
|                                                                                                                                      |                                        | XC5VFX30T  | 4.23        | 4.56 | 5.04 | ns    |
|                                                                                                                                      |                                        | XC5VFX70T  | 4.22        | 4.54 | 5.02 | ns    |
|                                                                                                                                      |                                        | XC5VFX100T | 4.35        | 4.70 | 5.19 | ns    |
|                                                                                                                                      |                                        | XC5VFX130T | 4.49        | 4.86 | 5.40 | ns    |
|                                                                                                                                      |                                        | XC5VFX200T | N/A         | 5.04 | 5.55 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 89: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

| Symbol                                                                                                                                       | Description                             | Device     | Speed Grade |      |      | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                              |                                         |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM and PLL in System-Synchronous Mode |                                         |            |             |      |      |       |
| T <sub>ICKOFDCM_PLL</sub>                                                                                                                    | Global Clock and OUTFF with DCM and PLL | XC5VLX20T  | N/A         | 2.45 | 2.84 | ns    |
|                                                                                                                                              |                                         | XC5VLX30   | 2.25        | 2.48 | 2.84 | ns    |
|                                                                                                                                              |                                         | XC5VLX30T  | 2.25        | 2.48 | 2.84 | ns    |
|                                                                                                                                              |                                         | XC5VLX50   | 2.27        | 2.50 | 2.86 | ns    |
|                                                                                                                                              |                                         | XC5VLX50T  | 2.27        | 2.50 | 2.86 | ns    |
|                                                                                                                                              |                                         | XC5VLX85   | 2.33        | 2.55 | 2.91 | ns    |
|                                                                                                                                              |                                         | XC5VLX85T  | 2.33        | 2.55 | 2.91 | ns    |
|                                                                                                                                              |                                         | XC5VLX110  | 2.38        | 2.61 | 2.97 | ns    |
|                                                                                                                                              |                                         | XC5VLX110T | 2.38        | 2.61 | 2.97 | ns    |
|                                                                                                                                              |                                         | XC5VLX155  | 2.43        | 2.66 | 3.01 | ns    |
|                                                                                                                                              |                                         | XC5VLX155T | 2.43        | 2.66 | 3.01 | ns    |
|                                                                                                                                              |                                         | XC5VLX220  | N/A         | 2.75 | 3.09 | ns    |
|                                                                                                                                              |                                         | XC5VLX220T | N/A         | 2.75 | 3.09 | ns    |
|                                                                                                                                              |                                         | XC5VLX330  | N/A         | 2.92 | 3.28 | ns    |
|                                                                                                                                              |                                         | XC5VLX330T | N/A         | 2.92 | 3.28 | ns    |
|                                                                                                                                              |                                         | XC5VSX35T  | 2.36        | 2.59 | 2.94 | ns    |
|                                                                                                                                              |                                         | XC5VSX50T  | 2.38        | 2.61 | 2.96 | ns    |
|                                                                                                                                              |                                         | XC5VSX95T  | N/A         | 2.56 | 2.91 | ns    |
|                                                                                                                                              |                                         | XC5VSX240T | N/A         | 2.92 | 3.27 | ns    |
|                                                                                                                                              |                                         | XC5VTX150T | N/A         | 2.69 | 3.06 | ns    |
|                                                                                                                                              |                                         | XC5VTX240T | N/A         | 2.70 | 3.06 | ns    |
|                                                                                                                                              |                                         | XC5VFX30T  | 2.47        | 2.74 | 3.11 | ns    |
|                                                                                                                                              |                                         | XC5VFX70T  | 2.40        | 2.66 | 3.03 | ns    |
|                                                                                                                                              |                                         | XC5VFX100T | 2.25        | 2.51 | 2.91 | ns    |
|                                                                                                                                              |                                         | XC5VFX130T | 2.32        | 2.59 | 2.98 | ns    |
|                                                                                                                                              |                                         | XC5VFX200T | N/A         | 2.79 | 3.18 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 90: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

| Symbol                                                                                                                                       | Description                             | Device     | Speed Grade |      |      | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|------------|-------------|------|------|-------|
|                                                                                                                                              |                                         |            | -3          | -2   | -1   |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM and PLL in Source-Synchronous Mode |                                         |            |             |      |      |       |
| T <sub>ICKOFDCM0_PLL</sub>                                                                                                                   | Global Clock and OUTFF with DCM and PLL | XC5VLX20T  | N/A         | 3.66 | 4.11 | ns    |
|                                                                                                                                              |                                         | XC5VLX30   | 3.37        | 3.63 | 4.06 | ns    |
|                                                                                                                                              |                                         | XC5VLX30T  | 3.37        | 3.63 | 4.06 | ns    |
|                                                                                                                                              |                                         | XC5VLX50   | 3.39        | 3.65 | 4.08 | ns    |
|                                                                                                                                              |                                         | XC5VLX50T  | 3.39        | 3.65 | 4.08 | ns    |
|                                                                                                                                              |                                         | XC5VLX85   | 3.52        | 3.78 | 4.20 | ns    |
|                                                                                                                                              |                                         | XC5VLX85T  | 3.52        | 3.78 | 4.20 | ns    |
|                                                                                                                                              |                                         | XC5VLX110  | 3.57        | 3.84 | 4.27 | ns    |
|                                                                                                                                              |                                         | XC5VLX110T | 3.57        | 3.84 | 4.27 | ns    |
|                                                                                                                                              |                                         | XC5VLX155  | 3.83        | 4.10 | 4.53 | ns    |
|                                                                                                                                              |                                         | XC5VLX155T | 3.83        | 4.10 | 4.53 | ns    |
|                                                                                                                                              |                                         | XC5VLX220  | N/A         | 4.33 | 4.76 | ns    |
|                                                                                                                                              |                                         | XC5VLX220T | N/A         | 4.33 | 4.76 | ns    |
|                                                                                                                                              |                                         | XC5VLX330  | N/A         | 4.50 | 4.95 | ns    |
|                                                                                                                                              |                                         | XC5VLX330T | N/A         | 4.50 | 4.95 | ns    |
|                                                                                                                                              |                                         | XC5VSX35T  | 3.55        | 3.81 | 4.24 | ns    |
|                                                                                                                                              |                                         | XC5VSX50T  | 3.57        | 3.83 | 4.26 | ns    |
|                                                                                                                                              |                                         | XC5VSX95T  | N/A         | 4.08 | 4.50 | ns    |
|                                                                                                                                              |                                         | XC5VSX240T | N/A         | 4.57 | 5.02 | ns    |
|                                                                                                                                              |                                         | XC5VTX150T | N/A         | 3.99 | 4.42 | ns    |
|                                                                                                                                              |                                         | XC5VTX240T | N/A         | 4.22 | 4.65 | ns    |
|                                                                                                                                              |                                         | XC5VFX30T  | 3.66        | 3.97 | 4.41 | ns    |
|                                                                                                                                              |                                         | XC5VFX70T  | 3.59        | 3.88 | 4.32 | ns    |
|                                                                                                                                              |                                         | XC5VFX100T | 3.74        | 4.02 | 4.44 | ns    |
|                                                                                                                                              |                                         | XC5VFX130T | 3.91        | 4.21 | 4.65 | ns    |
|                                                                                                                                              |                                         | XC5VFX200T | N/A         | 4.52 | 4.94 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

## Virtex-5 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 91. Values are expressed in nanoseconds unless otherwise noted.

Table 91: Global Clock Setup and Hold Without DCM or PLL

| Symbol                                                                                                | Description                                                                                          | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                                                                       |                                                                                                      |            | -3            | -2            | -1            |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                                      |            |               |               |               |       |
| T <sub>PSFD</sub> / T <sub>PHFD</sub>                                                                 | Full Delay (Legacy Delay or Default Delay)<br>Global Clock and IFF <sup>(2)</sup> without DCM or PLL | XC5VLX20T  | N/A           | 1.63<br>−0.41 | 1.86<br>−0.41 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX30   | 1.49<br>−0.35 | 1.60<br>−0.35 | 1.77<br>−0.35 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX30T  | 1.49<br>−0.35 | 1.60<br>−0.35 | 1.76<br>−0.35 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX50   | 1.48<br>−0.30 | 1.59<br>−0.30 | 1.76<br>−0.30 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX50T  | 1.48<br>−0.30 | 1.59<br>−0.30 | 1.76<br>−0.30 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX85   | 1.75<br>−0.49 | 1.89<br>−0.49 | 2.09<br>−0.49 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX85T  | 1.75<br>−0.49 | 1.89<br>−0.49 | 2.09<br>−0.49 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX110  | 1.74<br>−0.43 | 1.88<br>−0.43 | 2.09<br>−0.43 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX110T | 1.73<br>−0.43 | 1.88<br>−0.43 | 2.09<br>−0.43 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX155  | 2.06<br>−0.50 | 2.36<br>−0.50 | 2.78<br>−0.49 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX155T | 2.06<br>−0.50 | 2.36<br>−0.50 | 2.78<br>−0.49 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX220  | N/A           | 2.57<br>−0.74 | 2.86<br>−0.74 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX220T | N/A           | 2.57<br>−0.74 | 2.86<br>−0.74 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX330  | N/A           | 2.55<br>−0.56 | 2.85<br>−0.56 | ns    |
|                                                                                                       |                                                                                                      | XC5VLX330T | N/A           | 2.57<br>−0.56 | 2.86<br>−0.56 | ns    |
|                                                                                                       |                                                                                                      | XC5VSX35T  | 1.47<br>−0.16 | 1.59<br>−0.16 | 1.76<br>−0.16 | ns    |
|                                                                                                       |                                                                                                      | XC5VSX50T  | 1.62<br>−0.31 | 1.74<br>−0.31 | 1.93<br>−0.31 | ns    |
|                                                                                                       |                                                                                                      | XC5VSX95T  | N/A           | 2.10<br>−0.44 | 2.32<br>−0.44 | ns    |
|                                                                                                       |                                                                                                      | XC5VSX240T | N/A           | 2.01<br>0.18  | 2.28<br>0.18  | ns    |

Table 91: Global Clock Setup and Hold Without DCM or PLL (Cont'd)

| Symbol                                | Description                                                                                          | Device     | Speed Grade   |               |               | Units |
|---------------------------------------|------------------------------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                       |                                                                                                      |            | -3            | -2            | -1            |       |
| T <sub>PSFD</sub> / T <sub>PHFD</sub> | Full Delay (Legacy Delay or Default Delay)<br>Global Clock and IFF <sup>(2)</sup> without DCM or PLL | XC5VTX150T | N/A           | 2.35<br>-0.82 | 2.59<br>-0.82 | ns    |
|                                       |                                                                                                      | XC5VTX240T | N/A           | 2.59<br>-0.85 | 2.87<br>-0.85 | ns    |
|                                       |                                                                                                      | XC5VFX30T  | 2.05<br>-0.27 | 2.25<br>-0.27 | 2.57<br>-0.27 | ns    |
|                                       |                                                                                                      | XC5VFX70T  | 1.85<br>-0.30 | 2.06<br>-0.30 | 2.35<br>-0.30 | ns    |
|                                       |                                                                                                      | XC5VFX100T | 2.20<br>-0.42 | 2.38<br>-0.42 | 2.66<br>-0.42 | ns    |
|                                       |                                                                                                      | XC5VFX130T | 2.33<br>-0.55 | 2.59<br>-0.54 | 2.95<br>-0.54 | ns    |
|                                       |                                                                                                      | XC5VFX200T | N/A           | 2.52<br>-0.43 | 2.81<br>-0.43 | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 92: Global Clock Setup and Hold With DCM in System-Synchronous Mode

| Symbol                                                                                                | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                                                                       |                                                                                  |            | -3            | -2            | -1            |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                  |            |               |               |               |       |
| T <sub>PSDCM</sub> / T <sub>PHDCM</sub>                                                               | No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode | XC5VLX20T  | N/A           | 1.47<br>–0.56 | 1.59<br>–0.56 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30   | 1.53<br>–0.50 | 1.70<br>–0.50 | 1.88<br>–0.50 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30T  | 1.53<br>–0.50 | 1.70<br>–0.50 | 1.88<br>–0.50 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50   | 1.52<br>–0.48 | 1.68<br>–0.48 | 1.86<br>–0.48 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50T  | 1.52<br>–0.48 | 1.68<br>–0.48 | 1.86<br>–0.48 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85   | 1.58<br>–0.43 | 1.76<br>–0.43 | 1.95<br>–0.43 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85T  | 1.57<br>–0.43 | 1.76<br>–0.43 | 1.95<br>–0.43 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110  | 1.58<br>–0.37 | 1.76<br>–0.37 | 1.95<br>–0.37 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110T | 1.58<br>–0.37 | 1.76<br>–0.37 | 1.95<br>–0.37 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155  | 2.02<br>–0.32 | 2.16<br>–0.32 | 2.38<br>–0.32 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155T | 2.02<br>–0.32 | 2.16<br>–0.32 | 2.38<br>–0.32 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220  | N/A           | 2.17<br>–0.27 | 2.44<br>–0.27 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220T | N/A           | 2.17<br>–0.27 | 2.44<br>–0.27 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330  | N/A           | 2.17<br>–0.10 | 2.44<br>–0.10 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330T | N/A           | 2.17<br>–0.10 | 2.44<br>–0.10 | ns    |
|                                                                                                       |                                                                                  | XC5VSX35T  | 1.60<br>–0.39 | 1.78<br>–0.39 | 1.98<br>–0.39 | ns    |
|                                                                                                       |                                                                                  | XC5VSX50T  | 1.58<br>–0.37 | 1.76<br>–0.37 | 1.95<br>–0.37 | ns    |
|                                                                                                       |                                                                                  | XC5VSX95T  | N/A           | 2.34<br>–0.41 | 2.35<br>–0.41 | ns    |
|                                                                                                       |                                                                                  | XC5VSX240T | N/A           | 2.25<br>–0.10 | 2.54<br>–0.10 | ns    |

Table 92: Global Clock Setup and Hold With DCM in System-Synchronous Mode (Cont'd)

| Symbol                                  | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-----------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                         |                                                                                  |            | -3            | -2            | -1            |       |
| T <sub>PSDCM</sub> / T <sub>PHDCM</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode | XC5VTX150T | N/A           | 1.85<br>–0.33 | 2.05<br>–0.33 | ns    |
|                                         |                                                                                  | XC5VTX240T | N/A           | 2.11<br>–0.32 | 2.35<br>–0.32 | ns    |
|                                         |                                                                                  | XC5VFX30T  | 1.80<br>–0.28 | 1.89<br>–0.28 | 2.02<br>–0.28 | ns    |
|                                         |                                                                                  | XC5VFX70T  | 1.76<br>–0.36 | 1.86<br>–0.36 | 1.98<br>–0.36 | ns    |
|                                         |                                                                                  | XC5VFX100T | 2.27<br>–0.51 | 2.35<br>–0.51 | 2.49<br>–0.49 | ns    |
|                                         |                                                                                  | XC5VFX130T | 2.33<br>–0.43 | 2.48<br>–0.43 | 2.72<br>–0.42 | ns    |
|                                         |                                                                                  | XC5VFX200T | N/A           | 2.30<br>–0.23 | 2.43<br>–0.21 | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 93: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

| Symbol                                                                                                | Description                                                                      | Device     | Speed Grade  |              |              | Units |
|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------|--------------|--------------|--------------|-------|
|                                                                                                       |                                                                                  |            | -3           | -2           | -1           |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                  |            |              |              |              |       |
| T <sub>PSDCM0</sub> / T <sub>PHDCM0</sub>                                                             | No Delay Global Clock and IFF <sup>(2)</sup> with DCM in Source-Synchronous Mode | XC5VLX20T  | N/A          | 0.12<br>0.64 | 0.14<br>0.72 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30   | 0.27<br>0.62 | 0.27<br>0.62 | 0.27<br>0.66 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30T  | 0.27<br>0.62 | 0.27<br>0.62 | 0.27<br>0.66 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50   | 0.26<br>0.64 | 0.26<br>0.64 | 0.26<br>0.68 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50T  | 0.25<br>0.64 | 0.26<br>0.64 | 0.26<br>0.68 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85   | 0.23<br>0.76 | 0.24<br>0.76 | 0.24<br>0.80 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85T  | 0.23<br>0.76 | 0.24<br>0.76 | 0.24<br>0.80 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110  | 0.23<br>0.82 | 0.24<br>0.82 | 0.24<br>0.87 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110T | 0.23<br>0.82 | 0.24<br>0.82 | 0.24<br>0.87 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155  | 0.12<br>1.08 | 0.14<br>1.08 | 0.16<br>1.13 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155T | 0.12<br>1.08 | 0.14<br>1.08 | 0.16<br>1.13 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220  | N/A          | 0.21<br>1.31 | 0.22<br>1.36 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220T | N/A          | 0.21<br>1.31 | 0.22<br>1.36 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330  | N/A          | 0.21<br>1.48 | 0.22<br>1.55 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330T | N/A          | 0.21<br>1.48 | 0.22<br>1.55 | ns    |
|                                                                                                       |                                                                                  | XC5VSX35T  | 0.25<br>0.80 | 0.27<br>0.80 | 0.27<br>0.84 | ns    |
|                                                                                                       |                                                                                  | XC5VSX50T  | 0.24<br>0.82 | 0.25<br>0.82 | 0.25<br>0.86 | ns    |
|                                                                                                       |                                                                                  | XC5VSX95T  | N/A          | 0.24<br>1.06 | 0.24<br>1.11 | ns    |
|                                                                                                       |                                                                                  | XC5VSX240T | N/A          | 0.20<br>1.55 | 0.21<br>1.62 | ns    |

Table 93: Global Clock Setup and Hold With DCM in Source-Synchronous Mode (Cont'd)

| Symbol                                    | Description                                                                      | Device     | Speed Grade  |              |              | Units |
|-------------------------------------------|----------------------------------------------------------------------------------|------------|--------------|--------------|--------------|-------|
|                                           |                                                                                  |            | -3           | -2           | -1           |       |
| T <sub>PSDCM0</sub> / T <sub>PHDCM0</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with DCM in Source-Synchronous Mode | XC5VTX150T | N/A          | 0.25<br>0.97 | 0.25<br>1.03 | ns    |
|                                           |                                                                                  | XC5VTX240T | N/A          | 0.24<br>1.20 | 0.24<br>1.26 | ns    |
|                                           |                                                                                  | XC5VFX30T  | 0.16<br>0.91 | 0.18<br>0.95 | 0.19<br>1.01 | ns    |
|                                           |                                                                                  | XC5VFX70T  | 0.13<br>0.83 | 0.14<br>0.86 | 0.14<br>0.92 | ns    |
|                                           |                                                                                  | XC5VFX100T | 0.21<br>0.98 | 0.21<br>1.00 | 0.21<br>1.05 | ns    |
|                                           |                                                                                  | XC5VFX130T | 0.19<br>1.15 | 0.21<br>1.19 | 0.24<br>1.25 | ns    |
|                                           |                                                                                  | XC5VFX200T | N/A          | 0.14<br>1.50 | 0.16<br>1.55 | ns    |

**Notes:**

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 94: Global Clock Setup and Hold With PLL in System-Synchronous Mode

| Symbol                                                                                                | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                                                                       |                                                                                  |            | -3            | -2            | -1            |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                  |            |               |               |               |       |
| T <sub>PSPLL</sub> / T <sub>PHPLL</sub>                                                               | No Delay Global Clock and IFF <sup>(2)</sup> with PLL in System-Synchronous Mode | XC5VLX20T  | N/A           | 1.74<br>–0.82 | 2.02<br>–0.82 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30   | 1.53<br>–0.80 | 1.68<br>–0.80 | 1.90<br>–0.79 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30T  | 1.52<br>–0.80 | 1.68<br>–0.80 | 1.90<br>–0.79 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50   | 1.50<br>–0.64 | 1.65<br>–0.63 | 1.89<br>–0.62 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50T  | 1.50<br>–0.64 | 1.65<br>–0.63 | 1.89<br>–0.62 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85   | 1.83<br>–0.63 | 1.95<br>–0.62 | 2.09<br>–0.61 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85T  | 1.83<br>–0.63 | 1.95<br>–0.62 | 2.09<br>–0.61 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110  | 1.83<br>–0.58 | 1.96<br>–0.57 | 2.10<br>–0.57 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110T | 1.83<br>–0.58 | 1.96<br>–0.57 | 2.10<br>–0.57 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155  | 1.91<br>–0.49 | 2.09<br>–0.49 | 2.37<br>–0.47 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155T | 1.91<br>–0.49 | 2.09<br>–0.49 | 2.37<br>–0.47 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220  | N/A           | 1.93<br>–0.36 | 2.09<br>–0.36 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220T | N/A           | 1.93<br>–0.36 | 2.09<br>–0.36 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330  | N/A           | 2.09<br>–0.21 | 2.33<br>–0.21 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330T | N/A           | 2.12<br>–0.21 | 2.34<br>–0.21 | ns    |
|                                                                                                       |                                                                                  | XC5VSX35T  | 1.82<br>–0.82 | 2.02<br>–0.82 | 2.33<br>–0.82 | ns    |
|                                                                                                       |                                                                                  | XC5VSX50T  | 1.96<br>–0.72 | 2.07<br>–0.72 | 2.20<br>–0.72 | ns    |
|                                                                                                       |                                                                                  | XC5VSX95T  | N/A           | 2.17<br>–0.80 | 2.35<br>–0.79 | ns    |
|                                                                                                       |                                                                                  | XC5VSX240T | N/A           | 2.11<br>–0.14 | 2.33<br>–0.14 | ns    |

Table 94: Global Clock Setup and Hold With PLL in System-Synchronous Mode (Cont'd)

| Symbol                                  | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-----------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                         |                                                                                  |            | -3            | -2            | -1            |       |
| T <sub>PSPLL</sub> / T <sub>PHPLL</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with PLL in System-Synchronous Mode | XC5VTX150T | N/A           | 1.82<br>–0.56 | 1.95<br>–0.56 | ns    |
|                                         |                                                                                  | XC5VTX240T | N/A           | 2.05<br>–0.43 | 2.26<br>–0.43 | ns    |
|                                         |                                                                                  | XC5VFX30T  | 1.82<br>–0.40 | 1.93<br>–0.40 | 2.09<br>–0.40 | ns    |
|                                         |                                                                                  | XC5VFX70T  | 1.79<br>–0.30 | 1.90<br>–0.30 | 2.07<br>–0.30 | ns    |
|                                         |                                                                                  | XC5VFX100T | 1.81<br>–0.43 | 1.91<br>–0.40 | 2.09<br>–0.38 | ns    |
|                                         |                                                                                  | XC5VFX130T | 1.79<br>–0.29 | 1.95<br>–0.28 | 2.14<br>–0.24 | ns    |
|                                         |                                                                                  | XC5VFX200T | N/A           | 2.06<br>–0.14 | 2.29<br>–0.14 | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 95: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

| Symbol                                                                                                | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                                                                       |                                                                                  |            | -3            | -2            | -1            |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                  |            |               |               |               |       |
| T <sub>PSPLL0</sub> / T <sub>PHPLL0</sub>                                                             | No Delay Global Clock and IFF <sup>(2)</sup> with PLL in Source-Synchronous Mode | XC5VLX20T  | N/A           | −0.26<br>1.21 | −0.25<br>1.40 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30   | −0.33<br>1.13 | −0.33<br>1.22 | −0.33<br>1.34 | ns    |
|                                                                                                       |                                                                                  | XC5VLX30T  | −0.33<br>1.13 | −0.33<br>1.22 | −0.33<br>1.34 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50   | −0.24<br>1.21 | −0.24<br>1.30 | −0.23<br>1.42 | ns    |
|                                                                                                       |                                                                                  | XC5VLX50T  | −0.24<br>1.21 | −0.24<br>1.30 | −0.23<br>1.42 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85   | −0.25<br>1.23 | −0.23<br>1.30 | −0.22<br>1.39 | ns    |
|                                                                                                       |                                                                                  | XC5VLX85T  | −0.25<br>1.23 | −0.23<br>1.30 | −0.22<br>1.39 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110  | −0.26<br>1.27 | −0.24<br>1.34 | −0.23<br>1.43 | ns    |
|                                                                                                       |                                                                                  | XC5VLX110T | −0.26<br>1.27 | −0.25<br>1.34 | −0.23<br>1.43 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155  | −0.15<br>1.48 | −0.12<br>1.56 | −0.10<br>1.67 | ns    |
|                                                                                                       |                                                                                  | XC5VLX155T | −0.16<br>1.48 | −0.12<br>1.56 | −0.10<br>1.67 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220  | N/A           | −0.34<br>1.75 | −0.30<br>1.80 | ns    |
|                                                                                                       |                                                                                  | XC5VLX220T | N/A           | −0.34<br>1.75 | −0.31<br>1.80 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330  | N/A           | −0.34<br>1.90 | −0.30<br>1.95 | ns    |
|                                                                                                       |                                                                                  | XC5VLX330T | N/A           | −0.34<br>1.90 | −0.30<br>1.95 | ns    |
|                                                                                                       |                                                                                  | XC5VSX35T  | −0.19<br>1.36 | −0.18<br>1.44 | −0.16<br>1.54 | ns    |
|                                                                                                       |                                                                                  | XC5VSX50T  | −0.27<br>1.37 | −0.26<br>1.44 | −0.25<br>1.53 | ns    |
|                                                                                                       |                                                                                  | XC5VSX95T  | N/A           | −0.26<br>1.58 | −0.24<br>1.65 | ns    |
|                                                                                                       |                                                                                  | XC5VSX240T | N/A           | −0.35<br>1.97 | −0.31<br>2.02 | ns    |

Table 95: Global Clock Setup and Hold With PLL in Source-Synchronous Mode (Cont'd)

| Symbol                                    | Description                                                                      | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------|----------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                           |                                                                                  |            | -3            | -2            | -1            |       |
| T <sub>PSPLL0</sub> / T <sub>PHPLL0</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with PLL in Source-Synchronous Mode | XC5VTX150T | N/A           | −0.31<br>1.41 | −0.29<br>1.47 | ns    |
|                                           |                                                                                  | XC5VTX240T | N/A           | −0.31<br>1.61 | −0.29<br>1.66 | ns    |
|                                           |                                                                                  | XC5VFX30T  | −0.10<br>1.40 | −0.09<br>1.46 | −0.08<br>1.55 | ns    |
|                                           |                                                                                  | XC5VFX70T  | −0.12<br>1.38 | −0.10<br>1.44 | −0.09<br>1.53 | ns    |
|                                           |                                                                                  | XC5VFX100T | −0.18<br>1.51 | −0.18<br>1.60 | −0.18<br>1.71 | ns    |
|                                           |                                                                                  | XC5VFX130T | −0.12<br>1.66 | −0.11<br>1.76 | −0.09<br>1.92 | ns    |
|                                           |                                                                                  | XC5VFX200T | N/A           | −0.12<br>1.94 | −0.10<br>2.06 | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 96: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

| Symbol                                                                                                | Description                                                                              | Device     | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                                                                       |                                                                                          |            | -3            | -2            | -1            |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                          |            |               |               |               |       |
| T <sub>PSDCMPLL</sub> /<br>T <sub>PHDCMPLL</sub>                                                      | No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in System-Synchronous Mode | XC5VLX20T  | N/A           | 1.67<br>–0.64 | 1.78<br>–0.64 | ns    |
|                                                                                                       |                                                                                          | XC5VLX30   | 1.72<br>–0.58 | 1.89<br>–0.58 | 2.07<br>–0.58 | ns    |
|                                                                                                       |                                                                                          | XC5VLX30T  | 1.72<br>–0.58 | 1.89<br>–0.58 | 2.06<br>–0.58 | ns    |
|                                                                                                       |                                                                                          | XC5VLX50   | 1.69<br>–0.56 | 1.86<br>–0.56 | 2.04<br>–0.56 | ns    |
|                                                                                                       |                                                                                          | XC5VLX50T  | 1.69<br>–0.56 | 1.86<br>–0.56 | 2.04<br>–0.56 | ns    |
|                                                                                                       |                                                                                          | XC5VLX85   | 1.74<br>–0.51 | 1.93<br>–0.51 | 2.13<br>–0.51 | ns    |
|                                                                                                       |                                                                                          | XC5VLX85T  | 1.74<br>–0.51 | 1.93<br>–0.51 | 2.13<br>–0.51 | ns    |
|                                                                                                       |                                                                                          | XC5VLX110  | 1.73<br>–0.45 | 1.93<br>–0.45 | 2.13<br>–0.45 | ns    |
|                                                                                                       |                                                                                          | XC5VLX110T | 1.73<br>–0.45 | 1.93<br>–0.45 | 2.13<br>–0.45 | ns    |
|                                                                                                       |                                                                                          | XC5VLX155  | 2.14<br>–0.40 | 2.31<br>–0.40 | 2.55<br>–0.40 | ns    |
|                                                                                                       |                                                                                          | XC5VLX155T | 2.14<br>–0.40 | 2.31<br>–0.40 | 2.55<br>–0.40 | ns    |
|                                                                                                       |                                                                                          | XC5VLX220  | N/A           | 2.32<br>–0.35 | 2.61<br>–0.35 | ns    |
|                                                                                                       |                                                                                          | XC5VLX220T | N/A           | 2.32<br>–0.35 | 2.61<br>–0.35 | ns    |
|                                                                                                       |                                                                                          | XC5VLX330  | N/A           | 2.29<br>–0.18 | 2.60<br>–0.18 | ns    |
|                                                                                                       |                                                                                          | XC5VLX330T | N/A           | 2.32<br>–0.18 | 2.61<br>–0.18 | ns    |
|                                                                                                       |                                                                                          | XC5VSX35T  | 1.78<br>–0.47 | 1.97<br>–0.47 | 2.16<br>–0.47 | ns    |
|                                                                                                       |                                                                                          | XC5VSX50T  | 1.76<br>–0.45 | 1.94<br>–0.45 | 2.14<br>–0.45 | ns    |
|                                                                                                       |                                                                                          | XC5VSX95T  | N/A           | 2.51<br>–0.49 | 2.53<br>–0.49 | ns    |
|                                                                                                       |                                                                                          | XC5VSX240T | N/A           | 2.39<br>–0.18 | 2.70<br>–0.18 | ns    |

Table 96: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode (Cont'd)

| Symbol                                           | Description                                                                              | Device     | Speed Grade   |               |               | Units |
|--------------------------------------------------|------------------------------------------------------------------------------------------|------------|---------------|---------------|---------------|-------|
|                                                  |                                                                                          |            | -3            | -2            | -1            |       |
| T <sub>PSDCMPLL</sub> /<br>T <sub>PHDCMPLL</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in System-Synchronous Mode | XC5VTX150T | N/A           | 2.00<br>–0.41 | 2.22<br>–0.41 | ns    |
|                                                  |                                                                                          | XC5VTX240T | N/A           | 2.25<br>–0.40 | 2.51<br>–0.40 | ns    |
|                                                  |                                                                                          | XC5VFX30T  | 1.97<br>–0.36 | 2.08<br>–0.36 | 2.21<br>–0.36 | ns    |
|                                                  |                                                                                          | XC5VFX70T  | 1.92<br>–0.44 | 2.03<br>–0.44 | 2.16<br>–0.44 | ns    |
|                                                  |                                                                                          | XC5VFX100T | 2.40<br>–0.59 | 2.51<br>–0.59 | 2.66<br>–0.58 | ns    |
|                                                  |                                                                                          | XC5VFX130T | 2.46<br>–0.51 | 2.64<br>–0.51 | 2.89<br>–0.51 | ns    |
|                                                  |                                                                                          | XC5VFX200T | N/A           | 2.44<br>–0.31 | 2.59<br>–0.30 | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 97: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

| Symbol                                                                                                                                                                                                                                                                                                                                              | Description                                                                              | Device     | Speed Grade  |              |              | Units |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------------|--------------|--------------|--------------|-------|
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          |            | -3           | -2           | -1           |       |
| Example Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin, <sup>(1)</sup> Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in <a href="#">IOB Switching Characteristics, page 32</a> . |                                                                                          |            |              |              |              |       |
| T <sub>PSDCMPLL_0</sub> /<br>T <sub>PHDCMPLL_0</sub>                                                                                                                                                                                                                                                                                                | No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in Source-Synchronous Mode | XC5VLX20T  | N/A          | 0.32<br>0.56 | 0.33<br>0.63 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX30   | 0.45<br>0.54 | 0.46<br>0.54 | 0.46<br>0.57 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX30T  | 0.45<br>0.54 | 0.46<br>0.54 | 0.46<br>0.57 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX50   | 0.43<br>0.56 | 0.44<br>0.56 | 0.44<br>0.59 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX50T  | 0.43<br>0.56 | 0.44<br>0.56 | 0.44<br>0.59 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX85   | 0.40<br>0.68 | 0.42<br>0.68 | 0.42<br>0.71 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX85T  | 0.39<br>0.68 | 0.42<br>0.68 | 0.42<br>0.71 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX110  | 0.38<br>0.74 | 0.41<br>0.74 | 0.41<br>0.78 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX110T | 0.38<br>0.74 | 0.41<br>0.74 | 0.41<br>0.78 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX155  | 0.24<br>1.00 | 0.29<br>1.00 | 0.33<br>1.04 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX155T | 0.24<br>1.00 | 0.29<br>1.00 | 0.33<br>1.04 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX220  | N/A          | 0.36<br>1.23 | 0.38<br>1.27 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX220T | N/A          | 0.36<br>1.23 | 0.38<br>1.27 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX330  | N/A          | 0.34<br>1.40 | 0.37<br>1.46 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VLX330T | N/A          | 0.36<br>1.40 | 0.38<br>1.46 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VSX35T  | 0.44<br>0.72 | 0.46<br>0.72 | 0.46<br>0.75 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VSX50T  | 0.41<br>0.74 | 0.43<br>0.74 | 0.43<br>0.77 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VSX95T  | N/A          | 0.41<br>0.98 | 0.41<br>1.02 | ns    |
|                                                                                                                                                                                                                                                                                                                                                     |                                                                                          | XC5VSX240T | N/A          | 0.35<br>1.47 | 0.38<br>1.53 | ns    |

Table 97: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

| Symbol                                               | Description                                                                              | Device     | Speed Grade  |              |              | Units |
|------------------------------------------------------|------------------------------------------------------------------------------------------|------------|--------------|--------------|--------------|-------|
|                                                      |                                                                                          |            | -3           | -2           | -1           |       |
| T <sub>PSDCMPLL_0</sub> /<br>T <sub>PHDCMPLL_0</sub> | No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in Source-Synchronous Mode | XC5VTX150T | N/A          | 0.40<br>0.89 | 0.40<br>0.94 | ns    |
|                                                      |                                                                                          | XC5VTX240T | N/A          | 0.38<br>1.12 | 0.39<br>1.17 | ns    |
|                                                      |                                                                                          | XC5VFX30T  | 0.34<br>0.83 | 0.36<br>0.87 | 0.37<br>0.92 | ns    |
|                                                      |                                                                                          | XC5VFX70T  | 0.29<br>0.75 | 0.32<br>0.78 | 0.32<br>0.83 | ns    |
|                                                      |                                                                                          | XC5VFX100T | 0.35<br>0.90 | 0.35<br>0.92 | 0.35<br>0.96 | ns    |
|                                                      |                                                                                          | XC5VFX130T | 0.33<br>1.07 | 0.37<br>1.11 | 0.41<br>1.16 | ns    |
|                                                      |                                                                                          | XC5VFX200T | N/A          | 0.29<br>1.42 | 0.33<br>1.46 | ns    |

**Notes:**

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
- IFF = Input Flip-Flop.

## Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-5 FPGA source-synchronous transmitter and receiver data-valid windows.

**Table 98: Duty Cycle Distortion and Clock-Tree Skew**

| Symbol            | Description                                            | Device     | Speed Grade |      |      | Units |
|-------------------|--------------------------------------------------------|------------|-------------|------|------|-------|
|                   |                                                        |            | -3          | -2   | -1   |       |
| $T_{DCD\_CLK}$    | Global Clock Tree Duty Cycle Distortion <sup>(1)</sup> | All        | 0.12        | 0.12 | 0.12 | ns    |
| $T_{CKSKEW}$      | Global Clock Tree Skew <sup>(2)</sup>                  | XC5VLX20T  | N/A         | 0.24 | 0.25 | ns    |
|                   |                                                        | XC5VLX30   | 0.21        | 0.22 | 0.22 | ns    |
|                   |                                                        | XC5VLX30T  | 0.21        | 0.22 | 0.22 | ns    |
|                   |                                                        | XC5VLX50   | 0.26        | 0.27 | 0.28 | ns    |
|                   |                                                        | XC5VLX50T  | 0.26        | 0.27 | 0.28 | ns    |
|                   |                                                        | XC5VLX85   | 0.42        | 0.43 | 0.45 | ns    |
|                   |                                                        | XC5VLX85T  | 0.42        | 0.43 | 0.45 | ns    |
|                   |                                                        | XC5VLX110  | 0.48        | 0.50 | 0.51 | ns    |
|                   |                                                        | XC5VLX110T | 0.48        | 0.50 | 0.51 | ns    |
|                   |                                                        | XC5VLX155  | 0.82        | 0.85 | 0.88 | ns    |
|                   |                                                        | XC5VLX155T | 0.82        | 0.85 | 0.88 | ns    |
|                   |                                                        | XC5VLX220  | N/A         | 1.07 | 1.10 | ns    |
|                   |                                                        | XC5VLX220T | N/A         | 1.07 | 1.10 | ns    |
|                   |                                                        | XC5VLX330  | N/A         | 1.25 | 1.29 | ns    |
|                   |                                                        | XC5VLX330T | N/A         | 1.25 | 1.29 | ns    |
|                   |                                                        | XC5VSX35T  | 0.38        | 0.39 | 0.39 | ns    |
|                   |                                                        | XC5VSX50T  | 0.43        | 0.44 | 0.45 | ns    |
|                   |                                                        | XC5VSX95T  | N/A         | 0.72 | 0.74 | ns    |
|                   |                                                        | XC5VSX240T | N/A         | 1.32 | 1.36 | ns    |
|                   |                                                        | XC5VTX150T | N/A         | 0.70 | 0.73 | ns    |
|                   |                                                        | XC5VTX240T | N/A         | 0.97 | 1.00 | ns    |
|                   |                                                        | XC5VFX30T  | 0.34        | 0.35 | 0.35 | ns    |
|                   |                                                        | XC5VFX70T  | 0.41        | 0.42 | 0.43 | ns    |
|                   |                                                        | XC5VFX100T | 0.82        | 0.84 | 0.86 | ns    |
|                   |                                                        | XC5VFX130T | 0.82        | 0.84 | 0.86 | ns    |
|                   |                                                        | XC5VFX200T | N/A         | 1.24 | 1.29 | ns    |
| $T_{DCD\_BUFIO}$  | I/O clock tree duty cycle distortion                   | All        | 0.10        | 0.10 | 0.10 | ns    |
| $T_{BUFIO\_SKEW}$ | I/O clock tree skew across one clock region            | All        | 0.07        | 0.07 | 0.08 | ns    |
| $T_{DCD\_BUFR}$   | Regional clock tree duty cycle distortion              | All        | 0.25        | 0.25 | 0.25 | ns    |

### Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The  $T_{CKSKEW}$  value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA\_Editor and Timing Analyzer tools to evaluate clock skew specific to the application.

Table 99: Package Skew

| Symbol               | Description                 | Device     | Package | Value | Units |
|----------------------|-----------------------------|------------|---------|-------|-------|
| T <sub>PKGSKEW</sub> | Package Skew <sup>(1)</sup> | XC5VLX20T  | FF323   | 131   | ps    |
|                      |                             | XC5VLX30   | FF324   | 80    | ps    |
|                      |                             |            | FF676   | 142   | ps    |
|                      |                             | XC5VLX30T  | FF323   | 127   | ps    |
|                      |                             |            | FF665   | 93    | ps    |
|                      |                             | XC5VLX50   | FF324   | 80    | ps    |
|                      |                             |            | FF676   | 142   | ps    |
|                      |                             |            | FF1153  | 175   | ps    |
|                      |                             | XC5VLX50T  | FF665   | 93    | ps    |
|                      |                             |            | FF1136  | 162   | ps    |
|                      |                             | XC5VLX85   | FF676   | 142   | ps    |
|                      |                             |            | FF1153  | 174   | ps    |
|                      |                             | XC5VLX85T  | FF1136  | 164   | ps    |
|                      |                             | XC5VLX110  | FF676   | 142   | ps    |
|                      |                             |            | FF1153  | 173   | ps    |
|                      |                             |            | FF1760  | 190   | ps    |
|                      |                             | XC5VLX110T | FF1136  | 163   | ps    |
|                      |                             |            | FF1738  | 171   | ps    |
|                      |                             | XC5VLX155  | FF1153  | 161   | ps    |
|                      |                             |            | FF1760  | 181   | ps    |
|                      |                             | XC5VLX155T | FF1136  | 147   | ps    |
|                      |                             |            | FF1738  | 174   | ps    |
|                      |                             | XC5VLX220  | FF1760  | 178   | ps    |
|                      |                             | XC5VLX220T | FF1738  | 156   | ps    |
|                      |                             | XC5VLX330  | FF1760  | 177   | ps    |
|                      |                             | XC5VLX330T | FF1738  | 155   | ps    |
|                      |                             | XC5VSX35T  | FF665   | 103   | ps    |
|                      |                             | XC5VSX50T  | FF665   | 103   | ps    |
|                      |                             |            | FF1136  | 157   | ps    |
|                      |                             | XC5VSX95T  | FF1136  | 176   | ps    |
|                      |                             | XC5VSX240T | FF1738  | 161   | ps    |
|                      |                             | XC5VTX150T | FF1156  |       | ps    |
|                      |                             | XC5VTX150T | FF1759  | 157   | ps    |
|                      |                             | XC5VTX240T | FF1759  | 157   | ps    |
|                      |                             | XC5VFX30T  | FF665   | 102   | ps    |
|                      |                             | XC5VFX70T  | FF665   | 102   | ps    |
|                      |                             |            | FF1136  | 153   | ps    |
|                      |                             | XC5VFX100T | FF1136  | 144   | ps    |
|                      |                             |            | FF1738  | 172   | ps    |
|                      |                             | XC5VFX130T | FF1738  | 181   | ps    |
|                      |                             | XC5VFX200T | FF1738  | 164   | ps    |

**Notes:**

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 100: Sample Window

| Symbol            | Description                                                | Device | Speed Grade |     |     | Units |
|-------------------|------------------------------------------------------------|--------|-------------|-----|-----|-------|
|                   |                                                            |        | -3          | -2  | -1  |       |
| $T_{SAMP}$        | Sampling Error at Receiver Pins <sup>(1)</sup>             | All    | 450         | 500 | 550 | ps    |
| $T_{SAMP\_BUFIO}$ | Sampling Error at Receiver Pins using BUFIO <sup>(2)</sup> | All    | 350         | 400 | 450 | ps    |

**Notes:**

1. This parameter indicates the total sampling error of Virtex-5 FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 DCM jitter
  - DCM accuracy (phase offset)
  - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-5 FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 101: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out

| Symbol                                                                              | Description               | Speed Grade   |               |               | Units |
|-------------------------------------------------------------------------------------|---------------------------|---------------|---------------|---------------|-------|
|                                                                                     |                           | -3            | -2            | -1            |       |
| Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO |                           |               |               |               |       |
| T <sub>PSCS</sub> /T <sub>PHCS</sub>                                                | Setup/Hold of I/O clock   | −0.56<br>1.59 | −0.54<br>1.72 | −0.54<br>1.91 | ns    |
| Pin-to-Pin Clock-to-Out Using BUFIO                                                 |                           |               |               |               |       |
| T <sub>ICKOFCS</sub>                                                                | Clock-to-Out of I/O clock | 4.42          | 4.82          | 5.40          | ns    |

## Revision History

The following table shows the revision history for this document.

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 04/14/2006 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 05/12/2006 | 1.1     | <ul style="list-style-type: none"> <li>First version posted to the Xilinx website. Minor typographical edits. Revised design software version on <a href="#">page 30</a>.</li> <li>Revised <math>T_{IDELAYRESOLUTION}</math> in <a href="#">Table 64, page 44</a>.</li> <li>Revised TDSPCKO in <a href="#">Table 69, page 48</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 05/24/2006 | 1.2     | Added register-to-register parameters to <a href="#">Table 52</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 08/04/2006 | 1.3     | <ul style="list-style-type: none"> <li>Added <math>V_{DRINT}</math>, <math>V_{DRI}</math>, and <math>C_{IN}</math> values to <a href="#">Table 3</a>.</li> <li>Added HSTL_I_12 and LVCMOS12 to <a href="#">Table 7</a> and renumbered the notes.</li> <li>Removed pin-to-pin performance (Table 12). Updated and added values to register-register performance <a href="#">Table 52</a> (was Table 13).</li> <li>Added values to <a href="#">Table 53</a>.</li> <li>Updated the speed specification version above <a href="#">Table 54</a>.</li> <li>Added to <a href="#">Table 56</a> the I/O standards: HSTL_II_T_DCI, HSTL_II_T_DCI_18, SSTL2_II_T_DCI, and SSTL18_II_T_DCI.</li> <li>Revised <math>F_{MAX}</math> values in <a href="#">Table 68</a>, and RDWR_B Setup/Hold values in <a href="#">Table 70</a>.</li> <li>In <a href="#">Table 74</a>, changed <math>F_{VCOMAX}</math>, removed <math>T_{LOCKMIN}</math>, and revised <math>T_{LOCKMAX}</math> values, also removed note pointing to Architecture Wizard.</li> <li>Removed Note 2 on <a href="#">Table 88</a>.</li> </ul> |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 09/06/2006 | 2.0     | <ul style="list-style-type: none"> <li>Added new sections for LXT devices and added LXT devices to the appropriate tables. The addition of the <a href="#">GTP_DUAL Tile Specifications</a> required the tables to be renumbered.</li> <li>Changed maximum <math>V_{IN}</math> values in <a href="#">Table 1</a> and <a href="#">Table 2</a>.</li> <li>Updated values and added <math>T_j = 85^{\circ}\text{C}</math> to <a href="#">Table 4, page 3</a>.</li> <li>Revised the cascade block RAM <a href="#">Memory, page 28</a> section in <a href="#">Table 52</a> to 64K with new I/O delays.</li> <li>Revised the setup and hold times in <a href="#">Table 60, page 40</a>.</li> <li>Added <math>F_{MAX\_CASCADE}</math> to <a href="#">Table 68, page 47</a>.</li> <li>Revised <math>F_{FXLFMSMAX}</math> and <math>F_{CLKINLFFXMSMAX}</math> in <a href="#">Table 76, page 57</a>.</li> </ul>                                                                                                        |
| 10/13/2006 | 2.1     | <ul style="list-style-type: none"> <li>Added System Monitor parameters. Added XC5VLX85T to appropriate tables.</li> <li>Revised <a href="#">Table 28</a> including notes. Added <a href="#">Table 29</a>, and <a href="#">Figure 3</a> and <a href="#">Figure 4</a>.</li> <li>Added <a href="#">Table 48, page 25</a>: RocketIO CRC block.</li> <li>Revised design software version and <a href="#">Table 54</a> on <a href="#">page 30</a>.</li> <li>Updated <a href="#">ILOGIC Switching Characteristics, page 40</a></li> <li>Updated <math>F_{MAX\_ECC}</math> in <a href="#">Table 68, page 47</a>.</li> <li>Changed hold times for <math>T_{SMDCCCK}/T_{SMCCCKD}</math> and <math>T_{BPIDCC}/T_{BPICCD}</math> in <a href="#">Table 70, page 51</a>.</li> <li>Revised <math>T_{FBDELAY}</math>, <math>F_{OUTMIN}</math>, <math>F_{OUTMAX}</math>, and <math>F_{INJITTER}</math> <a href="#">Table 74, page 55</a>.</li> <li>Revised <a href="#">Table 76, page 57</a>.</li> </ul>                     |
| 01/05/2007 | 2.2     | <ul style="list-style-type: none"> <li>Added <math>I_{IN}</math> to <a href="#">Table 2</a>. Added XC5VLX220T to appropriate tables.</li> <li>Added LVDCI33, LVDCI25, LVDCI18, LVDCI15 to <a href="#">Table 7</a>.</li> <li>Update the symbols in the GTP Transceiver <a href="#">Table 24</a>, <a href="#">Table 25</a>, and <a href="#">Table 26</a>.</li> <li>Add values for -1 speed grade in <a href="#">Table 30, page 16</a>.</li> <li>Added SFI-4.1 values to <a href="#">Table 53, page 29</a>.</li> <li>Removed -3 speed grade from available LX220 device list in <a href="#">Table 54, page 30</a>.</li> <li>Added maximum frequency to <a href="#">Table 72</a> and <a href="#">Table 73, page 54</a>.</li> <li>In <a href="#">Table 76, page 57</a> changed the all the CLKDV, CLKFX, and CLKFX180 Min values and the CLKIN Min values in the Input Clocks (High Frequency Mode) section.</li> <li>Added values to <a href="#">Table 79</a> and <a href="#">Table 80, page 60</a>.</li> </ul> |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02/02/2007 | 3.0     | <ul style="list-style-type: none"> <li>Added XC5VSX35T, XC5VSX50T, and SX5VSX95T devices to appropriate tables.</li> <li>Revised the <math>I_{RPU}</math> values in <a href="#">Table 3, page 2</a>.</li> <li>Revised the <math>I_{CCAUXQ}</math> values in <a href="#">Table 4, page 3</a>.</li> <li>Added values to <a href="#">Table 5, page 6</a>.</li> <li>Minor added notes and changed descriptions in <a href="#">Table 25, page 13</a> and <a href="#">Table 26, page 13</a>.</li> <li>Revised the SFI-4.1 (SDR LVDS Interface) -1 values in <a href="#">Table 53, page 29</a>.</li> <li>Revised gain error, bipolar gain error, and event conversion time in <a href="#">Table 51, page 26</a>.</li> <li>Changed the design software version that matches this data sheet above <a href="#">Table 54 on page 30</a>.</li> <li>In <a href="#">Switching Characteristics</a>, the following values are revised: <ul style="list-style-type: none"> <li>LVC MOS25, Fast, 12 mA in <a href="#">Table 56, page 32</a>.</li> <li>Setup and Hold and <math>T_{ICKQ}</math> in <a href="#">Table 60, page 40</a>.</li> <li><math>T_{OCKQ}</math> in <a href="#">Table 61, page 41</a>.</li> <li>Sequential delay values in <a href="#">Table 63, page 43</a>.</li> <li><math>T_{CXB}</math>, <math>T_{CEO}</math>, and <math>T_{DICK}</math> in <a href="#">Table 65, page 44</a>.</li> <li><math>T_{RCKO\_DO}</math>, <math>T_{RCKO\_POINTERS}</math>, <math>T_{RCKO\_ECCR}</math>, <math>T_{RCKO\_ECC}</math>, <math>T_{RCCK\_ADDR}</math>, <math>T_{RDCK\_DI}</math>, <math>T_{RDCK\_DI\_ECC}</math>, <math>T_{RCCK\_WREN}</math>, and <math>T_{RCO\_FLAGS}</math> in <a href="#">Table 68, page 47</a>.</li> <li><math>T_{DSPDCK\_CC}</math>, <math>T_{DSPCCK\_RSTAA}</math>, <math>T_{DSPCCK\_RSTBB}</math>, <math>T_{DSPCKO\_PP}</math>, <math>T_{CRYOUTP}</math>, <math>F_{MAX\_MULT\_NOMREG}</math> and <math>F_{MAX\_MULT\_NOMREG\_PATDET}</math> in <a href="#">Table 69, page 48</a>.</li> <li><math>T_{BCKO\_O}</math>, and <math>T_{BGCKO\_O}</math> in <a href="#">Table 71, page 53</a>.</li> <li><math>T_{BUFIOCKO\_O}</math> and <math>F_{MAX}</math> in <a href="#">Table 72, page 53</a>.</li> <li><math>T_{BRCKO\_O}</math> and <math>T_{BRCKO\_O\_BYP}</math> in <a href="#">Table 73, page 54</a>.</li> <li>Parameters in <a href="#">Table 74, page 55</a> including notes.</li> </ul> </li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Output Parameter Guidelines</a>: <ul style="list-style-type: none"> <li>Revised values in <a href="#">Table 84</a>, <a href="#">Table 85</a>, and <a href="#">Table 86</a>.</li> </ul> </li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a>: <ul style="list-style-type: none"> <li>Clarified description in <a href="#">Table 91, page 69</a>.</li> <li>Revised values in <a href="#">Table 91</a>, <a href="#">Table 92</a>, and <a href="#">Table 93</a>.</li> <li>Removed duplicate <math>T_{BUFR\_MAX\_FREQ}</math> and <math>T_{BUFIO\_MAX\_FREQ}</math> from <a href="#">Table 98</a>.</li> </ul> </li> <li>Revised values in <a href="#">Table 101, page 85</a>.</li> </ul> |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 05/18/2007 | 3.1     | <ul style="list-style-type: none"> <li>Added typical values for n and r in <a href="#">Table 3</a>.</li> <li>Revised and added values to <a href="#">Table 4</a>.</li> <li>Revised standard I/O levels in <a href="#">Table 7</a>.</li> <li>Additions and updates to <a href="#">Table 26</a>, <a href="#">Table 28</a>, <a href="#">Table 29</a>, <a href="#">Table 30</a>, <a href="#">Table 48</a>, <a href="#">Table 32</a>, <a href="#">Table 33</a>, <a href="#">Table 34</a>, and <a href="#">Table 35</a>.</li> <li>Added <a href="#">Ethernet MAC Switching Characteristics</a>, page 25.</li> <li>Changed the design software version that matches this data sheet above <a href="#">Table 54</a> on page 30.</li> <li>Added new section: <a href="#">I/O Standard Adjustment Measurement Methodology</a>, page 37.</li> <li>In <a href="#">Switching Characteristics</a>, the following values are revised: <ul style="list-style-type: none"> <li>LVTTL, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 56</a>).</li> <li>LVC MOS33, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 56</a>).</li> <li>LVC MOS25, Slow and Fast, 2 mA and 4 mA, and Fast 12 mA (<a href="#">Table 56</a>).</li> <li>LVC MOS18, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 56</a>).</li> <li>LVC MOS15 and LVC MOS12, Slow and Fast, 2 mA (<a href="#">Table 56</a>).</li> <li>T<sub>IDOCK</sub> and T<sub>IDOCKD</sub> in <a href="#">Table 60</a>.</li> <li>Setup/Hold for Control Lines and Data Lines in <a href="#">Table 62</a>.</li> <li>Add T<sub>IDELAYPAT_JIT</sub> and revised T<sub>IDELAYRESOLUTION</sub> in <a href="#">Table 64</a>, page 44 and added Notes 1 and 2.</li> <li>Revised T<sub>RCK</sub> <a href="#">page 45</a> and removed T<sub>CKSR</sub> <a href="#">Table 65</a>, page 44.</li> <li>Replaced T<sub>TWC</sub> with T<sub>MCP</sub> symbol in <a href="#">Table 66</a>, page 46.</li> <li>Revised T<sub>CECK</sub> in <a href="#">Table 67</a>.</li> <li>Revised T<sub>RCKO_FLAGS</sub> and T<sub>RDCK_DI_ECC</sub> encode only in <a href="#">Table 68</a>.</li> <li>Revised Hold Times of Data/Control Pins to the Input Register Clock. Setup/Hold times of {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK. Hold times of some of the CE pins. Hold times of some of the RST pins. Hold times of {A, B} input to {P, CARRYOUT} output using multiplier and {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier, CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier, in <a href="#">Table 69</a>.</li> <li>Updated and added values to <a href="#">Table 70</a>, page 51.</li> <li>Revised -1 speed F<sub>MAX</sub> value in <a href="#">Table 72</a>, page 53.</li> <li>Added Note 4 to T<sub>LOCKMAX</sub> and revised F<sub>INDUTY</sub>, F<sub>INMAX</sub>, and F<sub>VCOMAX</sub> in <a href="#">Table 74</a>, page 55.</li> <li>Added ± values to <a href="#">Table 79</a> and <a href="#">Table 80</a>. Changed T<sub>OUT_OFFSET</sub> in <a href="#">Table 80</a>.</li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Output Parameter Guidelines</a>: <ul style="list-style-type: none"> <li>Revised values in <a href="#">Table 84</a> through <a href="#">Table 90</a>.</li> </ul> </li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a>: <ul style="list-style-type: none"> <li>Revised values in <a href="#">Table 91</a> through <a href="#">Table 97</a>.</li> </ul> </li> <li>In <a href="#">Source-Synchronous Switching Characteristics</a>: <ul style="list-style-type: none"> <li>Revised values in <a href="#">Table 98</a>, page 83.</li> <li>Added package skew values to <a href="#">Table 99</a>, page 84.</li> <li>Revised values in <a href="#">Table 101</a>, page 85.</li> </ul> </li> </ul> </li> </ul> |
| 06/15/2007 | 3.2     | <ul style="list-style-type: none"> <li>Updated T<sub>STG</sub> in <a href="#">Table 1</a>.</li> <li>Corrected V<sub>OH</sub>/V<sub>OL</sub> in <a href="#">Table 9</a> and <a href="#">Table 10</a>, page 8.</li> <li>Changed the design software version that matches this data sheet above <a href="#">Table 54</a> on page 30.</li> <li>Added <a href="#">Production Silicon and ISE Software Status</a>, page 31.</li> <li>Added T<sub>IDELAY_CLK_MAX</sub> and revised T<sub>CKSR</sub> in <a href="#">Table 64</a>, page 44.</li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Output Parameter Guidelines</a>: Revised values in <a href="#">Table 85</a> through <a href="#">Table 90</a>.</li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a>: Revised values in <a href="#">Table 92</a> through <a href="#">Table 97</a>.</li> <li>Corrected units to ns in <a href="#">Table 98</a>, page 83.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06/26/2007 | 3.3     | <ul style="list-style-type: none"> <li>Added conditions to <math>DV_{PPIN}</math> in <a href="#">Table 28, page 14</a>.</li> <li>Changed the <math>F_{GTXMAX}</math> symbol name to <math>F_{GTPMAX}</math>.</li> <li>Updated GTP maximum line rates to 3.75 Gb/s in <a href="#">Table 30, page 16</a>.</li> <li>Updated maximum frequencies in <a href="#">Table 33, page 17</a>.</li> <li>Added 3.75 Gb/s condition and changed maximum value of <math>F_{GTX}</math> in <a href="#">Table 34, page 17</a>.</li> <li>Added 3.75 Gb/s sinusoidal jitter specification and changed maximum value of <math>F_{GRX}</math> in <a href="#">Table 35, page 18</a>.</li> <li>Changed analog input common mode ranges in <a href="#">Table 51, page 26</a>.</li> <li>Changed <math>T_{PKGSKEW}</math> values in <a href="#">Table 99, page 84</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 07/26/2007 | 3.4     | <ul style="list-style-type: none"> <li>Added maximum value of <math>I_{REF}</math> to <a href="#">Table 3, page 2</a>.</li> <li>Revised <a href="#">Table 54</a> and changed the design software version in <a href="#">Table 55</a> for production devices.</li> <li>In <a href="#">Table 64, page 44</a>, added High Performance Mode to Note 2.</li> <li>In <a href="#">Table 70, page 51</a>, revised description of <math>T_{SMDCKK}/T_{SMCKKD}</math>.</li> <li>Added Note 4 to <math>T_{DUTYCYCRANGE\_200\_400}</math> frequency range in <a href="#">Table 78, page 59</a>.</li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a>: Revised note 1 in <a href="#">Table 91</a> through <a href="#">Table 96</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 09/27/2007 | 3.5     | <ul style="list-style-type: none"> <li>Added <math>I_{BATT}</math> value and Note 2 to <a href="#">Table 3</a>.</li> <li>Added <a href="#">DRP Clock Frequency</a> and Note 4 to <a href="#">Table 51</a>. Revised the typical and maximum values and units for gain error and bipolar gain error.</li> <li>Removed unsupported XC5VSX95T -3 speed grade from <a href="#">Table 54</a> and <a href="#">Table 55</a>.</li> <li>Removed unsupported I/O standards (LVDS_33, LVDSEXT_33, and ULVDS_25) from <a href="#">Table 51</a>. Also updated LVDSEXT, 2.5V in <a href="#">Table 59</a>.</li> <li>Added values to <a href="#">Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</a> in <a href="#">Table 70</a>.</li> <li>In <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a>: Revised note 1 in <a href="#">Table 91</a> through <a href="#">Table 97</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11/05/2007 | 3.6     | <ul style="list-style-type: none"> <li>Removed note 1 from <a href="#">Table 52, page 28</a>. <math>F_{MAX}</math> of clock is not an applicable limitation.</li> <li>Revised DDR2 memory interface performance in <a href="#">Table 53, page 29</a>.</li> <li>Revised <a href="#">Table 55</a> to add ISE 9.2i SP3 where applicable.</li> <li>Removed XC5VSX95T -3 speed grade support from applicable tables.</li> <li>Removed unsupported I/O standard (LVPECL_33) from <a href="#">Table 58</a> and added LVPECL_25.</li> <li>Added <math>T_{SMCO}</math> and <math>T_{SMCKBY}</math> to <a href="#">Table 70, page 51</a>.</li> <li>Revised note 3 in <a href="#">Table 76, page 57</a> and <a href="#">Table 77, page 58</a>.</li> <li>Clarified notes in <a href="#">Table 87</a> to <a href="#">Table 90</a>, and <a href="#">Table 94</a> to <a href="#">Table 97</a>.</li> <li>Revised note 1 in <a href="#">Table 99</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 12/11/2007 | 3.7     | <ul style="list-style-type: none"> <li>Added new devices (XC5VLX20T, XC5VLX155, and XC5VLX155T) throughout document.</li> <li>Removed -3 speed grade from XC5VSX95T device lists.</li> <li>Added <a href="#">Table 31, page 16</a>.</li> <li>Revised <a href="#">Virtex-5 Device Pin-to-Pin Output Parameter Guidelines</a> in <a href="#">Table 87</a> through <a href="#">Table 90</a>, and <a href="#">Virtex-5 Device Pin-to-Pin Input Parameter Guidelines</a> in <a href="#">Table 90</a> and <a href="#">Table 92</a> through <a href="#">Table 97</a>. Also revised Note 1 on <a href="#">Table 92</a> through <a href="#">Table 97</a>.</li> <li>Revised Note 1 on <a href="#">Table 99</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 02/05/2008 | 3.8     | <ul style="list-style-type: none"> <li>Updated date on version 3.7. Other minor typographical edits.</li> <li>Updated the sentence: Xilinx does not specify the current or I/O behavior for other power-on sequences, on <a href="#">page 6</a>.</li> <li>Added values and notes to <a href="#">Table 27, page 14</a>. Removed <math>I_{CCINTQ}</math> since it is included in <a href="#">Table 4, page 3</a>. Combined <math>I_{VTRXCQ}</math> into <math>I_{VTRXQ}</math> values.</li> <li>Revised <math>T_{LLSKEW}</math> values in <a href="#">Table 34, page 17</a>.</li> <li>Revised <math>R_{XPPMTOL}</math> values and note 1 in <a href="#">Table 35, page 18</a>.</li> <li>Revised -2 performance value for SPI-4.2 in <a href="#">Table 53, page 29</a>.</li> <li>Added <math>T_{IODDO\_T}</math>, <math>T_{IODDO\_IDATAIN}</math>, <math>T_{IODDO\_ODATAIN}</math>, and Note 3 to <a href="#">Table 64, page 44</a>.</li> <li>Split out the <math>F_{MAX}</math> rows in <a href="#">Table 71</a> and the <math>F_{OUTMAX}</math> rows in <a href="#">Table 74</a>, revised -2 value for smallest devices in both tables.</li> <li>Added <a href="#">Table 75: PLL in PMCD Mode Switching Characteristics, page 56</a>.</li> <li>Updated <a href="#">Table 4</a> and <a href="#">Table 84</a> to <a href="#">Table 98</a> to match speed grade designations listed in <a href="#">Table 54</a>.</li> <li>Revised Note 1 on <a href="#">Table 96</a> and <a href="#">Table 97</a>.</li> </ul> |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 03/31/2008 | 4.0     | <ul style="list-style-type: none"> <li>Added XC5VFX30T, XC5VFX70T, XC5VFX100T, XC5VFX130T, XC5VFX200T devices to appropriate tables.</li> <li>Updated <a href="#">Power-On Power Supply Requirements</a>, page 6.</li> <li>Added <a href="#">GTX_DUAL Tile Specifications</a> and <a href="#">PowerPC 440 Switching Characteristics</a> sections.</li> <li>Corrected MGTA VCC in <a href="#">Table 24</a>, page 13.</li> <li>Updated MGTR<sub>REF</sub> in <a href="#">Table 26</a>, page 13.</li> <li>Changed the symbol names to F<sub>GTPTX</sub> in <a href="#">Table 34</a> and F<sub>GTPRX</sub> in <a href="#">Table 35</a>.</li> <li>Moved the <a href="#">CRC Block Switching Characteristics</a> to <a href="#">Table 48</a>, page 25.</li> <li>Added notes to <a href="#">Table 53</a>.</li> <li>Revised speed specification version to 1.59.</li> </ul>                                                                                                                                                          |
| 04/25/2008 | 4.1     | <ul style="list-style-type: none"> <li>Added XC5VSX240T to appropriate tables.</li> <li>Clarified maximum frequency descriptions in <a href="#">Table 68</a>, page 47.</li> <li>Added Maximum Readback Frequency (F<sub>RBCK</sub>) to SelectMAP Mode Programming Switching in <a href="#">Table 70</a>.</li> <li>Revised speed specification version to 1.60.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 05/09/2008 | 4.2     | <ul style="list-style-type: none"> <li>Revised <a href="#">Ethernet MAC Switching Characteristics</a> and added <a href="#">Endpoint Block for PCI Express Designs Switching Characteristics</a>.</li> <li>Revised some V<sub>MEAS</sub> values and added note 6 to <a href="#">Table 58</a>, page 37. Added <a href="#">Figure 12</a>, page 38 to <a href="#">Output Delay Measurements</a>. Revised some V<sub>MEAS</sub> and R<sub>REF</sub> values and added note 4 to <a href="#">Table 59</a>, page 38.</li> <li>Reversed the order of the setup/hold values for T<sub>PLLCCK_REL</sub>/T<sub>PLLCCK_REL</sub> in <a href="#">Table 75</a>, page 56.</li> <li>Added Package Skew values to <a href="#">Table 99</a>, page 84.</li> </ul>                                                                                                                                                                                                                                                                               |
| 05/15/2008 | 4.3     | <ul style="list-style-type: none"> <li>Revised <a href="#">Table 12</a>, page 9.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 06/12/2008 | 4.4     | <ul style="list-style-type: none"> <li>Added values to some devices in <a href="#">Table 4</a>.</li> <li>Increased the maximum V<sub>IN</sub> in <a href="#">Table 28</a>, page 14.</li> <li>Revised V<sub>IDIFF</sub> and V<sub>ISE</sub> in <a href="#">Table 29</a>, <a href="#">Figure 3</a>, and <a href="#">Figure 4</a>, page 15. Same change for GTX transceivers in <a href="#">Table 41</a>, <a href="#">Figure 8</a>, and <a href="#">Figure 9</a>, page 21.</li> <li>Added values to <a href="#">Table 43</a>.</li> <li>Updated <a href="#">Table 54</a> and <a href="#">Table 55</a> with production status on some devices.</li> <li>In <a href="#">Table 71</a>, revised T<sub>BCK0_0</sub>, T<sub>BGCK0_0</sub>. In <a href="#">Table 73</a>, revised T<sub>BRCKO_0</sub>, and T<sub>BRCKO_0_BYP</sub>.</li> <li>Revised XC5VLX20T, XC5VLX155, XC5VLX155T, XC5VFX30T, XC5VFX70T, XC5VFX100T, XC5VFX130T, and some XC5VSX240T values in <a href="#">Table 84</a> through <a href="#">Table 98</a>.</li> </ul> |
| 06/18/2008 | 4.5     | <ul style="list-style-type: none"> <li>Added values to <a href="#">Table 5</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 06/26/2008 | 4.6     | <ul style="list-style-type: none"> <li>Added values to <a href="#">Table 5</a>.</li> <li>Moved XC5VLX20T to production in <a href="#">Table 54</a> and <a href="#">Table 55</a>.</li> <li>Updated the F<sub>OUTMAX</sub> in <a href="#">Table 74</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 09/23/2008 | 4.7     | <ul style="list-style-type: none"> <li>Added XC5VTX150T and XC5VTX240T devices to appropriate tables.</li> <li>Added values to <a href="#">Table 4</a> and <a href="#">Table 5</a>.</li> <li>Updated data in <a href="#">Table 38</a>, <a href="#">Table 39</a>, <a href="#">Table 40</a>, <a href="#">Table 41</a>, <a href="#">Table 42</a>, <a href="#">Table 44</a>, <a href="#">Table 45</a>, <a href="#">Table 46</a>, and <a href="#">Table 47</a>.</li> <li>Moved XC5VLX20T to production in <a href="#">Table 54</a> and <a href="#">Table 55</a>.</li> <li>Added note 8 to <a href="#">Table 68</a>, page 47.</li> <li>Added note 1 to <a href="#">Table 74</a>, page 55.</li> </ul>                                                                                                                                                                                                                                                                                                                               |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12/02/2008 | 4.8     | <ul style="list-style-type: none"> <li>Added <math>I_{IN}</math> row to Absolute Maximum Ratings in <a href="#">Table 1, page 1</a>.</li> <li>In <a href="#">Table 32, page 16</a>, changed duty cycle values for <math>T_{DCREF}</math> and added note 2.</li> <li>Changed Conditions for <math>T_{PHASE}</math> in <a href="#">Table 32, page 16</a> and <a href="#">Table 44, page 22</a>.</li> <li>In <a href="#">Table 35, page 18</a>, updated <math>R_{XPPMTOL}</math> values, updated note 1, and added note 2.</li> <li>In <a href="#">Table 45, page 23</a>, updated parameters with separate FXT and TXT values.</li> <li>In <a href="#">Table 46, page 23</a>, corrected units of <math>T_{LLSKEW}</math>.</li> <li>In <a href="#">Table 54, page 30</a>, updated SX240T, FXT, and TXT speed grade designations.</li> <li>In <a href="#">Table 55, page 31</a>, updated SX240T and FXT rows.</li> <li>In <a href="#">Table 58, page 37</a>, added LVCMOS, 1.2V row.</li> <li>In <a href="#">Table 59, page 38</a>, corrected <math>V_{MEAS}</math> value for LVCMOS, 1.2V row.</li> <li>In <a href="#">Table 80, page 60</a>, updated note 3 with sentence about global clock tree.</li> </ul> |
| 12/19/2008 | 4.9     | <ul style="list-style-type: none"> <li>Updated <a href="#">Table 5, page 6</a> with power-on current values for XC5VSX240T, XC5VTX150T, XC5VTX240T, XC5VFX100T, and XC5VFX200T devices.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 01/14/2009 | 4.10    | <ul style="list-style-type: none"> <li>In <a href="#">Table 1, page 1</a>, changed note 2 to refer to UG112 for soldering guidelines.</li> <li>In <a href="#">Table 54, page 30</a>, moved speed grades for the XC5VTX150T and XC5VTX240T devices to Production.</li> <li>In <a href="#">Table 55, page 31</a>, added the ISE software version for the XC5VTX150T and XC5VTX240T devices.</li> <li>In <a href="#">Table 80, page 60</a>, moved the reference to the duty cycle distortion note to apply to both <math>T_{DUTY\_CYC\_DLL}</math> and <math>T_{DUTY\_CYC\_FX}</math>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 02/06/2009 | 5.0     | <ul style="list-style-type: none"> <li>Changed document classification from Advance Product Specification to Product Specification.</li> <li>In <a href="#">Table 1, page 1</a>, changed <math>V_{IN}</math> and added note 5.</li> <li>In <a href="#">Table 5, page 6</a>, removed the Max columns and added note 2 about calculating the maximum startup current.</li> <li>In <a href="#">Table 74, page 55</a>, removed LX20T from second row of <math>F_{OUTMAX}</math>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 04/01/2009 | 5.1     | <ul style="list-style-type: none"> <li>In <a href="#">Table 65, page 44</a>, changed “A – D input” to “AX – DX input” for the <math>T_{DICK}/T_{CKDI}</math> parameter.</li> <li>In <a href="#">Table 74, page 55</a>, prepended “±” to all speed grade values for the <math>T_{OUTDUTY}</math> parameter.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 06/25/2009 | 5.2     | <ul style="list-style-type: none"> <li>In <a href="#">Table 2, page 2</a>, added note 6.</li> <li>In <a href="#">Table 11, page 9</a>, changed <math>V_{CCAUX}</math> to <math>V_{CCO}</math> in note 1.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 05/05/2010 | 5.3     | <p>Removed <math>DV_{PPIN}</math> from the examples in <a href="#">Figure 2</a> and <a href="#">Figure 7</a>.</p> <p>In <a href="#">Table 31</a>, changed “GTPDRPCLK” to “GTP DCLK (DRP clock)” in the Description column. In <a href="#">Table 35</a>, added table note 2 about <math>R_{XPPMTOL}</math>.</p> <p>In <a href="#">Table 41</a>, changed the maximum value of <math>V_{ISE}</math> to 1000 mV.</p> <p>In <a href="#">Table 42</a>, changed the minimum PLL frequency (<math>F_{GPLLMIN}</math>) to 1.48 GHz for all three speed grades. In <a href="#">Table 43</a>, changed “GTXDRPCLK” to “GTX DCLK (DRP clock)” in the Description column. In <a href="#">Table 45</a>, removed “2 byte or 4 byte interface” from the Conditions column for <math>T_{RX}</math> and <math>T_{TX}</math>. In <a href="#">Table 47</a>, added table note 2 about <math>R_{XPPMTOL}</math>.</p> <p>In <a href="#">Table 51</a>, changed the maximum value of <math>AI_{DD}</math> to 13 mA.</p> <p>In <a href="#">Table 74</a>, updated description of <math>T_{FBDELAY}</math>.</p>                                                                                                                         |
| 12/04/2014 | 5.4     | Revised $V_{CMOUT}$ in <a href="#">Table 40</a> . Updated <a href="#">Notice of Disclaimer</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 06/17/2016 | 5.5     | In <a href="#">Table 28</a> , edited for clarification the equation $V_{CMOUT}$ ( $1200 - \text{amplitude}/2$ is now $1200 - V_{SEOUT}/2$ ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at [www.xilinx.com/legal.htm#tos](http://www.xilinx.com/legal.htm#tos); IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at [www.xilinx.com/legal.htm#tos](http://www.xilinx.com/legal.htm#tos).

## Automotive Applications Disclaimer

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View XC5VLX30-1FFG324I](#) on WIN SOURCE

 [Xilinx Inc.](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management