THE DATASHEET OF

XC3SD1800A-4CSG484C

Extended Spartan-3A Family Overview

DS706 (v1.1) February 2, 2011 **Product Specification**

General Description

The Extended Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in many high-volume, cost-sensitive electronic applications. With 12 devices ranging from 50,000 to 3.4 million system gates (as shown in Table 1), the Extended Spartan-3A family provides a broad range of densities and package options, integrated DSP MACs, and low total system cost while increasing functionality. The Extended Spartan-3A family includes the Spartan-3A devices and the higher density Spartan-3A DSP devices. It also includes the nonvolatile Spartan-3AN devices, which combine leading-edge FPGA and flash technologies to provide a new evolution in security, protection and functionality, ideal for space-critical or secure applications.

The Extended Spartan-3A family improves system performance and reduces the cost of configuration. These enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar. Because of its exceptionally low cost, the Extended Spartan-3A family is ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Extended Spartan-3A family is a superior alternative to mask-programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Summary of Extended Spartan-3A Family Features

- Very low-cost, high-performance logic solution for high-volume, cost-conscious applications
- Low-cost QFP and BGA packaging, Pb-free options
- Flexible power management
- Leading connectivity platform
- Abundant, flexible logic resources
- Dedicated resources for high-speed digital signal processing applications
- Precise clock management with up to eight Digital Clock Managers (DCMs)
- Integrated flash memory in Spartan-3AN devices
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Hierarchical SelectRAM™ memory architecture
- Configuration interface to industry-standard PROMs
- Complete Xilinx® ISE® and free WebPACK™ development system software support
- MicroBlaze™ and PicoBlaze™ embedded processors reduce risk
- Low-cost starter kits from Xilinx, distributors, and third parties
- XA versions available for Automotive applications

Table 1: **Summary of Extended Spartan-3A Family Attributes**

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits(1)	Block RAM Bits(1)	In-System Flash Bits(2)	Dedicated Multipliers	DSP48As	DCMs	Maximum User I/O
XC3S50A/AN	50K	1,584	176	704	11K	54K	1M	3	-	2	144
XC3S200A/AN	200K	4,032	448	1,792	28K	288K	4M	16	-	4	248(3)
XC3S400A/AN	400K	8,064	896	3,584	56K	360K	4M	20	-	4	311
XC3S700A/AN	700K	13,248	1,472	5,888	92K	360K	8M	20	-	8	372
XC3S1400A/AN	1400K	25,344	2,816	11,264	176K	576K	16M	32	-	8	502
XC3SD1800A	1800K	37,440	4,160	16,640	260K	1,512K	-	-	84	8	519
XC3SD3400A	3400K	53,712	5,968	23,872	373K	2,268K	-	-	126	8	469

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.
2. In-System flash is available in the Spartan-3AN devices only.
3. Maximum user I/O for XC3S200AN is 195.

Extended Spartan-3A Family Features

This section describes the features of the Extended Spartan-3A family of FPGAs.

- Very low-cost, high-performance logic solution for high-volume, cost-conscious applications
  - Use fewer standard components
  - Increase system reliability
- Flexible power management
  - Low 1.2V core voltage
  - Selectable I/O voltage with 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Full 3.3V ±10% compatibility and hot swap compliance
  - Dual-range auxiliary voltage allows 3.3V setting to simplify 3.3V-only design
  - Suspend and hibernate modes reduce system power
- Leading connectivity platform
  - Multi-standard SelectIO™ interface pins support most popular and emerging signaling standards
  - Up to 519 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, SSTL single-ended I/O
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - 640+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - Compliant to 32-/64-bit, 33/66 MHz PCI™ technology
- Abundant, flexible logic resources
  - Densities up to 53,712 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers and wide logic improve performance and density
  - Fast look-ahead carry logic
  - IEEE 1149.1/1532 JTAG programming/debug port
- Dedicated resources for high-speed digital signal processing applications
  - 18-bit by 18-bit multiplier with optional pipeline
  - 250 MHz XtremeDSP™ DSP48A block in the largest two devices
    - 48-bit accumulator for multiply-accumulate (MAC) operation
    - Integrated 18-bit pre-adder for multiply or multiply-add operation
    - Optional cascaded Multiply or MAC
    - Fills the DSP performance gap between DSP processors and high-end custom solutions
- Precise clock management with up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Integrated flash memory in Spartan-3AN devices
  - Up to 16 Mb of internal flash for configuration and application storage
  - Up to 11 Mb of user storage available for embedded processing, code shadowing, or scratchpad memory
  - Enables single-chip board designs for space-conscious applications
  - Enhanced design security with flash memory protection and security register
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Hierarchical SelectRAM memory architecture
  - Up to 2.2 Mb of fast block RAM with byte write enables for processor applications
  - Up to 373 Kb of efficient distributed RAM
  - External DDR/DDR2 SDRAM support up to 400 Mb/s
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial flash PROM
  - x8 or x8/x16 parallel NOR flash PROM
  - Low-cost Xilinx Platform Flash with JTAG
  - Load multiple bitstreams under FPGA control with MultiBoot capability
- Complete Xilinx ISE and free WebPACK development system software support
  - Industry's most comprehensive IP library
- MicroBlaze and PicoBlaze embedded processors
  - Integrate soft processor into FPGA to reduce Bill of Materials
  - Reduce obsolescence risks with soft processors
- Low-cost QFP and BGA packaging, Pb-free options
  - Common footprints support easy density migration
- Low-cost starter kits from Xilinx, distributors, and third parties
  - Complete starter kits designed for cost-sensitive, high-volume applications with design examples
- XA versions available for Automotive applications

Architectural Overview

The Extended Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier or DSP48A Blocks** accept two 18-bit binary numbers as inputs and calculate the product. The DSP48A blocks in the two largest members of the Extended Spartan-3A family add an 18-bit pre-adder and 48-bit accumulator.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

Configuration

The Extended Spartan-3A family is programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA configuration data is stored externally in a PROM or some other nonvolatile medium, either on or off the board, or stored within the FPGA in the nonvolatile Spartan-3AN devices. After applying power, the configuration data is written to the FPGA using any of eight different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial flash
- Internal SPI flash memory (Spartan-3AN devices)
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester
- MultiBoot configuration

MultiBoot configuration allows two or more FPGA configuration bitstreams to be stored in a single SPI serial flash or a parallel NOR flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each FPGA in the Extended Spartan-3A family contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The SelectIO interface of the Extended Spartan-3A family supports many popular single-ended and differential standards. Table 2 shows the maximum number of user I/Os and input-only pins for each device/package combination.

FPGAs in the Extended Spartan-3A family support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

FPGAs in the Extended Spartan-3A family support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os**

Device	VQ100 VQG100	TQ144 TQG144	FT256 FTG256	FG320 FGG320	FG400 FGG400	CS484 CSG484	FG484 FGG484	FG676 FGG676
Body Size (mm)	**14 x 14(1)**	**20 x 20(1)**	**17 x 17**	**19 x 19**	**21 x 21**	**19 x 19**	**23 x 23**	**27 x 27**
XC3S50A/AN	68(2)	108	144	-	-	-	-	-
XC3S200A/AN	68(2)	-	195	248(2)	-	-	-	-
XC3S400A/AN	-	-	195	251(2)	311	-	-	-
XC3S700A/AN	-	-	161(2)	-	311(2)	-	372	-
XC3S1400A/AN	-	-	161(2)	-	-	-	375	502
XC3SD1800A	-	-	-	-	-	309	-	519
XC3SD3400A	-	-	-	-	-	309	-	469

Notes:

1. The footprints for the VQ/TQ packages are larger than the package body. See the package drawings (http://www.xilinx.com/support/documentation/package_specifications.htm) for details.
2. These options are available only in the Spartan-3A devices, not the Spartan-3AN devices. See the data sheets for each device for Pb and Pb-free package option availability.

Package Marking

Figure 1 provides a top marking example for the Extended Spartan-3A family in the quad-flat packages. Figure 2 shows the top marking for the Extended Spartan-3A family in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The “5C” and “4I” Speed Grade/Temperature Range part combinations might be dual marked as “5C/4I”.

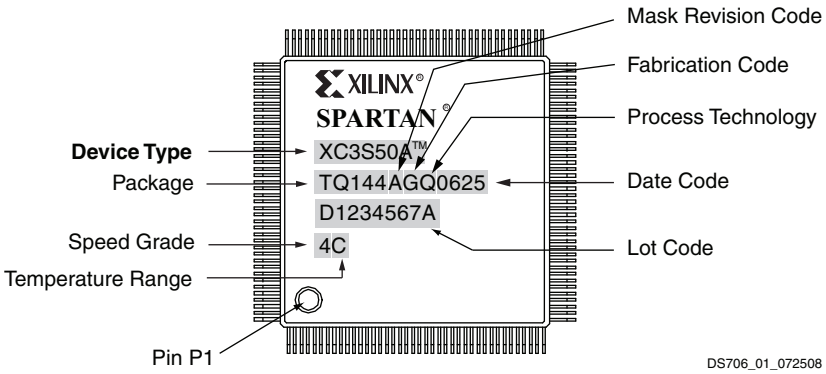

Figure 1: **Extended Spartan-3A Device QFP Package Marking Example**

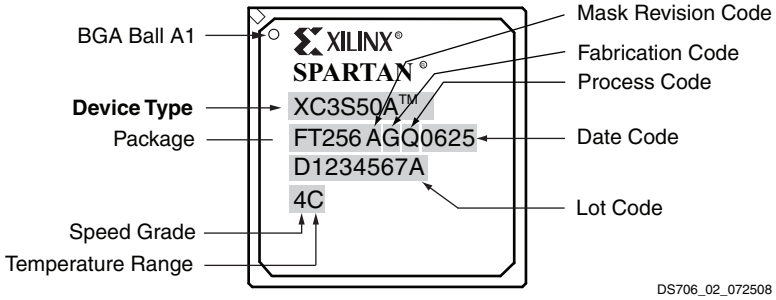

Figure 2: **Extended Spartan-3A Device BGA Package Marking Example**

Ordering Information

The Extended Spartan-3A family is available in both standard and Pb-free packaging options for all options of the Spartan-3A devices and the Spartan-3A DSP devices, and for most options of the Spartan-3AN devices (see DS557, *Spartan-3AN FPGA Family: Introduction and Ordering Information* for details).The Pb-free packages include a “G” character in the ordering code (see Figure 3).

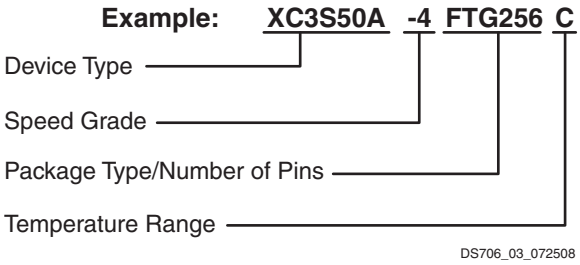

Figure 3: **Ordering Information**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XC3S50A/AN	–4	Standard Performance	VQ(G)100	100-pin Very Thin Quad Flat Pack (VQFP)	C	Commercial (0°C to 85°C)
XC3S200A/AN	–5	High Performance	TQ(G)144	144-pin Thin Quad Flat Pack (TQFP)	I	Industrial (–40°C to 100°C)
XC3S400A/AN			FT(G)256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	LI	Low Power Industrial (–40°C to 100°C) for Spartan-3A DSP devices (see DS610, *Spartan-3A DSP FPGA Data Sheet*)
XC3S700A/AN			FG(G)320	320-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400A/AN			FG(G)400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3SD1800A			CS(G)484	484-ball Chip-Scale Ball Grid Array (FBGA)		
XC3SD3400A			FG(G)484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG(G)676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:
1. The –5 speed grade is exclusively available in the Commercial temperature range.

Extended Spartan-3A Family Documentation

Complete and up-to-date documentation of the Extended Spartan-3A family of FPGAs is available on the Xilinx website. The following files are also available for download:

DS529, ***Spartan-3A FPGA Data Sheet***
DS610, ***Spartan-3A DSP FPGA Data Sheet***
DS557, ***Spartan-3AN FPGA Data Sheet***

These data sheets contain DC and Switching Characteristic specifications and pinouts for the Extended Spartan-3A family.

UG331, ***Spartan-3 Generation FPGA User Guide***

This guide includes chapters on:

- Clocking Resources
- Digital Clock Managers (DCMs)
- Block RAM
- Configurable Logic Blocks (CLBs)
- I/O Resources
- Embedded Multiplier Blocks
- Programmable Interconnect
- ISE Design Tools
- IP Cores
- Embedded Processing and Control Solutions
- Pin Types and Package Overview
- Package Drawings
- Powering FPGAs
- Power Management

UG332, ***Spartan-3 Generation Configuration User Guide***

This guide includes chapters on:

- Configuration Overview
- Detailed Descriptions by Mode
- ISE iMPACT Programming Examples
- MultiBoot Reconfiguration
- Design Authentication using Device DNA

UG333, ***Spartan-3AN FPGA In-System Flash User Guide***

This guide provides information for Spartan-3AN FPGA applications that write to or read from the In-System flash memory after configuration:

- SPI_ACCESS interface
- In-System flash memory architecture
- Read, program, and erase commands
- Status registers
- Sector Protection and Sector Lockdown features
- Security Register with Unique Identifier

UG431, ***XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide***

This guide describes the DSP48A slices and the DSP48A pre-adder.

Extended Spartan-3A Family Starter Kits

For specific hardware examples, see the Starter Kit boards for the Extended Spartan-3A family. The following web page has links to various boards for each family, including design examples and the user guides:

http://www.xilinx.com/products/boards/s3_sk_promo.htm

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/04/08	1.0	Initial Xilinx release.
01/29/10	1.0.1	Corrected typo in the slice count for XC3SD1800A in Table 1.
02/02/11	1.1	Updated for new Spartan-3AN family part/package combinations: XC3S50AN and XC3S400AN in FT(G)256 package, and XC3S1400AN in FG(G)484 package. Removed footnote for maximum user I/O for XC3S50A/AN in Table 1. Updated Table 2 content and table notes. Updated Device Temperature table.

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