THE DATASHEET OF

XC2C128-7VQ100I

www.win-source.net 0086-755-83957316

CoolRunner-II CPLD Family

DS090 (v3.1) September 11, 2008 **Product Specification**

Features

- Optimized for 1.8V systems
  - Industry's fastest low power CPLD
  - Densities from 32 to 512 macrocells
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - On-The-Fly Reconfiguration (OTF)
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt trigger input (per pin)
  - Multiple I/O banks on all devices
  - Unsurpassed low power management
    - DataGATE external signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (÷ 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Abundant product term clocks, output enables and set/resets
  - Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on select I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts
  - SSTL2_1,SSTL3_1, and HSTL_1 on 128 macrocell and denser devices
  - Hot pluggable
- PLA architecture
  - Superior pinout retention
  - 100% product term routability across function block
- Wide package availability including fine pitch:
  - Chip Scale Package (CSP) BGA, Fine Line BGA, TQFP, PQFP, VQFP, and QFN packages
  - Pb-free available for all packages
- Design entry/verification using Xilinx and industry standard CAE tools
- Free software support for all densities using Xilinx® WebPACK™ tool
- Industry leading nonvolatile 0.18 micron CMOS process
  - Guaranteed 1,000 program/erase cycles
  - Guaranteed 20 year data retention

Family Overview

Xilinx CoolRunner™-II CPLDs deliver the high speed and ease of use associated with the XC9500/XL/XV CPLD family with the extremely low power versatility of the XPLA3 family in a single CPLD. This means that the exact same parts can be used for high-speed data communications/computing systems and leading edge portable products, with the added benefit of In System Programming. Low power consumption and high-speed operation are combined into a single family that is easy to use and cost effective. Clocking techniques and other power saving features extend the users' power budget. The design features are supported starting with Xilinx ISE® 4.1i WebPACK tool. Additional details can be found in **Further Reading**, page 14.

Table 1 shows the macrocell capacity and key timing parameters for the CoolRunner-II CPLD family.

Table 1: **CoolRunner-II CPLD Family Parameters**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Macrocells	32	64	128	256	384	512
Max I/O	33	64	100	184	240	270
T_{PD} (ns)	3.8	4.6	5.7	5.7	7.1	7.1
T_{SU} (ns)	1.9	2.0	2.4	2.4	2.9	2.6
T_{CO} (ns)	3.7	3.9	4.2	4.5	5.8	5.8
$F_{SYSTEM1}$ (MHz)	323	263	244	256	217	179

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Table 2: **CoolRunner-II CPLD DC Characteristics**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
I_{CC} (µA), 0 MHz, 25°C (typical)	16	17	19	21	23	25
I_{CC} (mA), 50 MHz, 70°C (max)	2.5	5	10	27	45	55

1. I_{CC} is dynamic current.

Table 2 shows key DC characteristics for the CoolRunner-II family.

Table 3 shows the CoolRunner-II CPLD package offering with corresponding I/O count. All packages are surface mount, with over half of them being ball-grid technologies. The ultra tiny packages permit maximum functional capacity in the smallest possible area. The CMOS technology used in CoolRunner-II CPLDs generates minimal heat, allowing the use of tiny packages during high-speed operation.

With the exception of the Pb-free QF packages, there are at least two densities present in each package with three in the VQ100 (100-pin 1.0mm QFP), TQ144 (144-pin 1.4mm QFP), and FT256 (256-ball 1.0mm spacing FLBGA). The FT256 is particularly important for slim dimensioned portable products with mid- to high-density logic requirements.

Table 3: **CoolRunner-II CPLD Family Packages and I/O Count**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
QFG32(1)	21	-	-	-	-	-
VQ44	33	33	-	-	-	-
VQG44(1)	33	33	-	-	-	-
QFG48(1)	-	37	-	-	-	-
CP56	33	45	-	-	-	-
CPG56(1)	33	45	-	-	-	-
VQ100	-	64	80	80	-	-
VQG100(1)	-	64	80	80	-	-
CP132	-	-	100	106	-	-
CPG132(1)	-	-	100	106	-	-
TQ144	-	-	100	118	118	-
TQG144(1)	-	-	100	118	118	-
PQ208	-	-	-	173	173	173
PQG208(1)	-	-	-	173	173	173
FT256	-	-	-	184	212	212
FTG256(1)	-	-	-	184	212	212
FG324	-	-	-	-	240	270
FGG324(1)	-	-	-	-	240	270

Notes:
1. The letter "G" as the third character indicates a Pb-free package.

Table 4 details the distribution of advanced features across the CoolRunner-II CPLD family. The family has uniform basic features with advanced features included in densities where they are most useful. For example, it is very unlikely that four I/O banks are needed on 32 and 64 macrocell parts, but very likely they are for 384 and 512 macrocell parts. The I/O banks are groupings of I/O pins using any one of a subset of compatible voltage standards that share

the same V_{CCIO} level. (See Table 5 for a summary of CoolRunner-II CPLD I/O standards.)

Table 4: **CoolRunner-II CPLD Family Features**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
IEEE 1532	✓	✓	✓	✓	✓	✓
I/O banks	2	2	2	2	4	4
Clock division	-	-	✓	✓	✓	✓
DualEDGE Registers	✓	✓	✓	✓	✓	✓
DataGATE	-	-	✓	✓	✓	✓
LVTTL	✓	✓	✓	✓	✓	✓
LVCMOS33, 25, 18, and 15(1)	✓	✓	✓	✓	✓	✓
SSTL2_1	-	-	✓	✓	✓	✓
SSTL3_1	-	-	✓	✓	✓	✓
HSTL_1	-	-	✓	✓	✓	✓
Configurable ground	✓	✓	✓	✓	✓	✓
Quadruple data security	✓	✓	✓	✓	✓	✓
Open drain outputs	✓	✓	✓	✓	✓	✓
Hot plugging	✓	✓	✓	✓	✓	✓
Schmitt Inputs	✓	✓	✓	✓	✓	✓

1. LVCMOS15 requires the use of Schmitt-trigger inputs.

Architecture Description

CoolRunner-II CPLD is a highly uniform family of fast, low power CPLDs. The underlying architecture is a traditional CPLD architecture combining macrocells into Function Blocks (FBs) interconnected with a global routing matrix, the Xilinx Advanced Interconnect Matrix (AIM). The FBs use a Programmable Logic Array (PLA) configuration which allows all product terms to be routed and shared among any of the macrocells of the FB. Design software can efficiently synthesize and optimize logic that is subsequently fit to the FBs and connected with the ability to utilize a very high percentage of device resources. Design changes are easily and automatically managed by the software, which exploits the 100% routability of the Programmable Logic Array within each FB. This extremely robust building block delivers the industry's highest pinout retention, under very broad design conditions. The architecture is explained in more detail with the discussion of the underlying FBs, logic and interconnect.

The design software automatically manages these device resources so that users can express their designs using completely generic constructs without knowledge of these architectural details. More advanced users can take advantage of these details to more thoroughly understand the software's choices and direct its results.

Figure 1 shows the high-level architecture whereby FBs attach to pins and interconnect to each other within the internal interconnect matrix. Each FB contains 16 macrocells. The BSC path is the JTAG Boundary Scan Control

path. The BSC and ISP block has the JTAG controller and In-System Programming Circuits.

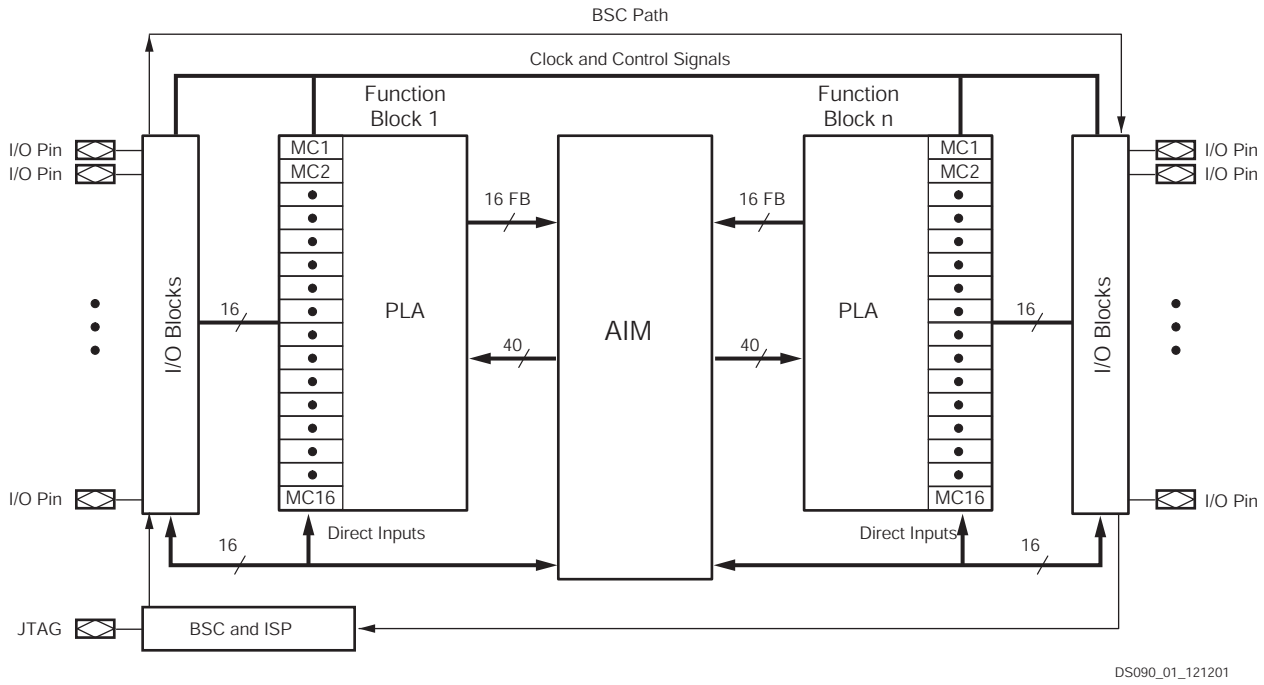

Figure 1: **CoolRunner-II CPLD Architecture**

Function Block

The CoolRunner-II CPLD FBs contain 16 macrocells, with 40 entry sites for signals to arrive for logic creation and connection. The internal logic engine is a 56 product term PLA. All FBs, regardless of the number contained in the device, are identical. For a high-level view of the FB, see Figure 2.

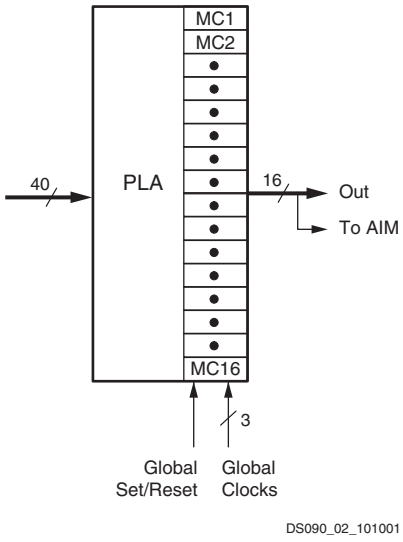

Figure 2: **CoolRunner-II CPLD Function Block**

At the high level, the product terms (p-terms) reside in a programmable logic array (PLA). This structure is extremely flexible, and very robust when compared to fixed or cascaded product term FBs.

Classic CPLDs typically have a few product terms available for a high-speed path to a given macrocell. They rely on capturing unused p-terms from neighboring macrocells to expand their product term tally, when needed. The result of this architecture is a variable timing model and the possibility of stranding unusable logic within the FB.

The PLA is different — and better. First, any product term can be attached to any OR gate inside the FB macrocell(s). Second, any logic function can have as many p-terms as needed attached to it within the FB, to an upper limit of 56. Third, product terms can be re-used at multiple macrocell OR functions so that within a FB, a particular logical product need only be created once, but can be re-used up to 16 times within the FB. Naturally, this plays well with the fitting software, which identifies product terms that can be shared.

The software places as many of those functions as it can into FBs, so it happens for free. There is no need to force macrocell functions to be adjacent or any other restriction save residing in the same FB, which is handled by the software. Functions need not share a common clock, common set/reset, or common output enable to take full advantage of the PLA. Also, every product term arrives with the same time delay incurred. There are no cascade time adders for putting more product terms in the FB. When the FB product term budget is reached, there is a small interconnect timing penalty to route signals to another FB to continue creating logic. Xilinx design software handles all this automatically.

Macrocell

The CoolRunner-II CPLD macrocell is extremely efficient and streamlined for logic creation. Users can develop sum of product (SOP) logic expressions that comprise up to 40 inputs and span 56 product terms within a single function block. The macrocell can further combine the SOP expression into an XOR gate with another single p-term expression. The resulting logic expression's polarity is also selectable. As well, the logic function can be pure combinatorial or registered, with the storage element operating selectably as a D or T flip-flop, or transparent latch. Available at each macrocell are independent selections of global, function block level or local p-term derived clocks, sets, resets, and output enables. Each macrocell flip-flop is configurable for either single edge or DualEDGE clocking, providing either double data rate capability or the ability to distribute a slower clock (thereby saving power). For single edge clocking or latching, either clock polarity can be selected per macrocell. CoolRunner-II CPLD macrocell details are shown in Figure 3. Note that in Figure 4, standard logic symbols are used except the trapezoidal multiplexers have input selection from statically programmed configuration select lines (not shown). Xilinx application note XAPP376 gives a detailed explanation of how logic is created in the CoolRunner-II CPLD family.

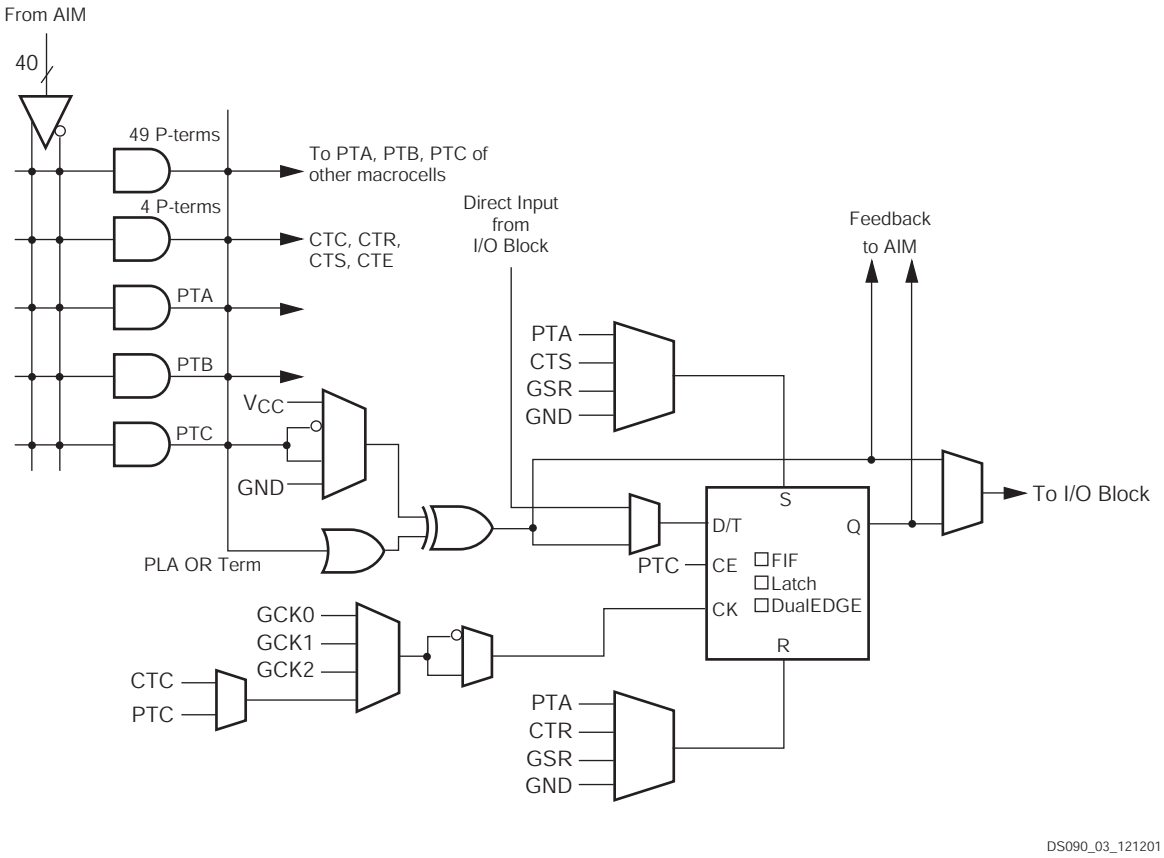

Figure 3: **CoolRunner-II CPLD Macrocell**

When configured as a D-type flip-flop, each macrocell has an optional clock enable signal permitting state hold while a clock runs freely. Note that Control Terms (CT) are available to be shared for key functions within the FB, and are generally used whenever the exact same logic function would be repeatedly created at multiple macrocells. The CT product terms are available for FB clocking (CTC), FB asynchronous set (CTS), FB asynchronous reset (CTR), and FB output enable (CTE).

Any macrocell flip-flop can be configured as an input register or latch, which takes in the signal from the macrocell's I/O pin, and directly drives the AIM. The macrocell combinational functionality is retained for use as a buried logic node if needed. F_{Toggle} is the maximum clock frequency to which a T flip-flop can reliably toggle.

Advanced Interconnect Matrix (AIM)

The Advanced Interconnect Matrix is a highly connected low power rapid switch. The AIM is directed by the software to deliver up to a set of 40 signals to each FB for the creation of logic. Results from all FB macrocells, as well as, all pin inputs circulate back through the AIM for additional connection available to all other FBs as dictated by the design

software. The AIM minimizes both propagation delay and power as it makes attachments to the various FBs.

I/O Block

I/O blocks are primarily transceivers. However, each I/O is either automatically compliant with standard voltage ranges or can be programmed to become so. See **XAPP382** for detailed information on CoolRunner-II I/Os.

In addition to voltage levels, each input can selectively arrive through Schmitt-trigger inputs. This adds a small time delay, but substantially reduces noise on that input pin. Approximately 500 mV of hysteresis is added when Schmitt-trigger inputs are selected. All LVCMOS inputs can have hysteresis input. Hysteresis also allows easy generation of external clock circuits. The Schmitt-trigger path is best seen in Figure 4. See Table 5 for Schmitt-trigger compatibility with I/O standards.

Outputs can be directly driven, 3-stated or open-drain configured. A choice of slow or fast slew rate output signal is also available. Table 5 summarizes various supported voltage standards associated with specific part capacities. All inputs and disabled outputs are voltage tolerant up to 3.3V.

The CoolRunner-II family supports SSTL2-1, SSTL3-1 and HSTL-1 high-speed I/O standards in the 128-macrocell and larger devices. Figure 4 details the I/O pin, where it is noted that the inputs requiring comparison to an external reference voltage are available. These I/O standards all require V_{REF} pins for proper operation. The CoolRunner-II CPLD allows any I/O pin to act as a V_{REF} pin, granting the board layout engineer extra freedom when laying out the pins. However, if V_{REF} pin placement is not done properly, additional V_{REF} pins might be required, resulting in a loss of potential I/O pins or board re-work. See **XAPP399** for details regarding V_{REF} pins and their placement.

V_{REF} has pin-range requirements that must be observed. The Xilinx software aids designers in remaining within the proper pin range.

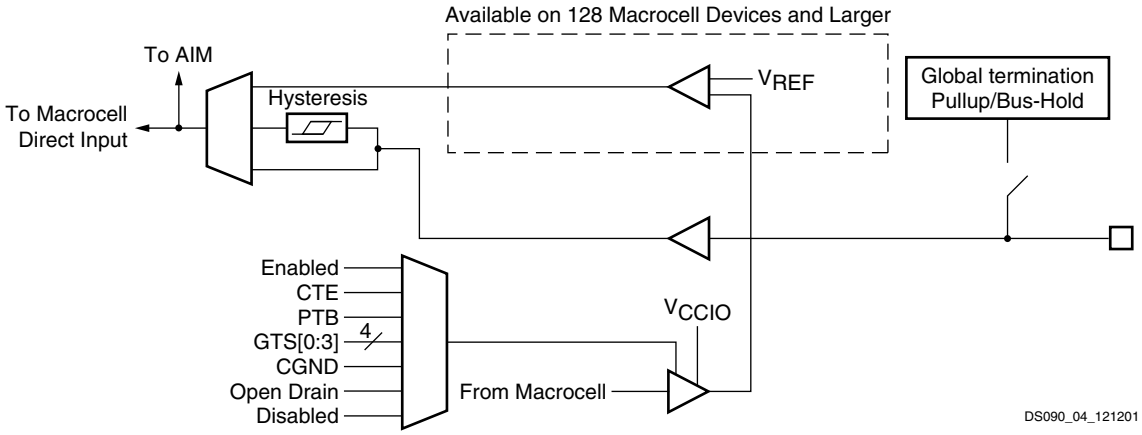

Figure 4: **CoolRunner-II CPLD I/O Block Diagram**

Table 5 summarizes the single ended I/O standard support and shows which standards require V_{REF} values and board termination. V_{REF} detail is given in specific data sheets.

Table 5: **CoolRunner-II CPLD I/O Standard Summary**

IOSTANDARD Attribute	V_{CCIO}	Input V_{REF}	Board Termination Voltage (V_{TT})	Schmitt-trigger Support
LVTTL	3.3	N/A	N/A	Optional
LVCMOS33	3.3	N/A	N/A	Optional
LVCMOS25	2.5	N/A	N/A	Optional
LVCMOS18	1.8	N/A	N/A	Optional
LVCMOS15	1.5	N/A	N/A	Not optional
HSTL_1	1.5	0.75	0.75	Not optional
SSTL2_1	2.5	1.25	1.25	Not optional
SSTL3_1	3.3	1.5	1.5	Not optional

Output Banking

CPLDs are widely used as voltage interface translators. To that end, the output pins are grouped in large banks. The XC2C32A, XC2C64A, XC2C128 and XC2C256 devices support two output banks. With two, the outputs switch to one of two selected output voltage levels, unless both banks are set to the same voltage. The larger parts (384 and 512 macrocell) support four output banks split evenly. They can support groupings of one, two, three, or four separate output voltage levels. This kind of flexibility permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V in a single part.

DataGATE

Low power is the hallmark of CMOS technology. Other CPLD families use a sense amplifier approach to creating product terms, which always has a residual current component being drawn. This residual current can be several hundred milliamps, making them unusable in portable systems. CoolRunner-II CPLDs use standard CMOS methods to create the CPLD architecture and deliver the corresponding low current consumption, without doing any special tricks. However, sometimes designers want to reduce their system current even more by selectively disabling circuitry not being used.

The patented DataGATE technology to permits a straightforward approach to additional power reduction. Each I/O pin has a series switch that can block the arrival of free running signals that are not of interest. Signals that serve no use might increase power consumption, and can be disabled. Users are free to do their design, then choose sections to participate in the DataGATE function. DataGATE is a logic function that drives an assertion rail threaded through the medium and high-density CoolRunner-II CPLD parts. Designers can select inputs to be blocked under the control of the DataGATE function, effectively blocking controlled switching signals so they do not drive internal chip capacitances. Output signals that do not switch are held by the bus hold feature. Any set of input pins can be chosen to participate in the DataGATE function. Figure 5 shows the familiar CMOS I_{CC} versus switching frequency graph. With DataGATE, designers can approach zero power, should they choose to, in their designs.

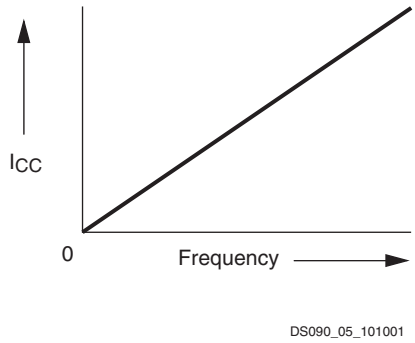

Figure 5: **CMOS I_{CC} vs. Switching Frequency Curve**

Figure 6 shows how DataGATE basically works. One I/O pin drives the DataGATE Assertion Rail. It can have any desired logic function on it. It can be as simple as mapping an input pin to the DataGATE function or as complex as a counter or state machine output driving the DataGATE I/O pin through a macrocell. When the DataGATE rail is asserted High, any pass transistor switch attached to it is blocked. Each pin has the ability to attach to the AIM through a DataGATE pass transistor, and thus be blocked. A latch automatically captures the state of the pin when it becomes blocked. The DataGATE Assertion Rail threads throughout all possible I/Os, so each can participate if chosen. Note that one macrocell is singled out to drive the rail, and that macrocell is exposed to the outside world through a pin, for inspection. If DataGATE is not needed, this pin is an ordinary I/O.

There are two attributes associated with the DataGATE feature in CoolRunner-II CPLDs. The first attribute specifies if an input is affected by DataGATE and the second designates the DataGATE control signal.

The DataGATE feature is selectable on a per pin basis. Each input pin that uses DataGATE must be assigned a DATA_GATE attribute.

The DataGATE assertion rail can be driven from either an I/O pin or internal logic. The DataGATE enable signal is a dedicated DGE/I/O pin for each package in CoolRunner-II CPLDs. Upon implementation, the software recognizes a design using DataGATE and automatically assigns this I/O pin to the DataGATE enable control function, DGE. Inter-

nally generated DataGATE control logic can be assigned to this I/O pin with the BUFG=DATA_GATE attribute.

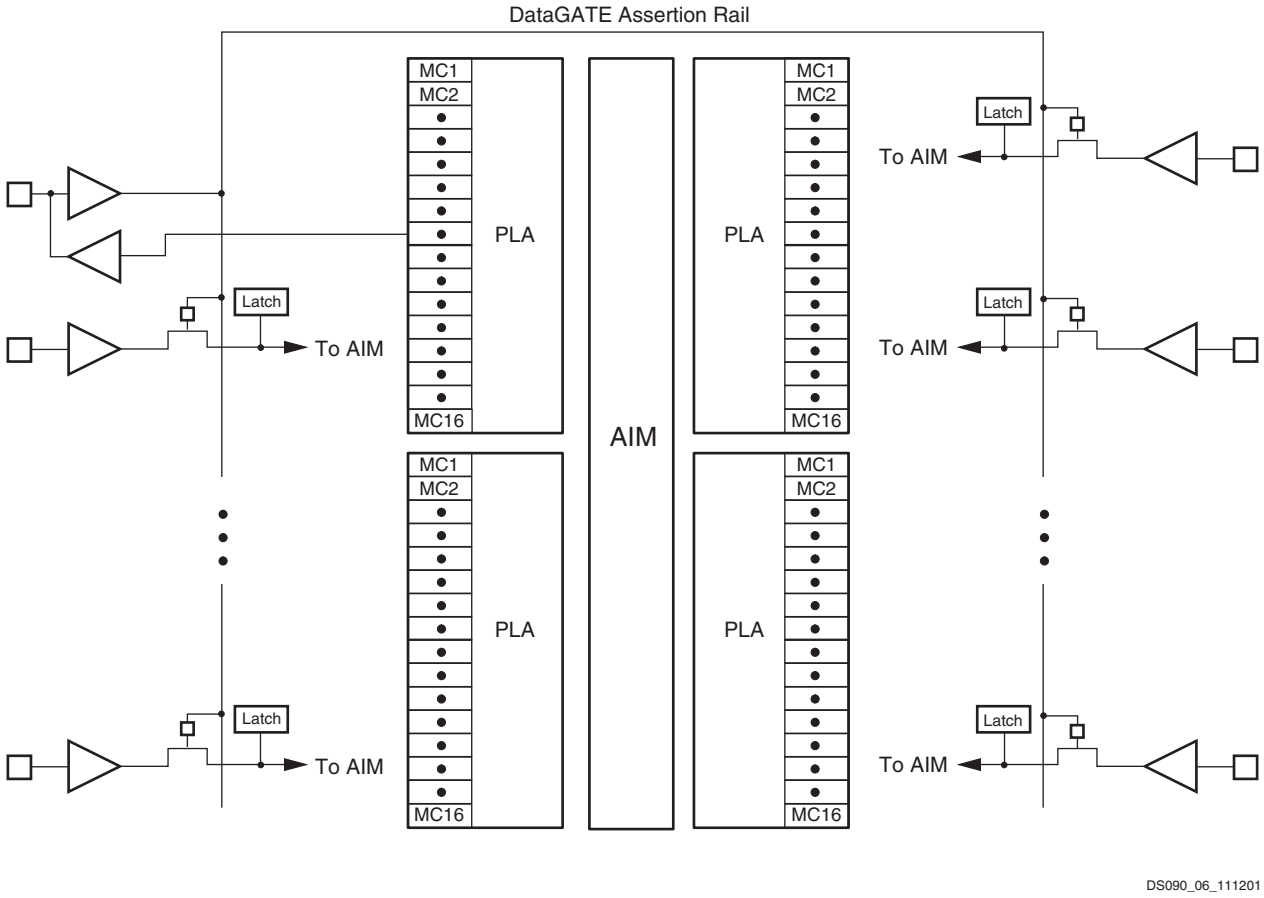

Figure 6: **DataGATE Architecture (output drivers not shown)**

Global Signals

Global signals, clocks (GCK), sets/resets (GSR), and output enables (GTS), are designed to strongly resemble each other. This approach enables design software to make the best utilization of their capabilities. Each global capability is supplemented by a corresponding product term version. Figure 7 shows the common structure of the global signal trees. The pin input is buffered, then drives multiple internal global signal traces to deliver low skew and reduce loading delays. GCK, GSR, and GTS can also be used as general purpose I/Os if they are not needed as global signals. The DataGATE assertion rail is also a global signal.

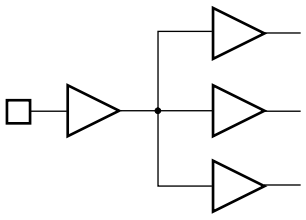

Figure 7: **Global Clocks (GCK), Sets/Resets (GSR), and Output Enables (GTS)**

Additional Clock Options: Division, DualEDGE, and CoolCLOCK

Clock Divider

A clock divider circuit has been included in the CoolRunner-II CPLD architecture to divide one externally supplied global clock by standard values. The allowable values for the division are 2, 4, 6, 8, 10, 12, 14, and 16 (see Figure 8). This capability is supplied on the GCK2 pin. The resulting clock produced has a 50% duty cycle for all possible divisions. The output of the clock divider is on global routing. If the clock divider is used, the undivided clock is available internally. If the undivided clock is required internally it is input through a separate clock pin.

The clock divider circuit encompasses a synchronous reset (CDRST) to guarantee no spurious clocks can carry through on to the global clock nets. When the CDRST signal is asserted, the clock divider output is disabled after the current cycle. When the CDRST signal is deasserted the clock divider output becomes active upon the first edge of GCK2. The CDRST pin functions as a reset pin regardless of which CLK_DIV primitive is used. If a clock divider is used in the design, the CDRST pin is reserved and if it is driven High the clock divider is reset. If a reset port of a clock divider is not used, it is tied Low on the board. The clock divider circuit includes an active High synchronous reset, referred to as CDRST.

The CoolRunner-II CPLD clock divider includes a built-in delay circuit. With the delay feature enabled, the output of the clock divider is delayed for one full count cycle. When used, the clock divider does not output a rising clock edge until after the divider reaches the delay value. The delay feature is either enabled or disabled upon configuration.

Xilinx Synthesis Technology (XST) allows a clock divider component to be instantiated directly in the HDL source code. See **XAPP378** for instantiation examples in VHDL, Verilog, and ABEL.

DualEDGE

Each macrocell has the ability to double its input clock switching frequency. Figure 9 shows the macrocell flip-flop with the DualEDGE option (doubled clock) at each macrocell. The source to double can be a control term clock, a product term clock or one of the available global clocks. The ability to switch on both clock edges, also known as dual edge triggered (DET), is vital for a number of synchronous memory interface applications as well as certain double data rate I/O applications.

CoolRunner-II CPLD DET registers can be used for logic functions that include shift registers, counters, comparators, and state machines. Designers must evaluate the desired performance of the CPLD logic to determine use of DET registers.

The DET register can be inferred in any ABEL, HDL, or schematic design. A designer can infer a single-edge triggered (SET) register in any HDL design. The DET register is available with all macrocells in all devices of the CoolRunner-II family.

CoolCLOCK

In addition to the DualEDGE flip-flop, power savings can occur by combining the clock division circuitry with the DualEDGE circuitry. This capability is called CoolCLOCK and is designed to reduce clocking power within the CPLD. Because the clock net can be an appreciable power drain, the clock power can be reduced by driving the net at half frequency, then doubling the clock rate using DualEDGE triggering at the macrocells. Figure 10 shows how CoolCLOCK is created by internal clock cascading with the divider and DualEDGE flip-flop working together.

GCK2 is the only clock network that can be divided, the CoolCLOCK feature is only available on GCK2. The CoolCLOCK feature can be implemented by assigning an attribute to an input clock. The CoolCLOCK attribute replaces the need to instantiate the clock divider and infer DET registers. The CoolCLOCK feature is available on CoolRunner-II 128 macrocell devices and larger. See **XAPP378** for more detail.

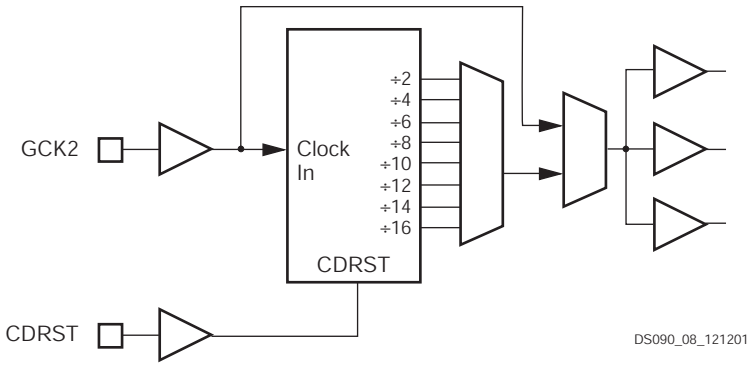

Figure 8: **Clock Division Circuitry for GCK2**

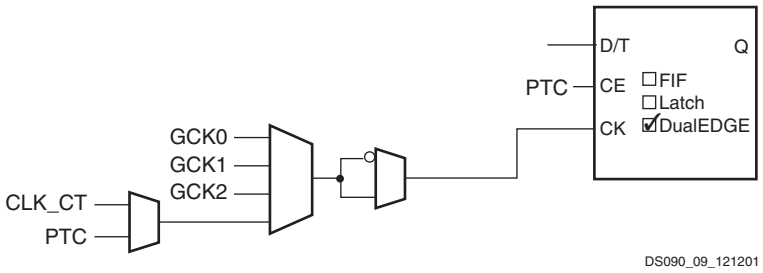

Figure 9: **Macrocell Clock Chain with DualEDGE Option Shown**

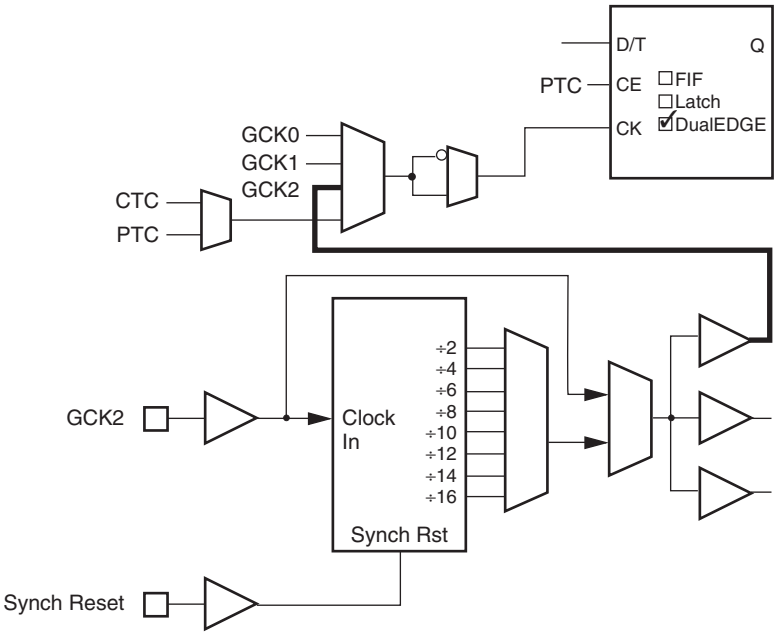

Figure 10: **CoolCLOCK Created by Cascading Clock Divider and DualEDGE Option**

Design Security

Designs can be secured during programming to prevent either accidental overwriting or pattern theft via readback. Four independent levels of security are provided on-chip, eliminating any electrical or visual detection of configuration patterns. These security bits can be reset only by erasing the entire device. See **WP170** for more detail.

Timing Model

Figure 11 shows the CoolRunner-II CPLD timing model. It represents one aspect of the overall architecture from a timing viewpoint. Each little block is a time delay that a signal incurs if the signal passes through such a resource. Timing reports are created by tallying the incremental signal delays as signals progress within the CPLD. Software creates the timing reports after a design has been mapped onto the specific part, and knows the specific delay values for a given speed grade. Equations for the higher level timing values (i.e., T_{PD} and F_{SYSTEM}) are available. Table 6 summarizes the individual parameters and provides a brief definition of their associated functions. Xilinx application note XAPP375 details the CoolRunner-II CPLD family timing with several examples.

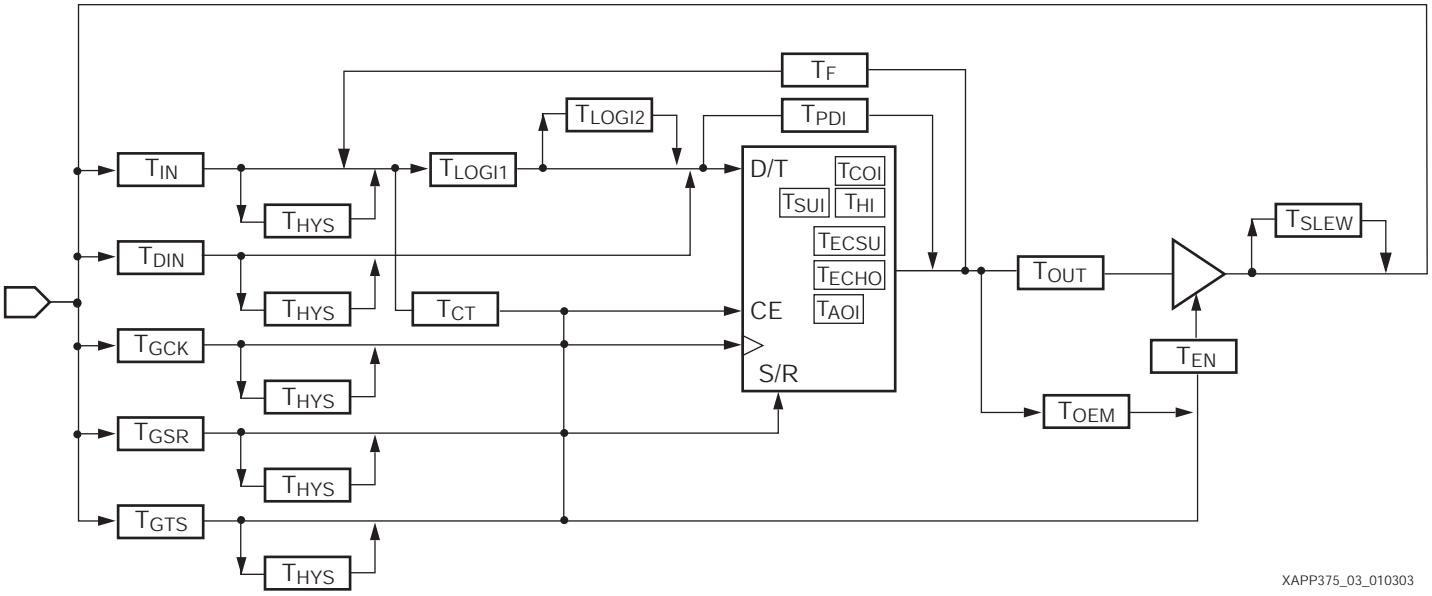

Figure 11: **CoolRunner-II CPLD Timing Model**

Note: Always refer to the timing report in ISE Software for accurate timing values for paths.

Table 6: **Timing Parameter Definitions**

Symbol	Parameter
Buffer Delays	
T_{IN}	Input Buffer Delay
T_{DIN}	Direct data register input delay
T_{GCK}	Global clock (GCK) buffer delay
T_{GSR}	Global set/reset (GSR) buffer delay
T_{GTS}	Global output enable (GTS) buffer delay
T_{OUT}	Output buffer delay
T_{EN}	Output buffer enable/disable delay
T_{SLEW}	Output buffer slew rate control delay
P-term Delays	
T_{CT}	Control Term delay (single PT or FB-CT)
T_{LOGI1}	Single P-term logic delay
T_{LOGI2}	Multiple P-term logic delay adder

Table 6: **Timing Parameter Definitions *(Continued)***

Symbol	Parameter
Macrocell Delays	
T_{PDI}	Macrocell input to output valid
T_{SUI}	Macro register setup before clock
T_{HI}	Macro register hold after clock
T_{ECSU}	Macro register enable clock setup time
T_{ECHO}	Macro register enable clock hold time
T_{COI}	Macro register clock to output valid
T_{AOI}	Macro register set/reset to output valid
T_{HYS}	Hysteresis selection delay adder
Feedback Delays	
T_F	Feedback delay
T_{OEM}	Macrocell to Global OE delay

Programming

The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. See **CoolRunner-II CPLD Application Notes** for more information on how to program.

In System Programming

All CoolRunner-II CPLD parts are 1.8V in system programmable. This means they derive their programming voltage and currents from the 1.8V V_{CC} (internal supply voltage) pins on the part. The V_{CCIO} pins do not participate in this operation, as they might assume another voltage ranging as high as 3.3V down to 1.5V (however, all V_{CCIO}, V_{CCINT}, V_{CCAUX}, and GND pins must be connected for the device to be programmed, and operate correctly). A 1.8V V_{CC} is required to properly operate the internal state machines and charge pumps that reside within the CPLD to do the nonvolatile programming operations. I/O pins are not in user mode during JTAG programming; they are held in 3-state with a weak pullup. The JTAG interface buffers are powered by a dedicated power pin, V_{CCAUX}, which is independent of all other supply pins. V_{CCAUX} must be connected. Xilinx software is provided to deliver the bitstream to the CPLD and drive the appropriate IEEE 1532 protocol. To that end, there is a set of IEEE 1532 commands that are supported in the CoolRunner-II CPLD parts. Programming times are less than one second for 32 to 256 macrocell parts. Programming times are less than four seconds for 384 and 512 macrocell parts. Programming of CoolRunner-II CPLDs is only guaranteed when operating in the commercial temperature and voltage ranges as defined in the device-specific data sheets.

On-The-Fly Reconfiguration (OTF)

The Xilinx ISE 5.2i tool supports OTF for CoolRunner-II CPLDs. This permits programming a new nonvolatile pattern into the part while another pattern is currently in use. OTF has the same voltage and temperature specifications as system programming. During pattern transition I/O pins are in high impedance with a weak pullup to V_{CCIO}. Transition time typically lasts between 50 and 300 µs, depending on density. See **XAPP388** for more information.

JTAG Instructions

Table 7 shows the commands available to users. These same commands can be used by third party ATE products, as well. The internal controllers can operate as fast as 66 MHz.

Table 7: **JTAG Instructions**

Code	Instruction	Description
00000000	EXTEST	Force boundary scan data onto outputs
00000011	PRELOAD	Latch macrocell data into boundary scan cells
11111111	BYPASS	Insert bypass register between TDI and TDO
00000010	INTEST	Force boundary scan data onto inputs and feedbacks
00000001	IDCODE	Read IDCODE
11111101	USERCODE	Read USERCODE
11111100	HIGHZ	Force output into high impedance state
11111010	CLAMP	Latch present output state

Power-Up Characteristics

CoolRunner-II CPLD parts must operate under the demands of both the high-speed and the portable market places; therefore, they must support hot plugging for the high-speed world and tolerate most any power sequence to its various voltage pins. They must also not draw excessive current during power-up initialization. To those ends, the general behavior is summarized as follows:

1. I/O pins are disabled until the end of power-up.
2. As supply rises, configuration bits transfer from nonvolatile memory to SRAM cells.
3. As power up completes, the outputs become as configured (input, output, or I/O).
4. For specific configuration times and power up requirements, see **XAPP389**.

CoolRunner-II CPLD I/O pins are well behaved under all operating conditions. During power-up, CoolRunner-II devices employ internal circuitry which keeps the devices in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 1.3V). In the quiescent state, JTAG pins are disabled, and all device outputs are disabled with the pins weakly pulled High, as shown in Table 8. When the supply voltage reaches a safe level, all user registers become initialized, and the device is immediately available for operation, as shown in Figure 12. Best results are obtained with a smooth V_{CC} rise in less than 4 ms. Final V_{CC} value should occur within 1 second.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with a weak pull-up. The JTAG pins are enabled to allow the device

to be programmed at any time. All devices are shipped in the erased state from the factory.

Applying power to a blank part might result in a higher current flow as the part initializes. This behavior is normal and might persist for approximately 2 seconds, depending on the power supply ramp.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

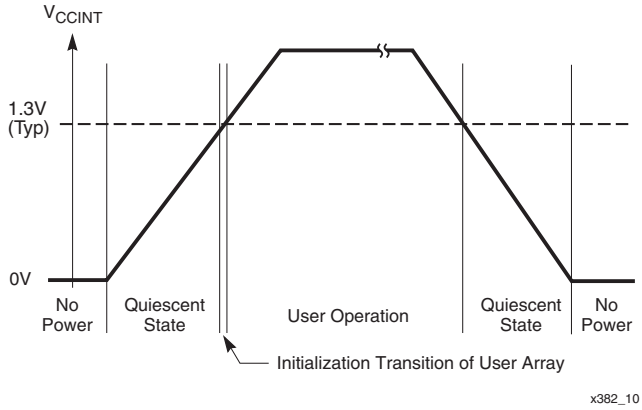

Figure 12: **Device Behavior During Power Up**

Table 8: **I/O Power-Up Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold/Weak Pullup	Weak Pull-up	Weak Pull-up	Bus-Hold/Weak Pullup
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

I/O Banking

CoolRunner-II CPLD XC2C32A and XC2C64A macrocell parts support two V_{CCIO} rails that can range from 3.3V down to 1.5V operation. Two V_{CCIO} rails are supported on the 128 and 256 macrocell parts where outputs on each rail can independently range from 3.3V down to 1.5V operation. Four V_{CCIO} rails are supported on the 384 and 512 macrocell parts. Any of the V_{CCIO} rails can assume any one of the V_{CCIO} values of 1.5V, 1.8V, 2.5V, or 3.3V. Designers should assign input and output voltages to a bank with V_{CCIO} set at the voltage range of that input or output voltage. The V_{CC} (internal supply voltage) for a CoolRunner-II CPLD must be maintained within 1.8V ±5% for correct speed operation and proper in system programming.

Mixed Voltage, Power Sequencing, and Hot Plugging

As mentioned in I/O Banking, CoolRunner-II CPLD parts support mixed voltage I/O signals. It is important to assign signals to an I/O bank with the appropriate I/O voltage. Driving a high voltage into a low voltage bank can result in negative current flow through the power supply pins. The power applied to the V_{CCIO} and V_{CC} pins can occur in any order and the CoolRunner-II CPLD will not be damaged. For best results, Xilinx recommends that V_{CCINT} be applied before V_{CCIO} To ensure that the internal logic is correct before the I/Os are active. CoolRunner-II CPLDs can reside on boards where the board is inserted into a “live” connector (hot plugged) and the parts will be well-behaved as if powering up in a standard way.

Development System Support

Xilinx CoolRunner-II CPLDs are supported by all configurations of Xilinx standard release development software as well as the freely available ISE WebPACK software available from www.xilinx.com. Third party development tools include synthesis tools from Cadence, Exemplar, Mentor Graphics, Synplicity, and Synopsys.

ATE Support

Third party ATE development support is available for both programming and board/chip level testing. Vendors providing this support include Agilent, GenRad, and Teradyne. Other third party providers are expected to deliver solutions in the future.

Absolute Maximum Ratings

Symbol	Parameter[1]	Min.	Max.	Unit
V_{CC}[2]	Supply voltage relative to GND	–0.5	2.0	V
V_I[3]	Input voltage relative to GND	–0.5	4.0	V
T_A	Ambient Temperature (C-grade)	0	70	°C
	Ambient Temperature (I-grade)	–40	85	°C
T_J[4]	Maximum junction temperature	–40	150	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:
1. Stresses above those listed might cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage should rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins might undershoot to –2.0V or overshoot to 4.5 V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. The I/O voltage can never exceed 4.0V.
4. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Quality and Reliability Parameters

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic discharge(1)	2,000	-	Volts

Notes:
1. ESD is measured to 2000V using the human body model. Pins exposed to this limit can incur additional leakage current to a maximum of 10 µA when driven to 3.9V.

Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT **http://www.xilinx.com/warranty.htm**. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Further Reading

Application Notes

http://www.xilinx.com/support/documentation/application_notes/xapp784.pdf
(Bulletproof Design Practices)

http://www.xilinx.com/support/documentation/application_notes/xapp375.pdf (Timing Model)

http://www.xilinx.com/support/documentation/application_notes/xapp376.pdf (Logic Engine)

http://www.xilinx.com/support/documentation/application_notes/xapp317.pdf
(Power Evaluation Equation for CoolRunner-II CPLDs)

http://www.xilinx.com/support/documentation/application_notes/xapp377.pdf (Low Power Design)

http://www.xilinx.com/support/documentation/application_notes/xapp378.pdf (Advanced Features)

http://www.xilinx.com/support/documentation/application_notes/xapp379.pdf (High Speed Design)

http://www.xilinx.com/support/documentation/application_notes/xapp380.pdf (Cross Point Switch)

http://www.xilinx.com/support/documentation/application_notes/xapp381.pdf (Demo Board)

http://www.xilinx.com/support/documentation/application_notesxapp382.pdf (I/O Characteristics)

http://www.xilinx.com/support/documentation/application_notes/xapp383.pdf (Single Error Correction Double Error Detection)

http://www.xilinx.com/support/documentation/application_notes/xapp384.pdf (DDR SDRAM Interface)

http://www.xilinx.com/support/documentation/application_notes/xapp387.pdf (PicoBlaze Microcontroller)

http://www.xilinx.com/support/documentation/application_notes/xapp388.pdf (On the Fly Reconfiguration)

http://www.xilinx.com/support/documentation/application_notes/xapp389.pdf (Powering CoolRunner-II)

http://www.xilinx.com/support/documentation/application_notes/xapp393.pdf (8051 Microcontroller Interface)

http://www.xilinx.com/support/documentation/application_notes/xapp394.pdf (Interfacing with Mobile SDRAM)

http://www.xilinx.com/support/documentation/application_notes/xapp399.pdf (Assigning CoolRunner-II VREF Pins)

CoolRunner-II CPLD Data Sheets

http://www.xilinx.com/support/documentation/data_sheets/ds090.pdf (CoolRunner-II Family Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds310.pdf (XC2C32A Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds311.pdf (XC2C64A Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds093.pdf (XC2C128 Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds094.pdf (XC2C256 Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds095.pdf (XC2C384 Data Sheet)

http://www.xilinx.com/support/documentation/data_sheets/ds096.pdf (XC2C512 Data Sheet)

CoolRunner-II CPLD White Papers

http://www.xilinx.com/support/documentation/white_papers/wp170.pdf (Secure Applications)

Packages

Package Drawings

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/03/02	1.0	Initial Xilinx release
07/04/02	1.1	Revisions and updates
07/24/02	1.2	Revisions and updates
09/24/02	1.3	Additions to "Power Characteristics" section
01/28/03	1.4	Addition of the "Further Reading" section
02/26/03	1.5	Multiple minor revisions
03/12/03	1.6	Minor revision to "Quality and Reliability Parameters"
10/09/03	1.7	Update Hewlett-Packard to Agilent, OFR to OTF, and other revisions
01/26/04	1.8	Incorporate links to Data Sheets, Application Notes, and Device Packages
02/26/04	1.9	Change to Power-Up Characteristics, page 11. Change T_{FIN} to T_{DIN}. Add Schmitt-trigger I/O compatibility information. Added T_{SOL} specification.
05/21/04	2.0	Add XC2C32A and XC2C64A devices.
07/30/04	2.1	Pb-free documentation. Changes to T_{SU} and F_{system} to match individual data sheets.
01/10/05	2.2	Added information about programming options, page 11.
03/07/05	2.3	Changes to Table 1, T_{PD}, T_{SU}, T_{CO}, and $F_{SYSTEM1}$. Removed link to obsolete White Paper. Modifications to Table 5, IOSTANDARDs. Added Table 2, DC Characteristics.

Date	Version	Revision
04/15/05	2.4	Change to $F_{SYSTEM1}$ for XC2C128.
06/28/05	2.5	Move to Product Specification
03/20/06	2.6	Add Warranty Disclaimer; modified Global Signals section to say that GCK, GSR and GTS can be used as general purpose I/O.
07/24/06	2.7	Change to Hot Plugging recommendations, page 13 (V_{CCINT} before V_{CCIO} power sequencing).
12/7/06	2.8	Add description of I/O pin status during JTAG programming, page 12. Add note about power pins during programming. Add link to application note 389, page 12. Added clarification to clock divider description, page 9.
02/15/07	2.9	Add greater description to advanced features. Added Ambient Temperature specification.
03/08/07	3.0	Add link to power estimation appnote, page 14.
09/11/08	3.1	Removed reference to XC2C32 and XC2C64 devices. See Product Discontinuation Notice **xcn05017.pdf**. Removed references to PC44 and PCG44 packages. See Product Discontinuation Notice **xcn07022.pdf**.

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