THE DATASHEET OF

A8500EECTR-T

ALLEGRO microsystems

A8500

Flexible WLED/RGB Backlight Driver for Medium Size LCDs

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: April 1, 2024

Deadline for receipt of LAST TIME BUY orders: July 31, 2024

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

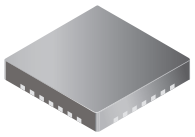
Flexible WLED/RGB Backlight Driver for Medium Size LCDs

FEATURES AND BENEFITS

- Active current sharing between LED strings for ±1.5% typical current matching and ±1.2% typical accuracy
- Drive up to 12 series × 8 parallel = 96 LEDs (V_f = 3.2 V, I_f = 20 mA)
- Flexible dimming, using alternative methods:
  - LED duty cycle control (PWM pin)
  - DC current using serial programming (EN pin)
  - DC current using external PWM signal (APWM pin)
  - An external resistor
- Boost converter with integrated 50 V, 2 A DMOS
- LED sinks rated for 25 mA
- 200 kHz to 2 MHz switching frequency
- Open LED disconnect
- Boost current limit, thermal shutdown, and soft start
- No audible ceramic capacitor noise during PWM dimming
- Adjustable overvoltage protection (OVP)
- No pull-up resistors required for LED modules that use ESD capacitors

PACKAGE: 26 pin QFN/MLP (suffix EC)

Approximate Scale 1:1



DESCRIPTION

The A8500 is a multi-output WLED driver for medium display backlighting. The A8500 integrates a boost converter and eight current-sinks to provide a flexible WLED/RGB backlight driver. The boost converter can provide output voltage up to 47 V. The flexible channel selection control and high voltage capability allow a wide range of LED backlight applications. The A8500 can support any application requiring 4 to 96 WLEDs. The boost converter is a constant frequency current-mode converter.

Each LED channel can sink 25 mA, and channels can be paralleled for higher currents. Flexible dimming allows output channels to either run at an adjustable DC value or with externally controlled PWM duty cycles.

The A8500 is available in a 26 pin, 4 mm × 4 mm QFN/MLP package that is only 0.75 mm nominal in height. Applications include:

- Thin notebook displays
- LCD TV
- RGB backlight
- GPS systems
- Portable DVD players

Typical Application

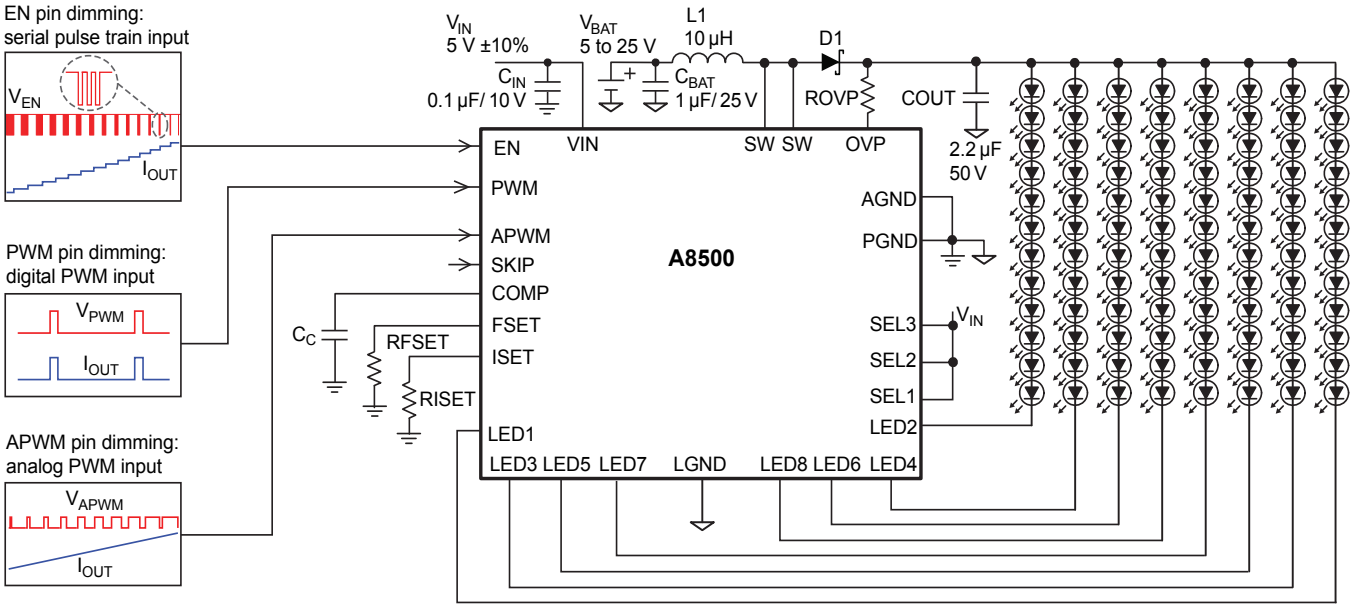


Figure 1. LCD monitor backlight, driving 96 LEDs. LED V_f = 3.2 V, 20 mA per LED string. Overvoltage protection set to 45 V nominal (40.5 V minimum). Alternative dimming control pulse trains illustrated for EN, PWM, and APWM control. See also: Recommended Components table, page 14.

Selection Guide

Part Number	Ambient Temperature, T_A	Package	Packing*
A8500EECTR-T	–40 to 85	4 mm × 4 mm QFN/MLP	1500 pieces / 7-in. reel
A8500GECTR-T	–40 to 105		

*Contact Allegro for additional packing options

Device package is lead (Pb) free, with 100% matte tin leadframe plating.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
SW and OVP Pins			–0.3 to 50	V
LED1 through LED8 Pins			–0.3 to 23	V
VIN Pin	V_{IN}		–0.3 to 6	V
Remaining Pins			–0.3 to V_{IN} + 0.3	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range G	–40 to 105	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Package Thermal Characteristics*

Characteristic	Symbol	Note	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Measured on 3 in. × 3 in., 2-layer PCB	48.5	°C/W

*Additional information is available on the Allegro website

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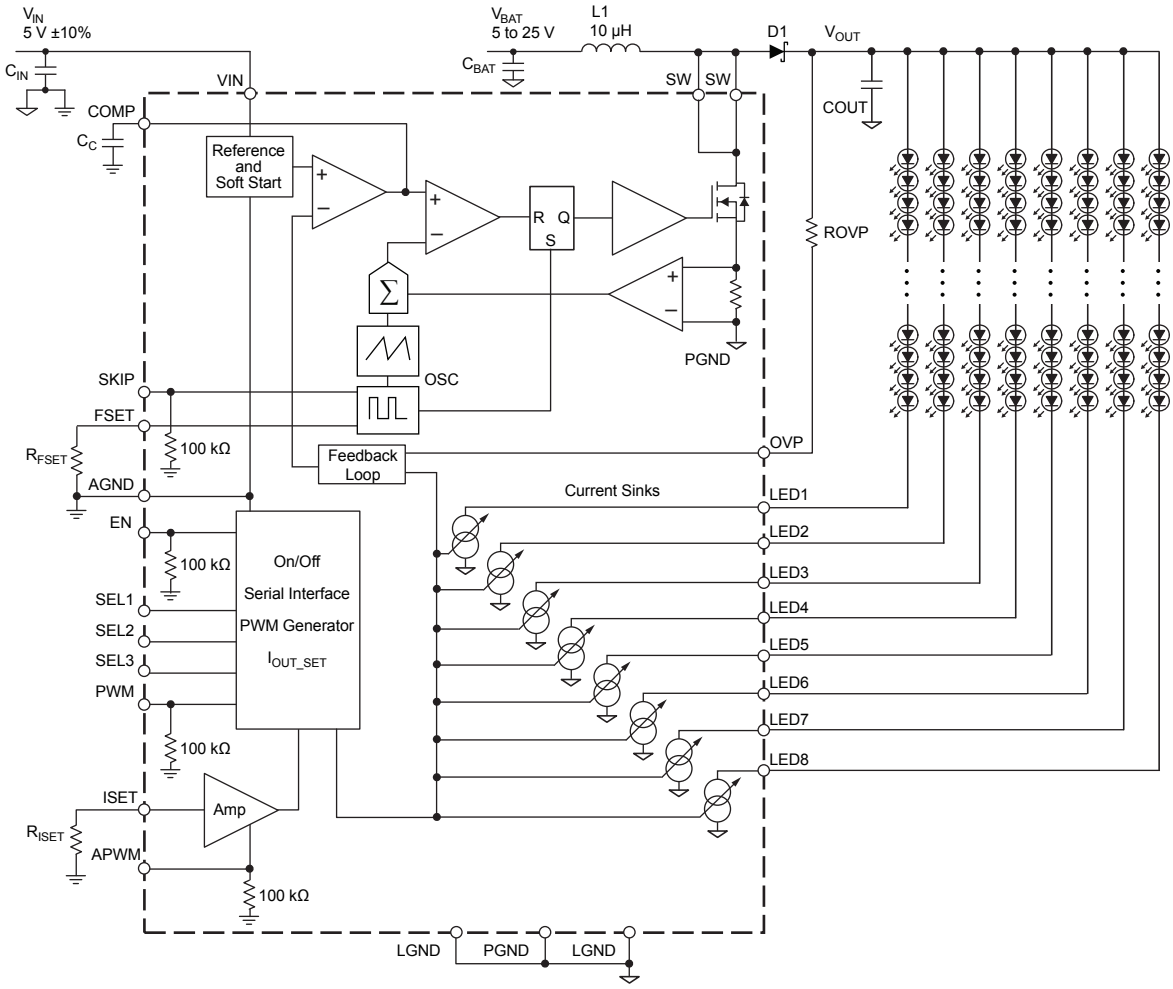
Functional Block Diagram



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ELECTRICAL CHARACTERISTICS, valid at T_A = –40°C to 85°C, typical values at T_A = 25°C, V_{IN} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		4.2	–	5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling	–	–	4	V
UVLO Hysteresis Window	$V_{UVLOhys}$		–	0.2	–	V
Supply Current	I_{SUP}	Switching at no load	–	5	–	mA
		Shutdown EN = PWM = APWM = V_{IL}, T_A = 25°C	–	0.1	1	µA
APWM Frequency Range	f_{APWM}		20	–	2000	kHz
Error Amplifier						
Error Amplifier Open Loop Gain	A_{VEA}		–	60	–	dB
Error Amplifier Unity Gain Bandwidth	UGB_{EA}		–	3	–	MHz
Error Amplifier Transconductance	Gm_{EA}	ΔI_{COMP} = ±10 µA	–	850	–	µA/V
Error Amplifier Output Sink Current	I_{EAsink}	V_{LED1-8} = 1 V	–	280	–	µA
Error Amplifier Output Source Current	$I_{EAsource}$	V_{LED1-8} = 0 V	–	–280	–	µA
Boost Controller						
Switching Frequency	f_{SW}	R_{FSET} = 13 kΩ, SKIP = V_{IL}	1.8	2	2.2	MHz
		R_{FSET} = 26.1 kΩ, SKIP = V_{IL}	–	1	–	MHz
		R_{FSET} = 32.4 kΩ, SKIP = V_{IH}	–	200	–	kHz
Minimum Switch Off-Time	t_{OFFmin}		–	70	–	ns
Logic Input Levels (APWM , EN, MODE, PWM, SEL*x*, and SKIP pins unless otherwise specified)						
Input Voltage Level Low	V_{IL}		–	–	0.4	V
Input Voltage Level High	V_{IH}		1.5	–	–	V
Input Leakage Current (APWM, EN, PWM, and SKIP pins)	I_{Ileak}	$V_{I(pin)}$ = 5 V, T_A = 25°C	–	–	100	µA
Input Leakage Current (SEL*x* pins)	$I_{SELleak}$		–	–	1	µA
Over Voltage Protection (OVP)						
Output Overvoltage Rising Limit	V_{OVP}	ROVP = 0 Ω	28	–	34	V
OVP Sense Current	I_{OVPH}		–	54.9	–	µA
OVP Release Current	I_{OVPL}		–	47.8	–	µA
OVP Leakage Current	$I_{OVPleak}$	V_{VOP} = 21 V	–	0.1	–	µA
Boost Switch						
Switch On Resistance	$R_{ds(on)}$	I_{SW} = 1.5 A	–	225	–	mΩ
Switch Leakage Current	I_{SWleak}	V_{SW} = 5 V, T_A = 25°C	–	–	1	µA
		V_{SW} = 21 V	–	1	–	µA
Switch Current Limit	I_{SWlim}		1.8	2	–	A

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued), valid at T_A = –40°C to 85°C, typical values at T_A = 25°C, V_{IN} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
LED Current Sinks							
LED*x* Regulation Voltage	V_{LEDx}			–	500	–	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 100 µA		–	210	–	–
Voltage on ISET Pin	V_{ISET}			–	1.23	–	V
I_{SET} Allowable Current Range	I_{SET}			40	–	120	µA
LED*x* Accuracy	Err_{LEDx}	R_{ISET} = 12 kΩ; 100% current ratio, measured as average of LED1 to LED8; LED1 to LED8 = 0.5 V		–	±1.2	–	%
LED*x* Matching	Δ_{LEDx}	I_{SET} = 100 µA , 100% current ratio; LED1 to LED8 = 0.5 V		–	±1.5	–	%
LED*x* Switch Leakage Current	$I_{LSleak5}$	V_{LEDx}= 5 V, EN = PWM = APWM = 0, T_A = 25°C		–	–	1	µA
LEDx Switch Leakage Current	$I_{LSleak21}$	V_{LEDx}= 21 V, EN = PWM = APWM=0		–	1	–	µA
Serial Pulse Timing (see figure 4 for further explanation)							
EN Pulse Low Time	t_{LO}			0.5	–	100	µs
EN Pulse High Time	t_{HI}			0.5	–	100	µs
Initial EN or APWM Pulse High Time (relative to switching period)	$t_{HI(init)}$	First EN or APWM pulse after shutdown	SKIP = Low	–	256	–	Switching Pulses
			SKIP = High	–	64	–	Switching Pulses
Level Change Delay (relative to switching period)	t_{HID}		SKIP = Low	–	256	–	Switching Pulses
			SKIP = High	–	64	–	Switching Pulses
Shutdown Delay (relative to switching period on EN or APWM)	t_{SHDN}	Falling edge of EN or APWM pulse	SKIP = Low	–	256	–	Switching Pulses
			SKIP = High	–	64	–	Switching Pulses
Soft Start							
Soft Start Boost Current Limit	I_{SWSS}	Initial soft start current for boost switch		-	1	-	A
Soft Start LED*x* Current Limit	I_{LEDSS}	Current through enabled LED*x* pins during soft start, R_{ISET}=12 kΩ		-	1.25	-	mA
Thermal Shutdown Threshold	T_{SHDN}	40°C hysteresis		–	165	–	°C

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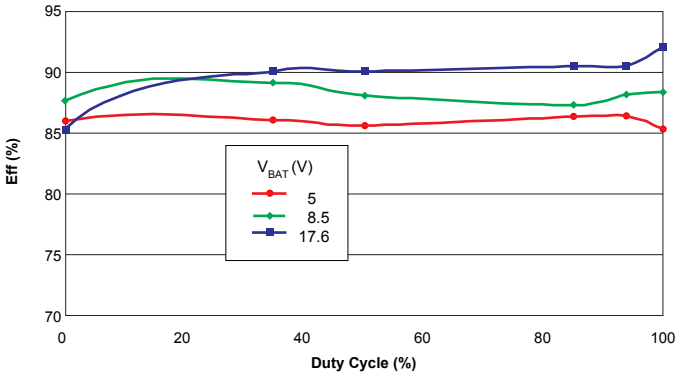
Performance Characteristics

Efficiency with EN dimming is similar to that with APWM dimming. APWM light load efficiency can be improved by reducing boost switching frequency with SKIP set high.

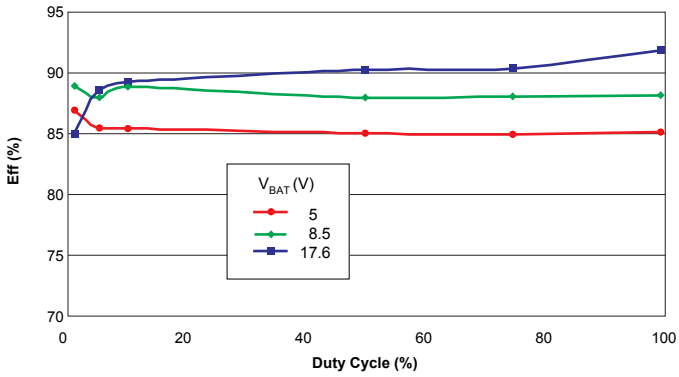
PWM Efficiency

V_{IN}= 5 V, 6 ch. with 7 LEDs per ch., 20 mA per ch., f_{SW} = 1 MHz



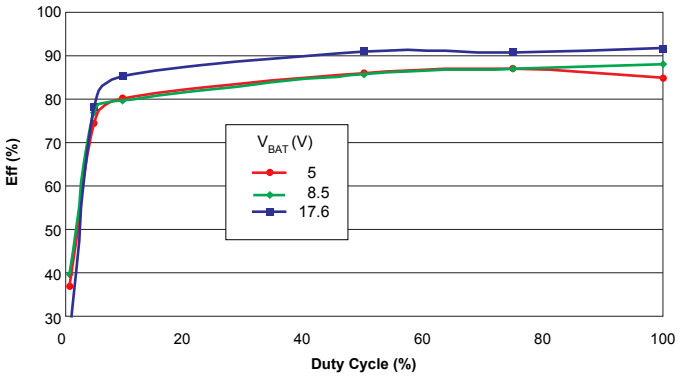
PWM Efficiency

V_{IN}= 5 V, 6 ch. with 7 LEDs per ch., 20 mA per ch., f_{SW} = 2 MHz



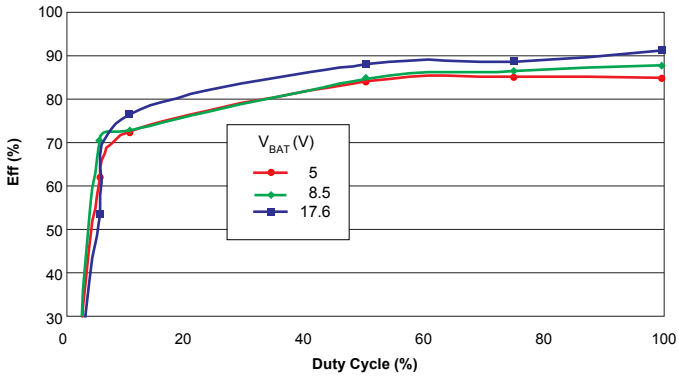
APWM Efficiency

V_{IN}= 5 V, 6 ch. with 7 LEDs per ch., 20 mA per ch., f_{SW} = 1 MHz



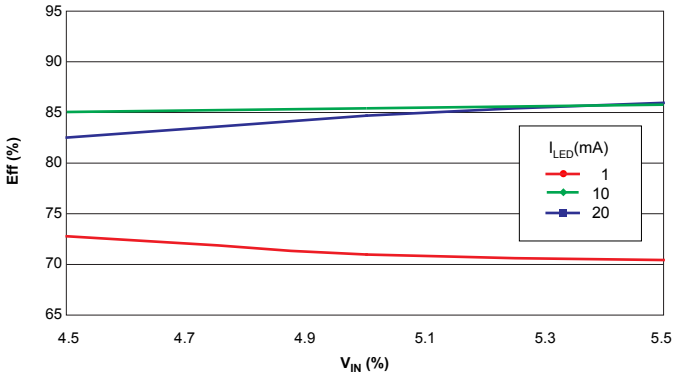
APWM Efficiency

V_{IN}= 5 V, 6 ch. with 7 LEDs per ch., 20 mA per ch., f_{SW} = 2 MHz



Efficiency versus Input Voltage with EN Dimming

V_{IN}= V_{BAT}, 8 ch. with 8 LEDs per ch., f_{SW} = 1 MHz



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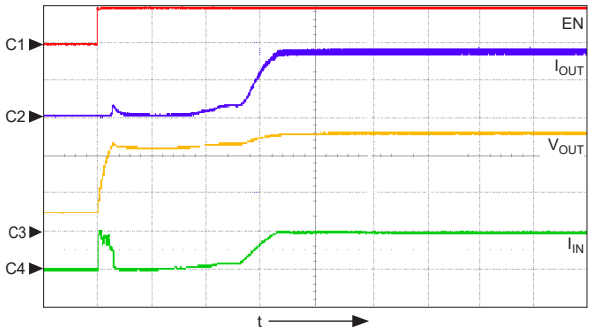
Performance Characteristics

EN Pin Turn On

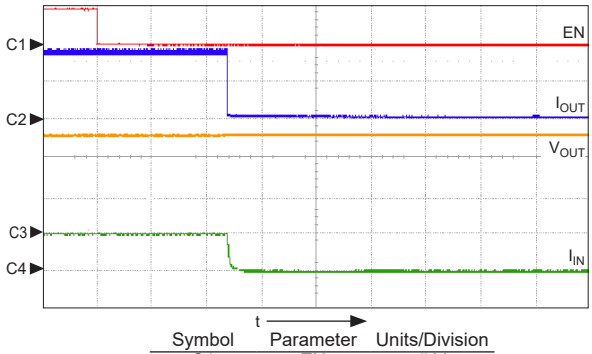
$V_{IN} = V_{BAT} = 5\,V$; 8 ch., 8 LEDs per ch.



Symbol	Parameter	Units/Division
C1	EN	5 V
C2	I_{OUT}	100 mA
C3	V_{OUT}	10 V
C4	I_{IN}	1 A
t	time	500 µs

EN Pin Turn Off

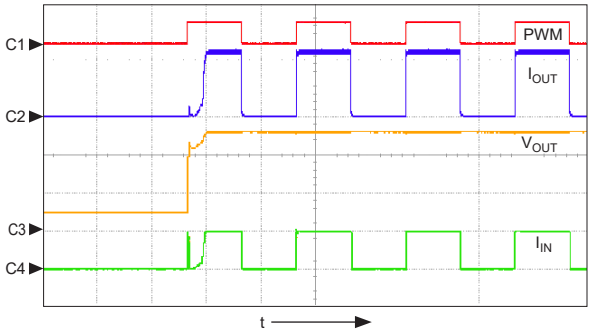
$V_{IN} = V_{BAT} = 5\,V$; 8 ch., 8 LEDs per ch.



Symbol	Parameter	Units/Division
C1	EN	5 V
C2	I_{OUT}	100 mA
C3	V_{OUT}	10 V
C4	I_{IN}	1 A
t	time	100 µs

PWM Turn On at 50% Duty Cycle

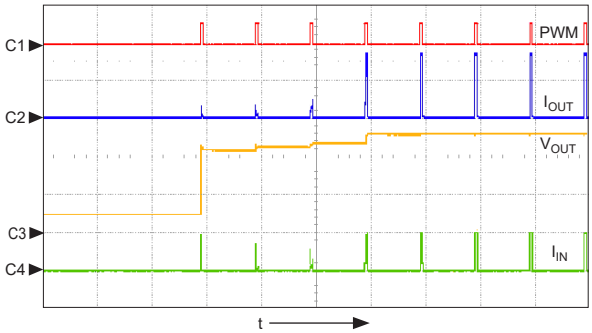
$V_{IN} = V_{BAT} = 5\,V$; 8 ch., 8 LEDs per ch.



Symbol	Parameter	Units/Division
C1	PWM	5 V
C2	I_{OUT}	100 mA
C3	V_{OUT}	10 V
C4	I_{IN}	1 A
t	time	5 ms

PWM Turn On at 5% Duty Cycle

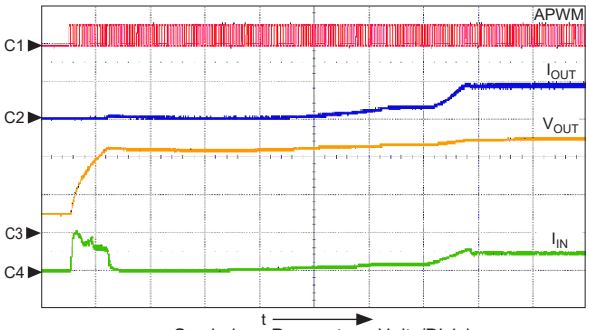
$V_{IN} = V_{BAT} = 5\,V$; 8 ch., 8 LEDs per ch.



Symbol	Parameter	Units/Division
C1	PWM	5 V
C2	I_{OUT}	100 mA
C3	V_{OUT}	10 V
C4	I_{IN}	1 A
t	time	10 ms

APWM Turn On at 50% Duty Cycle

F_{APWM}=100 kHz



Symbol	Parameter	Units/Division
C1	APWM	5 V
C2	I_{OUT}	100 mA
C3	V_{OUT}	10 V
C4	I_{IN}	1 A
t	time	200 µs

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Functional Description

The A8500 is a multioutput WLED driver for medium display backlighting. The A8500 works with 4.2 to 5.5 V input supply, and it has an integrated boost converter to boost a 5 V battery voltage up to 47 V, to drive up to 12 WLEDs in 6 series (V_f = 3.2 V, I_f = 20 mA), or 8 WLEDs in 8 series at 20 mA per LED string. For higher LED power or more LEDs, an inductor can be connected to a separate power supply, V_{BAT}, from 5 to 25 V, with the A8500 IC powered from a 5 V source. The LED sinks can sink up to a 25 mA current.

The boost converter is a constant frequency current-mode converter. The integrated boost DMOS switch is rated for 50 V at 2 A. This switch has pulse-by-pulse current limiting, with the current limit independent of duty cycle. The switch also has output overvoltage protection (OVP), with the OVP level adjustable, typically from 30 to 47 V, as described in the Device Internal Protection section.

The A8500 has individual open LED detection. If any LED opens, the corresponding LED pin is removed from regulation logic. This allows the remaining LED strings to function normally, without excessive power dissipation.

The switching frequency, f_{SW}, can be set from 600 kHz to 2 MHz by a single resistor, RFSET, connected across the FSET and AGND pins, and with the SKIP pin set to logic low (see figure 2).

The switching frequency is set as:

$$f_{SW} = 26.03 / R_{FSET},$$

where f_{SW} is in MHz and R_{FSET} is in kΩ When the SKIP pin is connected to logic low, switching frequency is as set by RFSET.

When the SKIP pin is connected to logic high, the switching frequency is divided by 4. The SKIP pin can be used to reduce switching frequency in order to reduce switching losses and improve efficiency at light loads.

The IC offers a wide-bandwidth transconductance amplifier with external COMP pin. External compensation offers optimum performance for the desired application.

The A8500 has eight well-matched current sinks to provide regulated current through LEDs for uniform display brightness. The quantity of LED*x* pins used is determined by the SEL*x* pins. Refer to table 1 for further description.

The boost converter is controlled such that the minimum voltage on any LED*x* pin is 500 mV. In a typical application, the LED*x* pin connected to the LED string with the maximum voltage drop controls the boost loop, so the remaining pins will also have the higher voltage drop. All LED sinks are rated for 21 V, to allow PWM dimming control.

LED Current Setting

The maximum LED current can be set at up to 25 mA per channel, by using the ISET pin. To set the reference current, I_{SET}, connect a resistor, RISET, between this pin and ground, valued according to the following formula:

$$I_{SET} = 1.23 / R_{ISET},$$

where I_{SET} is in mA and R_{ISET} is in kΩ.

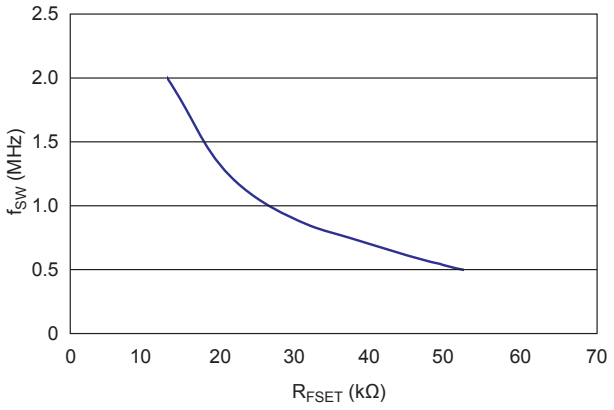

Figure 2. Switching frequency setting by value of RFSET.

Table 1. LEDx Channel Enable Table

SEL1	SEL2	SEL3	LED*x* Outputs
0	0	0	Only LED1 on
1	0	0	LED1 through LED2 on
0	1	0	LED1 through LED3 on
1	1	0	LED1 through LED4 on
0	0	1	LED1 through LED5 on
1	0	1	LED1 through LED6 on
0	1	1	LED1 through LED7 on
1	1	1	LED1 through LED8 on

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This current is multiplied internally with a gain of 210, and then mirrored on all enabled LED*x* pins. This sets the maximum current through the LEDs, referred to as "100% current." The effects of the value of R_{ISET} are shown in figure 3.

The LED current can be reduced from 100% by any of three alternative methods. These modes are:

- serial dimming through the EN pin,
- on/off control (PWM) with an external PWM signal on the PWM pin, and
- analog dimming with an external PWM signal on the APWM pin.

Note: Only one dimming technique can be used at a time.

Serial Dimming Through the EN Pin. When the EN pin is pulled high with PWM, and the APWM pin is low, the A8500 starts up in serial programming mode. In this mode, series of pulses applied to the EN pin are used to adjust the output current level, I_{LEDx}, to a proportion of the ISET current, in equal increments, as listed in table 2.

As shown in the timing diagram in figure 4, serial dimming is disabled during startup, for the $t_{HI(init)}$ period. After that, the A8500 begins evaluating pulse patterns applied on the EN pin. Until a valid series is evaluated, the count remains 0 and the default I_{LEDx} level remains at "100% current." A count in the range 1 to 15 is evaluated proportionately; for example, when a series of 12 pulses is evaluated, I_{LEDx} is set to 25% (100% × 4/16) of 100% current. At a 16th pulse, the counter resets to 0 and continues to count if additional pulses are applied.

Table 2. Serial Dimming Levels

Pulse Count	I_{LEDx}	Pulse Count	I_{LEDx}
0	100%	8	100%×8/16
1	100%×15/16	9	100%×7/16
2	100%×14/16	10	100%×6/16
3	100%×13/16	11	100%×5/16
4	100%×12/16	12	100%×4/16
5	100%×11/16	13	100%×3/16
6	100%×10/16	14	100%×2/16
7	100%× 9/16	15	100%×1/16
		16*	100%

*The counter resets on the sixteenth pulse.

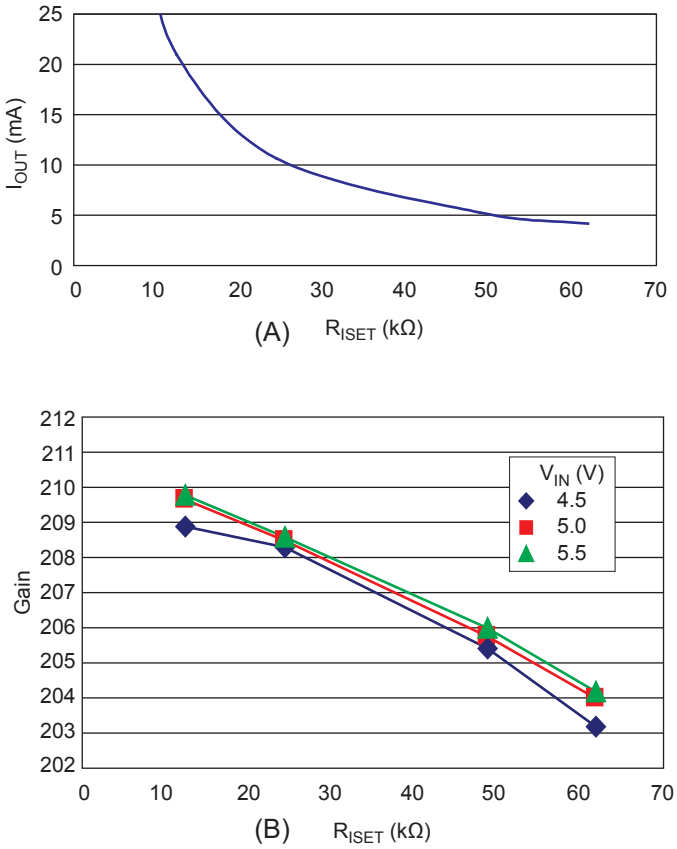

Figure 3. Effect of value of RISET on (A) "100% current" level, and (B) LED*x* gain.

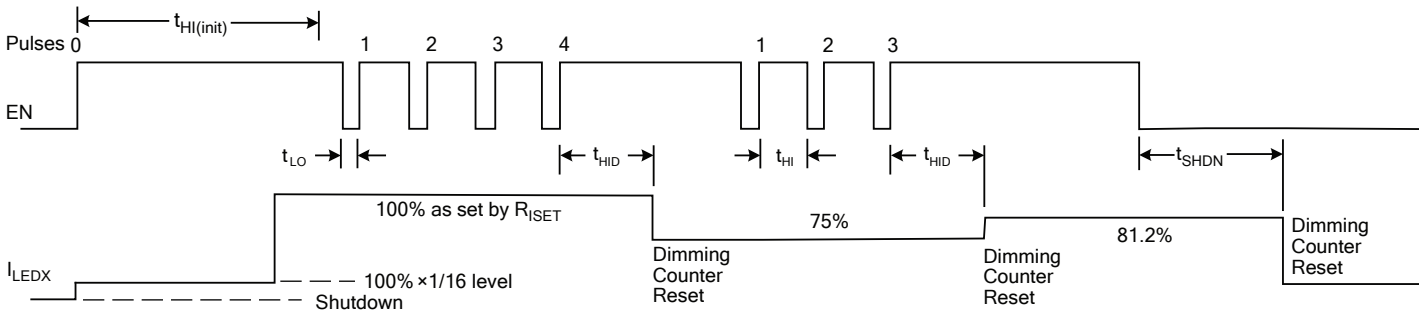

Figure 4. Timing diagram for serial dimming.

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To indicate the end of a programming sequence, set the EN pin high for a period, t_{HID}, which is either (a) greater than 256 oscillator periods when the SKIP pin is high, or (b) greater than 64 oscillator periods when SKIP is low. When the A8500 evaluates the end of a programming sequence, it changes the current level to match the existing count (per table 2). The counter is then reset to 0 and begins counting pulses again at the next valid pulse.

If the EN pin, along with the PWM and APWM pins, is pulled low for period greater than t_{SHDN}, the A8500 shuts down. When the IC enters shutdown, LED1 through LED8 and the boost switch turn off after the t_{SHDN} period. During t_{SHDN}, the converter continues to work in normal fashion.

When enabled through the EN pin, internal references ramp up during the $t_{HI(init)}$ period. The boost converter starts with soft start to limit input inrush current. During soft start, the boost stage is peak current limited to 1 A. All enabled LED*x* sinks are set to $^1/_{16}$ of the set 100% current level, as V_{OUT} and the voltage on the LED*x* pins increases. When all LED*x* pins reach the regulation level of 0.5 V, the IC comes out of soft start, resuming normal operation with 2 A current limit on boost and 100% current through LED*x* pins. A typical step response in steady state is shown in figure 5.

On/off Control (PWM) with an External PWM Signal on the PWM Pin. When the PWM pin is pulled high with the EN and APWM pins low, the A8500 turns on and all enabled LED*x* pins sink 100% current. When the PWM pin is pulled low, the IC shuts down with the LED*x* pins disabled. External PWM applied to the PWM pin should be in the range of 100 to 400 Hz for optimal accuracy.

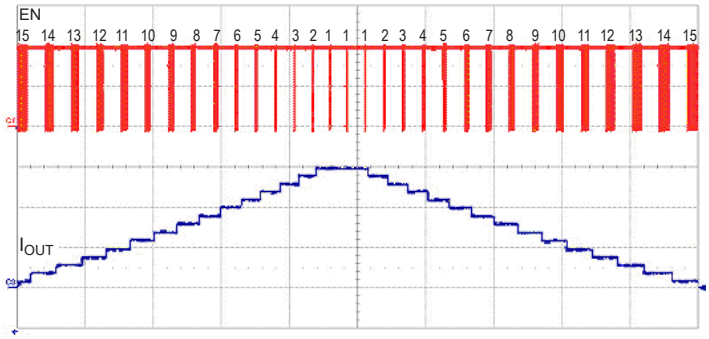
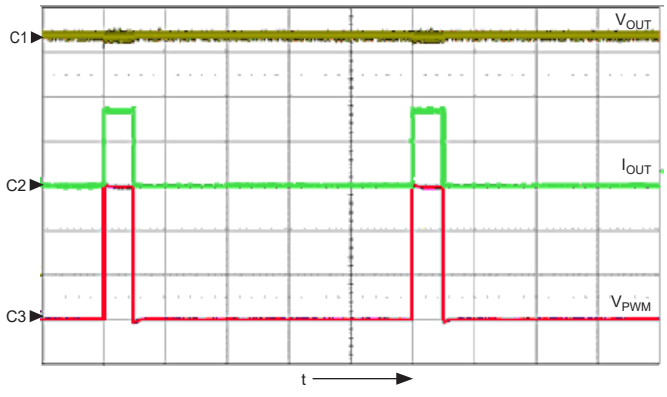


Figure 5. Serial dimming response. The numbers indicate the quantity of EN pulses at each step.



Symbol	Parameter	Units/Division
C1	V_{OUT}	5.00 V
C2	I_{OUT}	100 mA
C3	V_{PWM}	1.00 V
t	time	1.00 ms

Figure 7. PWM pin dimming f_{PWM} = 200 Hz, Duty Cycle =10%. Waveform is captured with AC coupling. DC value is zero.

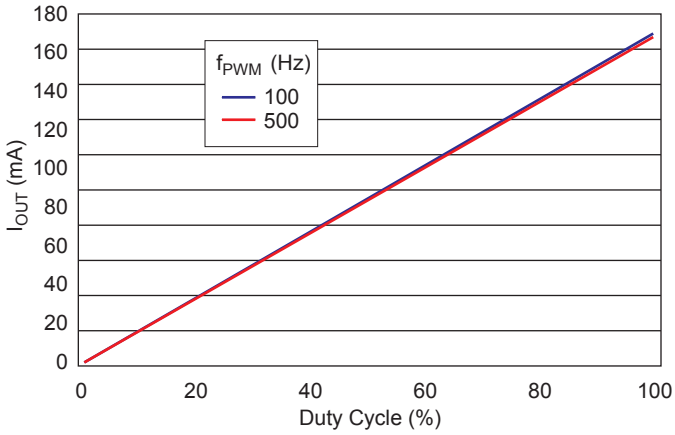


Figure 8. PWM pin dimming linearity.

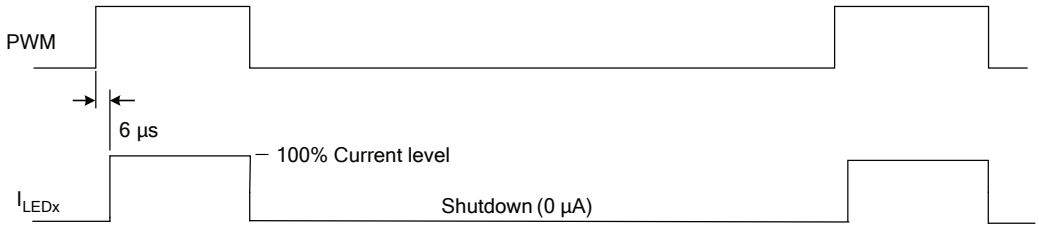


Figure 6. Timing diagram for dimming using the PWM pin.

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At startup, the output capacitor is discharged and the IC enters soft start. The boost current is limited to 1 A, and all active LED*x* pins sink $^{1}/_{16}$ of the set 100% current until all of the enabled LED*x* pins reach 0.5 V. After the IC comes out of soft start, the boost current and the LED*x* pin currents are set to 100% current. The output capacitor charges to the voltage level required to supply full LED*x* current within a few cycles. The IC is shut down immediately when PWM goes low.

Analog Dimming with an External PWM Signal on the APWM Pin. When the APWM pin is pulled high, with the EN and PWM pins low, the A8500 turns on in this mode. The first pulse after shutdown should be greater than $t_{HI(init)}$. The logic level PWM signal applied to the APWM pin multiplies I_{SET} by the duty cycle to set the reference current level for the LED pins. The typical range for the APWM signal frequency is 20 kHz to 2 MHz. The output current ripple at 20 kHz, 50% duty cycle, is less than 5% of the set value. The LED current accuaracy at 2 MHz, 50% duty cycle, is less than 3%. In this mode, the A8500 goes through a soft start routine similar to serial dimming.

Device Internal Protection

Overcurrent Protection (OCP). The A8500 has a pulse-by-pulse current limit of 2 A on the boost switch. This current limit is independent of duty cycle.

Thermal Shutdown Protection (TSD). The IC shuts down when junction temperature exceeds 165°C and restarts when the junction temperature falls by 40°C.

Overvoltage Protection (OVP). The A8500 has overvoltage protection to protect the IC against output overvoltage. The overvoltage level can be set, from 30 to 45 V typical, with an external resistor, ROVP, as shown in figure 10. When the current though the OVP pin exceeds 54.9 µA, the OVP comparator goes high. When the OVP pin current falls below 47.8 µA, OVP is reset.

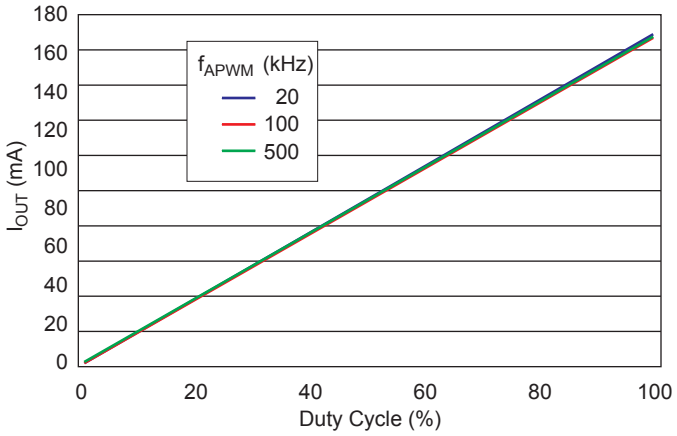

Figure 9. APWM pin dimming linearity.

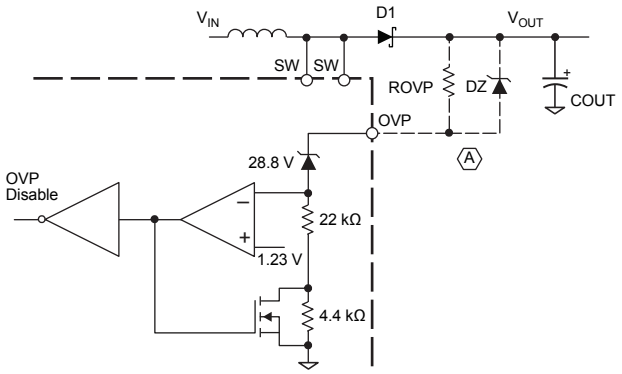

Figure 10. Overvoltage protection circuit. Three alternative configurations at (A) are available, as follows:

External Component	OVP Rating
ROVP only	up to 45 V
DZ only	up to 47 V
both ROVP and DZ	redundancy

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Calculate the value for R_{OVP} as follows:

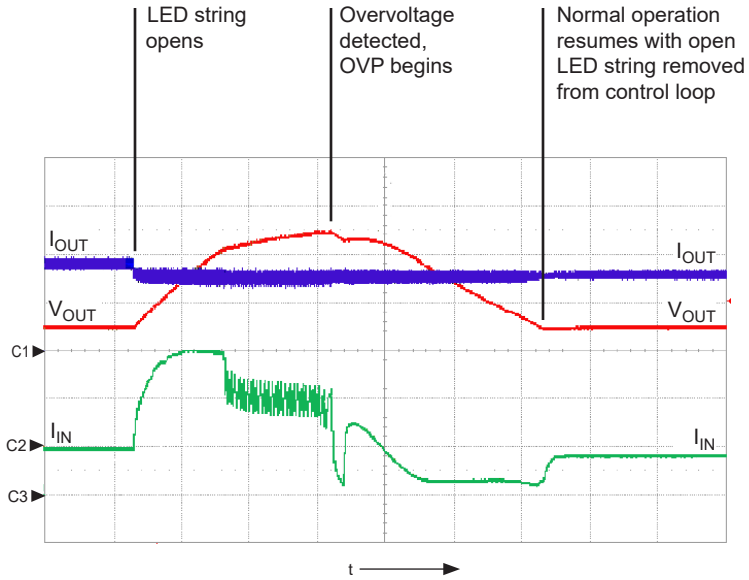
$$R_{OVP} = (V_{OVP} - 30) / 54.9\ \mu A\ ,$$

where V_{OVP} is the desired typical OVP level in V, and R_{OVP} is in Ω. For tighter OVP limits, a low–leakage-current Zener diode, DZ, can be used, instead of ROVP, to set OVP at up to 47 V. For redundancy, DZ can be connected across ROVP to provide additional protection, if ROVP should open. Select a 17 V low-leakage Zener diode for DZ.

Open LED Protection. The A8500 has protection against open LEDs. If any enabled LED string opens, voltage on the corresponding LED*x* pin goes to zero. The boost loop operates in open loop till the OVP level is reached. The A8500 identifies the open LED string when overvoltage on the OVP pin is detected. This string is then removed from the boost controlling loop. The boost circuit is then controlled in the normal manner, and the output voltage is regulated, to provide the output required to drive the remaining strings. If the open LED string is reconnected, it will sink current up to the programmed current level.

Note: Open strings are removed from boost regulation, but not disabled. This keeps the string in operation if LEDs open for only a short length of time, or reach OVP level on a transient event.

The disconnected string can be restored to normal mode by re-enabling the IC. It can also restored to normal operation if the fault signal is removed from the corresponding LED*x* pin, but an OVP event occurs on any other LED*x* pin.



Symbol	Parameter	Units/Division
C1	I_{OUT}	50 mA
C2	V_{OUT}	10 V
C3	I_{IN}	500 mA
t	time	200 µs

Figure 11. Open LED fault protection.

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Application Information

A typical application circuit for dimming an LCD monitor backlight with 96 LEDs is shown in figure 1. Figure 12 shows two dimming methods: digital PWM control (PWM signal on the PWM pin) and analog PWM control, with the analog signal, V_A, applied to the ISET pin through a resistor, RA.

The current flowing through RA can be calculated as:

$$I_A = V_A / R_A .$$

This current changes the reference current, I_{SET}, as follows:

$$I_{SET} = V_{SET} / R_{SET} - (V_A - V_{SET}) / R_A .$$

LED current can be changed by changing V_A. I_{SET} can be changed in the range from 40 µA to 120 µA.

Application Circuit for 1000:1 Dimming Level

A wider dimming range can be achieved by changing the reference current, I_{SET}, while using PWM dimming. For higher output, current levels turn on Q1. R_{ISET} and R_{ISETP} set the 100% current level. This current level can be set to 25 mA, and then it can be dimmed by applying 100% to 0.32% duty cycle on the PWM pin. The reference current can be reduced by turning off Q1. LED current can be dimmed to 8 mA by reducing reference current through ISET pin. This provides 1000:1 combined dimming level range. Figure 14 shows the accuracy, Err_{LEDX}, results using this circuit.

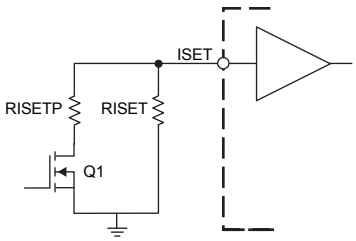

Figure 13. Configuration for 1000:1 dimming.

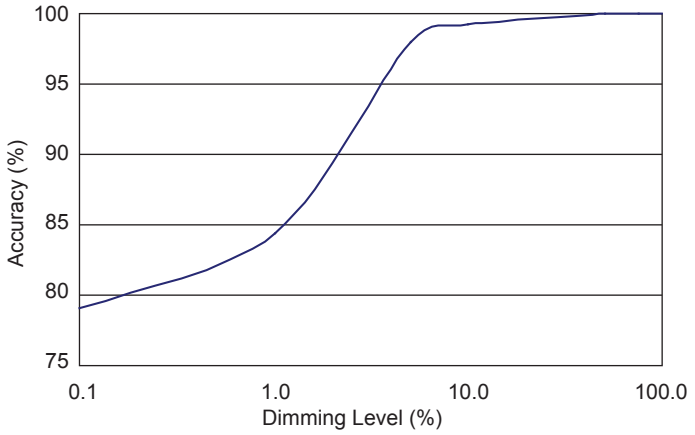

Figure 14. Typical accuracy, normalized to the 100% current level, versus dimming level, with F_{PWM} = 100 Hz.

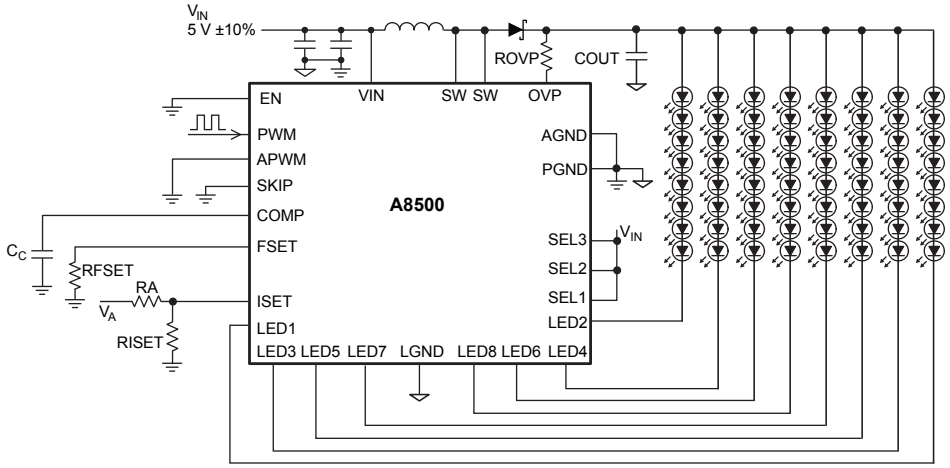

Figure 12. Typical application circuit for PWM dimming, using digital PWM (on the PWM pin, with APWM high).

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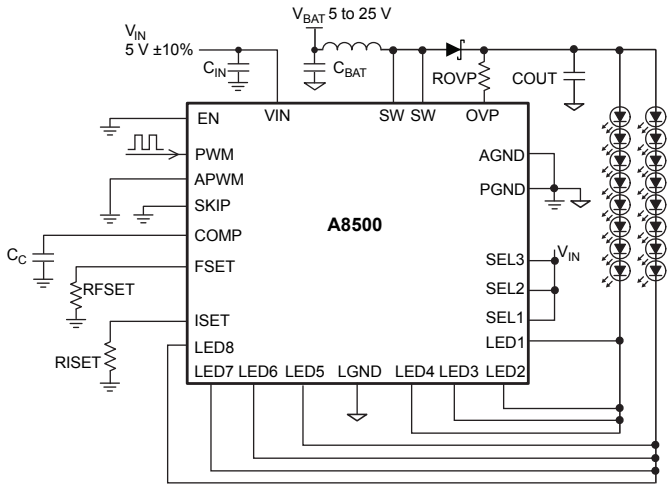

Figure 15. Typical application circuit for PWM dimming, using digital PWM (on the PWM pin, with APWM high). Showing configuration of 16 WLEDs at 100 mA, in two strings of 8 LEDs each.

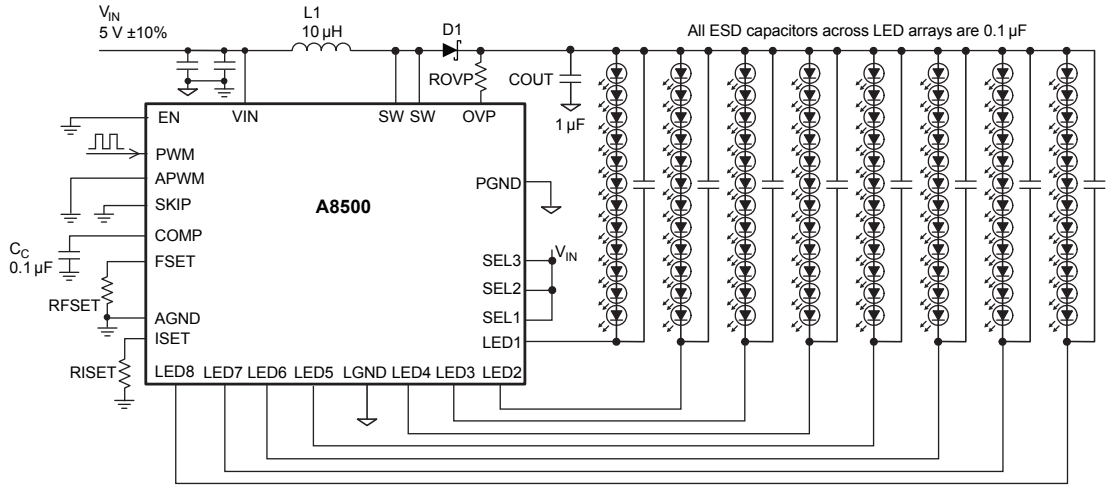

Figure 16. Typical application circuit for LED modules with ESD capacitors.

Recommended Components Table (for application shown in figure 1)

Component	Reference Designator	Value	Part Number	Vendor
Capacitor	C_{BAT}	1 µF / 50 V	C3216X7R1H105K	TDK
Capacitor	C_{OUT}	1 µF / 50 V	C3216X7R1H105K	TDK
Capacitor	C_{IN}, C_C	0.1 µF / 6.3 V		
Diode	D1	60 V / 1.5 A	IR 10MQ060NTRPBF	International Rectifier
IC	A8500	–	A8500	Allegro MicroSystems
Inductor	L1	10 µH	SLF6028T-100M1R3-PF	TDK
Resistor	RISET	12 kΩ		
Resistor	RFSET	24 kΩ		
Resistor	ROVP	270 kΩ		

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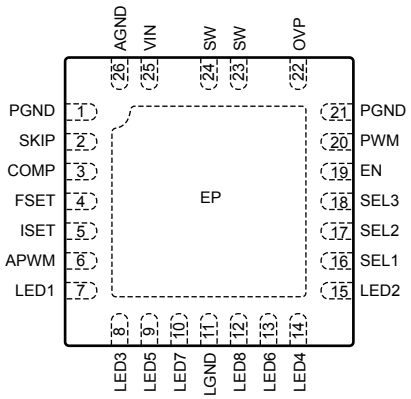
Pin-out Diagram



(Top View)

Terminal List Table

Number	Name	Description
1	PGND	Power ground pin.
2	SKIP	Reduces boost switching frequency in case of light load to improve frequency. Normally, this pin should be low; when high, f_{SW} is divided by 4.
3	COMP	Compensation pin; connect external compensation network for boost converter.
4	FSET	Sets boost switching frequency. Connect RFSET from FSET to GND to set frequency. Range for RFSET is 13 to 40 kΩ.
5	ISET	Sets 100% current through LED string. Connect RISET from ISET to GND. Range for RISET is 10 to 30 kΩ.
6	APWM	On/off and analog LED current control with external PWM. Apply logic level PWM (1.2 V < V_{IH} < 5 V) for PWM controlled dimming mode. When unused, connect to AGND.
7	LED1	LED*x* capable of 25 mA.
8	LED3	
9	LED5	
10	LED7	
11	LGND	Power ground pin for LED current sink.
12	LED8	LED*x* capable of 25 mA.
13	LED6	
14	LED4	
15	LED2	
16	SEL1	SEL1, SEL2, and SEL3 decide active LED strings.
17	SEL2	
18	SEL3	
19	EN	On/off and serial dimming control. EN high enables IC and EN low disables IC. This pin can also be used to program LEDx current. When unused, connect to AGND.
20	PWM	On/off and on/off LED current control with external PWM. Apply logic level PWM for PWM controlled dimming mode. When unused, connect to AGND.
21	PGND	Power ground pin.
22	OVP	Connect to this pin to output capacitor +Ve node through a resistor to enable OVP (overvoltage protection). Default OVP level with 0 Ω resistor is 30 V, and it can be programmed up to 47 V.
23	SW	DMOS drain node.
24	SW	
25	VIN	Input supply for the IC. Decouple with a 0.1 µF ceramic capacitor.
26	AGND	Circuit ground pin.
–	EP	Exposed pad. Electrically connectred to PGND and LGND; connect to PCB copper plane for heat transfer.

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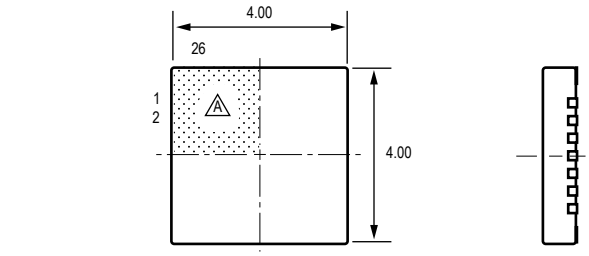
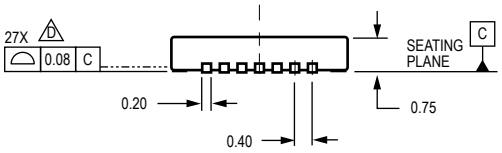
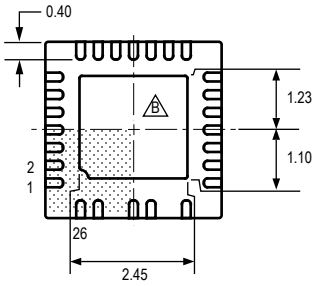
Package EC, 4 × 4 mm 26-Pin QFN/MLP

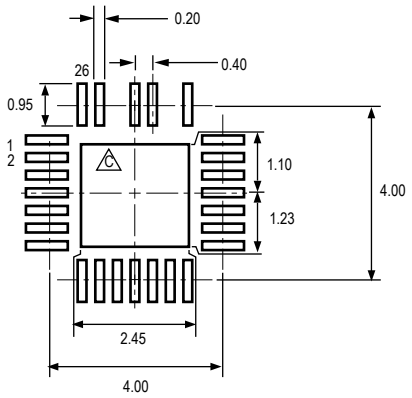


(Top View)





(Bottom View)



(Pads on PCB)

All dimensions nomianl, not for tooling use
(reference JEDEC MO-220WGGE)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN40P400X400X80-29M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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Revision History

Number	Date	Description
4	February 8, 2019	Product status changed to Pre-End-of-Life
5	February 20, 2020	Minor editorial updates
6	March 22, 2024	Updated product status to Last-Time Buy

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