



**THE DATASHEET OF  
A8439EEJTR-T**



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## *Protected Quad Driver with Fault Detection and Sleep Mode*

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### **Discontinued Product**

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 3, 2013

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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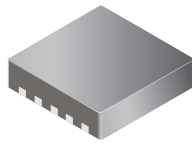
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## Photoflash Capacitor Charger with IGBT Driver and Refresh

### Features and Benefits

- Power with 1 Li+ or 2 Alkaline/NiMH/NiCAD batteries
- Adjustable output voltage
- Auto-refresh
- >75% efficiency
- Eight-level, digitally-programmable current limit
- Charge complete indication
- Integrated IGBT driver with trigger
- No primary-side Schottky diode needed
- Low-profile package (0.75 mm nominal height)

Package: 10 pin TDFN/MLP (suffix EJ)



Approximate Scale



### Description

The A8439 is a highly integrated IC that charges photoflash capacitors for digital and film cameras. An integrated MOSFET switch drives the transformer in a flyback topology. It also features an integrated IGBT driver that facilitates the flash discharge function and saves board space.

The CHARGE pin enables the A8439 and starts the charging of the output capacitor. When the designated output voltage is reached, the A8439 stops the charging until the CHARGE pin is toggled again, or when output voltage falls below 90% of the designated value. Pulling the CHARGE pin low stops the charging. The  $\overline{\text{DONE}}$  pin is an open-drain indicator of when the designated output voltage is reached.

The peak current limit can be adjusted to eight different levels between 270 mA and 1.4 A, by clocking the CHARGE pin. This allows the user to operate the flash even at low battery voltages.

The A8439 can be used with two Alkaline/NiMH/NiCAD or one single-cell Li+ battery connected to the transformer primary. Connect the VIN pin to a 3.0 to 5.5 V supply, which can be either the system rail or the Li+ battery, if used.

The A8439 is available in a very low profile (0.75 mm) 10-terminal 3×3 mm MLP/TDFN package, making it ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Applications include the following:

- Digital camera flash
- Cell phone flash
- Film camera flash
- Emergency strobe light

### Typical Applications

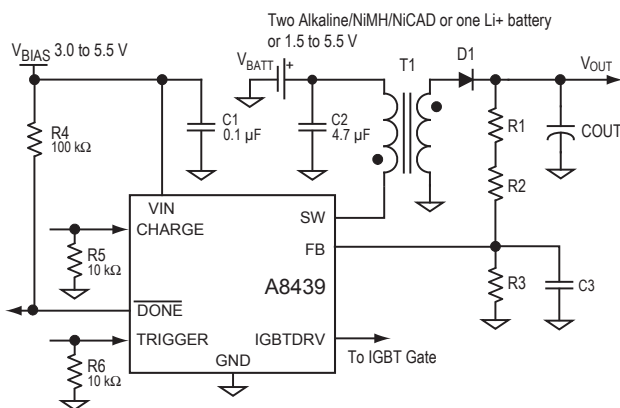


Figure 1. Typical circuit with separate power supply to transformer

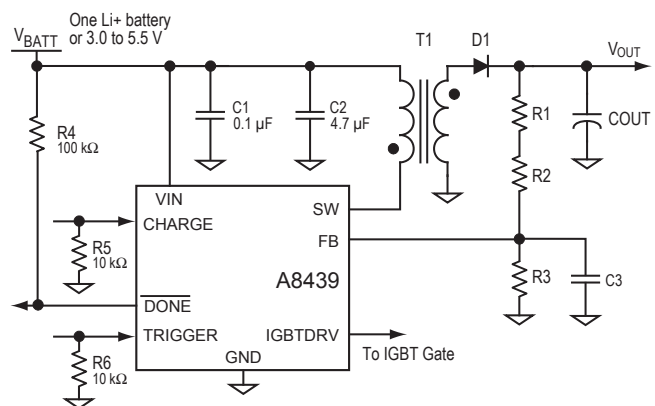


Figure 2. Typical circuit with single power supply

# A8439

## Photoflash Capacitor Charger with IGBT Driver and Refresh

### Selection Guide

Part Number	Package	Packing*
A8439EEJTR-T	10-pin TDFN/MLP	1500 pieces/ 7-in. reel

\*Contact Allegro for additional packing options



### Absolute Maximum Ratings

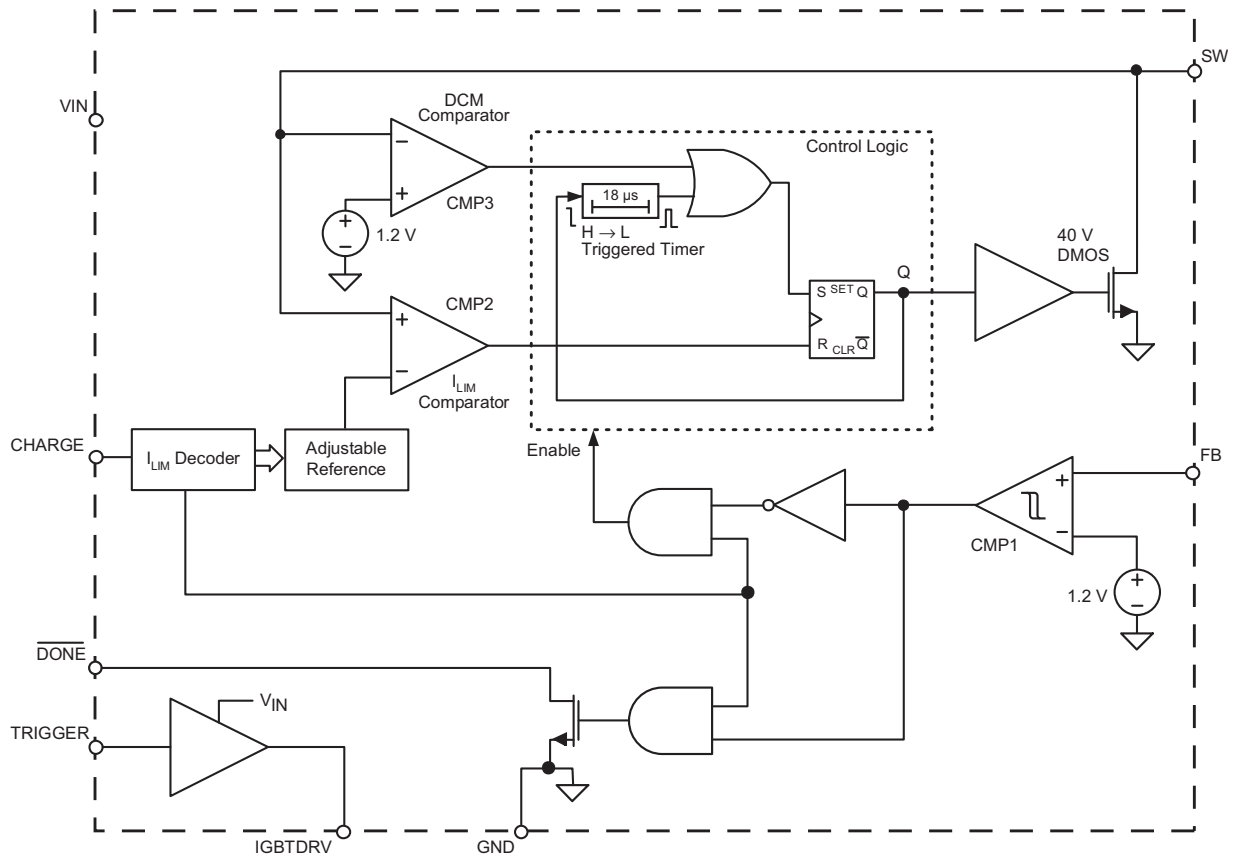
Characteristic	Symbol	Notes	Rating	Units
SW pin	$V_{SW}$		-0.3 to 40	V
IGBTDRV pin	$V_{IGBTDRV}$		-0.3 to $V_{IN} + 0.3$	V
FB pin	$V_{FB}$		-0.3 to $V_{IN}$	V
All other pins	$V_X$		-0.3 to 7	V
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

### Package Thermal Characteristics

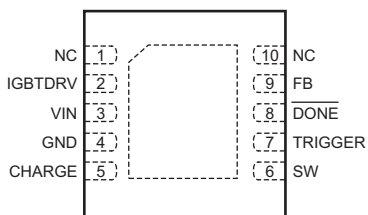
Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	4layer PCB, based on JEDEC standard	45	°C/W

\*Additional information is available on the Allegro website.

## Functional Block Diagram



## Device Pin-out Diagram



## Terminal List Table

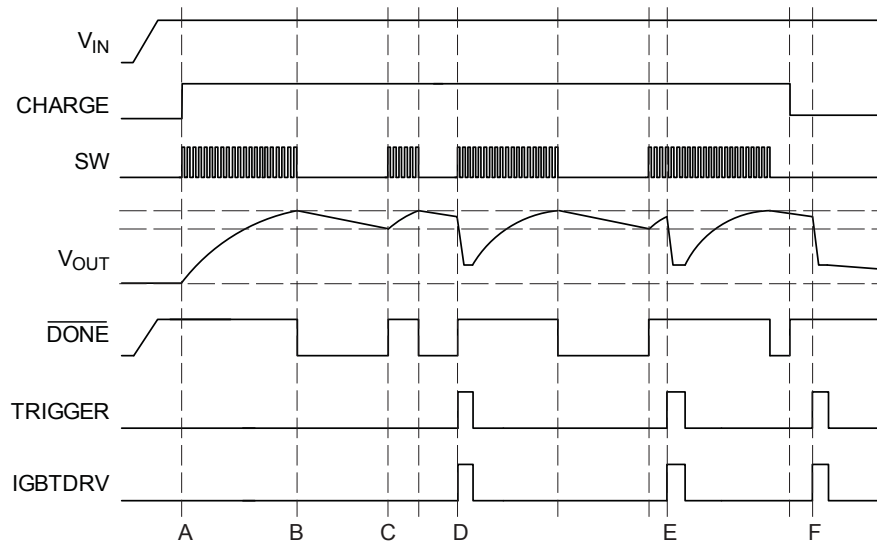
Number	Name	Function
1,10	NC	No connection
2	IGBTDRV	IGBT driver gate drive output
3	VIN	Power supply input
4	GND	Device ground
5	CHARGE	Charging enable and ISWLIM code input; set to low to power-off the A8439
6	SW	Switch, internally connected to the DMOS power FET drain
7	TRIGGER	Strobe signal input
8	$\overline{\text{DONE}}$	Open drain, when pulled low by internal MOSFET, indicates that charging target level has been reached
9	FB	Output voltage feedback

ELECTRICAL CHARACTERISTICS Typical values at  $T_A = 25^\circ\text{C}$  and  $V_{IN} = 3.3\text{ V}$  (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage*	$V_{IN}$		3	–	5.5	V
Supply Current	$I_{IN}$	Charging	–	1.5	–	mA
		Charging done / Refresh monitoring	–	300	600	$\mu\text{A}$
		Shutdown ( $V_{CHARGE} = 0\text{ V}$ , $V_{TRIGGER} = 0\text{ V}$ )	–	0.01	1	$\mu\text{A}$
Primary Side Current Limit (ILIM clock input at CHARGE pin)	$I_{SWLIM1}$		1.2	1.4	1.6	A
	$I_{SWLIM2}$		–	1.2	–	A
	$I_{SWLIM3}$		–	1.0	–	A
	$I_{SWLIM4}$		–	0.86	–	A
	$I_{SWLIM5}$		–	0.7	–	A
	$I_{SWLIM6}$		–	0.55	–	A
	$I_{SWLIM7}$		–	0.4	–	A
	$I_{SWLIM8}$		–	0.27	–	A
SW On Resistance	$R_{DS(On)SW}$	$V_{IN} = 3.3\text{ V}$ , $I_D = 800\text{ mA}$ , $T_A = 25^\circ\text{C}$	–	0.27	–	$\Omega$
SW Leakage Current*	$I_{SWLKG}$	$V_{SW} = 35\text{ V}$	–	–	1	$\mu\text{A}$
SW Maximum Off-Time	$t_{OFF(Max)}$		–	18	–	$\mu\text{s}$
SW Maximum On-Time	$t_{ON(Max)}$		–	18	–	$\mu\text{s}$
CHARGE Input Current	$I_{CHARGE}$	$V_{CHARGE} = V_{IN}$	–	–	1	$\mu\text{A}$
CHARGE Input Voltage*	$V_{CHARGE(H)}$		2	–	–	V
	$V_{CHARGE(L)}$		–	–	0.8	V
ILIM Clock High Time at CHARGE Pin	$t_{ILIM1(H)}$	Initial pulse	20	–	–	$\mu\text{s}$
	$t_{ILIM(H)}$	Subsequent pulses	0.2	–	–	$\mu\text{s}$
ILIM Clock Low Time at CHARGE Pin	$t_{ILIM(L)}$		0.2	–	–	$\mu\text{s}$
Total ILIM Setup Time	$t_{ILIM(SU)}$		–	54	–	$\mu\text{s}$
$\overline{\text{DONE}}$ Output Leakage Current*	$I_{DONELKG}$		–	–	1	$\mu\text{A}$
$\overline{\text{DONE}}$ Output Low Voltage*	$V_{DONE(L)}$	32 $\mu\text{A}$ into $\overline{\text{DONE}}$ pin	–	–	100	mV
FB Voltage Threshold*	$V_{FB}$		1.187	1.205	1.223	V
FB Input Current	$I_{FB}$	$V_{FB} = 1.205\text{ V}$	–	–120	–	nA
Auto-Refresh Threshold Level	$V_{FBR}$		–	1.07	–	V
UVLO Enable Threshold	$V_{UVLO}$	$V_{IN}$ rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{UVLOHYS}$		–	150	–	mV
IGBT Driver						
IGBTDRV On Resistance to VIN	$R_{DS(On)I-V}$	$V_{IN} = 3.3\text{ V}$ , $V_{IGBTDRV} = 1.5\text{ V}$ , $V_{TRIGGER} = V_{IN}$	–	5	–	$\Omega$
IGBTDRV On Resistance to GND	$R_{DS(On)I-G}$	$V_{IN} = 3.3\text{ V}$ , $V_{IGBTDRV} = 1.5\text{ V}$ , $V_{TRIGGER} = 0\text{ V}$	–	6	–	$\Omega$
TRIGGER Input Current	$I_{TRIGGER}$	$V_{TRIGGER} = V_{IN}$	–	–	1	$\mu\text{A}$
TRIGGER Input Voltage*	$V_{TRIGGER(H)}$		2	–	–	V
	$V_{TRIGGER(L)}$		–	–	0.8	V
Propagation Delay, Rising	$t_{Dr}$	$R_{gate} = 12\ \Omega$ , $C_{LOAD} = 6500\text{ pF}$ , $V_{IN} = 3.3\text{ V}$	–	30	–	ns
Propagation Delay, Falling	$t_{Df}$	$R_{gate} = 12\ \Omega$ , $C_{LOAD} = 6500\text{ pF}$ , $V_{IN} = 3.3\text{ V}$	–	30	–	ns
Output Rise Time	$t_r$	$R_{gate} = 12\ \Omega$ , $C_{LOAD} = 6500\text{ pF}$ , $V_{IN} = 3.3\text{ V}$	–	70	–	ns
Output Fall Time	$t_f$	$R_{gate} = 12\ \Omega$ , $C_{LOAD} = 6500\text{ pF}$ , $V_{IN} = 3.3\text{ V}$	–	70	–	ns

\*Guaranteed by design and characterization over operating temperature range,  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

## Operation Timing Diagram



## Explanation of Events:

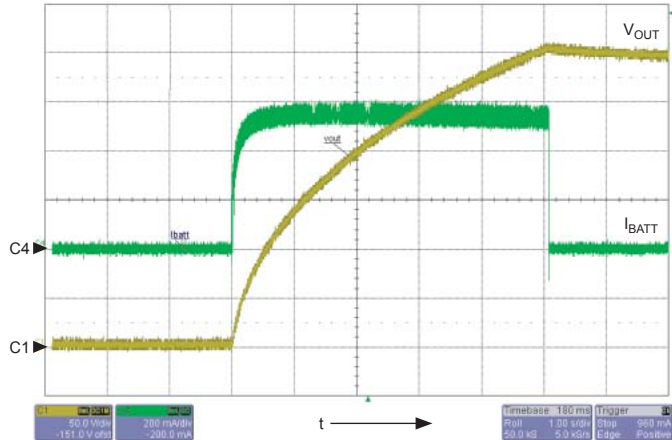
- Start charging by pulling  $CHARGE$  to high, provided that  $V_{IN}$  is above the  $V_{UVLO}$  level.
- Charging stops when  $V_{OUT}$  reaches the target voltage.  $\overline{DONE}$  goes low, to signal the completion of the charging process.
- When  $V_{OUT}$  drops below approximately 90% of target voltage, charging restarts to replenish the output capacitor ('auto-refresh').
- When  $TRIGGER$  is pulled high,  $IGBTDRV$  goes high to fire the IGBT and flash tube.  $V_{OUT}$  drops, and charging restarts to replenish the output capacitor.
- If  $TRIGGER$  is pulled high during an auto-refresh period, the flash fires normally and the output capacitor is replenished.
- If  $TRIGGER$  is pulled high when  $CHARGE$  is low, the flash fires normally but the output capacitor is not replenished.

Performance Characteristics

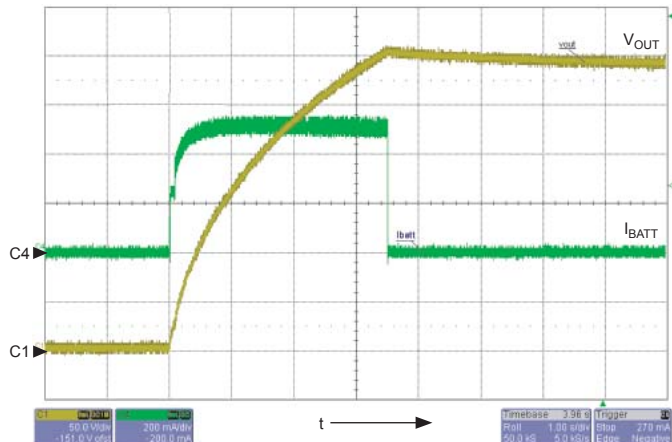
Tests performed using application circuit shown in figure 8  
with  $I_{SWLIM}$  set to 1.4A (Single rising edge on CHARGE pin), unless otherwise noted

Charging Waveforms

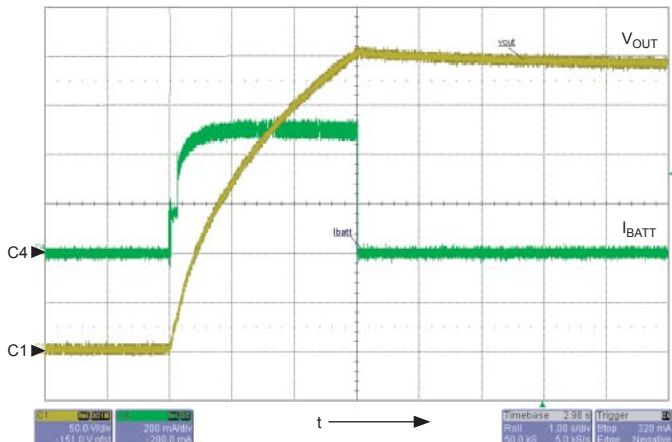
Symbol	Parameter	Units/Division
C1	$V_{OUT}$	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	Parameter	Value
	$V_{BATT}$	2.5 V
	$V_{BIAS}$	3.3 V
	$C_{OUT}$	100 $\mu$ F



Symbol	Parameter	Units/Division
C1	$V_{OUT}$	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	Parameter	Value
	$V_{BATT}$	3.6 V
	$V_{BIAS}$	3.3 V
	$C_{OUT}$	100 $\mu$ F



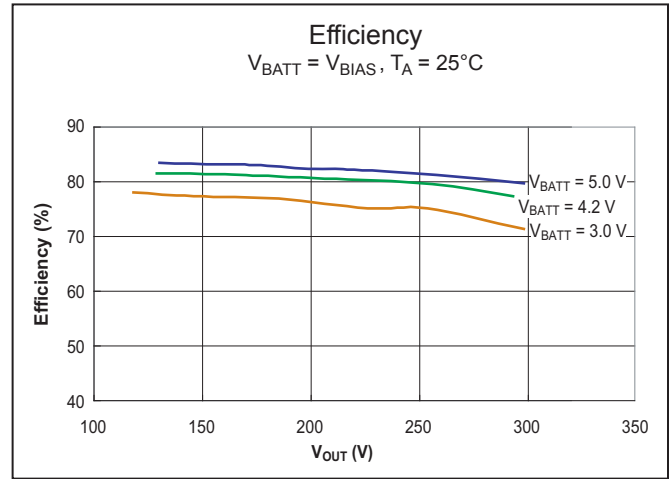
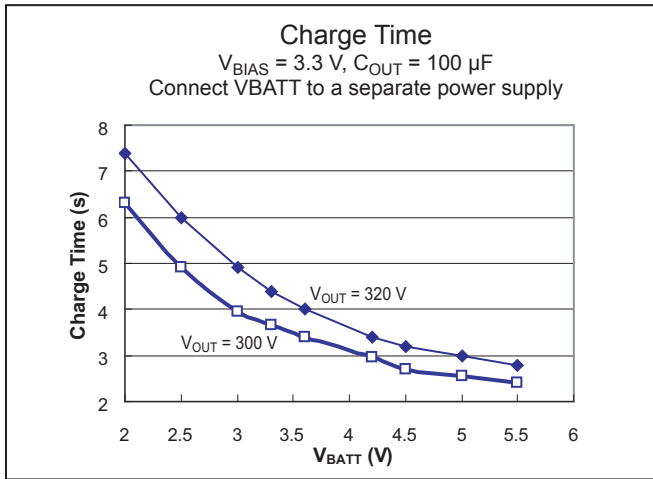
Symbol	Parameter	Units/Division
C1	$V_{OUT}$	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	Parameter	Value
	$V_{BATT}$	4.2 V
	$V_{BIAS}$	3.3 V
	$C_{OUT}$	100 $\mu$ F



## Performance Characteristics, continued

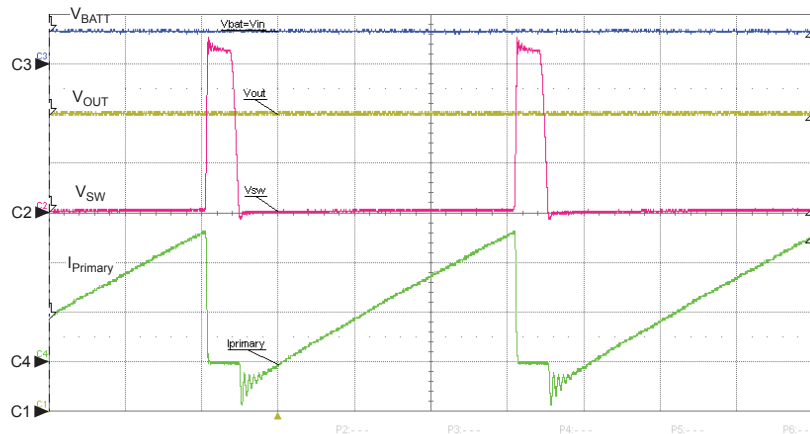
Tests performed using application circuit shown in figure 8

with  $I_{SWLIM}$  set to 1.4A (Single rising edge on CHARGE pin), unless otherwise noted

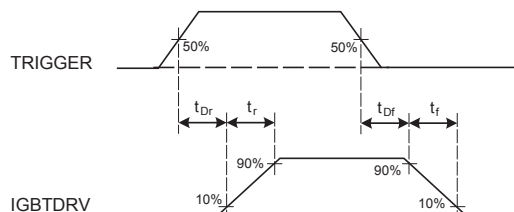


## Typical Switching Waveform

Symbol	Parameter	Units/Division
C1	$V_{OUT}$	50 V
C2	$V_{SW}$	10 V
C3	$V_{BATT}$	5 V
C4	$I_{Primary}$	500 mA
t	time	2 $\mu\text{s}$
Conditions	Parameter	Value
	$V_{OUT}$	300 V
	$V_{BATT}$	$V_{IN}$



## IGBT Drive Timing Definition



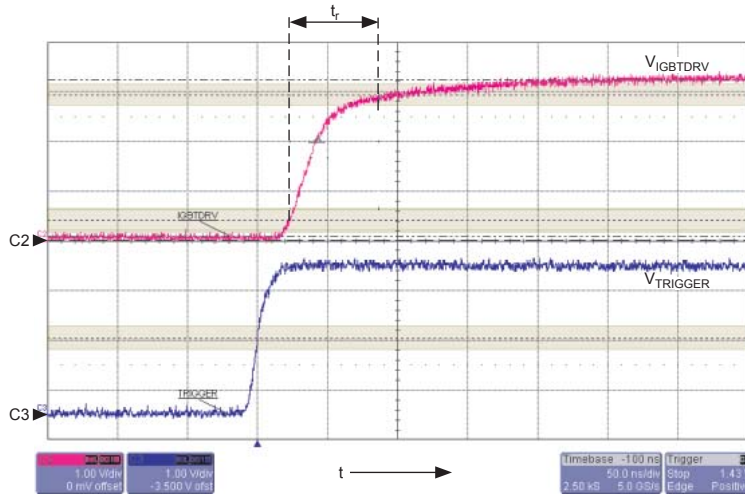
## Performance Characteristics, continued

IGBT Drive waveforms are measured with R-C load (12 Ω, 6800 pF)

### IGBT Drive Performance

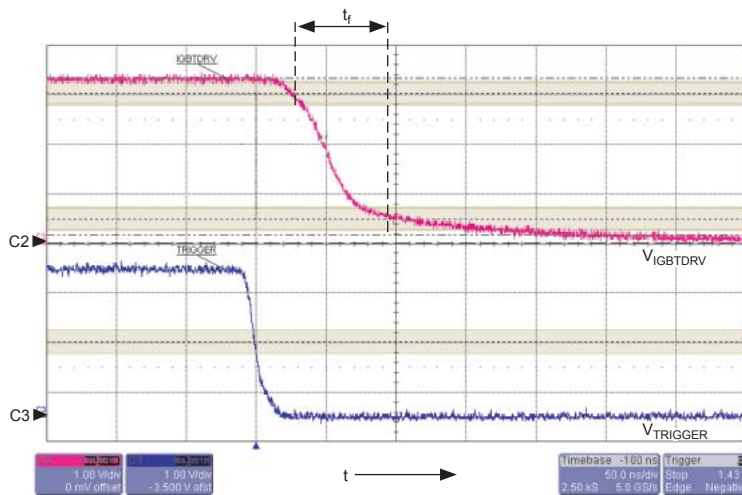
#### Rising Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	Parameter	Value
	$t_{Dr}$	22.881 ns
	$t_r$	63.125 ns
	$C_{LOAD}$	6800 pF
	$R_{gate}$	12 Ω



#### Falling Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	Parameter	Value
	$t_{Dr}$	27.427 ns
	$t_f$	65.529 ns
	$C_{LOAD}$	6800 pF
	$R_{gate}$	12 Ω



## Functional Description

### Overview

The A8439 is a photoflash capacitor charger control IC with adjustable input current limiting and automatic refresh. It also integrates an IGBT driver for strobe operation of the flash tube, dramatically saving board space in comparison to discrete solutions for strobe flash operation. The control logic is shown in the functional block diagram.

The charging operation of the A8439 is started by a low-to-high signal on the CHARGE pin, provided that  $V_{IN}$  is above  $V_{UVLO}$  level. If CHARGE is already high before  $V_{IN}$  reaches  $V_{UVLO}$ , another low-to-high transition on the CHARGE pin is required to start the charging. The primary peak current is set by input clock signals from the CHARGE pin. When a charging cycle is initiated, the transformer primary side current,  $I_{Primary}$ , ramps up linearly at a rate determined by the combined effect of the battery voltage,  $V_{BATT}$ , and the primary side inductance,  $L_{Primary}$ . When  $I_{Primary}$  reaches the current limit,  $I_{SWLIM}$ , the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor,  $C_{OUT}$ , from the secondary winding. The secondary side current drops linearly as  $C_{OUT}$  charges. The recharging cycle starts again, either after the transformer flux is reset, or after a predetermined time period,  $t_{OFF(Max)}$  ( $18 \mu s$ ), whichever occurs first.

The output voltage,  $V_{OUT}$ , is sensed by a resistor string,  $R_1$ ,  $R_2$ , and  $R_3$  (see application circuit diagrams), connected between the positive terminal of the output capacitor and ground. This resistor string forms a voltage divider that feeds back to the FB pin. The resistors must be sized to achieve a desired output voltage level based on a typical value of 1.205 V at the FB pin. As soon as  $V_{OUT}$  reaches the desired value, the charging process is terminated. The A8439 automatically starts a new charging cycle when the internal voltage sensing circuit detects a 10% drop in the output voltage. Toggling the CHARGE pin can also start a refresh operation.

### Auto-Refresh

The A8439 features auto-refresh when the feedback resistor network is connected at the output. Auto-refresh initiates when the output voltage drops to  $\approx 90\%$  of the set stop voltage of the resistor network. The operation is shown in figure 3.

### Input Current Limiting

The peak current limit can be adjusted to eight different levels, from 270 mA to 1.4 A, by clocking the CHARGE pin. An internal digital circuit decodes the input clock signals to a counter, which sets the charging time. This flexible scheme allows the user to operate the flash circuit according to different battery input voltages. The battery life can be effectively extended by setting a lower current limit at low battery voltages.

Figure 4 shows the ILIM clock timing scheme protocol. The total ILIM setup time,  $t_{LIM(SU)}$ , denotes the time needed for the

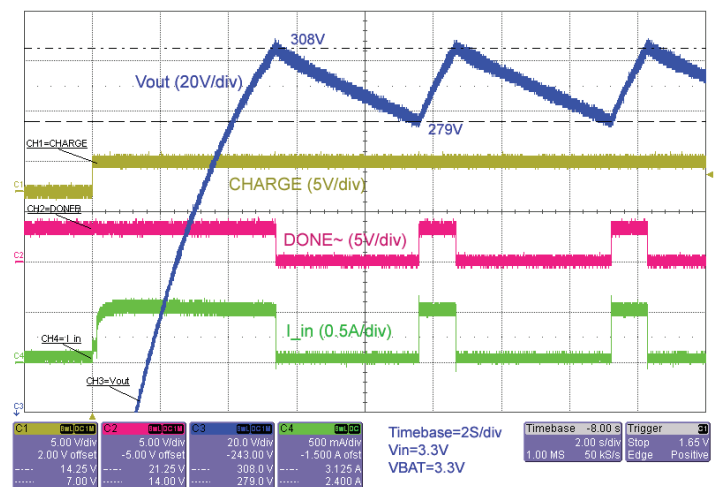


Figure 3. Auto-refresh waveform of A8439.

decoder circuit to receive ILIM inputs and set  $I_{SWLIM}$ , and has a minimum duration of 54  $\mu s$ .

Figure 5 shows the timing definition of the primary current limiting circuit. At the end of the setup period,  $t_{ILIM(SU)}$ , primary current starts to ramp up to the set  $I_{SWIM}$ . The  $I_{SWLIM}$  setting remains in effect as long as the CHARGE pin is high. To reset the ILIM counter, pull the CHARGE pin low before clocking in the new setting.

After the first start-up or an ILIM counter reset, each new current limit can be set by sending a burst of pulses to the CHARGE pin. The first rising edge starts the ILIM counter, and up to 8 rising edges will be counted to set the  $I_{SWLIM}$  level. The first pulse width,  $t_{ILIM1(H)}$ , must be at least 20  $\mu s$  long. Subsequent pulses (up to 7 more) can be as short as 0.2  $\mu s$ . The last low-to-high edge must arrive within 54  $\mu s$  from the first edge. The CHARGE pin will stay high afterwards. The four panels of figure 6 show examples of the pulse streams and the resulting current levels.

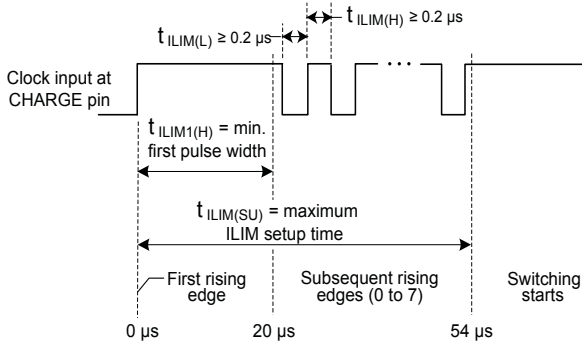


Figure 4. ILIM Clock Timing Definition

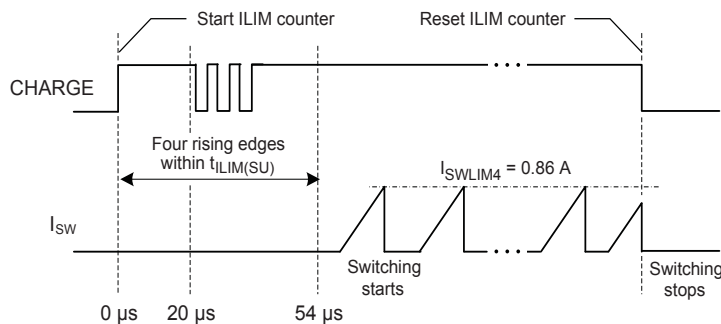


Figure 5. Current Limit Programming Example ( $I_{SWLIM4}$  selected).

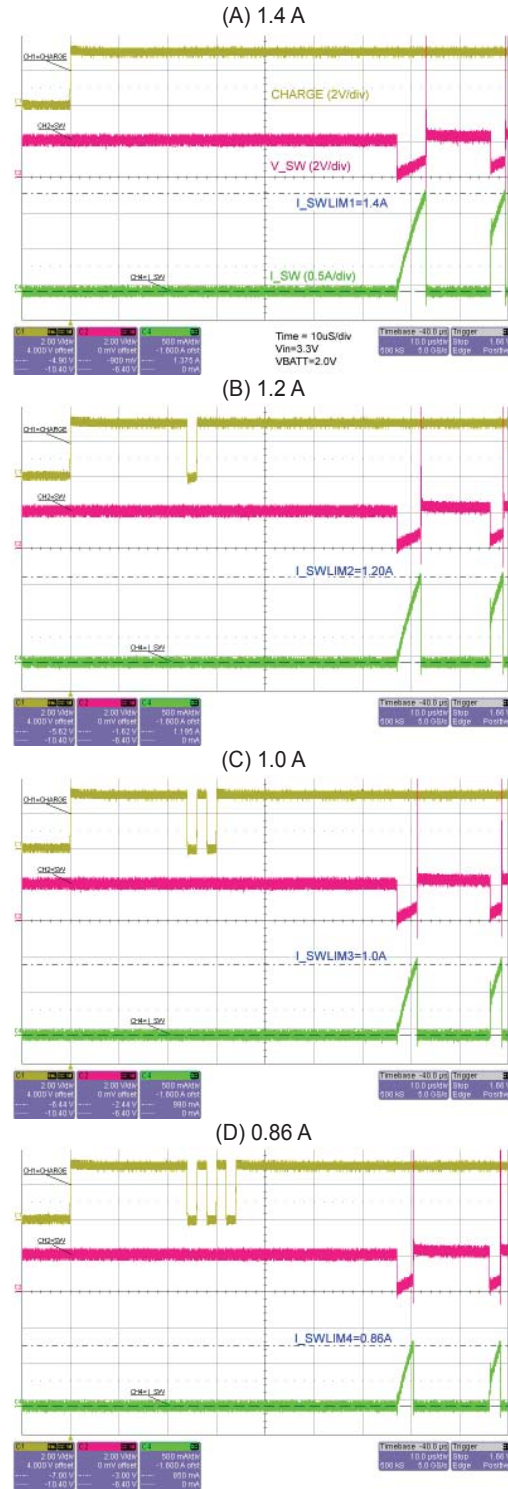


Figure 6. ILIM programming waveforms for  $I_{SWLIM} = 1.4 A, 1.2 A, 1.0 A,$  and  $0.86 A$ .

Figure 7 shows the last charging cycle, when the CHARGE pin is forced low before charging has been completed.

The A8439 implements an adaptive off-time,  $t_{OFF}$ , control.

After the switch is turned off, a sensing circuit tracks the flyback

voltage at the SW node. As soon as this voltage swings below 1.2 V, the switch is turned on again for the next charging cycle. However, when the photoflash capacitor charger circuit starts up at low output voltage, a timeout may be triggered to limit the maximum switch off-time to 20  $\mu$ s.

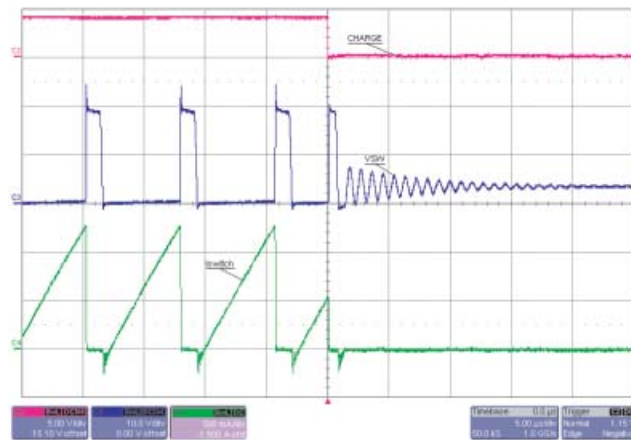


Figure 7. Last charging cycle, when the CHARGE pin is forced low before charging is complete.

## Applications Information

### Transformer Design

**Turns Ratio.** The minimum transformer turns ratio,  $N$ , (Secondary:Primary) should be chosen based on the following formula:

$$N \geq \frac{V_{OUT} + V_{D\_Drop}}{40 - V_{BATT}} \quad (1)$$

where:

- $V_{OUT}$  (V) is the required output voltage level,
- $V_{D\_Drop}$  (V) is the forward voltage drop of the output diode(s),
- $V_{BATT}$  (V) is the transformer battery supply, and
- 40 (V) is the rated voltage for the internal MOSFET switch, representing the maximum allowable reflected voltage from the output to the SW pin.

For example, if  $V_{BATT}$  is 3.5 V and  $V_{D\_Drop}$  is 1.7 V (which could be the case when two high voltage diodes were in series), and the desired  $V_{OUT}$  is 320 V, then the turns ratio should be at least 8.9.

In a worst case, when  $V_{BATT}$  is highest and  $V_{D\_Drop}$  and  $V_{OUT}$  are at their maximum tolerance limit,  $N$  will be higher. Taking  $V_{BATT} = 5.5$  V,  $V_{D\_Drop} = 2$  V, and  $V_{OUT} = 320$  V  $\times$  102 % = 326.4 V as the worst case condition,  $N$  can be determined to be 9.5.

In practice, always choose a turns ratio that is higher than the calculated value to give some safety margin. In the worst case example, a minimum turns ratio of  $N = 10$  is recommended.

**Primary Inductance.** As a loose guideline when choosing the

primary inductance,  $L_{Primary}$  ( $\mu$ H), use the following formula:

$$L_{Primary} \geq \frac{300 \times 10^{-9} \times V_{OUT}}{N \times I_{SWLIM}} \quad (2)$$

Ideally, the charging time is not affected by transformer primary inductance. In practice, however, it is recommended that a primary inductance be chosen between 10  $\mu$ H and 20  $\mu$ H. When  $L_{Primary}$  is lower than 10  $\mu$ H, the converter operates at higher frequency, which increases switching loss proportionally. This leads to lower efficiency and longer charging time. When  $L_{Primary}$  is greater than 20  $\mu$ H, the rating of the transformer must be dramatically increased to handle the required power density, and the series resistances are usually higher. A design that is optimized to achieve a small footprint solution would have an  $L_{Primary}$  of 12 to 14  $\mu$ H, with minimized leakage inductance and secondary capacitance, and minimized primary and secondary series resistance. Please refer to the table Recommended Components for more information.

**Leakage Inductance and Secondary Capacitance.** The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the 40 V limit. An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by  $N^2$  when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

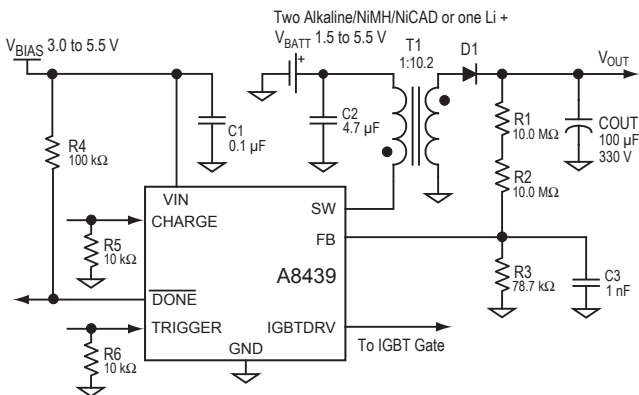


Figure 8. Typical circuit for photoflash capacitor charging application.

Symbol	Rating
C1	0.1 $\mu$ F, X5R or X7R, 10 V
C2	4.7 $\mu$ F, X5R or X7R, 10 V
C3	1 nF, X5R or X7R, 10 V
D1	Fairchild Semiconductor BAV23S (dual diode connected in series)
T1	Tokyo Coil Engineering T-16-024A, $L_{Primary} = 12$ $\mu$ H, $N = 10.2$
R1, R2	0805 resistors, 1%
R3	0603 resistor, 1%
R4	Pull-up resistor
R5, R6	Pull-down resistors

## Adjusting Output Voltage

The A8439 senses output voltage continuously in order to provide auto-refresh function. The output voltage can be adjusted by selecting proper values of the voltage divider resistors. Use the following equation to calculate values for  $R_x$  ( $\Omega$ ):

$$\frac{R_1 + R_2}{R_3} = \frac{V_{OUT}}{V_{FB}} - 1 \quad (3)$$

$R_1$  and  $R_2$  together need to have a breakdown voltage of at least 300 V. A typical 0805 surface mount resistor has a 150 V breakdown voltage rating. It is recommended that  $R_1$  and  $R_2$  have similar values to ensure an even voltage stress between them. Recommended values are:

$$R_1 = R_2 = 10.0 \text{ M}\Omega \text{ (0805 or 1206)}$$

$$R_3 = 78.7 \text{ k}\Omega \text{ (0402 or 0603)}$$

which together yield a stop voltage of 305 V.

If desired, larger resistance values may be used to reduce leakage current from sensing network. (For example:  $R_1=R_2=15 \text{ M}\Omega$ , and  $R_3 = 118 \text{ k}\Omega$ .)

## Output Diode Selection

Choose the rectifying diode(s),  $D_1$ , to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements.

The peak reverse voltage of the diode,  $V_{D\_Peak}$ , occurs when the internal MOSFET switch is closed, and the primary-side current

starts to ramp-up. It can be calculated as:

$$V_{D\_Peak} = V_{OUT} + N \times V_{BATT} \quad (4)$$

The peak current of the rectifying diode,  $I_{D\_Peak}$ , is calculated as:

$$I_{D\_Peak} = I_{Primary\_Peak} / N \quad (5)$$

## Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor,  $C_2$ . It should be rated at least  $4.7 \mu\text{F}/6.3 \text{ V}$  to decouple the battery input,  $V_{BATT}$ , at the primary of the transformer. When using a separate bias,  $V_{BIAS}$ , for the A8439 VIN supply, connect at least a  $0.1 \mu\text{F}/6.3 \text{ V}$  bypass capacitor to the VIN pin.

## Layout Guidelines

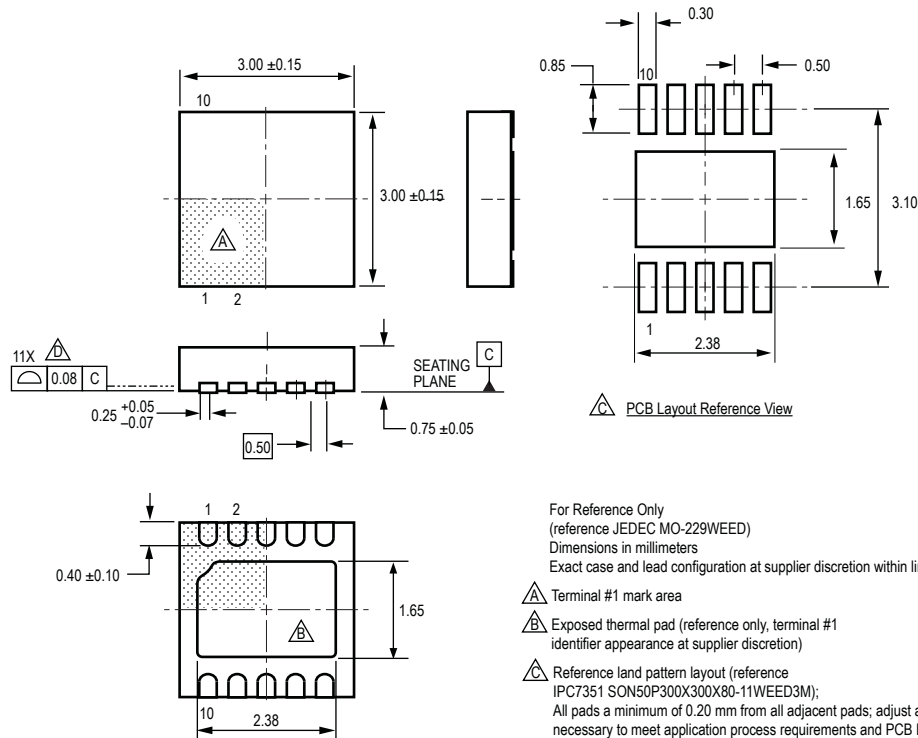
Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin.

Output voltage sensing circuit elements must be kept away from switching nodes such as SW pin. It is important that the  $\overline{DONE}$  signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Recommended Components Table

Component	Rating	Part Number	Source
C1, Input Capacitor	0.1 $\mu\text{F}$ , $\pm 10\%$ , 16 V X7R ceramic capacitor (0603)	GRM188R71C104KA01D	Murata
C2, Input Capacitor	4.7 $\mu\text{F}$ , $\pm 10\%$ , 10 V, X5R ceramic capacitor (0805)	LMK212BJ475KG	Taiyo Yuden
COUT, Photoflash Capacitor	330 V 100 $\mu\text{F}$ (or 19 to 180 $\mu\text{F}$ )	EPH-331ELL101B131S	Chemi-Con
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
R1, R2, FB Resistors	10.0 M $\Omega$ , $1/8 \text{ W}$ $\pm 1\%$ (0805)	9C08052A1005FKHFT	Yageo
R3, FB Resistor	78.7 k $\Omega$ $1/10 \text{ W}$ $\pm 1\%$ (0603)	9C06031A7872FKHFT	Yageo
T1, Transformer	1:10.2, $L_{Primary} = 14.5 \mu\text{H}$	LDT565630T-002	TDK
	1:10.2, $L_{Primary} = 12 \mu\text{H}$	T-16-024A	Tokyo Coil Engineering
	1:10, $L_{Primary} = 10.8 \mu\text{H}$	ST-532517A	Asatech

## Package EJ, 10-Contact TDFN/MLP



For Reference Only  
 (reference JEDEC MO-229WEED)  
 Dimensions in millimeters  
 Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- △ Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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