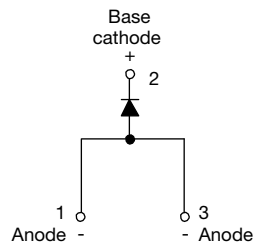




# High Voltage Surface Mount Input Rectifier Diode, 8 A



TO-252AA (D-PAK)


**FEATURES**

- Glass passivated pellet chip junction
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

**APPLICATIONS**

- Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

**DESCRIPTION**

The 8EWS..SPbF rectifier high voltage series has been optimized for very low forward voltage drop, with moderate leakage. The glass passivation technology used has reliable operation up to 150 °C junction temperature.

The **high reverse voltage** range available allows design of input stage primary rectification with **outstanding voltage surge** capability.

PRODUCT SUMMARY	
Package	TO-252AA (D-PAK)
$I_{F(AV)}$	8 A
$V_R$	800 V, 1200 V
$V_F$ at $I_F$	1.1 V
$I_{FSM}$	150 A
$T_J$ max.	150 °C
Diode variation	Single die

OUTPUT CURRENT IN TYPICAL APPLICATIONS			
APPLICATIONS	SINGLE-PHASE BRIDGE	THREE-PHASE BRIDGE	UNITS
NEMA FR-4 or G10 glass fabric-based epoxy with 4 oz. (140 $\mu$ m) copper	1.2	1.6	A
Aluminum IMS, $R_{thCA} = 15$ °C/W	2.5	2.8	
Aluminum IMS with heatsink, $R_{thCA} = 5$ °C/W	5.5	6.5	

**Note**

- $T_A = 55$  °C,  $T_J = 125$  °C, footprint 300 mm<sup>2</sup>

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Sinusoidal waveform at $T_C = 116$ °C	8	A
$V_{RRM}$		800/1200	V
$I_{FSM}$		150	A
$V_F$	8 A, $T_J = 25$ °C	1.10	V
$T_J$		-55 to +150	°C

VOLTAGE RATINGS			
PART NUMBER	$V_{RRM}$ , MAXIMUM PEAK REVERSE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ AT 150 °C mA
8EWS08SPbF	800	900	0.5
8EWS12SPbF	1200	1300	



ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	$T_C = 105\text{ }^\circ\text{C}$ , 180° conduction half sine wave	8	A
Maximum peak one cycle non-repetitive surge current	$I_{FSM}$	10 ms sine pulse, rated $V_{RRM}$ applied	125	
		10 ms sine pulse, no voltage reapplied	150	
Maximum $I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied	78	$\text{A}^2\text{s}$
		10 ms sine pulse, no voltage reapplied	110	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$ , no voltage reapplied	1100	$\text{A}^2\sqrt{\text{s}}$

ELECTRICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum forward voltage drop	$V_{FM}$	8 A, $T_J = 25\text{ }^\circ\text{C}$	1.1	V
Forward slope resistance	$r_t$	$T_J = 150\text{ }^\circ\text{C}$	20	$\text{m}\Omega$
Threshold voltage	$V_{F(TO)}$		0.82	V
Maximum reverse leakage current	$I_{RM}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{Rated } V_{RRM}$	0.05
		$T_J = 150\text{ }^\circ\text{C}$		0.50

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-55 to +150	$^\circ\text{C}$
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation	2.5	$^\circ\text{C/W}$
Typical thermal resistance, junction to ambient (PCB mount)	$R_{thJA}^{(1)}$		62	
Approximate weight			1	g
			0.03	oz.
Marking device		Case style TO-252AA (D-PAK)	8EWS12S	

**Note**

- <sup>(1)</sup> When mounted on 1" square (650 mm<sup>2</sup>) PCB of FR-4 or G-10 material 4 oz. (140  $\mu\text{m}$ ) copper 40  $^\circ\text{C/W}$   
For recommended footprint and soldering techniques refer to application note #AN-994

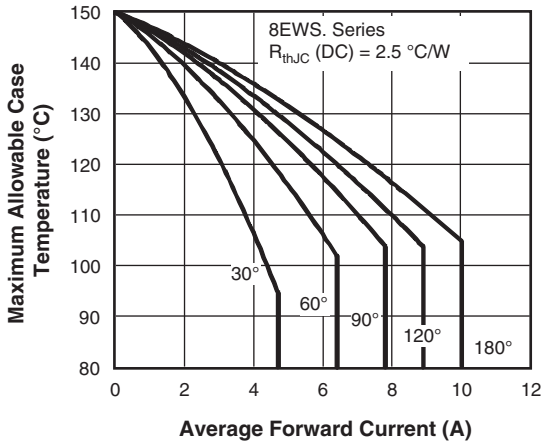


Fig. 1 - Current Rating Characteristics

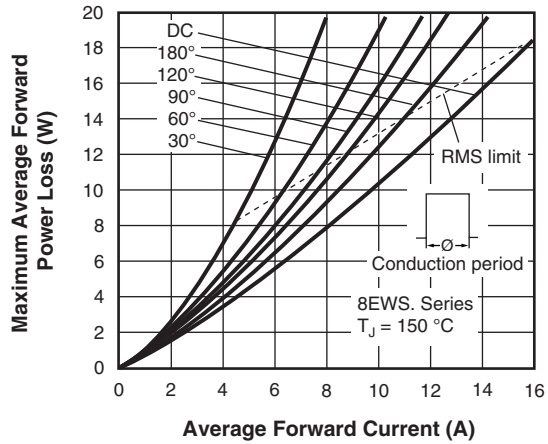


Fig. 4 - Forward Power Loss Characteristics

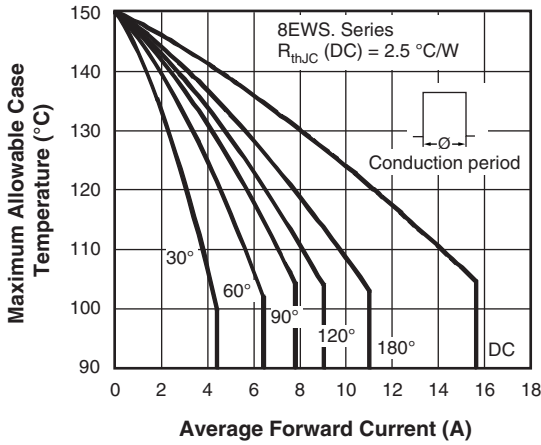


Fig. 2 - Current Rating Characteristics

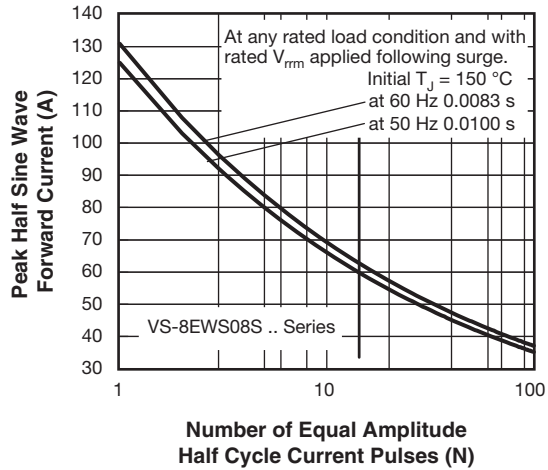


Fig. 5 - Maximum Non-Repetitive Surge Current

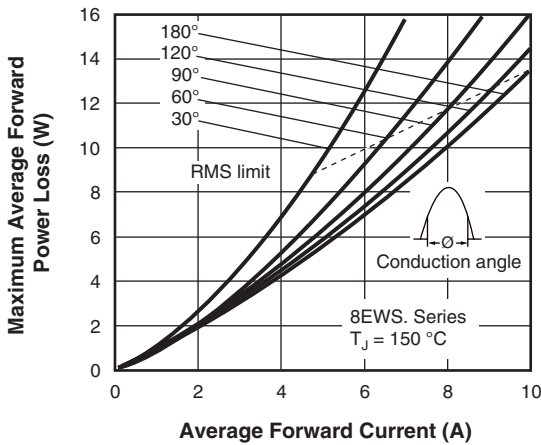


Fig. 3 - Forward Power Loss Characteristics

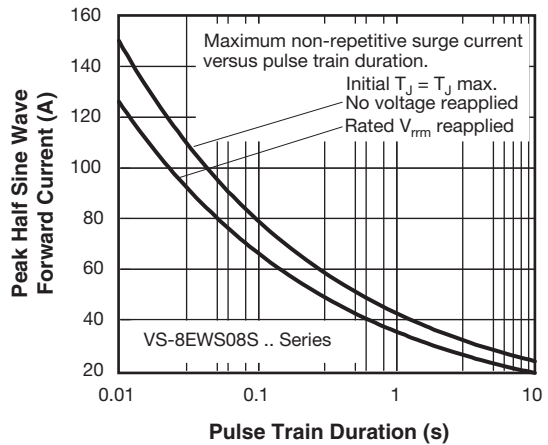


Fig. 6 - Maximum Non-Repetitive Surge Current

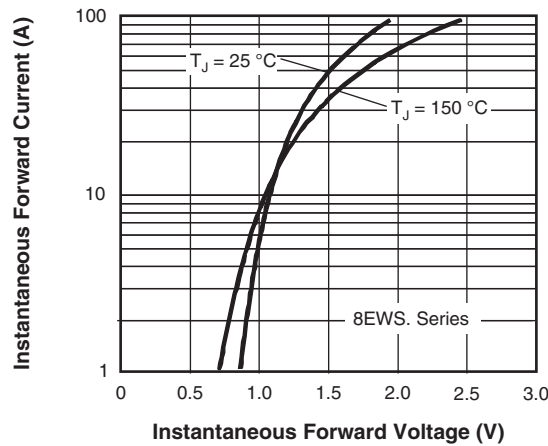


Fig. 7 - Forward Voltage Drop Characteristics

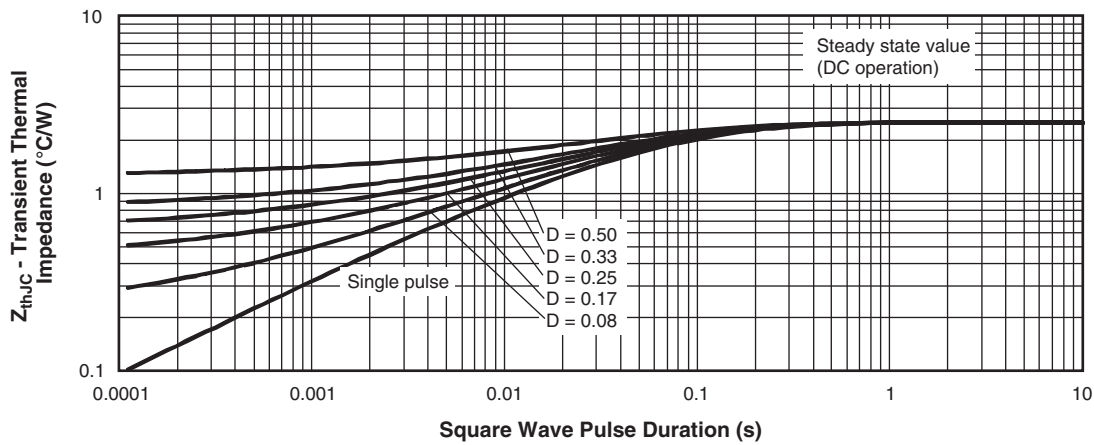
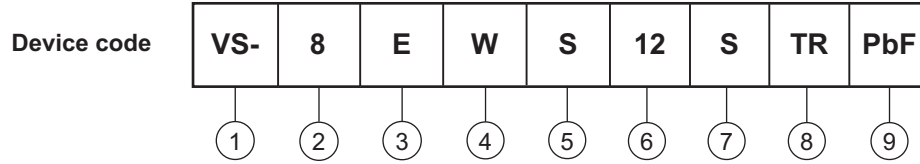


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics



## ORDERING INFORMATION TABLE

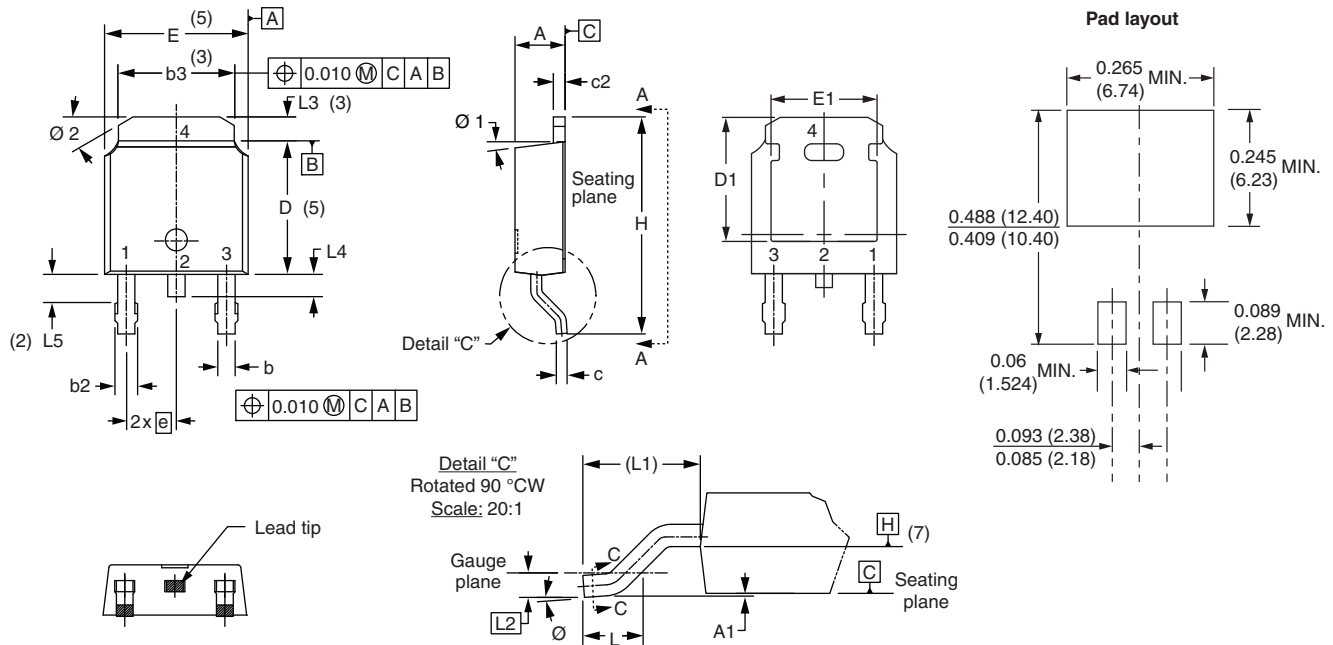


- 1** - Vishay Semiconductors product
- 2** - Current rating (8 = 8 A)
- 3** - Circuit configuration:  
E = single diode
- 4** - Package:  
W = D-PAK
- 5** - Type of silicon:  
S = standard recovery rectifier
- 6** - Voltage ratings 08 = 800 V  
12 = 1200 V
- 7** - S = surface mountable
- 8** -
  - TR = tape and reel
  - TRR = tape and reel (right oriented)
  - TRL = tape and reel (left oriented)
- 9** - PbF = lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95016">www.vishay.com/doc?95016</a>
Part marking information	<a href="http://www.vishay.com/doc?95059">www.vishay.com/doc?95059</a>
Packaging information	<a href="http://www.vishay.com/doc?95033">www.vishay.com/doc?95033</a>

### D-PAK (TO-252AA)

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094		e	2.29 BSC		0.090 BSC		
A1	-	0.13	-	0.005		H	9.40	10.41	0.370	0.410	
b	0.64	0.89	0.025	0.035		L	1.40	1.78	0.055	0.070	
b2	0.76	1.14	0.030	0.045		L1	2.74 BSC		0.108 REF.		
b3	4.95	5.46	0.195	0.215	3	L2	0.51 BSC		0.020 BSC		
c	0.46	0.61	0.018	0.024		L3	0.89	1.27	0.035	0.050	3
c2	0.46	0.89	0.018	0.035		L4	-	1.02	-	0.040	
D	5.97	6.22	0.235	0.245	5	L5	1.14	1.52	0.045	0.060	2
D1	5.21	-	0.205	-	3	∅	0°	10°	0°	10°	
E	6.35	6.73	0.250	0.265	5	∅1	0°	15°	0°	15°	
E1	4.32	-	0.170	-	3	∅2	25°	35°	25°	35°	

**Notes**

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA



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