



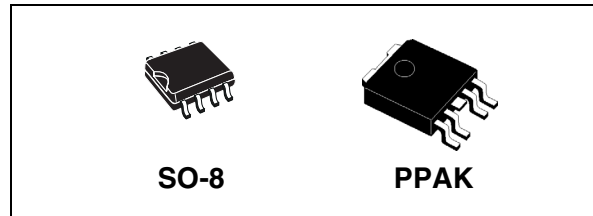
**THE DATASHEET OF
VN800STR-E**



Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN800S VN800PT	135 m Ω	0.7 A	36 V

- CMOS-compatible input
- Thermal shutdown
- Current limitation
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protected (see [Application schematic](#))



Description

The VN800S and VN800PT are monolithic devices designed in STMicroelectronics VIPower M0-3 technology. The VN800S and VN800PT are intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device automatically turns off in the case where the ground pin becomes disconnected.

This device is especially suitable for industrial applications in norms conformity with IEC1131 (programmable controllers international standard).

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-8	VN800S	VN800S13TR
PPAK	VN800PT	VN800PT13TR

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	13
3	Application information	15
3.1	GND protection network against reverse battery	15
3.1.1	Solution 1: resistor in the ground line (RGND only)	15
3.1.2	Solution 2: diode (DGND) in the ground line	16
3.2	MCU I/Os protection	16
3.3	SO-8 maximum demagnetization energy (VCC = 13.5V)	17
3.4	PPAK maximum demagnetization energy (VCC = 13.5V)	18
4	Package and PCB thermal data	19
4.1	SO-8 thermal data	19
4.2	PPAK thermal data	21
5	Package and packing information	24
5.1	ECOPACK® packages	24
5.2	SO-8 package information	24
5.3	PPAK mechanical data	26
5.4	SO-8 packing information	28
5.5	PPAK packing information	29
6	Revision history	31

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	5
Table 3.	Absolute maximum ratings	6
Table 4.	Thermal data.	7
Table 5.	Power	8
Table 6.	Switching ($V_{CC}=13V$)	8
Table 7.	Input pin	9
Table 8.	V_{CC} output diode.	9
Table 9.	Status pin	9
Table 10.	Protections	9
Table 11.	Truth table.	10
Table 12.	SO-8 thermal parameters	21
Table 13.	PPAK thermal parameters	23
Table 14.	SO-8 mechanical data	25
Table 15.	PPAK mechanical data	26
Table 16.	Document revision history	31

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Current and voltage conventions	6
Figure 4.	Over-temperature status timing	10
Figure 5.	Switching time waveforms	10
Figure 6.	Peak short circuit current test circuit.	11
Figure 7.	Avalanche energy test circuit	11
Figure 8.	Waveforms	12
Figure 9.	Off-state output current.	13
Figure 10.	High-level input current.	13
Figure 11.	Over-voltage shutdown.	13
Figure 12.	Status leakage current	13
Figure 13.	Turn-on voltage slope.	13
Figure 14.	Turn-off voltage slope.	13
Figure 15.	On-state resistance Vs T_{case}	14
Figure 16.	On-state resistance Vs V_{CC}	14
Figure 17.	I_{lim} Vs T_{case}	14
Figure 18.	Input high-level	14
Figure 19.	Input low-level.	14
Figure 20.	Input hysteresis voltage	14
Figure 21.	Application schematic	15
Figure 22.	SO-8 maximum turn-off current versus inductance	17
Figure 23.	PPAK maximum turn-off current versus inductance	18
Figure 24.	SO-8 PC board	19
Figure 25.	SO-8 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition	19
Figure 26.	SO-8 thermal impedance junction ambient single pulse	20
Figure 27.	SO-8 thermal fitting model of a single channel	20
Figure 28.	PPAK PC board	21
Figure 29.	PPAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition	22
Figure 30.	PPAK thermal impedance junction ambient single pulse	22
Figure 31.	PPAK thermal fitting model of a single channel	23
Figure 32.	SO-8 package dimensions	24
Figure 33.	PPAK package dimensions	26
Figure 34.	SO-8 tube shipment (no suffix)	28
Figure 35.	SO-8 tape and reel shipment (suffix "TR")	28
Figure 36.	PPAK suggested pad layout.	29
Figure 37.	PPAK tube shipment (no suffix)	29
Figure 38.	PPAK tape and reel (suffix "13TR")	30

1 Block diagram and pin description

Figure 1. Block diagram

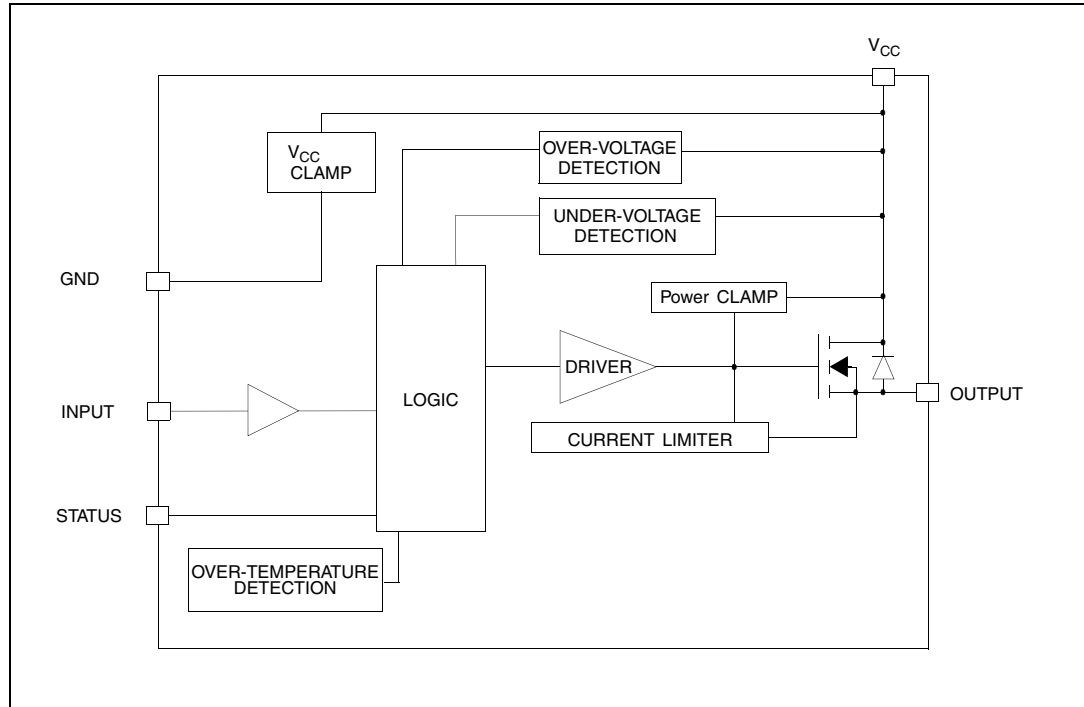


Figure 2. Configuration diagram (top view)

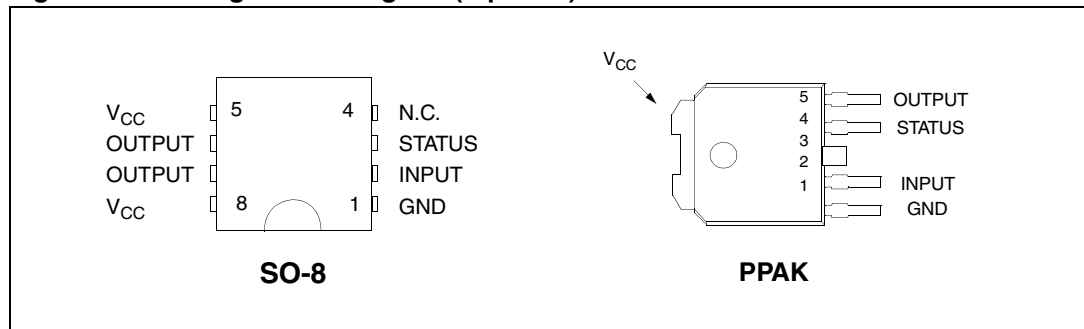
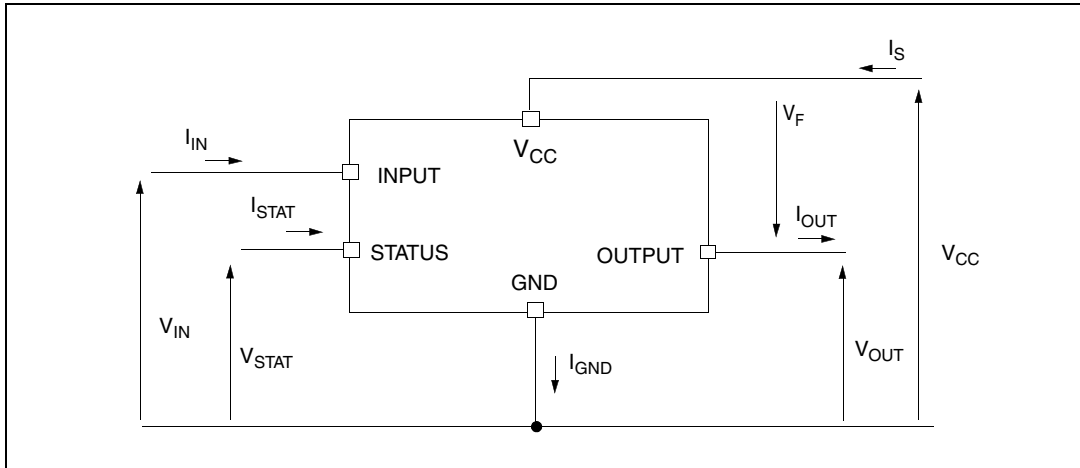


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
V_{CC}	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	- 0.3		V
$-I_{GND}$	DC reverse ground pin current	- 200		mA
I_{OUT}	DC output current	Internally limited		A
$-I_{OUT}$	Reverse DC output current	- 6		A
I_{IN}	DC input current	+/- 10		mA
V_{IN}	Input voltage range	- 3 / + V_{CC}		mA
V_{STAT}	DC status voltage	+ V_{CC}		
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5K\Omega$; $C = 100pF$)			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	- V_{CC}	5000		V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
E_{MAX}	Maximum switching energy ($L = 77.5\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_L = 1.5\text{A}$)	121	-	mJ
E_{MAX}	Maximum switching energy ($L = 125\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_L = 1.5\text{A}$)	-	195	mJ
P_{tot}	Power dissipation $T_C = 25^\circ\text{C}$	4.2	41.7	W
T_j	Junction operating temperature	Internally limited		$^\circ\text{C}$
T_C	Case operating temperature	- 40 to 150		$^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 150		$^\circ\text{C}$
L_{max}	Max inductive load ($V_{CC} = 30\text{V}$; $I_{LOAD} = 0.5\text{A}$; $T_{amb} = 100^\circ\text{C}$; $R_{th_{case > ambient}} \leq 25^\circ\text{C/W}$)		2	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
		SO-8	PPAK	
$R_{thj-case}$	Thermal resistance junction-case	-	3	$^\circ\text{C/W}$
$R_{thj-lead}$	Thermal resistance junction-lead	30	-	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	93 ⁽¹⁾	78 ⁽²⁾	$^\circ\text{C/W}$
		82 ⁽³⁾	45 ⁽⁴⁾	$^\circ\text{C/W}$

1. When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35µm thick) connected to all V_{CC} pins.
2. When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35µm thick) connected to all V_{CC} pins.
3. When mounted on FR4 printed circuit board with 2 cm² of copper area (at least 35µm thick).
4. When mounted on FR4 printed circuit board with 6 cm² of copper area (at least 35µm thick).

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
V_{OV}	Over-voltage shutdown		36	42		V
R_{ON}	On-state resistance	$I_{OUT} = 0.5A$; $T_j = 25^{\circ}C$; $I_{OUT} = 0.5A$;			135 270	$m\Omega$ $m\Omega$
I_S	Supply current	Off-state; $V_{CC} = 24V$; $T_{case} = 25^{\circ}C$		10	25	μA
		On-state; $V_{CC} = 24V$;		10	20	μA
		On-state; $V_{CC} = 24V$;		2	3.5	mA
I_{LGND}	Output current at turn-off	$V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24V$; $V_{OUT} = 0V$			1	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			5	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			3	μA

Table 6. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 48\Omega$ from V_{IN} rising edge to $V_{OUT} = 2.4V$		10		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 48\Omega$ from V_{IN} falling edge to $V_{OUT} = 21.6V$		40		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 2.4V$ to $V_{OUT} = 19.2V$	See Figure 13.			$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 21.6V$ to $V_{OUT} = 2.4V$	See Figure 14.			$V/\mu s$

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level				1.25	V
I_{IL}	Low-level input current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input high-level		3.25			V
I_{IH}	High-level input current	$V_{IN} = 3.25V$			10	μA
V_{hyst}	Input hysteresis voltage		0.5			V
I_{IN}	Input clamp voltage	$V_{IN} = V_{CC} = 36V$			200	μA

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- $I_{OUT} = 0.6A$; $T_j = 150^\circ C$			0.7	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = V_{CC} = 36V$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			30	pF

Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ C$
T_R	Reset temperature		135			$^\circ C$
T_{hyst}	Thermal hysteresis		7	15		$^\circ C$
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	μs
I_{lim}	Current limitation	$V_{CC} = 24V$ $R_{LOAD} = 10m\Omega$	0.7		2	A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 0.5A$; $L = 6mH$	$V_{CC} - 47$	$V_{CC} - 52$	$V_{CC} - 57$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Figure 4. Over-temperature status timing

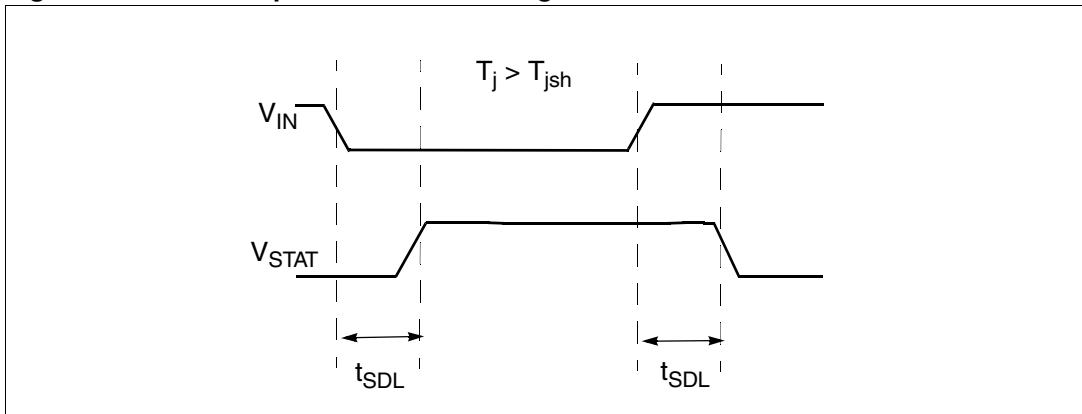


Figure 5. Switching time waveforms

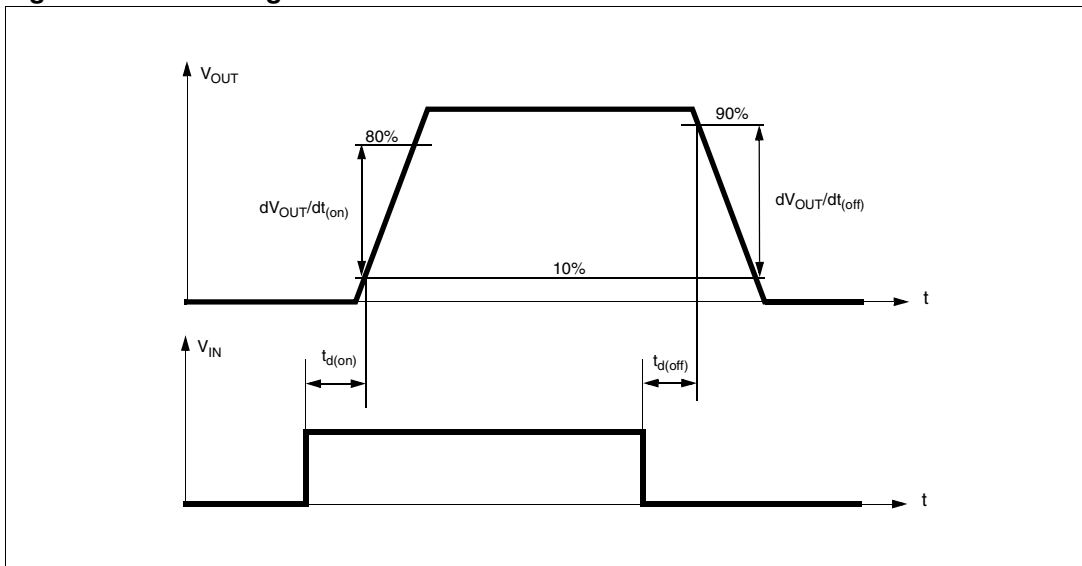


Table 11. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Over-temperature	L	L	H
	H	L	L
Under-voltage	L	L	X
	H	L	X
Over-voltage	L	L	H
	H	L	H

Figure 6. Peak short circuit current test circuit

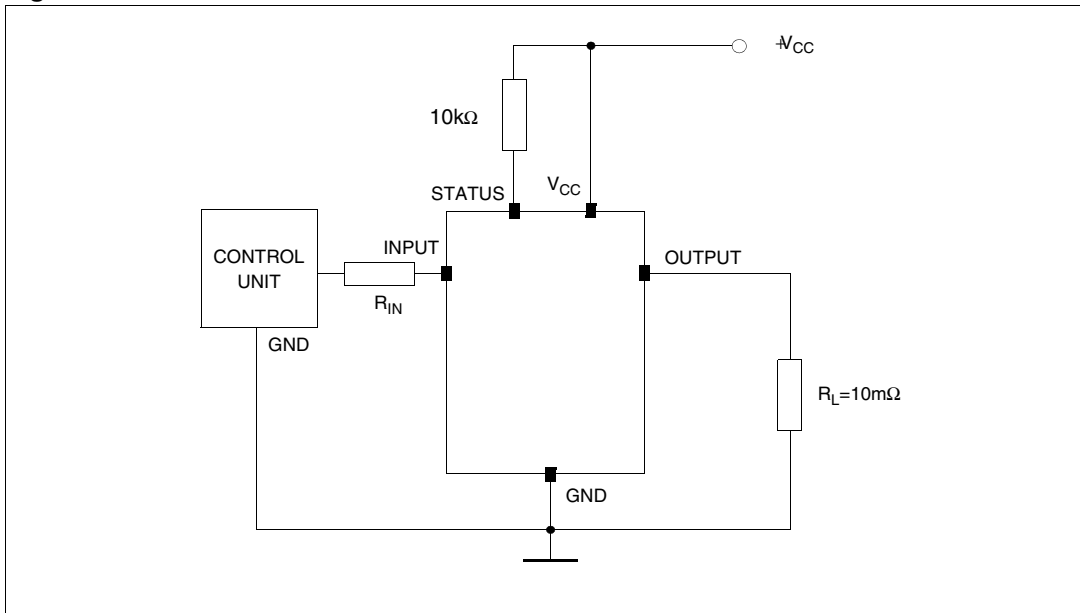


Figure 7. Avalanche energy test circuit

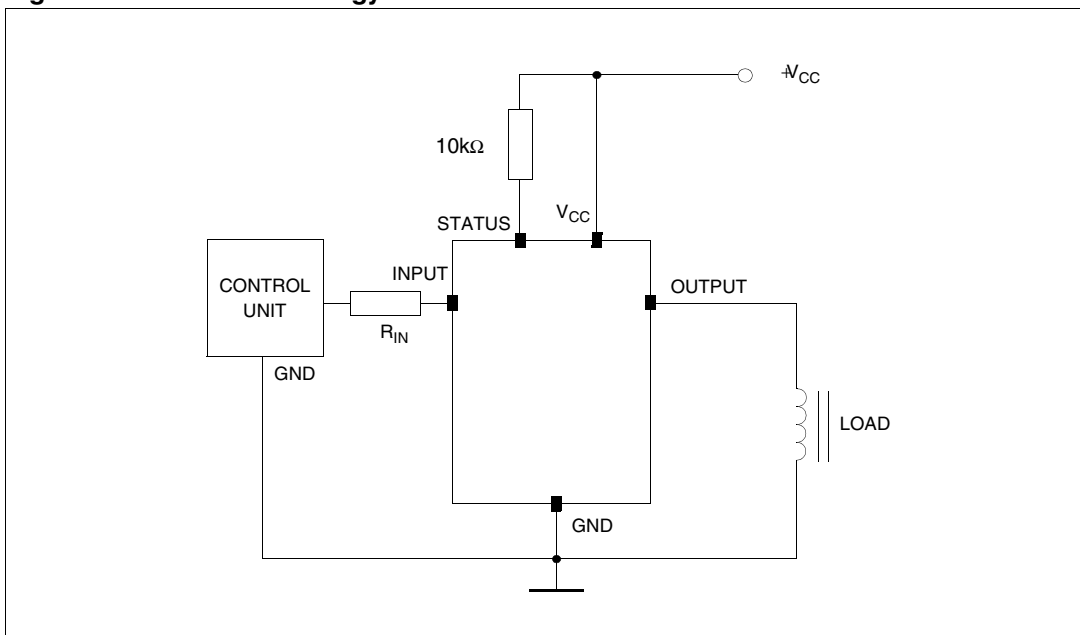
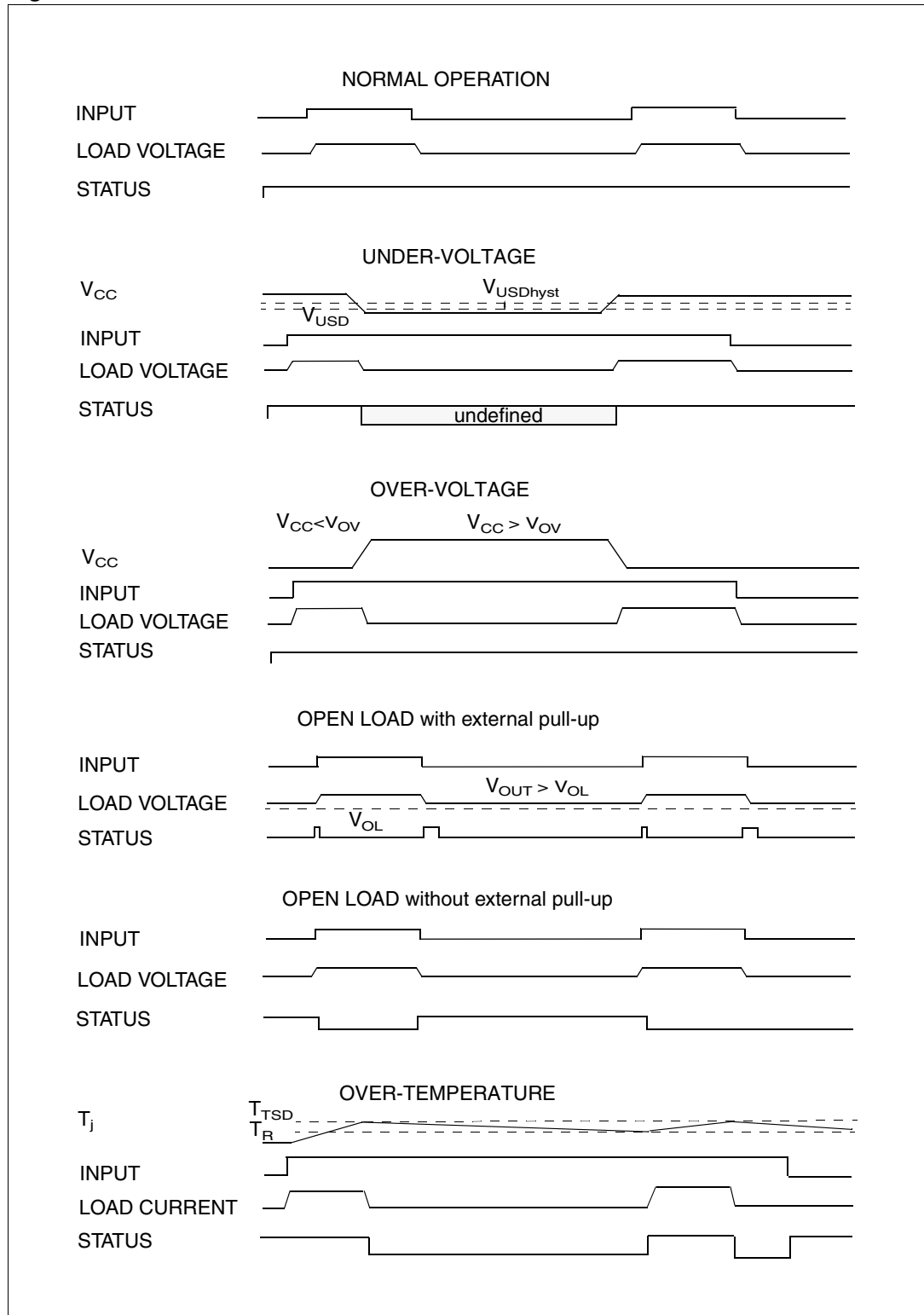


Figure 8. Waveforms



2.4 Electrical characteristics curves

Figure 9. Off-state output current

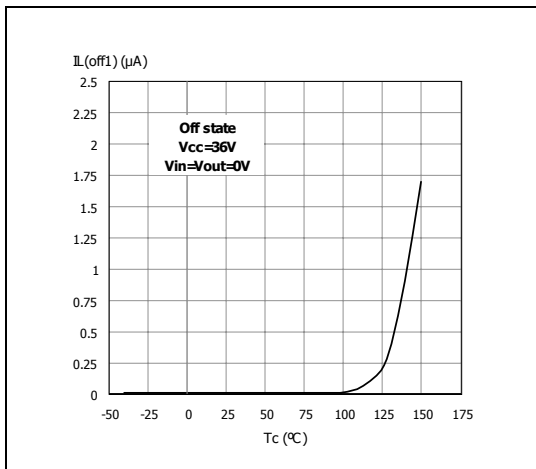


Figure 10. High-level input current

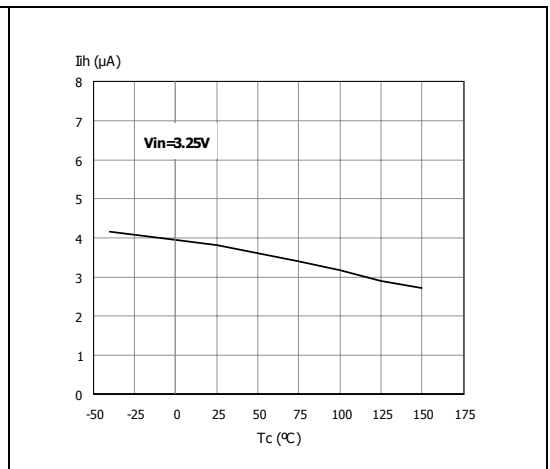


Figure 11. Over-voltage shutdown

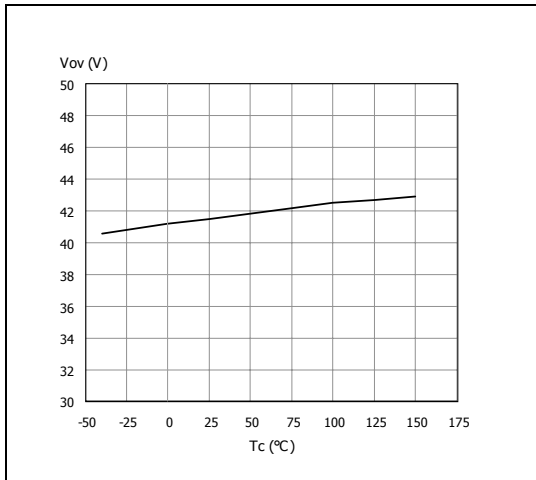


Figure 12. Status leakage current

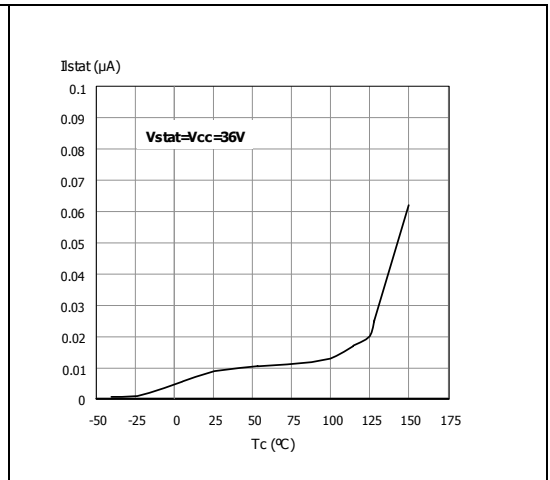


Figure 13. Turn-on voltage slope

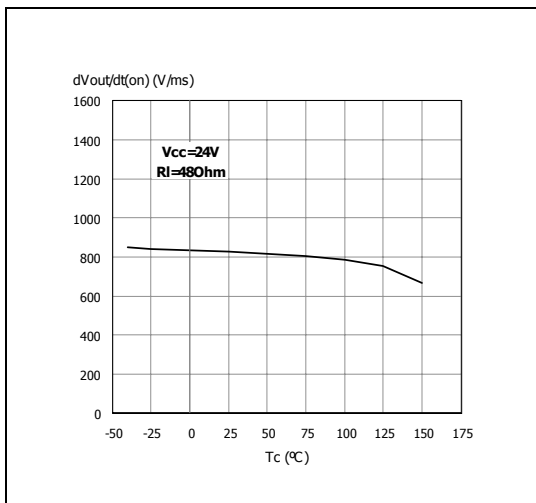


Figure 14. Turn-off voltage slope

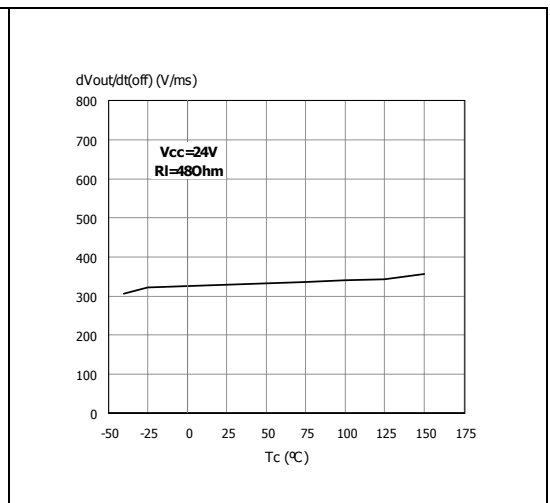


Figure 15. On-state resistance Vs T_{case}

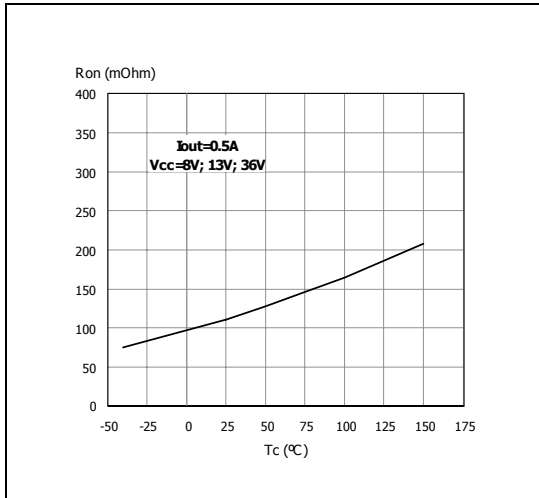


Figure 16. On-state resistance Vs V_{CC}

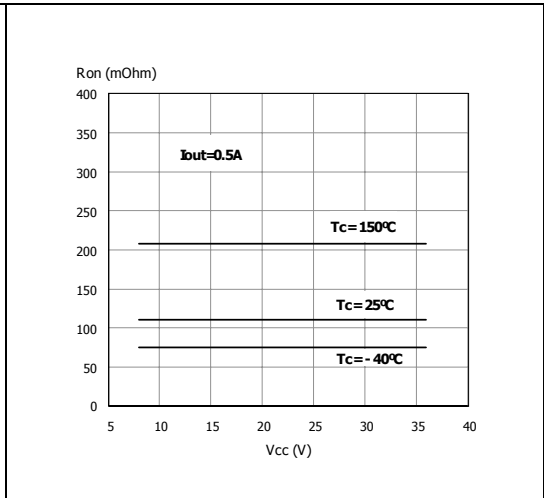


Figure 17. I_{lim} Vs T_{case}

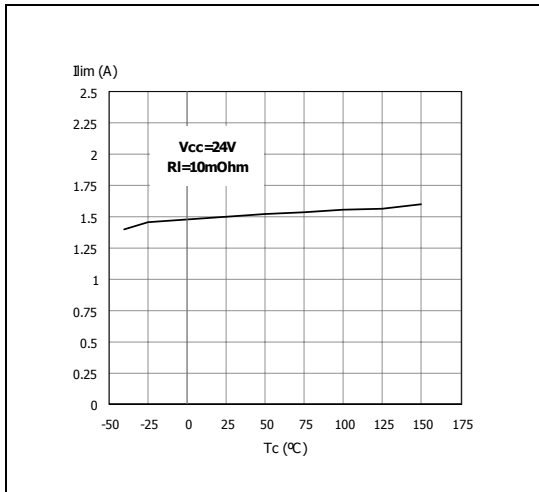


Figure 18. Input high-level

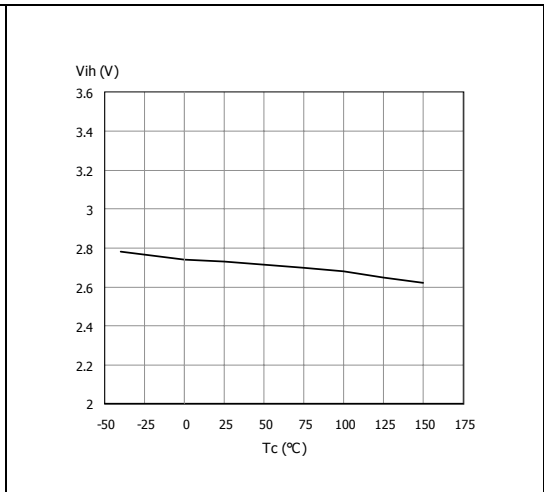


Figure 19. Input low-level

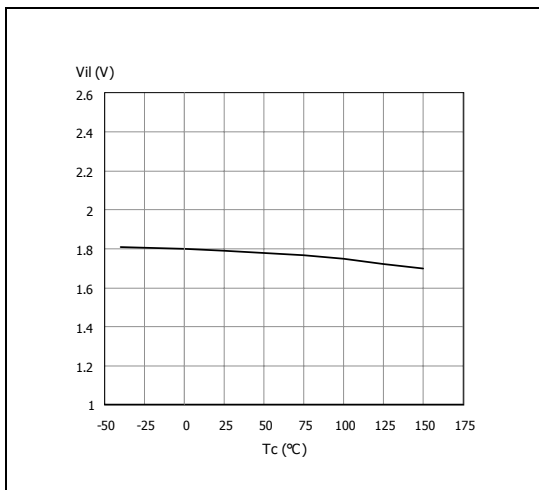
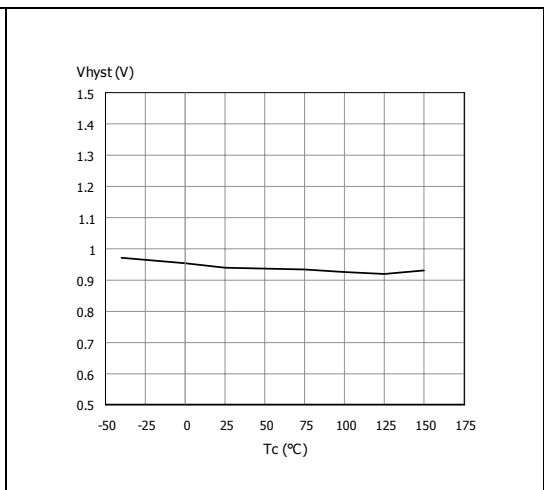
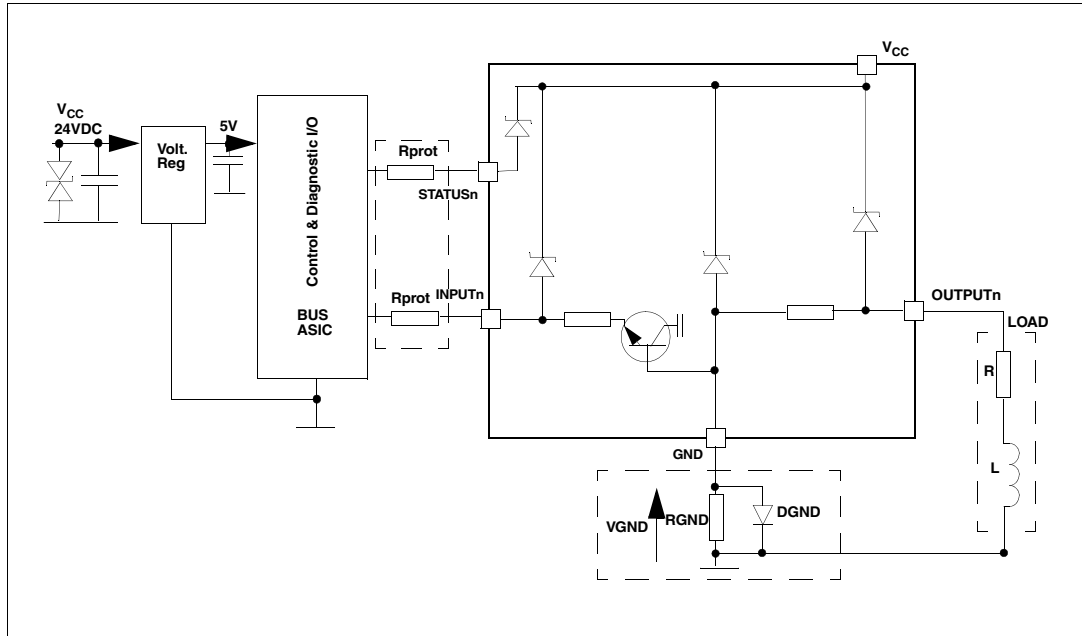


Figure 20. Input hysteresis voltage



3 Application information

Figure 21. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

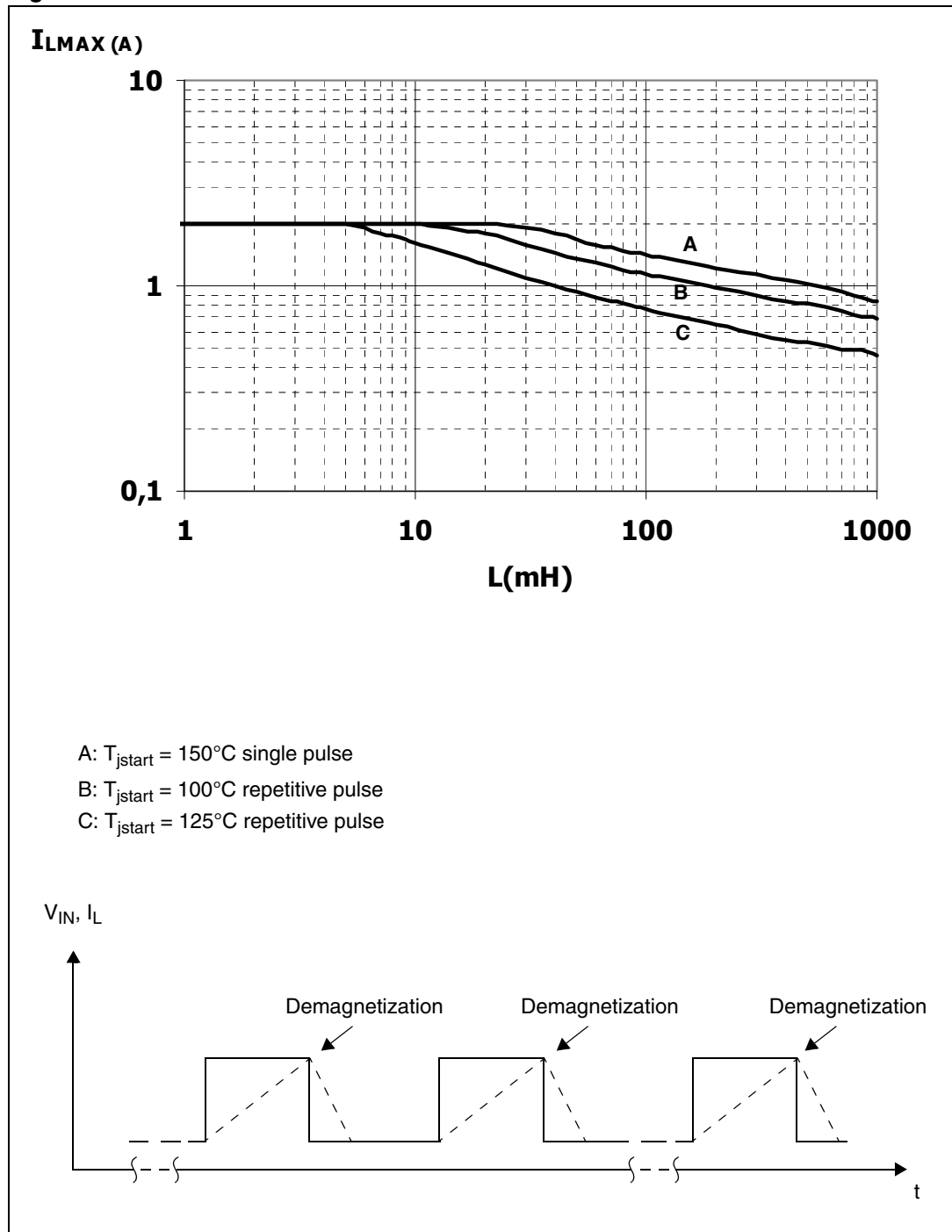
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$.

3.3 SO-8 maximum demagnetization energy ($V_{CC} = 13.5V$)

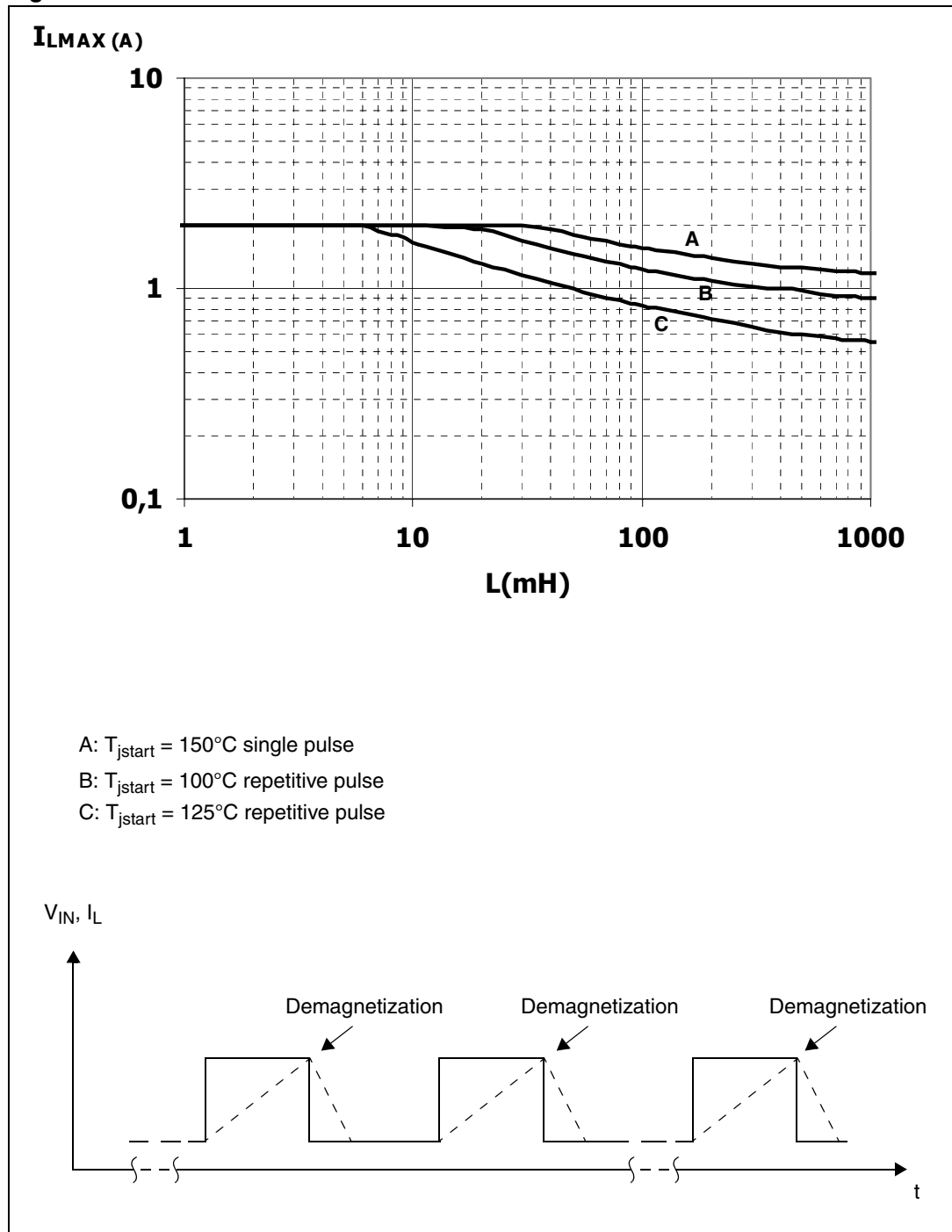
Figure 22. SO-8 maximum turn-off current versus inductance



Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.4 PPAK maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 23. PPAK maximum turn-off current versus inductance

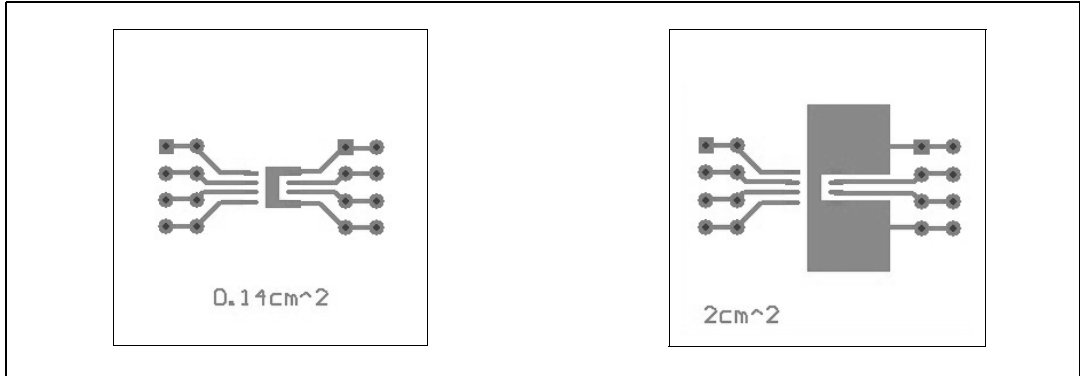


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 24. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: 0.14 cm², 2 cm²).

Figure 25. SO-8 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

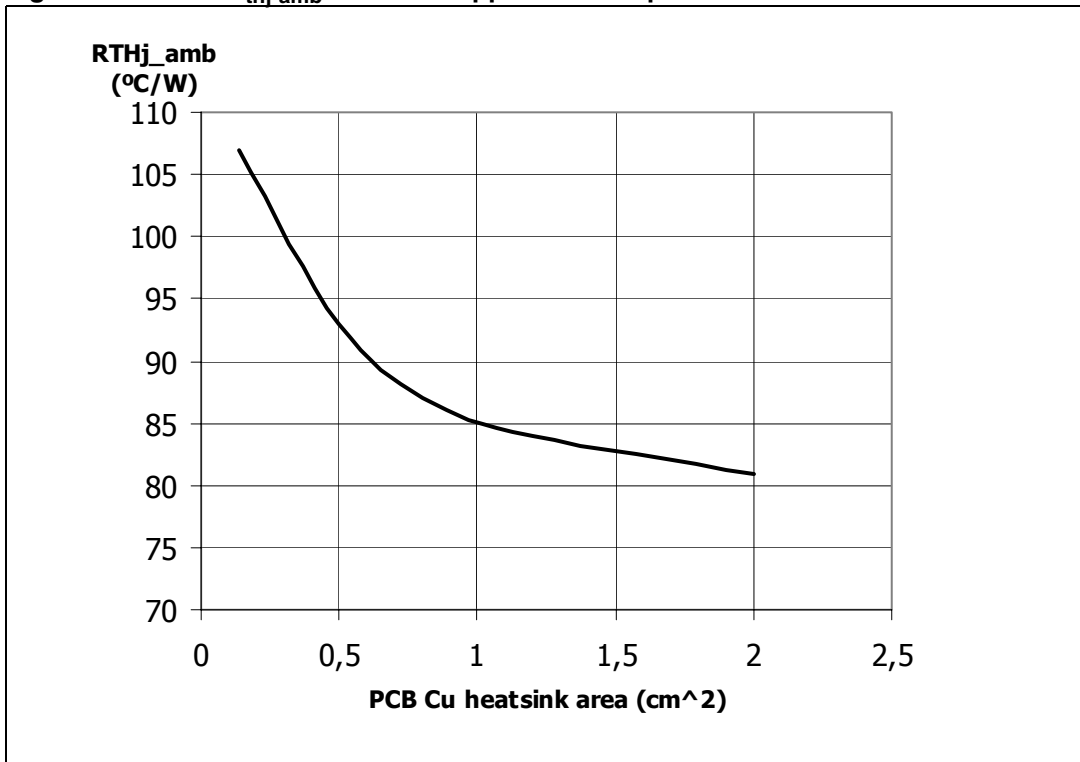
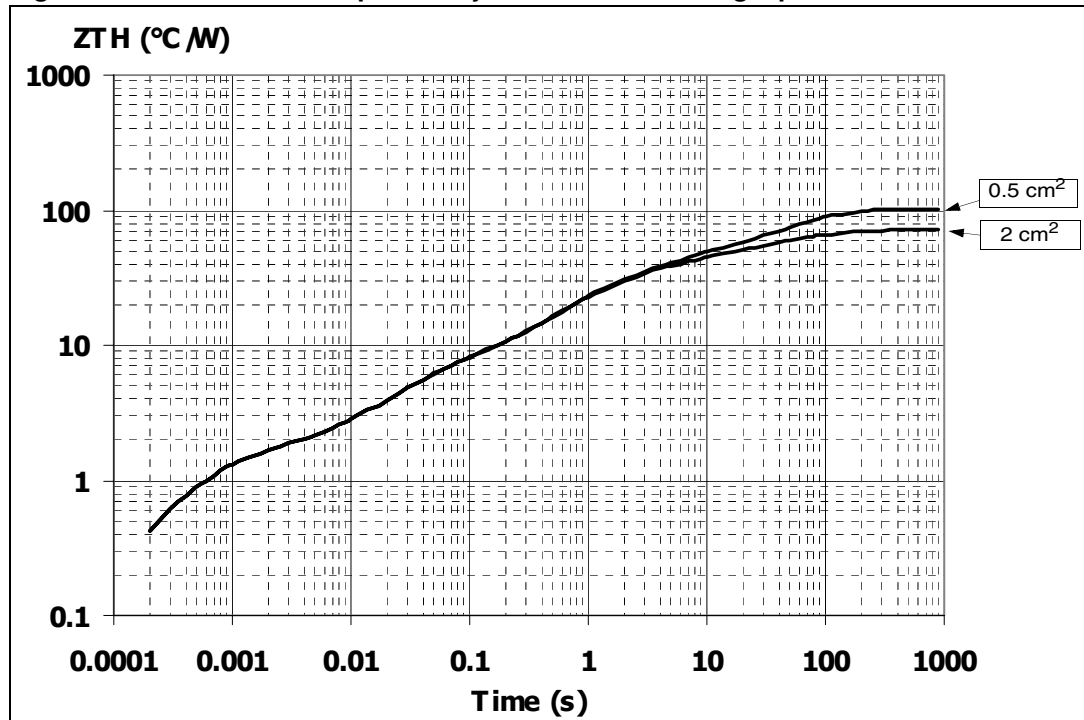


Figure 26. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 27. SO-8 thermal fitting model of a single channel

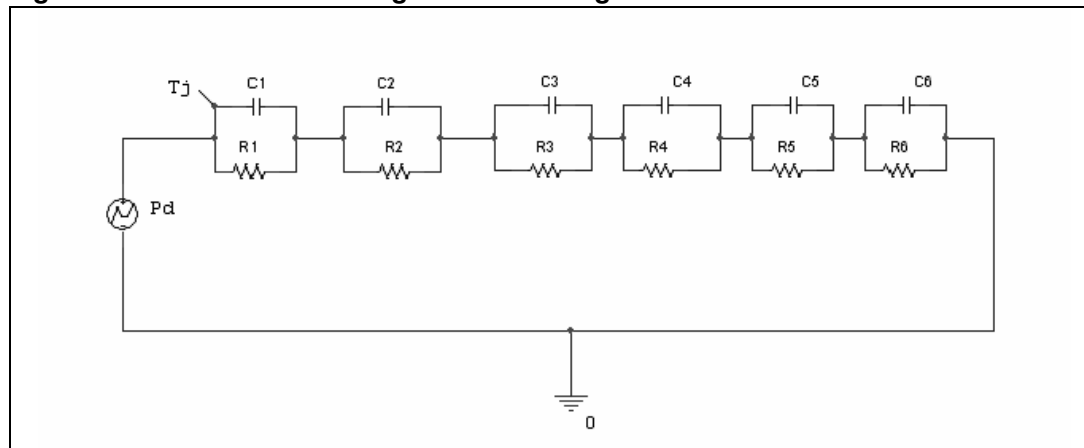
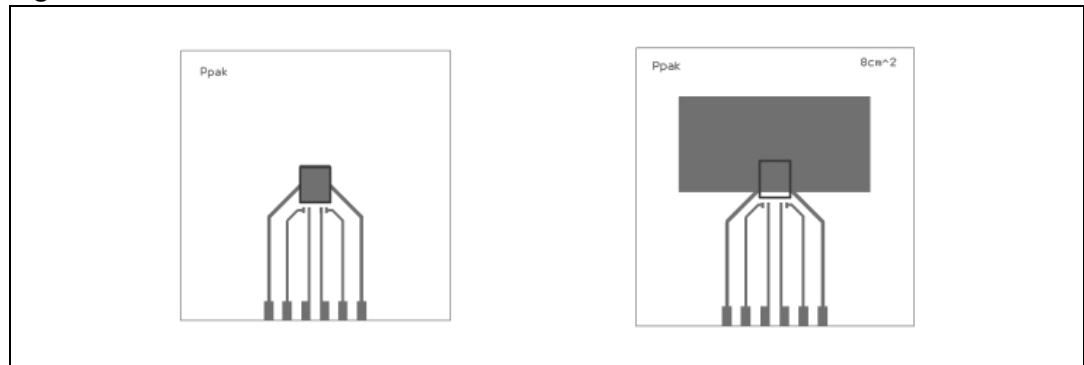


Table 12. SO-8 thermal parameters

Area/island (cm ²)	0.14	2
R1 (°C/W)	0.24	
R2 (°C/W)	1.2	
R3 (°C/W)	4.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.00015	
C2 (W·s/°C)	0.0005	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

4.2 PPAK thermal data

Figure 28. PPAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness=35 μ m , Copper areas: 0.44 cm², 8 cm²).

Figure 29. PPAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

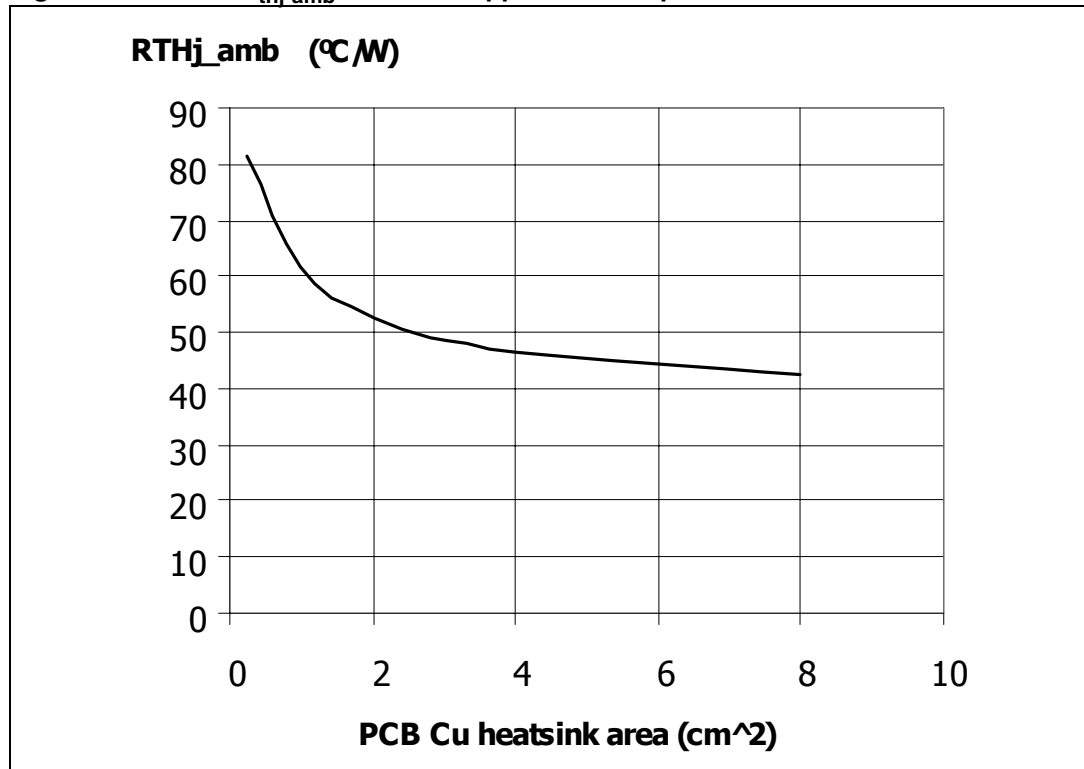
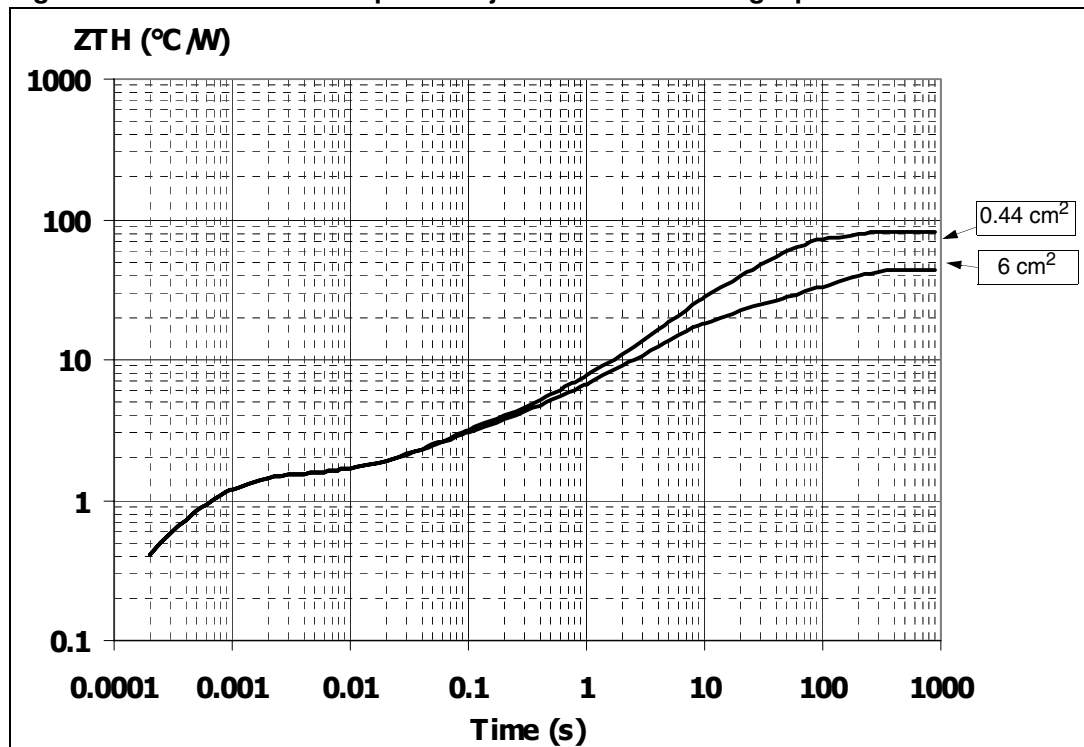


Figure 30. PPAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. PPAK thermal fitting model of a single channel

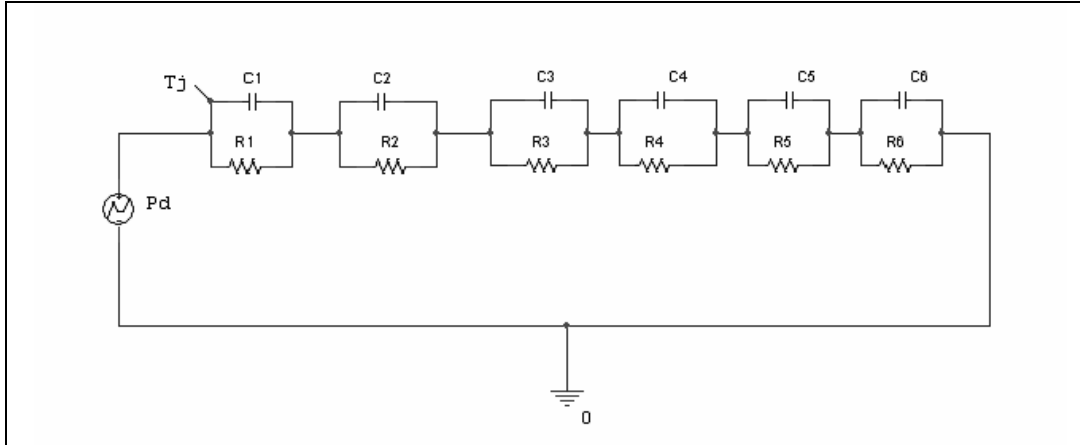


Table 13. PPAK thermal parameters

Area/island (cm ²)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.02	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 package information

Figure 32. SO-8 package dimensions

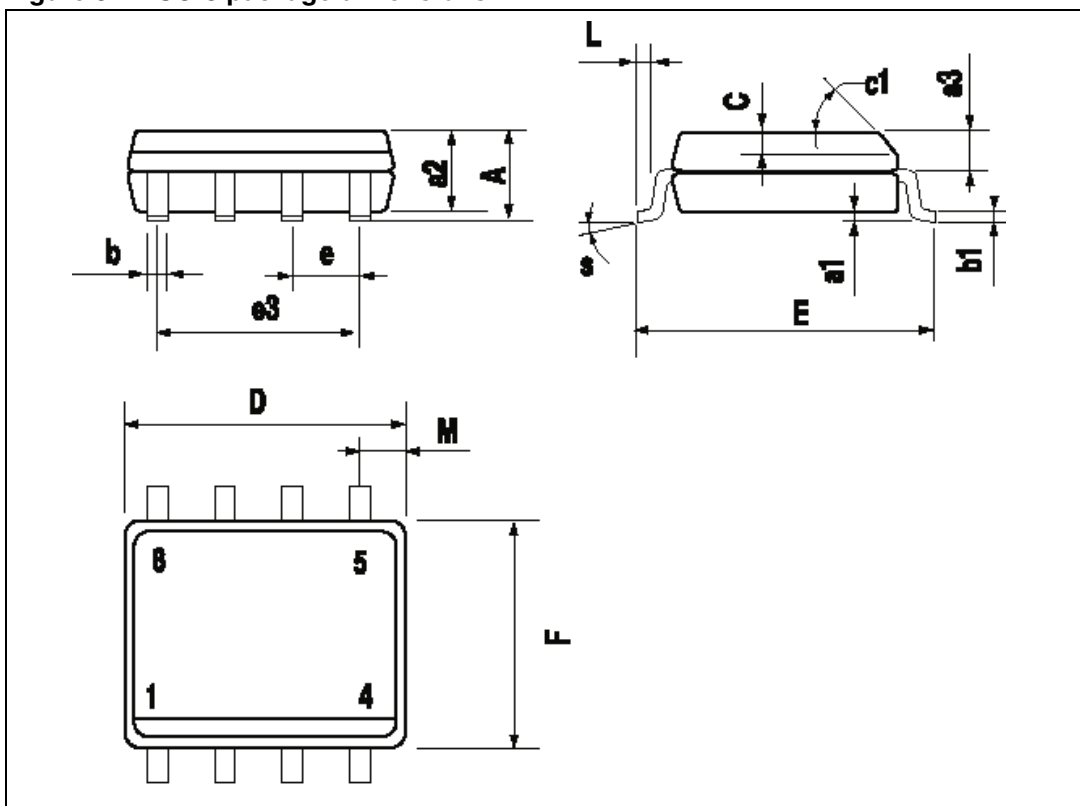


Table 14. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

5.3 PPAK mechanical data

Figure 33. PPAK package dimensions

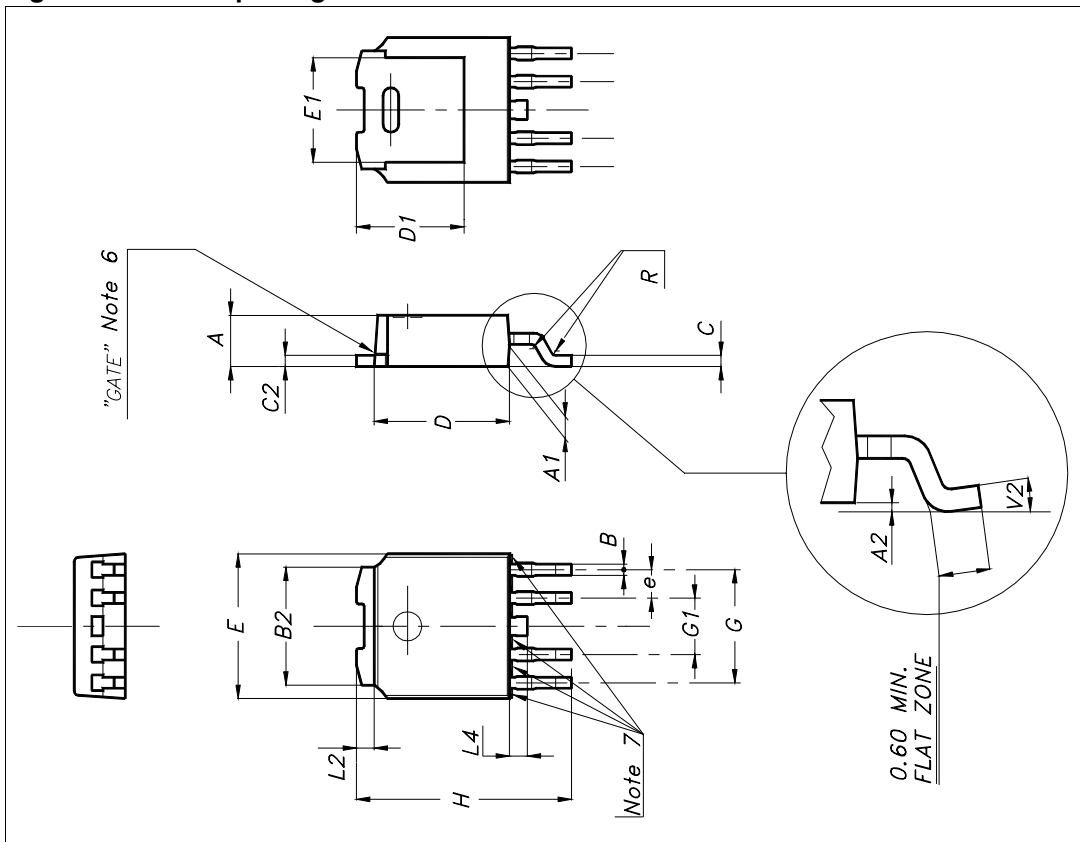


Table 15. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60

Table 15. PPAK mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

5.4 SO-8 packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 34. SO-8 tube shipment (no suffix)

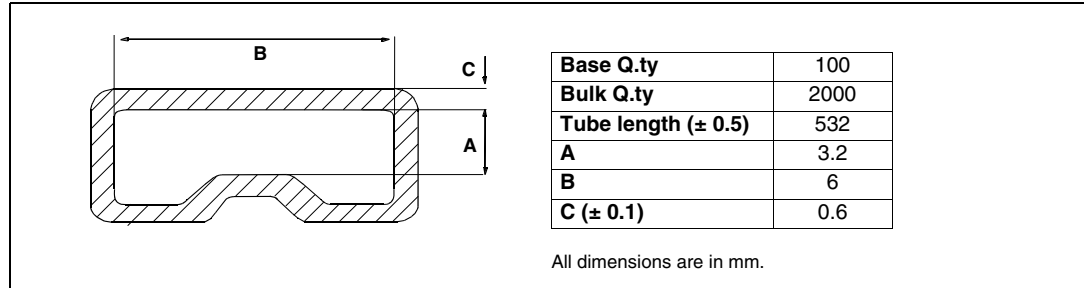
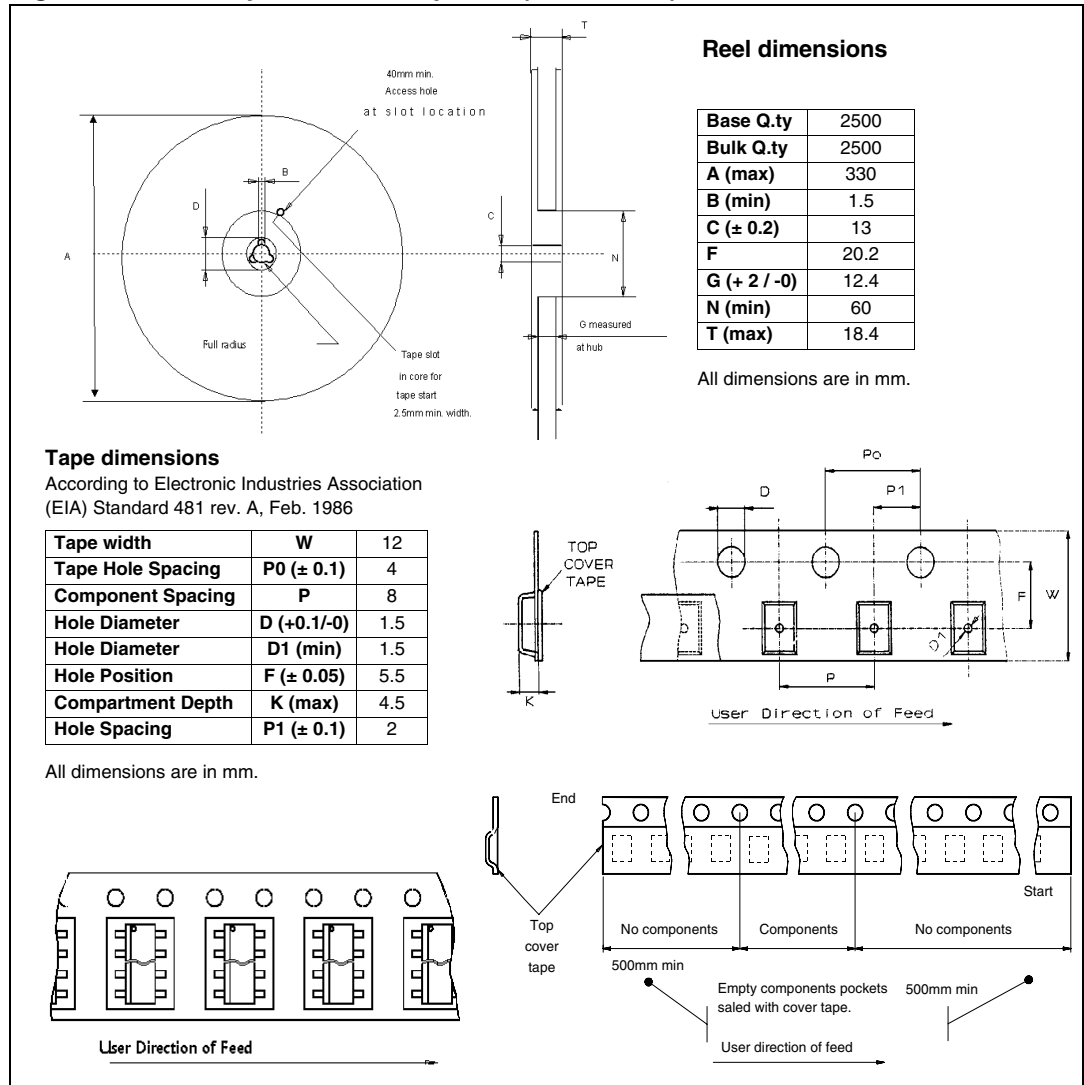


Figure 35. SO-8 tape and reel shipment (suffix “TR”)



5.5 PPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 36. PPAK suggested pad layout

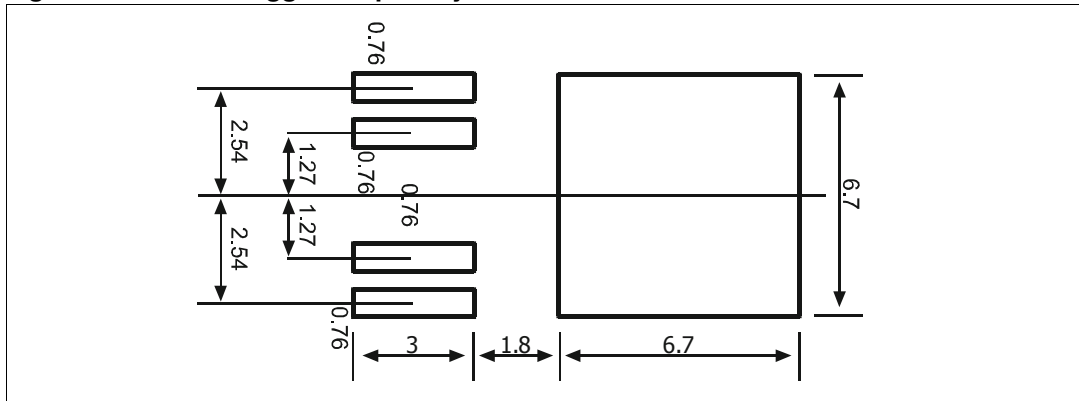


Figure 37. PPAK tube shipment (no suffix)

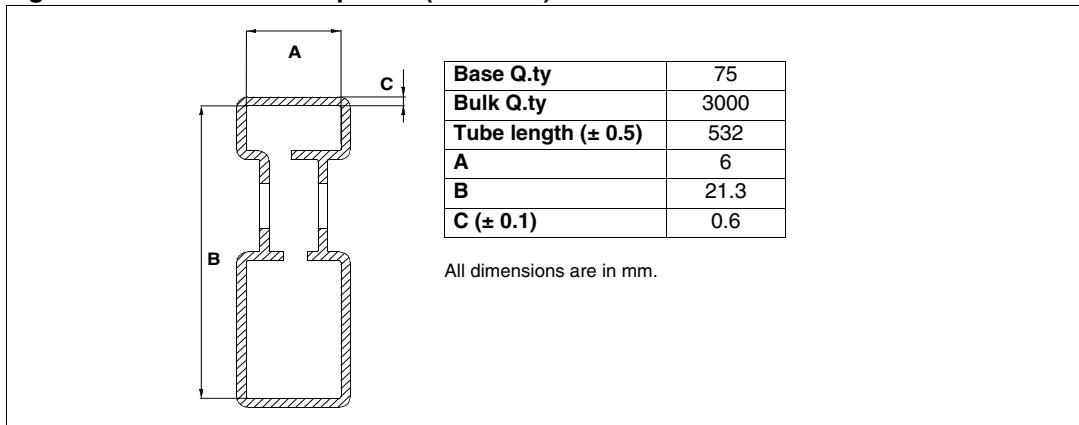
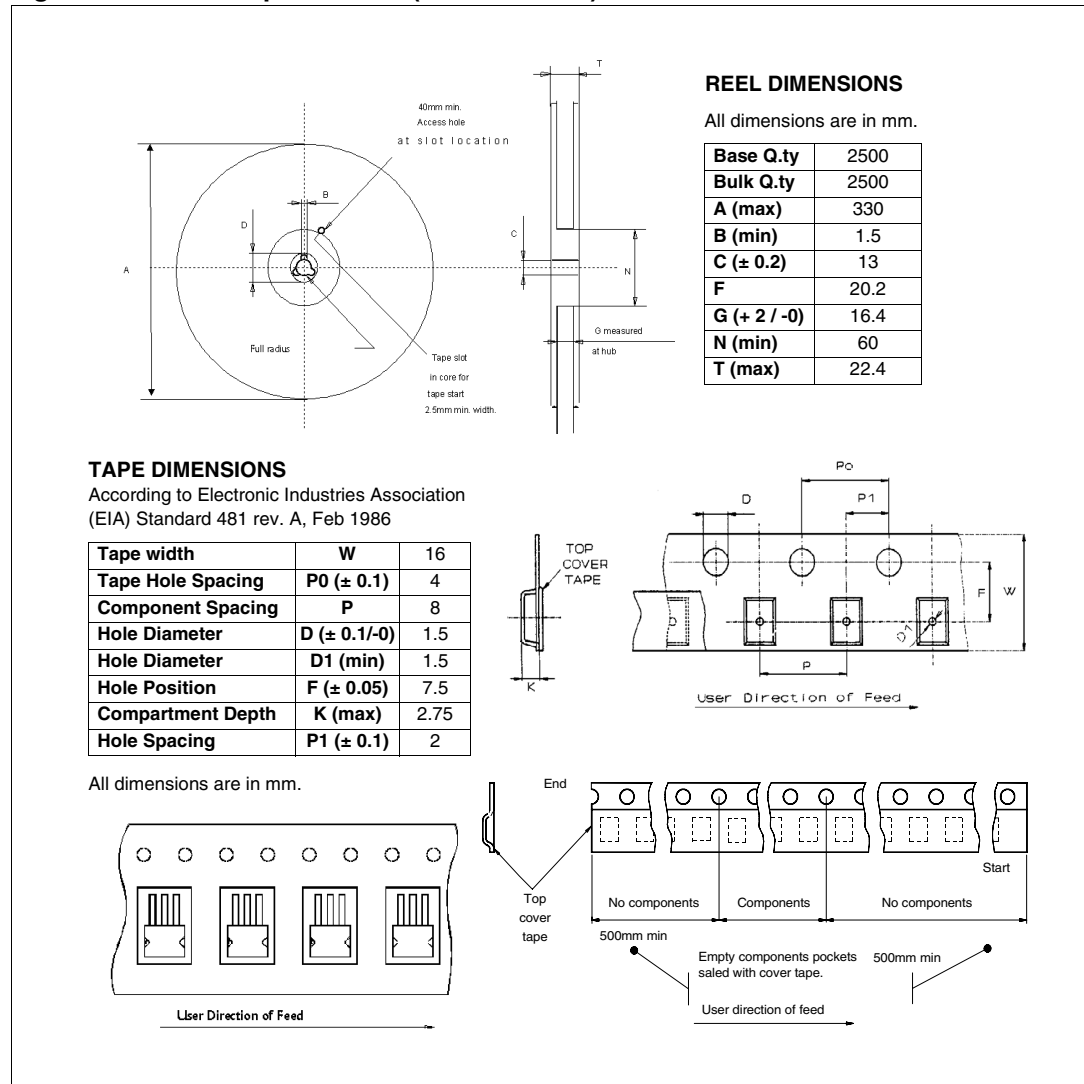


Figure 38. PPAK tape and reel (suffix "13TR")



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
09-Sep-2004	1	Initial release.
03-May-2006	2	Current and voltage convention update (page 2). Configuration diagram (top view) and suggested connections for unused and n.c. pins insertion (page 2). 6cm ² Cu condition insertion in thermal data table (page 3). V _{CC} - output diode section update (page 4). Protections note insertion (page 4). Revision history table insertion (page 21). Disclaimers update (page 22).
24-Nov-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK[®] packages</i> information.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View VN800STR-E on WIN SOURCE](#)
-  [STMicroelectronics](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management