



**THE DATASHEET OF  
A6821SLW-T**



## DABiC-5 8-Bit Serial Input Latched Sink Drivers

### Features and Benefits

- 3.3 to 5 V logic supply range
- Power on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible
- -40°C operation available
- Schmitt trigger inputs for improved noise immunity
- Low-power CMOS logic and latches
- High-voltage current-sink outputs
- Internal pull-up/pull down resistors

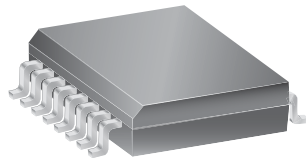
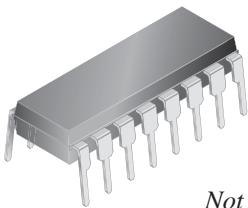
### Applications:

- Multiplexed LED displays
- Incandescent lamps

### Packages:

Package A 16-pin DIP

Package LW 16-pin SOICW



Not to scale

### Description

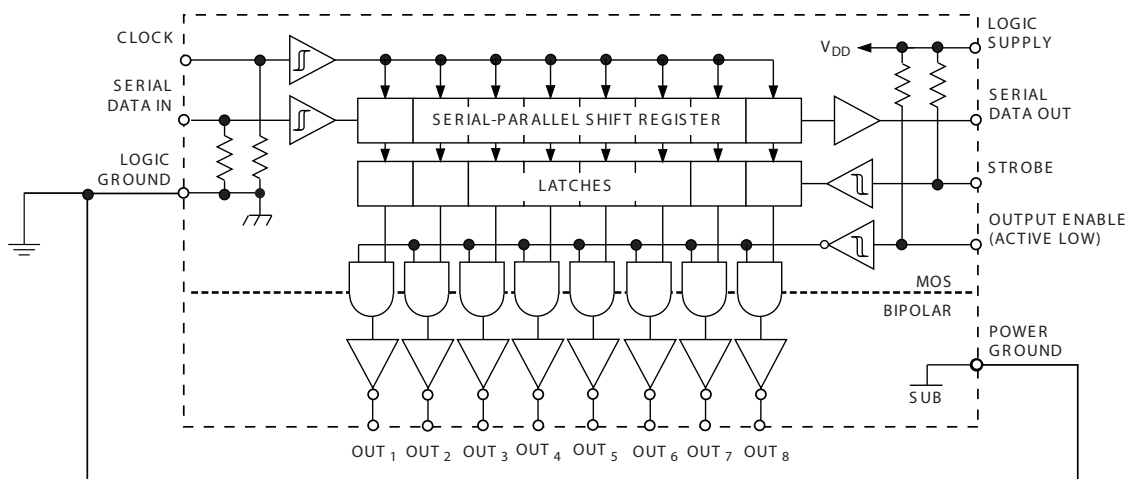
A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Typical applications include driving multiplexed LED displays or incandescent lamps.

The A6821 has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The A6821SA is furnished in a standard 16-pin plastic DIP. The A6821EA is a 16-pin plastic DIP, capable of operation from -40°C to 85°C. The A6821SLW is a 16-lead wide-body SOIC, for surface-mount applications. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

### Functional Block Diagram



## Selection Guide

Part Number	Package	Ambient (°C)	Packing
A6821SA-T	16-pin DIP	-20 to 85	25 pieces per tube
A6821EA-T*	16-pin DIP	-40 to 85	25 pieces per tube
A6821SLWTR-T	16-pin wide body SOIC	-20 to 85	1000 pieces per reel



\*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 2, 2009. Deadline for receipt of LAST TIME BUY orders is April 30, 2010.

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Logic Supply Voltage	$V_{DD}$		7	V
Input Voltage Range	$V_{IN}$	Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.	-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$		50	V
Continuous Output Current	$I_{OUT}$		500	mA
Power Dissipation	$P_D$	A package	2.1	W
		LW package	1.5	W
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

**ELECTRICAL CHARACTERISTICS**<sup>1</sup> Unless otherwise noted: T<sub>A</sub> = 25°C, logic supply operating voltage V<sub>dd</sub> = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V <sub>dd</sub> = 3.3 V			V <sub>dd</sub> = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I <sub>CEX</sub>	V <sub>OUT</sub> = 50 V	–	–	10	–	–	10	μA
Collector–Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>OUT</sub> = 100 mA	–	–	1.1	–	–	1.1	V
		I <sub>OUT</sub> = 200 mA	–	–	1.3	–	–	1.3	V
		I <sub>OUT</sub> = 350 mA	–	–	1.6	–	–	1.6	V
Input Voltage	V <sub>IN(1)</sub>		2.2	–	–	3.3	–	–	V
	V <sub>IN(0)</sub>		–	–	1.1	–	–	1.7	V
Input Resistance	R <sub>IN</sub>		50	–	–	50	–	–	kΩ
Serial Data Output Voltage	V <sub>OUT(1)</sub>	I <sub>OUT</sub> = –200 μA	2.8	3.05	–	4.5	4.75	–	V
	V <sub>OUT(0)</sub>	I <sub>OUT</sub> = 200 μA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency <sup>2</sup>	f <sub>c</sub>		10	–	–	10	–	–	MHz
Logic Supply Current	I <sub>DD(1)</sub>	One output on, OE = L, ST = H	–	–	2.0	–	–	2.0	mA
	I <sub>DD(0)</sub>	All outputs off, OE = H, ST = H, P1 through P8 = L	–	–	100	–	–	100	μA
Output Enable-to-Output Delay	t <sub>dis(BQ)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
	t <sub>en(BQ)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
Strobe-to-Output Delay	t <sub>p(STH-QL)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
	t <sub>p(STH-QH)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
Output Fall Time	t <sub>f</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
Output Rise Time	t <sub>r</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	μs
Clock-to-Serial Data Out Delay	t <sub>p(CH-SQX)</sub>	I <sub>OUT</sub> = ±200 μA	–	50	–	–	50	–	ns

<sup>1</sup>Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

<sup>2</sup>Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

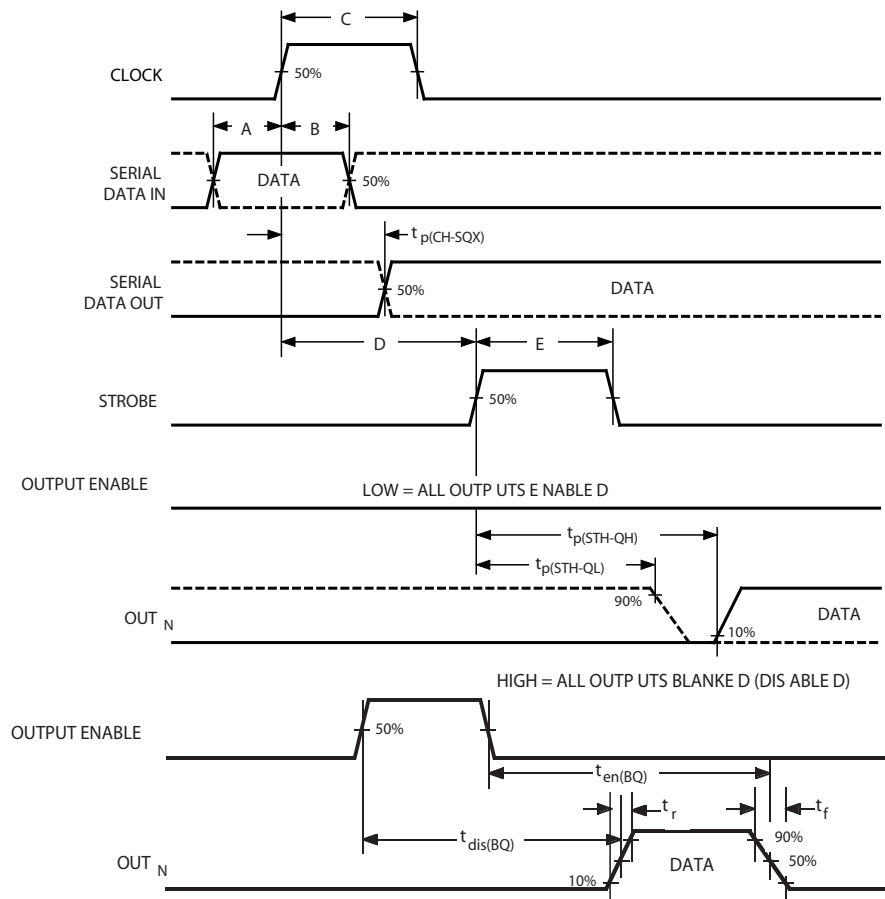
Truth Table

Serial Data Input	Clock Input	Shift Register Contents					Serial Data Output	Strobe Input	Latch Contents					Output Enable Input	Output Contents				
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>8</sub>			L <sub>1</sub>	L <sub>2</sub>	L <sub>3</sub>	...	L <sub>8</sub>		O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	...	O <sub>8</sub>
H	⌋	H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>7</sub>	R <sub>7</sub>												
L	⌋	L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>7</sub>	R <sub>7</sub>												
X	⌋	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>8</sub>	R <sub>8</sub>												
		X	X	X	...	X	X	L	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>8</sub>						
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>8</sub>	P <sub>8</sub>	H	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>8</sub>	L					P <sub>1</sub> P <sub>2</sub> P <sub>3</sub> ... P <sub>8</sub>
									X	X	X	...	X	H					H H H ... H

L = Low Logic Level  
 H = High Logic Level  
 X = Irrelevant  
 P = Present State

R = Previous State  
 OE = Output Enable  
 ST = Strobe

Timing Requirements and Specifications  
(Logic Levels are  $V_{DD}$  and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_h(D)$	25
C	Clock Pulse Width	$t_w(CH)$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_w(STH)$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

Maximum Allowable Duty Cycle,  $I_{OUT} = 200\text{ mA}$ ,  $V_{DD} = 5\text{ V}$

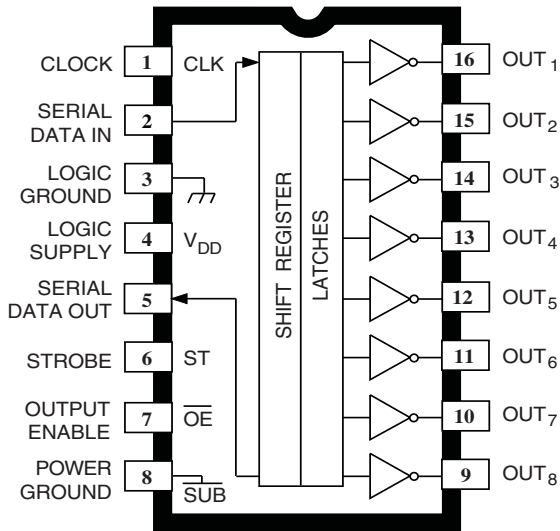
Number of Outputs ON	Ambient Temperature				
	25°C	40°C	50°C	60°C	70°C
<b>A6821SA/A6821EA</b>					
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%
<b>A6821SLW</b>					
8	67%	59%	54%	49%	43%
7	77%	68%	62%	56%	49%
6	90%	79%	72%	65%	57%
5	100%	95%	86%	78%	68%
4	100%	100%	100%	98%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Terminal List Table

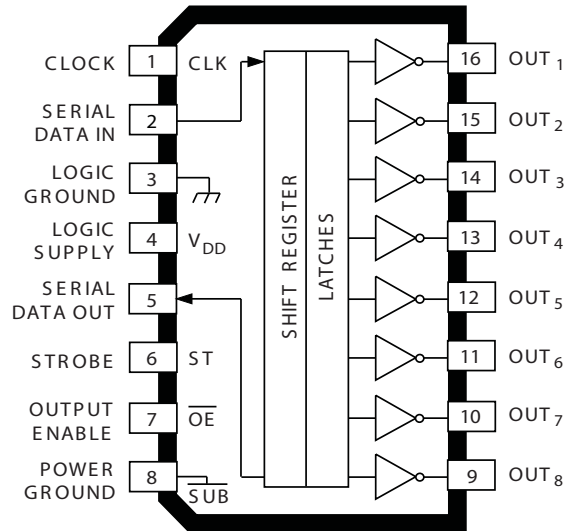
Name	Description	Pin
CLK	Clock	1
	Serial Data In	2
	Logic Ground*	3
VDD	Logic Supply	4
	Serial Data Out	5
ST	Strobe	6
$\overline{OE}$	Output Enable (active low)	7
SUB	Power Ground*	8
OUT <sub>8</sub>	Serial Data Output	9
OUT <sub>7</sub>	Serial Data Output	10
OUT <sub>6</sub>	Serial Data Output	11
OUT <sub>5</sub>	Serial Data Output	12
OUT <sub>4</sub>	Serial Data Output	13
OUT <sub>3</sub>	Serial Data Output	14
OUT <sub>2</sub>	Serial Data Output	15
OUT <sub>1</sub>	Serial Data Output	16

\* There is an indeterminate resistance between logic ground and power ground. For proper operation, these terminals must be externally connected together.

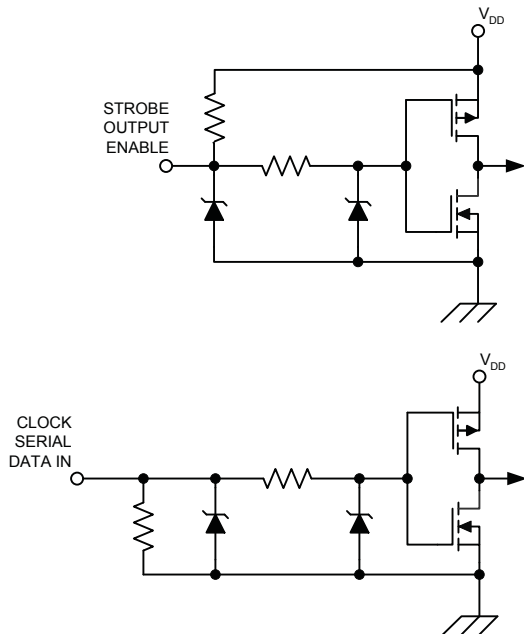
Package A  
16-pin DIP



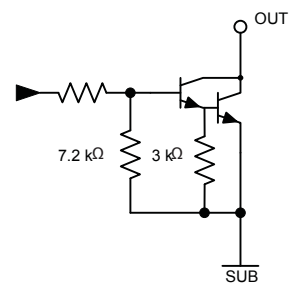
Package LW  
16-pin Wide Body SOIC



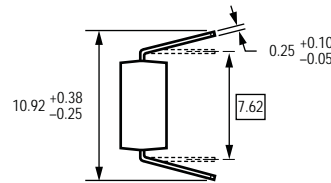
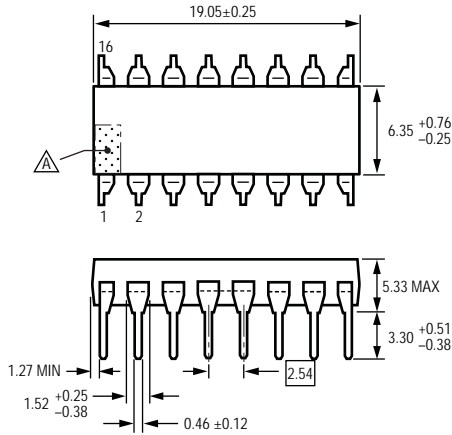
Typical Input Circuits



Typical Output Driver

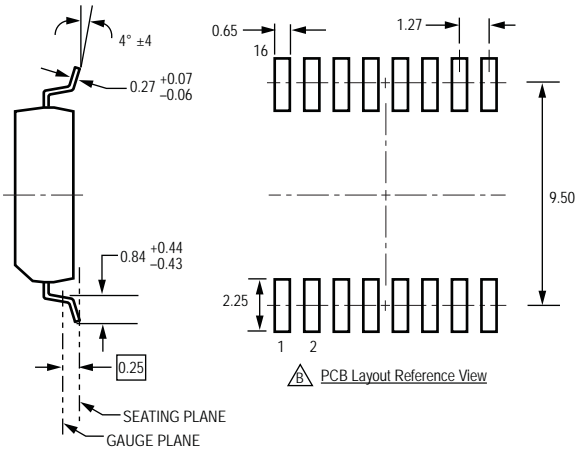
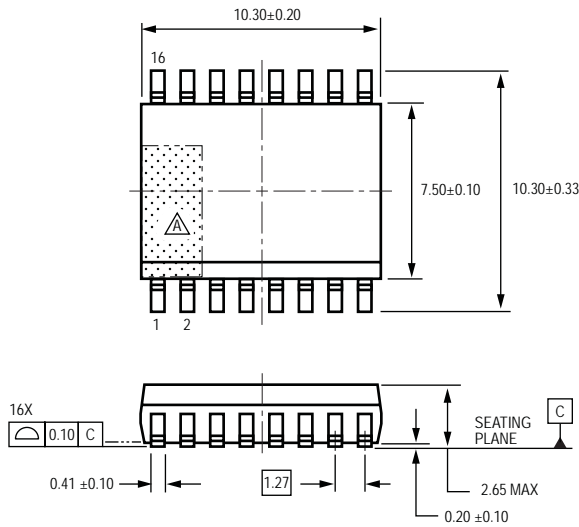


Package A  
16-pin DIP



For Reference Only  
(reference JEDEC MS-001 BB)  
Dimensions in inches, metric dimensions (mm) in brackets, for reference only  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown  
⚠ Terminal #1 mark area

Package LW  
16-pin Wide Body SOIC



For Reference Only  
Dimensions in millimeters  
(reference JEDEC MS-013 AA)  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

⚠ Terminal #1 mark area  
⚠ Reference pad layout (reference IPC SOIC127P1030X265-16M)  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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