THE DATASHEET OF

VCA810AID

VCA810 High Gain Adjust Range, Wideband and Variable Gain Amplifier

1 Features

- High Gain Adjust Range: ±40 dB
- Differential In, Single-Ended Out
- Low Input Noise Voltage: 2.4 nV/√Hz
- Constant Bandwidth vs Gain: 35 MHz
- High dB/V Gain Linearity: ±0.3 dB
- Gain Control Bandwidth: 25 MHz
- Low Output DC Error: < ±40 mV
- High Output Current: ±60 mA
- Low Supply Current: 24.8 mA
  (Maximum for –40°C to 85°C Temperature Range)

2 Applications

- Optical Receiver Time Gain Control
- Sonar Systems
- Voltage-Tunable Active Filters
- Log Amplifiers
- Pulse Amplitude Compensation
- AGC receivers With RSSI
- Improved Replacement for VCA610

3 Description

The VCA810 is a DC-coupled, wideband, continuously variable, voltage-controlled gain amplifier. The device provides a differential input to single-ended output conversion with a high-impedance gain control input used to vary the gain over a –40-dB to 40-dB range linear in dB/V.

Operating from ±5-V supplies, the device gain control voltage adjusts the gain from –40 dB at a 0-V input to 40 dB at a –2-V input. Increasing the control voltage above ground attenuates the signal path to greater than 80 dB. Signal bandwidth and slew rate remain constant over the entire gain adjust range. This 40-dB/V gain control is accurate within ±1.5 dB (±0.9 dB for high grade), allowing the gain control voltage in an AGC application to be used as a received signal strength indicator (RSSI) with ±1.5-dB accuracy.

Excellent common-mode rejection and common-mode input range at the two high-impedance inputs allow the device to provide a differential receiver operation with gain adjust. The output signal is referenced to ground. Zero differential input voltage gives a 0-V output with a small DC offset error. Low input noise voltage ensures good output SNR at the highest gain settings.

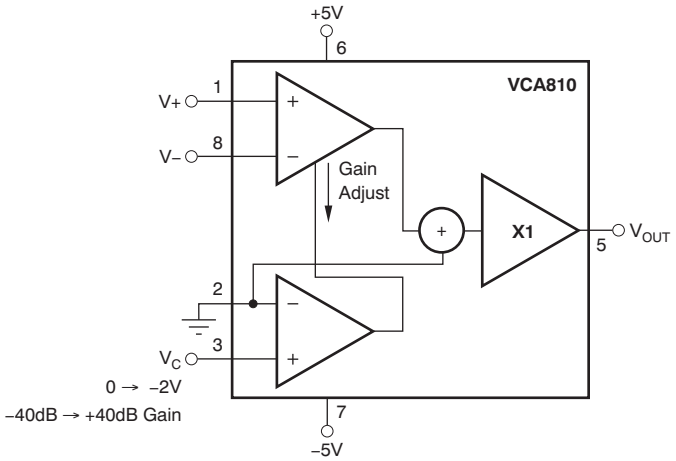
In applications where pulse edge information is critical, and the device is being used to equalize varying channel loss, minimal change in group delay over gain setting retains excellent pulse edge information.

An improved output stage provides adequate output current to drive the most demanding loads. Although principally intended to drive analog-to-digital converters (ADCs) or second-stage amplifiers, the ±60-mA output current easily drives doubly-terminated 50-Ω lines or a passive post-filter stage over the ±1.7-V output voltage range.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
VCA810	SOIC (8)	4.90 mm × 3.91 mm

Functional Block Diagram



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4 Revision History

Changes from Revision F (December 2010) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed DC Performance, *Input offset current* parameter unit from mA to nA in High Grade DC Characteristics table ... 9

Changes from Revision E (August 2008) to Revision F **Page**

- Deleted lead temperature specification from *Absolute Maximum Ratings* table ... 4
- Corrected typo in Figure 34 ... 21

Changes from Revision D (February, 2006) to Revision E **Page**

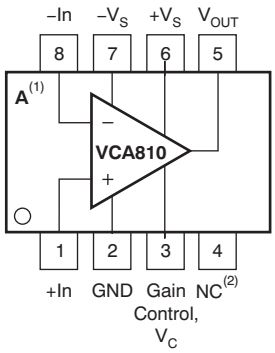
- Changed storage temperature minimum value in *Absolute Maximum Ratings* table from –40°C to –65°C ... 4

5 Device Comparison Table

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/√Hz)	SIGNAL BANDWIDTH (MHz)
VCA811	—	80	2.4	80
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2614	45	3.6	40
—	VCA2616	45	3.3	40
—	VCA2618	45	5.5	30

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



(1) High grade version indicator.

(2) NC = Not connected.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	+In	I	Noninverting input
2	GND	P	Ground, serves as reference for gain control pin
3	Gain Control, V_C	I	Gain control
4	NC	—	No connect
5	V_{OUT}	O	Output
6	$+V_S$	P	Positive supply
7	$–V_S$	P	Negative supply
8	–In	I	Inverting input

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

	MIN	MAX	UNIT
Power supply		±6.5	V
Internal power dissipation	See *Thermal Information*		
Differential input voltage		$\pm V_S$	V
Input common-mode voltage		$\pm V_S$	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
	Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature	–40	25	85	°C
Supply voltage	±4	±5	±5.5	V

7.4 Thermal Information

THERMAL METRIC(1)		VCA810 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
	Small-signal bandwidth (see *Functional Block Diagram*)	−2 V ≤ V_C ≤ 0 V	T_J = 25°C			35		MHz
			T_J = 25°C(2)	B	30			
			T_J = 0°C to 70°C(3)		29			
			T_J = –40°C to 85°C(3)		29			
	Large-signal bandwidth	V_O = 2 V_{PP}, −2 ≤ V_C ≤ −1	T_J = 25°C	B		35		MHz
			T_J = 25°C(2)		30			
			T_J = 0°C to 70°C(3)		29			
			T_J = –40°C to 85°C(3)		29			
	Frequency response peaking	V_O < 500 mV_{PP}, −2 V ≤ V_C ≤ 0 V	T_J = 25°C	B		0.1		dB
			T_J = 25°C(2)		0.5			
			T_J = 0°C to 70°C(3)		0.5			
			T_J = –40°C to 85°C(3)		0.5			
	Slew rate	V_O = 3.5-V step, −2 ≤ V_C ≤ −1, 10% to 90%	T_J = 25°C	B		350		V/µs
			T_J = 25°C(2)		300			
			T_J = 0°C to 70°C(3)		300			
			T_J = –40°C to 85°C(3)		295			
	Settling time to 0.01%	V_O = 1-V step, −2 ≤ V_C ≤ −1	T_J = 25°C	B		30		ns
			T_J = 25°C(2)		40			
			T_J = 0°C to 70°C(3)		41			
			T_J = –40°C to 85°C(3)		41			
	Rise-and-fall time	V_O = 1-V step, −2 ≤ V_C ≤ −1	T_J = 25°C	B		10		ns
			T_J = 25°C(2)		12			
			T_J = 0°C to 70°C(3)		12.1			
			T_J = –40°C to 85°C(3)		12.1			
	Group delay	G = 0 dB, V_C= −1 V, f = 5 MHz, V_O = 500 mV_{PP}	T_J = 25°C	C		6.2		ns
	Group delay variation	V_O < 500 mV_{PP}, −2 V ≤ V_C ≤ 0 V, f = 5 MHz	T_J = 25°C	C		3.5		ns
HD2	Second harmonic distortion	V_O = 1 V_{PP}, f = 1 MHz, V_C = −1 V, G = 0 dB	T_J = 25°C	B		–71		dBc
			T_J = 25°C(2)		–51			
			T_J = 0°C to 70°C(3)		–50			
			T_J = –40°C to 85°C(3)		–49			
HD3	Third harmonic distortion	V_O = 1 V_{PP}, f = 1 MHz, V_C = −1 V, G = 0 dB	T_J = 25°C	B		−35		dBc
			T_J = 25°C(2)		–34			
			T_J = 0°C to 70°C(3)		–32			
			T_J = –40°C to 85°C(3)		–29			
	Input voltage noise	V_C = −2 V	T_J = 25°C	B		2.4		nV/√Hz
			T_J = 25°C(2)				2.8	
			T_J = 0°C to 70°C(3)				3.4	
			T_J = –40°C to 85°C(3)				3.5	
	Input current noise	−2 V ≤ V_C ≤ 0 V	T_J = 25°C	B		1.4		pA/√Hz
			T_J = 25°C(2)				1.8	
			T_J = 0°C to 70°C(3)				2	
			T_J = –40°C to 85°C(3)				2.1	
	Fully attenuated feedthrough	f ≤ 1 MHz, V_C > 200 mV	T_J = 25°C	B		−80		dB
			T_J = 25°C(2)				−70	
	Overdrive recovery	V_{IN} = 2 V to 0 V, V_C = −2 V, G = 40 dB	T_J = 25°C	B		100		ns
			T_J = 25°C(2)		150			

(1) Test levels: **(A)** 100% tested at 25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value; only for information.
(2) Junction temperature = ambient for 25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient 30°C at high temperature limit for over temperature specifications.

Electrical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
DC PERFORMANCE (Single-Ended or Differential Input)							
Output offset voltage (both inputs grounded)(4)	−2 V ≤ V_C ≤ 0 V	T_J = 25°C	A		±4		mV
		T_J = 25°C(2)				±22	
		T_J = 0°C to 70°C(3)				±30	
		T_J = –40°C to 85°C(3)				±32	
Output offset voltage drift	T_J = 0°C to 70°C(3)		B			±125	V/°C
	T_J = –40°C to 85°C(3)					±125	
Input offset voltage(4)	Both inputs grounded	T_J = 25°C	A		±0.1		mV
		T_J = 25°C(2)				±0.25	
		T_J = 0°C to 70°C(3)				±0.3	
		T_J = –40°C to 85°C(3)				±0.35	
input offset voltage drift	T_J = 0°C to 70°C(3)		B			±1	µV/°C
	T_J = –40°C to 85°C(3)					±1.2	
Input bias current	−2 V ≤ V_C ≤ 0 V	T_J = 25°C	A		−6		µA
		T_J = 25°C(2)				−10	
		T_J = 0°C to 70°C(3)				−12	
		T_J = –40°C to 85°C(3)				−14	
Input bias current drift	T_J = 0°C to 70°C(3)		B			±25	nA/°C
	T_J = –40°C to 85°C(3)					±30	
Input offset current	−2 V ≤ V_C ≤ 0 V	T_J = 25°C	A		±100		nA
		T_J = 25°C(2)				±600	
		T_J = 0°C to 70°C(3)				±700	
		T_J = –40°C to 85°C(3)				±800	
Input offset current drift	T_J = 0°C to 70°C(3)		B			±1.4	nA/°C
	T_J = –40°C to 85°C(3)					±2.2	
INPUT							
Common-mode input range	T_J = 25°C		A		±2.4		V
	T_J = 25°C(2)			±2.3			
	T_J = 0°C to 70°C(3)			±2.3			
	T_J = –40°C to 85°C(3)			±2.2			
Common-mode rejection ratio	V_{CM} = 0.5 V, V_C = −2 V, input-referred	T_J = 25°C	A		95		dB
		T_J = 25°C(2)		85			
		T_J = 0°C to 70°C(3)		83			
		T_J = –40°C to 85°C(3)		80			
Input impedance	V_{CM} = 0 V, single-ended	T_J = 25°C	C		1 || 1		MΩ || pF
	V_{CM} = 0 V, differential	T_J = 25°C	C		> 10 || < 2		MΩ || pF
Differential input range(5)	V_C = 0 V, V_{CM} = 0 V	T_J = 25°C	C		3		V_{PP}
OUTPUT							
Voltage output swing	V_C = −2 V, R_L = 100 Ω	T_J = 25°C	A		±1.8		V
		T_J = 25°C(2)		±1.7			
		T_J = 0°C to 70°C(3)		±1.4			
		T_J = –40°C to 85°C(3)		±1.3			
	V_C = −2 V, R_L = 100 Ω	T_J = 25°C	A		±1.7		V
		T_J = 25°C(2)		±1.6			
		T_J = 0°C to 70°C(3)		±1.3			
		T_J = –40°C to 85°C(3)		±1.2			
Output current	V_O = 0 V	T_J = 25°C	A		±60		mA
		T_J = 25°C(2)		±40			
		T_J = 0°C to 70°C(3)		±35			
		T_J = –40°C to 85°C(3)		±32			
Output short-circuit current	V_O = 0 V	T_J = 25°C	C		±120		mA
Output impedance	V_O = 0 V, f < 100 kHz	T_J = 25°C	C		0.2		Ω

(4) Total output offset is: (Output Offset Voltage ± Input Offset Voltage x Gain).
(5) Maximum input at minimum gain for < 1-dB gain compression.

Electrical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
GAIN CONTROL (V_C, Pin 3, Single-Ended or Differential Input)							
Specified gain range	ΔV_C / ΔdB = 25 mV/dB	T_J = 25°C	C		±40		dB
Maximum control voltage	G = −40 dB	T_J = 25°C	C		0		V
Minimum control voltage	G = 40 dB	T_J = 25°C	C		–2		V
Gain accuracy	−1.8 V ≤ V_C ≤ −0.2 V	T_J = 25°C	A		±0.4		dB
		T_J = 25°C(2)				±1.5	
		T_J = 0°C to 70°C(3)				±2.5	
		T_J = –40°C to 85°C(3)				±3.5	
	V_C < −1.8 V, V_C > −0.2 V	T_J = 25°C	A		±0.5		dB
		T_J = 25°C(2)				±2.2	
		T_J = 0°C to 70°C(3)				±3.7	
		T_J = –40°C to 85°C(3)				±4.7	
Gain drift	−1.8 V ≤ V_C ≤ −0.2 V	T_J = 0°C to 70°C(3)	B			±0.02	dB/°C
		T_J = –40°C to 85°C(3)				±0.03	
	V_C < −1.8 V, V_C > −0.2 V	T_J = 0°C to 70°C(3)	B			±0.03	dB/°C
		T_J = –40°C to 85°C(3)				±0.04	
Gain control slope	25°C		C		–40		dB/V
Gain control linearity(6)	−1.8 V ≤ V_C ≤ 0 V	T_J = 25°C	A		±0.3		dB
		T_J = 25°C(2)				±1	
		T_J = 0°C to 70°C(3)				±1.1	
		T_J = –40°C to 85°C(3)				±1.2	
	V_C < −1.8 V	T_J = 25°C	A		±0.7		dB
		T_J = 25°C(2)				±1.6	
		T_J = 0°C to 70°C(3)				±2.5	
		T_J = –40°C to 85°C(3)				±3.2	
Gain control bandwidth	T_J = 25°C		B		25		MHz
	T_J = 25°C(2)			20			
	T_J = 0°C to 70°C(3)			19			
	T_J = –40°C to 85°C(3)			19			
Gain control slew rate	80-dB gain step	T_J = 25°C	C		900		dB/ns
Gain settling time	1%, 80-dB step	T_J = 25°C	C		0.8		µs
Input bias current	V_C = −1 V	T_J = 25°C	A		–1.5		µA
		T_J = 25°C(2)				–3.5	
		T_J = 0°C to 70°C(3)				–4.5	
		T_J = –40°C to 85°C(3)				–8	
Gain + power-supply rejection ratio	V_C = −2 V, G = 40 dB, +V_S = 5 V ± 0.5 V	T_J = 25°C	A		0.5		dB/V
		T_J = 25°C(2)				1.5	
		T_J = 0°C to 70°C(3)				1.8	
		T_J = –40°C to 85°C(3)				2	
Gain – power-supply rejection ratio	V_C = −2 V, G = 40 dB, –V_S = –5 V ± 0.5 V	T_J = 25°C	A		0.7		dB/V
		T_J = 25°C(2)				1.5	
		T_J = 0°C to 70°C(3)				1.8	
		T_J = –40°C to 85°C(3)				2	
POWER SUPPLY							
Specified operating voltage	T_J = 25°C(2)		C		±5		V
Minimum operating voltage	T_J = 25°C(2)		A	±4			V
	T_J = 0°C to 70°C(3)			±4			
	T_J = –40°C to 85°C(3)			±4			
Maximum operating voltage	T_J =25°C(2)		A			±6	V
	T_J = 0°C to 70°C(3)					±6	
	T_J = –40°C to 85°C(3)					±6	

(6) Maximum deviation from best line fit.

Electrical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Positive maximum supply quiescent current		$+V_S$ = 5 V, G = −40 dB	T_J = 25°C	A		10		mA
			T_J = 25°C(2)		12.5			
			T_J = 0°C to 70°C(3)		12.6			
			T_J = –40°C to 85°C(3)		12.7			
		$+V_S$ = 5 V, G = 40 dB	T_J = 25°C	A		18		mA
			T_J = 25°C(2)		20.5			
			T_J = 0°C to 70°C(3)		22			
			T_J = –40°C to 85°C(3)		22.3			
Positive minimum supply quiescent current		$+V_S$ = 5 V, G = –40 dB	T_J = 25°C	A		10		mA
			T_J = 25°C(2)				7.5	
			T_J = 0°C to 70°C(3)				7.2	
			T_J = –40°C to 85°C(3)				7.1	
		$+V_S$ = 5 V, G = 40 dB	T_J = 25°C	A		18		mA
			T_J = 25°C(2)				15.5	
			T_J = 0°C to 70°C(3)				14.5	
			T_J = –40°C to 85°C(3)				13.5	
Negative maximum supply quiescent current(7)		$-V_S$ = −5 V, G = −40 dB	T_J = 25°C	A		12		mA
			T_J = 25°C(2)				14.5	
			T_J = 0°C to 70°C(3)				14.6	
			T_J = –40°C to 85°C(3)				14.7	
		$-V_S$ = −5 V, G = 40 dB	T_J = 25°C	A		20		mA
			T_J = 25°C(2)				22.5	
			T_J = 0°C to 70°C(3)				24.5	
			T_J = –40°C to 85°C(3)				24.8	
Negative minimum supply quiescent current(7)		$-V_S$ = −5 V, G = −40 dB	T_J = 25°C	A		12		mA
			T_J = 25°C(2)		9.5			
			T_J = 0°C to 70°C(3)		9.4			
			T_J = –40°C to 85°C(3)		9.3			
		$-V_S$ = −5 V, G = 40 dB	T_J = 25°C	A		20		mA
			T_J = 25°C(2)		17.5			
			T_J = 0°C to 70°C(3)		16.5			
			T_J = –40°C to 85°C(3)		16			
+PSRR	Positive power-supply rejection ratio	Input-referred, V_C = −2 V	T_J = 25°C	A		90		dB
			T_J = 25°C(2)		75			
			T_J = 0°C to 70°C(3)		75			
			T_J = –40°C to 85°C(3)		73			
–PSRR	Negative power-supply rejection ratio	Input-referred, V_C = −2 V	T_J = 25°C	A		85		dB
			T_J = 25°C(2)		70			
			T_J = 0°C to 70°C(3)		70			
			T_J = –40°C to 85°C(3)		68			
THERMAL CHARACTERISTICS								
	Specified operating range, ID package			C	–40		85	°C

(7) Magnitude.

7.6 High Grade DC Characteristics: V_S = ±5 V (VCA810AID)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
DC PERFORMANCE (Single-Ended or Differential Input)							
Output offset voltage	−2 V < V_C < 0 V	T_J = 25°C	A		±4		mV
		T_J = 25°C(2)				±14	
		T_J = 0°C to 70°C(3)				±24	
		T_J = –40°C to 85°C(3)				±26	
Input offset voltage	T_J = 25°C		A		±0.1		mV
	T_J = 25°C(2)					±0.2	
	T_J = 0°C to 70°C(3)					±0.25	
	T_J = –40°C to 85°C(3)					±0.3	
Input offset current	T_J = 25°C		A		±100		nA
	T_J = 25°C(2)					±500	
	T_J = 0°C to 70°C(3)					±600	
	T_J = –40°C to 85°C(3)					±700	
GAIN CONTROL (V_C, Pin 3, Single-Ended or Differential Input)							
Gain accuracy	−1.8 V ≤ V_C ≤ −0.2 V	T_J = 25°C	A		±0.4		dB
		T_J = 25°C(2)				±0.9	
		T_J = 0°C to 70°C(3)				±1.9	
		T_J = –40°C to 85°C(3)				±2.9	
	V_C < −1.8 V, V_C > −0.2 V	T_J = 25°C	A		±0.5		dB
		T_J = 25°C(2)				±1.5	
		T_J = 0°C to 70°C(3)				±3.0	
		T_J = –40°C to 85°C(3)				±4.0	
Gain control linearity(4)	−1.8 V ≤ V_C ≤ 0 V	T_J = 25°C	A		±0.3		dB
		T_J = 25°C(2)				±0.6	
		T_J = 0°C to 70°C(3)				±0.7	
		T_J = –40°C to 85°C(3)				±0.8	
	V_C < −1.8 V	T_J = 25°C	A		±0.7		dB/V
		T_J = 25°C(2)				±1.1	
		T_J = 0°C to 70°C(3)				±1.9	
		T_J = –40°C to 85°C(3)				±2.7	
POWER SUPPLY							
Positive maximum supply quiescent current	+V_S = 5 V, G = −40 dB	T_J = 25°C	A		10		mA
		T_J = 25°C(2)		11.5			
		T_J = 0°C to 70°C(3)		11.6			
		T_J = –40°C to 85°C(3)		11.7			
	+V_S = 5 V, G = 40 dB	T_J = 25°C	A		18		mA
		T_J = 25°C(2)		19.5			
		T_J = 0°C to 70°C(3)		21			
		T_J = –40°C to 85°C(3)		21.3			
Positive minimum supply quiescent current	+V_S = 5 V, G = −40 dB	T_J = 25°C	A		10		mA
		T_J = 25°C(2)				8.5	
		T_J = 0°C to 70°C(3)				8.2	
		T_J = –40°C to 85°C(3)				8.1	
	+V_S = 5 V, G = 40 dB	T_J = 25°C	A		18		mA
		T_J = 25°C(2)				16.5	
		T_J = 0°C to 70°C(3)				15.5	
		T_J = –40°C to 85°C(3)				14.5	

(1) Test levels: **(A)** 100% tested at 25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value; only for information.
(2) Junction temperature = ambient for 25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient 30°C at high temperature limit for over temperature specifications.
(4) Maximum deviation from best line fit.

High Grade DC Characteristics: V_S = ±5 V (VCA810AID) (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Negative maximum supply quiescent current(5)	$-V_S$ = −5 V, G = −40 dB	T_J = 25°C	A		12		mA
		T_J = 25°C(2)		14			
		T_J = 0°C to 70°C(3)		14.1			
		T_J = –40°C to 85°C(3)		14.2			
	$-V_S$ = −5 V, G = 40 dB	T_J = 25°C	A		20		mA
		T_J = 25°C(2)		22			
		T_J = 0°C to 70°C(3)		24			
		T_J = –40°C to 85°C(3)		24.3			
Negative minimum supply quiescent current(5)	$-V_S$ = −5 V, G = −40 dB	T_J = 25°C	A		12		mA
		T_J = 25°C(2)				10	
		T_J = 0°C to 70°C(3)				9.9	
		T_J = –40°C to 85°C(3)				9.8	
	$-V_S$ = −5 V, G = 40 dB	T_J = 25°C	A		20		mA
		T_J = 25°C(2)				18	
		T_J = 0°C to 70°C(3)				17	
		T_J = –40°C to 85°C(3)				16.5	

(5) Magnitude.

7.7 Typical Characteristics

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

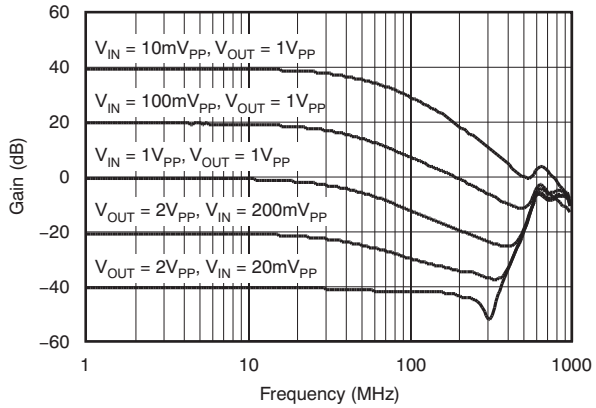


Figure 1. Small-Signal Frequency Response

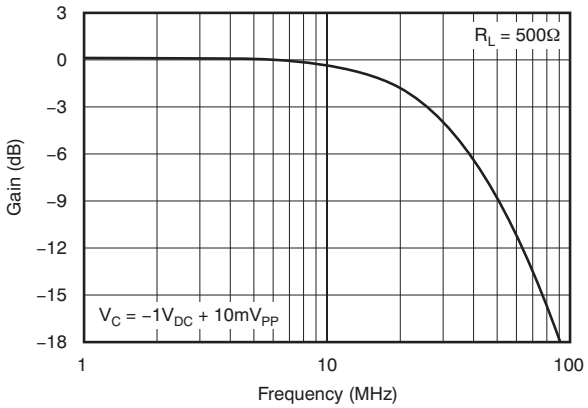


Figure 2. Gain Control Frequency Response

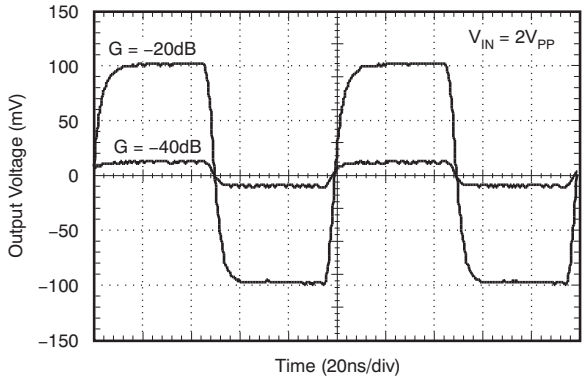


Figure 3. Attenuated Pulse Response

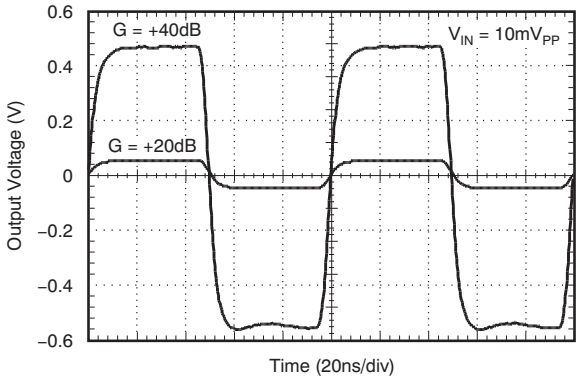


Figure 4. High Gain Pulse Response

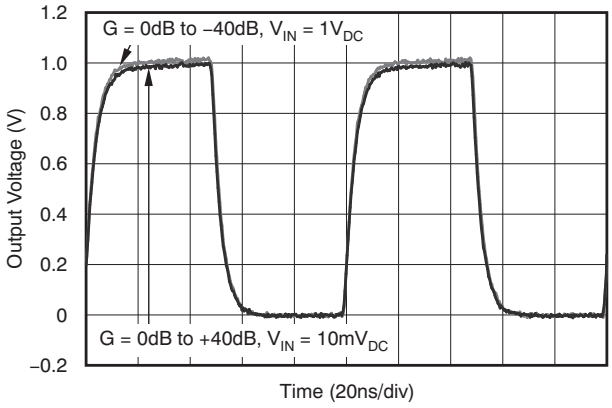


Figure 5. Gain Control Pulse Response

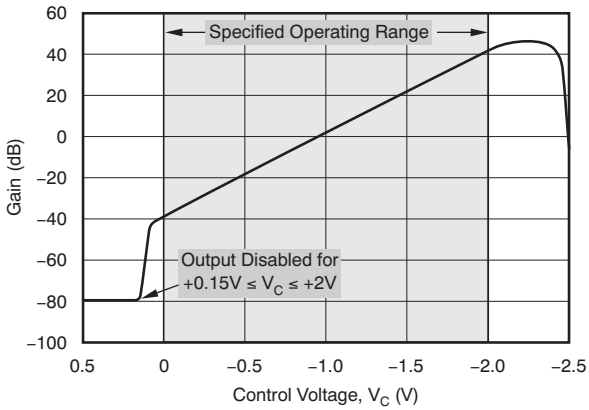


Figure 6. Gain vs Control Voltage

Typical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

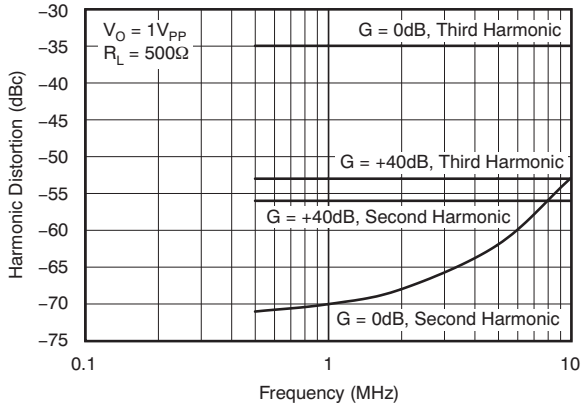


Figure 7. Harmonic Distortion vs Frequency

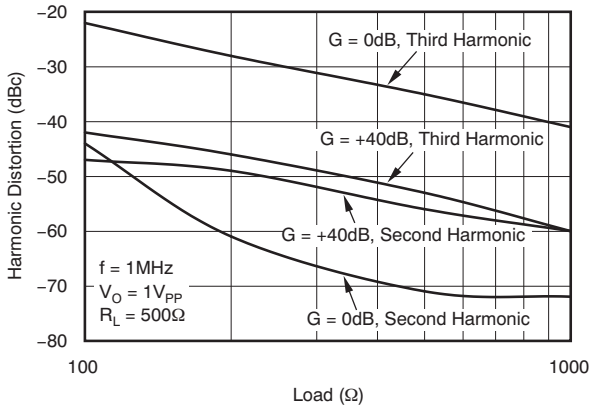


Figure 8. Harmonic Distortion vs R_{LOAD}

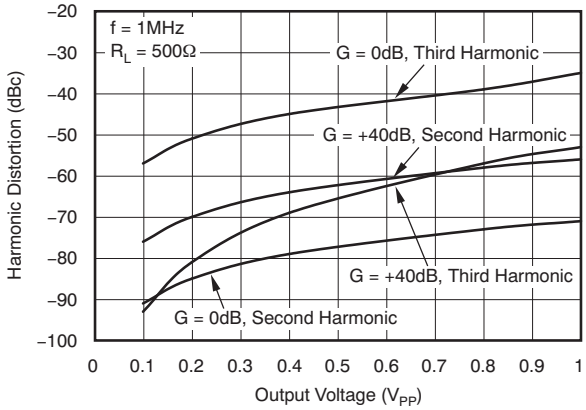


Figure 9. Harmonic Distortion vs Output Voltage

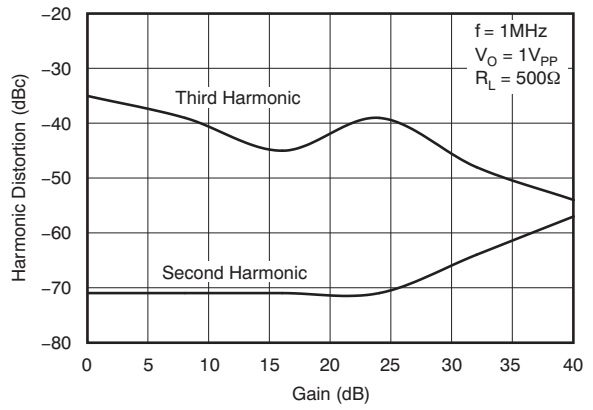


Figure 10. Harmonic Distortion vs Gain

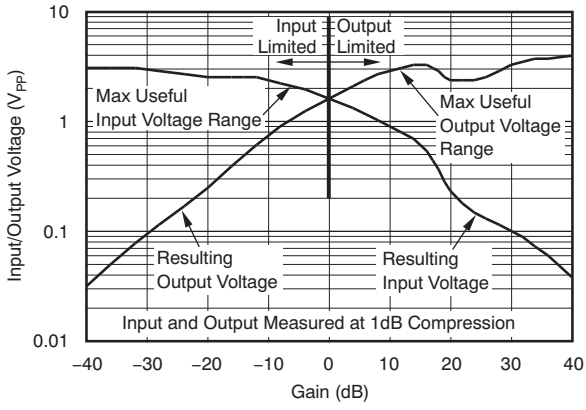


Figure 11. Input, Output Range vs Gain

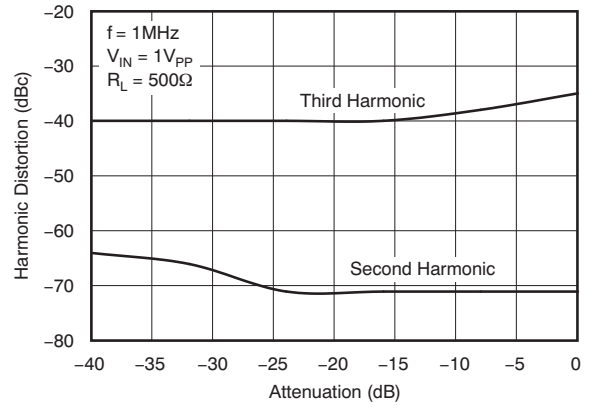


Figure 12. Harmonic Distortion vs Attenuation

Typical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

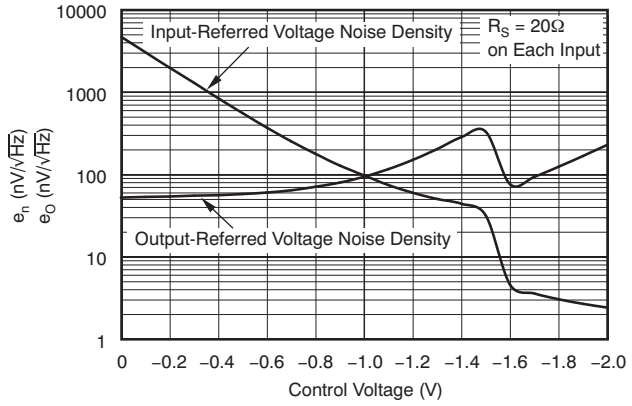


Figure 13. Noise Density vs Control Voltage

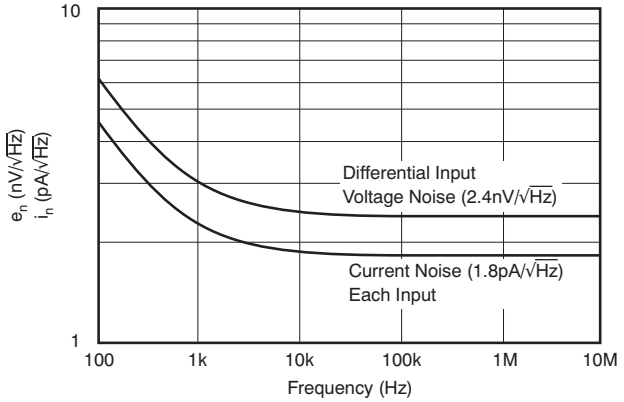


Figure 14. Input Voltage and Current Noise

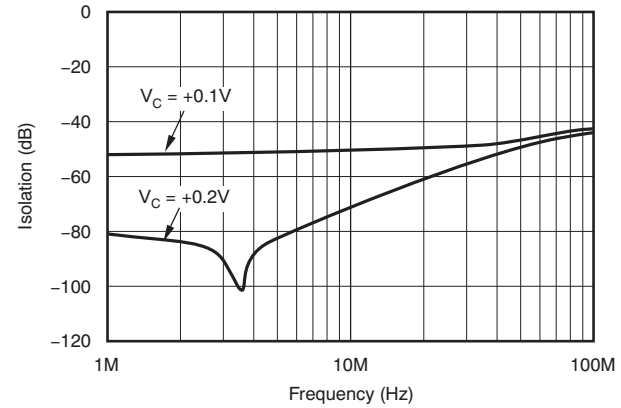


Figure 15. Fully Attenuated Isolation vs Frequency

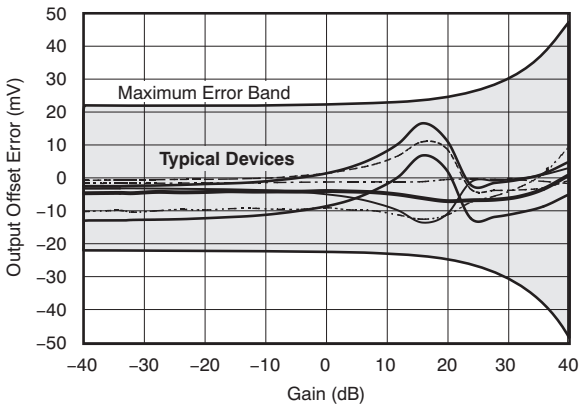


Figure 16. Output Offset Voltage Total Error Band vs Gain

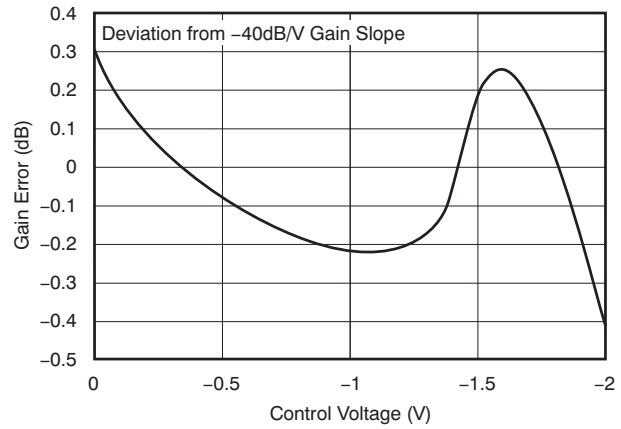


Figure 17. Typical Gain Error Plot

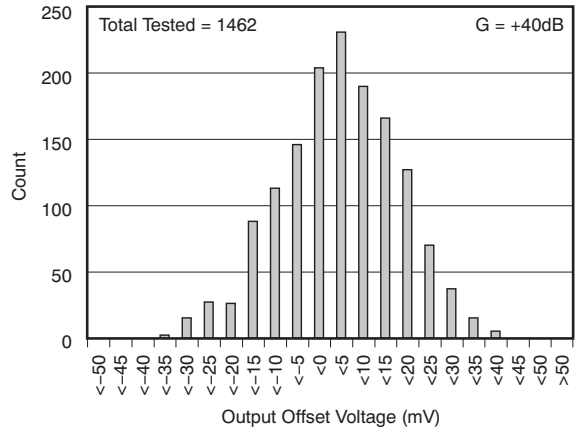


Figure 18. Output Offset Voltage Distribution

Typical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

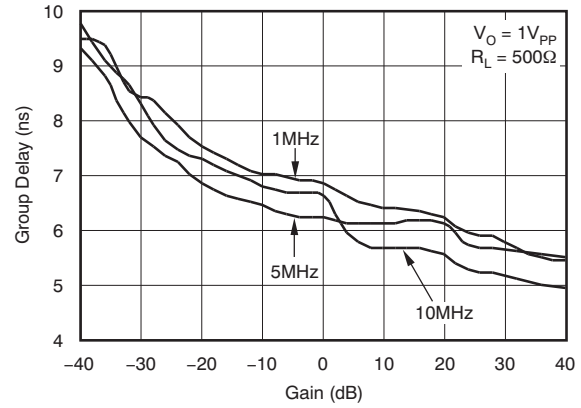


Figure 19. Group Delay vs Gain

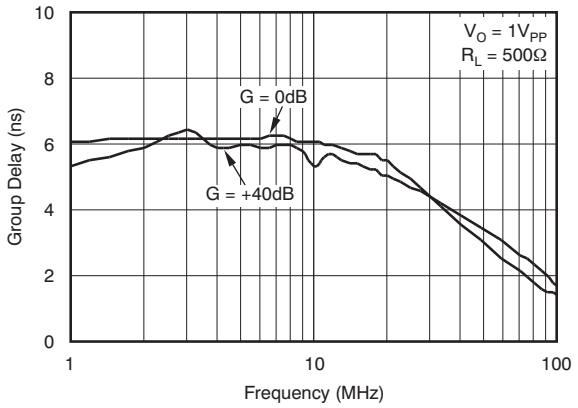


Figure 20. Group Delay vs Frequency

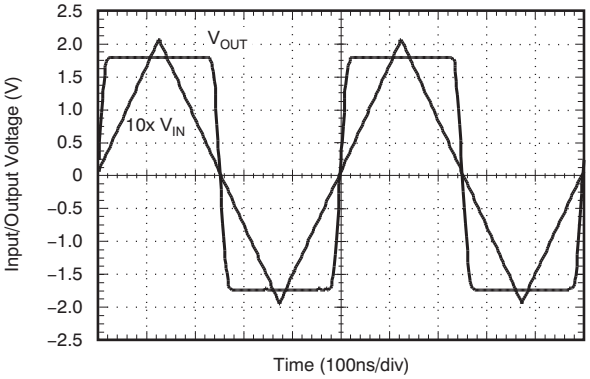


Figure 21. Overdrive Recovery at Maximum Gain

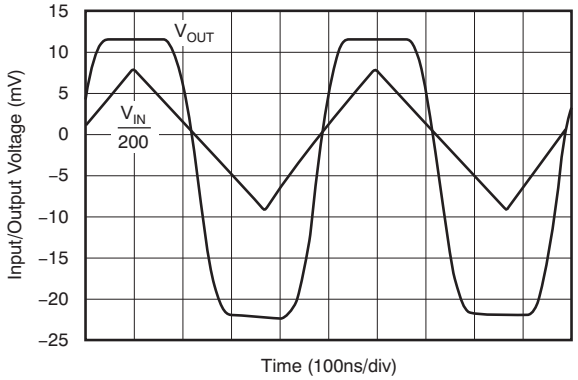


Figure 22. Overdrive Recovery at Maximum Attenuation

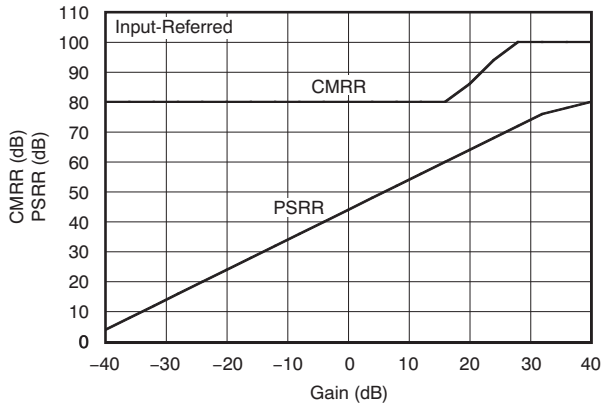


Figure 23. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Gain

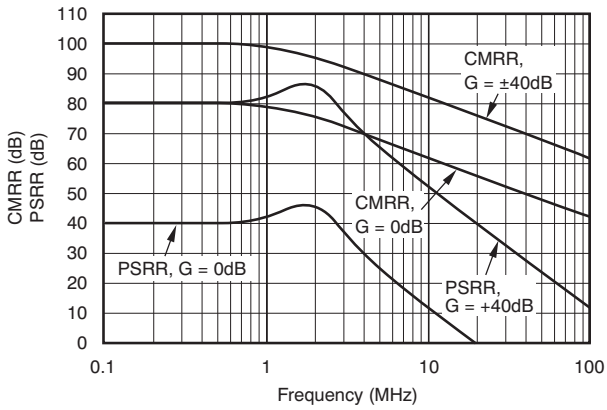


Figure 24. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

At R_L = 500 Ω and V_{IN} = single-ended input on V+ with V− at ground, V_S = ±5 V, unless otherwise noted.

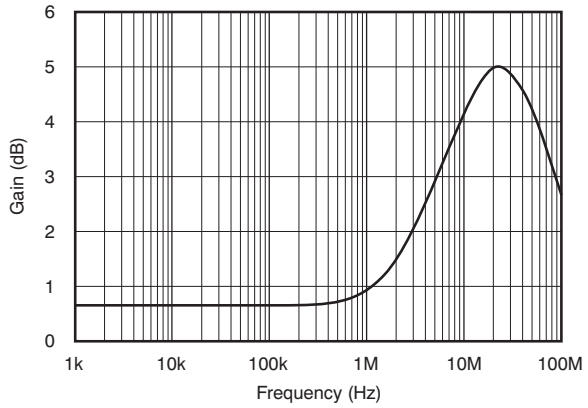


Figure 25. Gain Control +PSRR at Max Gain

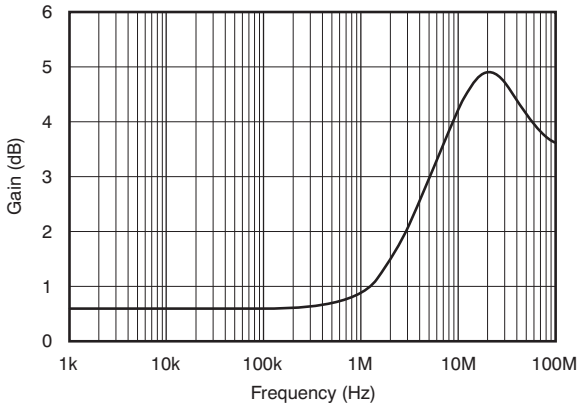


Figure 26. Gain Control −PSRR at Max Gain

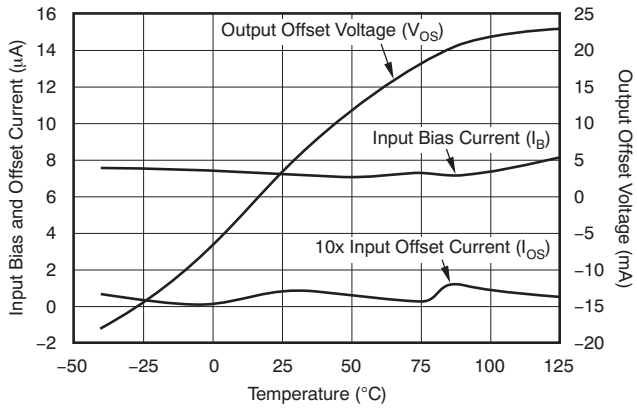


Figure 27. Typical DC Drift vs Temperature

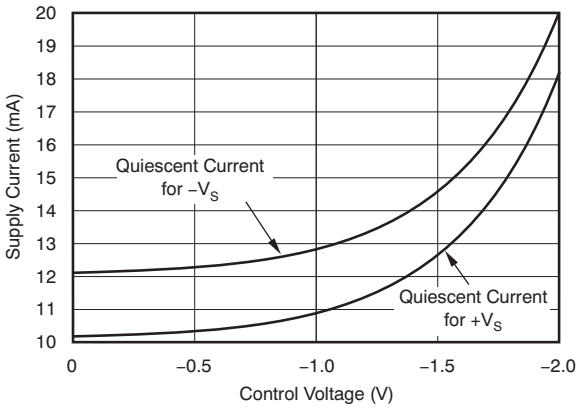


Figure 28. Typical Supply Current vs Control Voltage

8 Detailed Description

8.1 Overview

The VCA810 is a high gain adjust range, wideband, voltage amplifier with a voltage-controlled gain, as shown in *Functional Block Diagram*. The circuit's basic voltage amplifier responds to the control of an internal gain-control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting flexible input impedance matching. To preserve termination options, no internal circuitry connects to the input bases of this differential stage. For this reason, the user must provide DC paths for the input base currents from a signal source, either through a grounded termination resistor or by a direct connection to ground. The differential input stage also permits rejection of common-mode signals. At its output, the voltage amplifier presents a low impedance, simplifying impedance matching. An open-loop design produces wide bandwidth at all gain settings. A ground-referenced differential to single-ended conversion at the output retains the low output offset voltage.

A gain control voltage, V_C, controls the amplifier gain magnitude through a high-speed control circuit. Gain polarity can be either inverting or noninverting, depending upon the amplifier input driven by the input signal. The gain control circuit presents the high-input impedance of a noninverting operational amplifier connection. The control voltage pin is referred to ground as shown in *Functional Block Diagram*. The control voltage V_C varies the amplifier gain according to the exponential relationship:

$$G_{(V/V)} = 10^{-2(V_C + 1)} \quad (1)$$

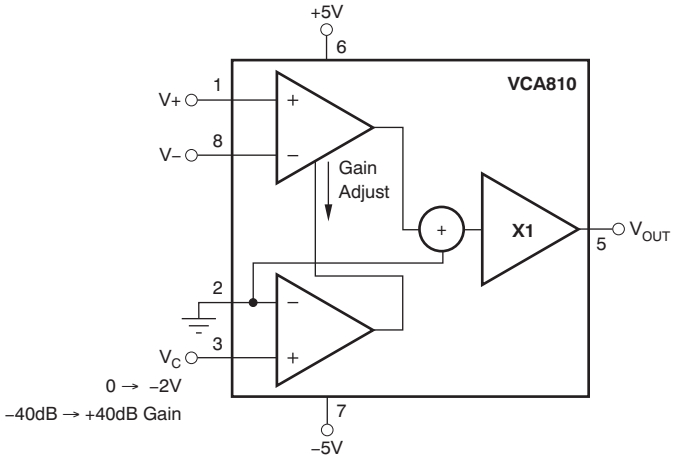
This translates to the log gain relationship:

$$G_{(dB)} = -40 \times (V_C + 1)\text{dB} \quad (2)$$

Thus, $G_{(dB)}$ varies linearly over the specified −40 dB to 40 dB range as V_C varies from 0 V to −2 V. Optionally, making V_C slightly positive (≥ 0.15 V) effectively disables the amplifier, giving greater than 80 dB of signal path attenuation at low frequencies.

Internally, the gain-control circuit varies the amplifier gain by varying the transconductance, g_m, of a bipolar transistor using the transistor bias current. Varying the bias currents of differential stages varies g_m to control the voltage gain of the VCA810. A g_m-based gain adjust normally suffers poor thermal stability. The VCA810 includes circuitry to minimize this effect.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input and Output Range

The VCA810's 80 dB gain range allows the user to handle an exceptionally wide range of input signal levels. If the input and output voltage range specifications are exceeded, however, signal distortion and amplifier overdrive will occur. Figure 11 shows the maximum input and output voltage range. This chart plots input and output voltages versus gain in dB.

Feature Description (continued)

The maximum input voltage range is the largest at full attenuation (−40 dB) and decreases as the gain increases. Similarly, the maximum useful output voltage range increases as the input decreases. We can distinguish three overloading issues as a result of the operating mode: high attenuation, mid-range gain-attenuation, and high gain.

From –40 dB to –10 dB, gain overdriving the input stage is the only method to overdrive the VCA810. Preventing this type of overdrive is achieved by limiting the input voltage range.

From –10 dB to 40 dB, overdriving can be prevented by limiting the output voltage range. There are two limiting mechanisms operating in this situation. From –10 dB to 10 dB, an internal stage is the limiting factor; from 10 dB to 40 dB, the output stage is the limiting factor.

Output overdriving occurs when either the maximum output voltage swing or output current is exceeded. The VCA810 high output current of ±60 mA ensures that virtually all output overdrives will be limited by voltage swing rather than by current limiting. Table 1 summarizes these overdrive conditions.

Table 1. Output Signal Compression

GAIN RANGE	LIMITING MECHANISM	TO PREVENT, OPERATE DEVICE WITHIN:
−40 dB < G < −10 dB	Input Stage Overdrive	Input Voltage Range
−10 dB < G < 10 dB	Internal Stage Overdrive	Output Voltage Range
5 dB < G < 40 dB	Output Stage Overdrive	Output Voltage Range

8.3.2 Overdrive Recovery

As shown in Figure 11, the onset of overdrive occurs whenever the actual output begins to deviate from the ideal expected output. If possible, the user should operate the VCA810 within the linear regions shown in order to minimize signal distortion and overdrive delay time. However, instances of amplifier overdrive are quite common in automatic gain control (AGC) circuits, which involve the application of variable gain to input signals of varying levels. The VCA810 design incorporates circuitry that allows it to recover from most overdrive conditions in 200 ns or less. Overdrive recovery time is defined as the time required for the output to return from overdrive to linear operation, following the removal of either an input or gain-control overdrive signal. See *Typical Characteristics* for the overdrive plots for maximum gain and maximum attenuation.

8.3.3 Output Offset Error

Several elements contribute to the output offset voltage error; among them are the input offset voltage, the output offset voltage, the input bias current and the input offset current. To simplify the following analysis, the output offset voltage error is dependent only on the output-offset voltage of the VCA810 and the input offset voltage. The output offset error can then be expressed as Equation 3:

$$V_{OS} = V_{OSO} + 10^{\left(\frac{G_{dB}}{20}\right)} \bullet V_{IOS} \quad (3)$$

where

- V_{OS} = Output offset error
- V_{OSO} = Output offset voltage
- G_{dB} = VCA810 gain in dB
- V_{IOS} = Input offset voltage

This is shown in Figure 29.

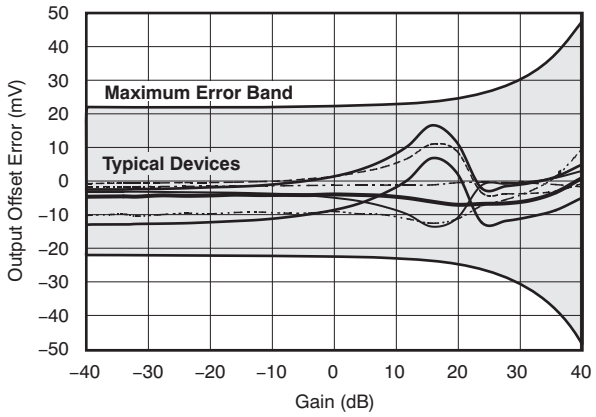


Figure 29. Output Offset Error versus Gain

Figure 18 shows the distribution for the output offset voltage at maximum gain.

8.3.4 Offset Adjustment

Where desired, the offset of the VCA810 can be removed as shown in Figure 30. This circuit simply presents a DC voltage to one of the amplifier inputs to counteract the offset error voltage. For best offset performance, the trim adjustment should be made with the amplifier set at the maximum gain of the intended application. The offset voltage of the VCA810 varies with gain as shown in Figure 29, limiting the complete offset cancellation to one selected gain. Selecting the maximum gain optimizes offset performance for higher gains where high amplification of the offset effects produces the greatest output offset. Two features minimize the offset control circuit noise contribution to the amplifier input circuit. First, making the resistance of R_2 a low value minimizes the noise directly introduced by the control circuit. This approach reduces both the thermal noise of the resistor and the noise produced by the resistor with the amplifier input noise current. A second noise reduction results from capacitive bypass of the potentiometer output. This reduction filters out power-supply noise that would otherwise couple to the amplifier input.

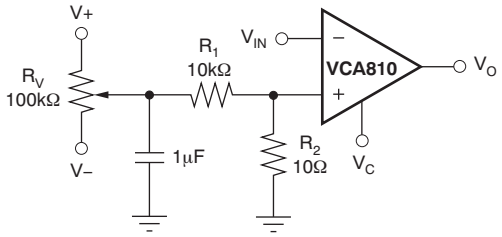


Figure 30. Optional Offset Adjustment

This filtering action diminishes as the wiper position approaches either end of the potentiometer, but practical conditions prevent such settings. Over its full adjustment range, the offset control circuit produces a ±5-mV input offset correction for the values shown. However, the VCA810 only requires one-tenth of this range for offset correction, assuring that the potentiometer wiper will always be near the potentiometer center. With this setting, the resistance seen at the wiper remains high, which stabilizes the filtering function.

8.3.5 Gain Control

The VCA810 gain is controlled by means of a unipolar negative voltage applied between ground and the gain control input, pin 3. If use of the output disable feature is required, a ground-referenced bipolar voltage is needed. Output disable occurs for 0.15 V ≤ V_C ≤ 2 V, and produces greater than 80 dB of attenuation. The control voltage should be limited to 2 V in disable mode, and –2.5 V in gain mode to prevent saturation of internal circuitry. The VCA810 gain-control input has a –3-dB bandwidth of 25 MHz and varies with frequency, as shown in *Typical Characteristics*. This wide bandwidth, although useful for many applications, can allow high-frequency noise to modulate the gain control input. In practice, this can be easily avoided by filtering the control input, as shown in Figure 31. R_P should be no greater than 100 Ω so as not to introduce gain errors by interacting with the gain control input bias current of 6 µA.

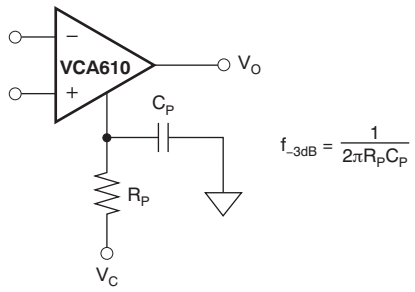


Figure 31. Control Line Filtering

8.3.6 Gain Control and Teeple Point

When the VCA810 control voltage reaches −1.5 V, also referred to as the *Teeple point*, the signal path undergoes major changes. From 0 V to the Teeple point, the gain is controlled by one bank of amplifiers: a low-gain VCA. As the Teeple point is passed, the signal path is switched to a higher gain VCA. This gain-stage switching can be seen most clearly in Figure 13. The output-referred voltage noise density increases proportionally to the control voltage and reaches a maximum value at the Teeple point. As the gain increases and the internal stages switch, the output-referred voltage noise density drops suddenly and restarts its proportional increase with the gain.

8.3.7 Noise Performance

The VCA810 offers 2.4-nV/√Hz input-referred voltage noise and 1.8-pA/√Hz input-referred current noise at a gain of 40 dB. The input-referred voltage noise, and the input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 32 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

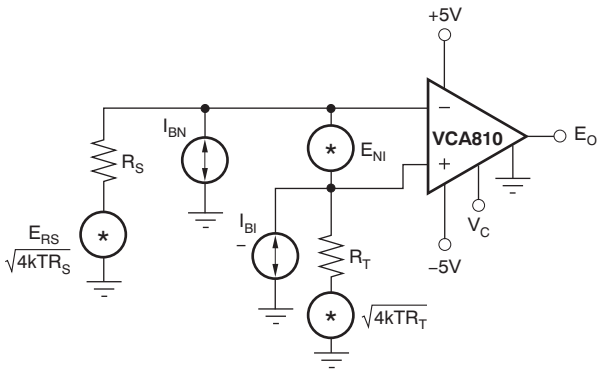


Figure 32. VCA810 Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 32.

$$E_O = G_{(V/V)} \bullet \sqrt{E_{NI}^2 + (I_{BI}R_T)^2 + (I_{BN}R_S)^2 + 4kT(R_S + R_T)} \quad (4)$$

Dividing this expression by the gain will give the equivalent input-referred spot-noise voltage at the noninverting input as shown by Equation 5.

$$E_N = \sqrt{E_{NI}^2 + (I_{BI}R_T)^2 + (I_{BN}R_S)^2 + 4kT(R_S + R_T)} \quad (5)$$

Evaluating these two equations for the VCA810 circuit and component values shown in Figure 34 (maximizing gain) will give a total output spot-noise voltage of 272.3 nV$\sqrt{\text{Hz}}$ and a total equivalent input-referred spot-noise voltage of 2.72 nV$\sqrt{\text{Hz}}$. This total input-referred spot-noise voltage is higher than the 2.4-nV$\sqrt{\text{Hz}}$ specification for the VCA810 alone. This reflects the noise added to the output by the input current noise times the input resistance R_S and R_T. Keeping input impedance low is required to maintain low total equivalent input-referred spot-noise voltage.

8.3.8 Input and ESD Protection

The VCA810 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in *Absolute Maximum Ratings*

All pins on the VCA810 are internally protected from ESD by means of a pair of back-to-back, reverse-biased diodes to either power supply, as shown in Figure 33. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7 V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30 mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10 mA whenever possible.

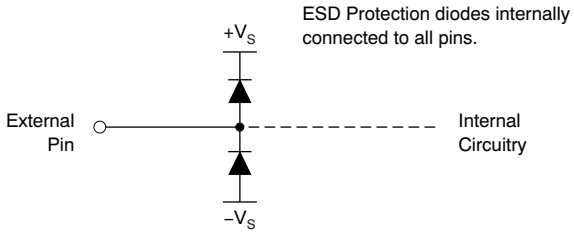


Figure 33. Internal ESD Protection

8.4 Device Functional Modes

The VCA824 functions as a differential input, single-ended output variable gain amplifier. This functional mode is enabled by applying power to the amplifier supply pins and is disabled by turning the power off.

The gain is continuously variable through the analog gain control input. The gain is set by an external, analog, control voltage as shown in the functional block diagram. The signal gain is equal to G = (V/V) 10–2(V + 1) as detailed in *Overview*. The gain changes in a linear in dB fashion with over 80 dB of gain range from –2-V to –0-V control voltage. As with most other differential input amplifiers, inputs can be applied to either one or both of the amplifier inputs. The amplifier gain is controlled through the gain control pin.

In addition to gain control, the gain control pin can also be used to disable the amplifier. This is accomplished by applying a slightly positive voltage to this pin. This is detailed *Feature Description*.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 VCA810 Operation

Figure 34 shows the circuit configuration used as the basis of the *Electrical Characteristics* and *Typical Characteristics*. Voltage swings reported in the specifications are taken directly at the input and output pins. For test purposes, the input impedance is set to 50 Ω with a resistance to ground. A 25-Ω resistance (R_T) is included on the V− input to get bias current cancellation. Proper supply bypassing is shown in Figure 34, and consists of two capacitors on each supply pin: one large electrolytic capacitor (2.2 µF to 6.8 µF), effective at lower frequencies, and one small ceramic capacitor (0.1 µF) for high-frequency decoupling.

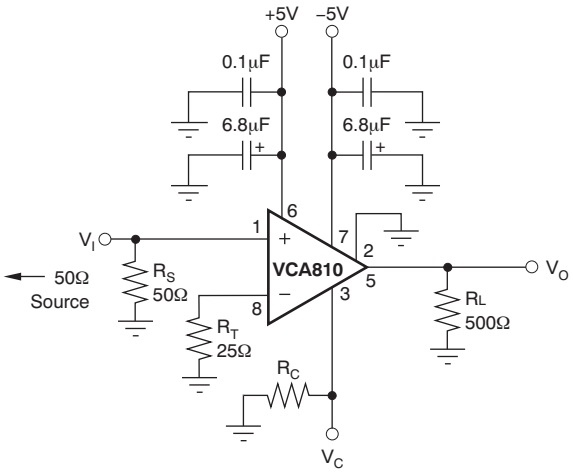


Figure 34. Variable Gain, Specification and Test Circuit

Notice that both inverting and noninverting inputs are connected to ground with a resistor (R_S and R_T). Matching the DC source impedance looking out of each input will minimize input offset voltage error.

9.1.2 Range-Finding TGC Amplifier

The block diagram in Figure 35 illustrates the fundamental configuration common to pulse-echo range finding systems. A photodiode preamp provides an initial gain stage to the photodiode.

Application Information (continued)

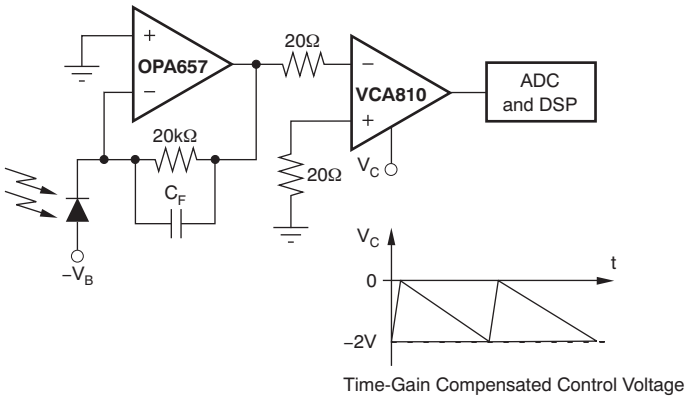


Figure 35. Typical Range-Finding Application

The control voltage V_C varies the amplifier gain for a basic signal-processing requirement: compensation for distance attenuation effects, sometimes called *time-gain compensation* (TGC). Time-gain compensation increases the amplifier gain as the signal moves through the air to compensate for signal attenuation. For this purpose, a ramp signal applied to the VCA810 gain control input linearly increases the dB gain of the VCA810 with time.

9.1.3 Wide-Range AGC Amplifier

The voltage-controlled gain feature of the VCA810 makes this amplifier ideal for precision AGC applications with control ranges as large as 60 dB. The AGC circuit of Figure 36 adds an operational amplifier and diode for amplitude detection, a hold capacitor to store the control voltage and resistors R_1 through R_3 that determine attack and release times. Resistor R_4 and capacitor C_C phase-compensate the AGC feedback loop. The operational amplifier compares the positive peaks of output V_O with a DC reference voltage, V_R. Whenever a V_O peak exceeds V_R, the OPA820 output swings positive, forward-biasing the diode and charging the holding capacitor. This charge drives the capacitor voltage in a positive direction, reducing the amplifier gain. R_3 and the C_H largely determine the attack time of this AGC correction. Between gain corrections, resistor R_1 charges the capacitor in a negative direction, increasing the amplifier gain. R_1, R_2, and C_H determine the release time of this action. Resistor R_2 forms a voltage divider with R_1, limiting the maximum negative voltage developed on C_H. This limit prevents input overload of the VCA810 gain control circuit.

Figure 37 shows the AGC response for the values shown in Figure 36.

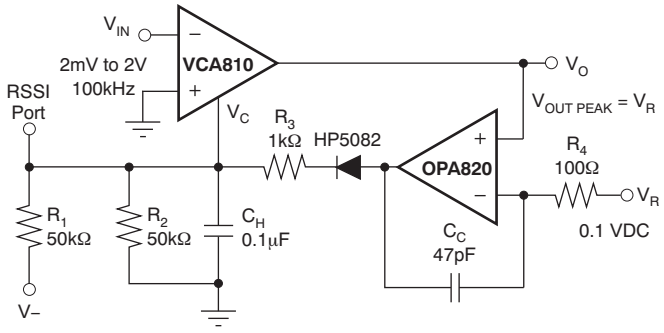


Figure 36. 60-dB Input Range AGC

Application Information (continued)

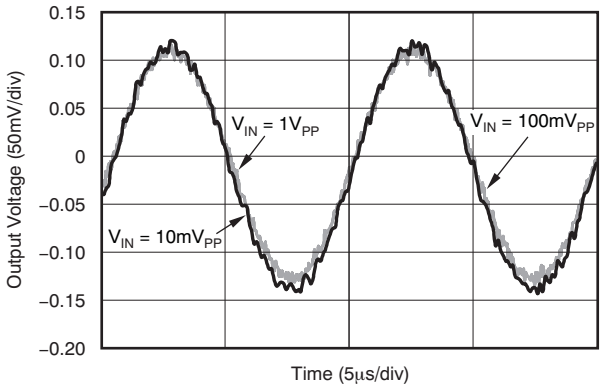


Figure 37. AGC Output Voltage for 100-kHz Sinewave at 10 mV_{PP}, 100 mV_{PP}, and 1 V_{PP}

9.1.4 Stabilized Wein-Bridge Oscillator

Adding Wein-bridge feedback to the above AGC amplifier produces an amplitude-stabilized oscillator. As Figure 38 shows, this alternative requires the addition of just two resistors (R_{W1}, R_{W2}) and two capacitors (C_{W1}, C_{W2}).

Connecting the feedback network to the amplifier noninverting input introduces positive feedback to induce oscillation. The feedback factor displays a frequency dependence due to the changing impedances of the C_W capacitors. As frequency increases, the decreasing impedance of the C_{W2} capacitor increases the feedback factor. Simultaneously, the decreasing impedance of the C_{W1} capacitor decreases this factor. Analysis shows that the maximum factor occurs at $f_W = \frac{1}{2\pi R_W C_W}$ Hz, making this the frequency most conducive to oscillation. At this frequency, the impedance magnitude of C_W equals R_W, and inspection of the circuit shows that this condition produces a feedback factor of 1/3. Thus, self-sustaining oscillation requires a gain of three through the amplifier. The AGC circuitry establishes this gain level. Following initial circuit turn-on, R_1 begins charging C_H negative, increasing the amplifier gain from its minimum. When this gain reaches three, oscillation begins at f_W; the continued charging effect of R_1 makes the oscillation amplitude grow. This growth continues until that amplitude reaches a peak value equal to V_R. Then, the AGC circuit counteracts the R_1 effect, controlling the peak amplitude at V_R by holding the amplifier gain at a level of three. Making V_R an AC signal, rather than a DC reference, produces amplitude modulation of the oscillator output.

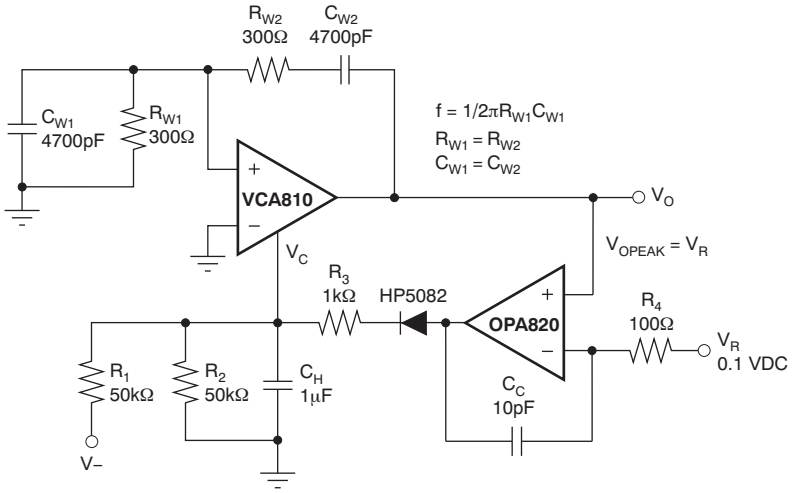


Figure 38. Amplitude-Stabilized Oscillator

Application Information (continued)

9.1.5 Low-Drift Wideband Log Amplifier

The VCA810 can be used to provide a 2.5-MHz (–3 dB) log amp with low offset voltage and low gain drift. The exponential gain-control characteristic of the VCA810 permits simple generation of a temperature-compensated logarithmic response. Enclosing the exponential function in an op-amp feedback path inverts this function, producing the log response. Figure 39 shows the practical implementation of this technique. A DC reference voltage, V_R, sets the VCA810 inverting input voltage. This configuration makes the amplifier output voltage $V_{OA} = -GV_R$, where $G = 10^{-2\,(V_C + 1)}$.

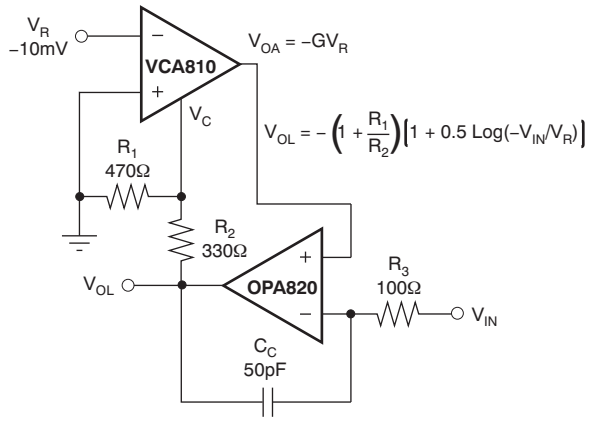


Figure 39. Temperature-Compensated Log Response

A second input voltage also influences V_{OA} through control of gain G. The feedback operational amplifier forces V_{OA} to equal the input voltage V_{IN} connected at the operational amplifier inverting input. Any difference between these two signals drops across R_3, producing a feedback current that charges C_C. The resulting change in V_{OL} adjusts the gain of the VCA810 to change V_{OA}.

At equilibrium:

$$V_{OA} = V_{IN} = -V_R \bullet 10^{-2\,(V_C + 1)} \tag{6}$$

The operational amplifier forces this equality by supplying the gain control voltage, $V_C = \dfrac{R_1 \bullet V_{OL}}{R_1 + R_2}$.

Combining the last two expressions and solving for V_{OL} yields the circuit's logarithmic response:

$$V_{OL} = -\left(1 + \frac{R_2}{R_1}\right) \bullet \left[1 + 0.5 \bullet \log\left(-\frac{V_{IN}}{V_R}\right)\right] \tag{7}$$

An examination of this result illustrates several circuit characteristics. First, the argument of the log term, $-V_{IN}/V_R$, reveals an option and a constraint. In Figure 39, V_R represents a DC reference voltage. Optionally, making this voltage a second signal produces log-ratio operation. Either way, the log term's argument constrains the polarities of V_R and V_{IN}. These two voltages must be of opposite polarities to ensure a positive argument. This polarity combination results when V_R connects to the inverting input of the VCA810. Alternately, switching V_R to the amplifier noninverting input removes the minus sign of the log term argument. Then, both voltages must be of the same polarity in order to produce a positive argument. In either case, the positive polarity requirement of the argument restricts V_{IN} to a unipolar range. Figure 40 illustrates these constraints.

Application Information (continued)

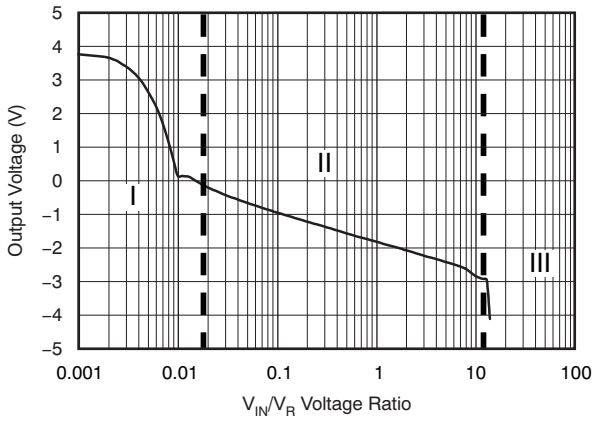


Figure 40. Test Result for LOG Amp for V_R = −100 mV

The above V_{OL} expression reflects a circuit gain introduced by the presence of R_1 and R_2. This feature adds a convenient scaling control to the circuit. However, a practical matter sets a minimum level for this gain. The voltage divider formed by R_1 and R_2 attenuates the voltage supplied to the V_C terminal by the operational amplifier. This attenuation must be great enough to prevent any possibility of an overload voltage at the V_C terminal. Such an overload saturates the VCA810 gain-control circuitry, reducing the amplifier's gain. For the feedback connection of Figure 39, this overload condition permits a circuit latch. To prevent this, choose R_1 and R_2 to ensure that the operational amplifier cannot possibly deliver a more negative input than −2.5 V to the V_C terminal.

Figure 40 exhibits three zones of operation described below:

Zone I: V_C > 0 V. The VCA810 is operating in full attenuation (−80 dB). The noninverting input of the OPA820 will see ~0 V. V_{OL} is going to be the integration of the input signal.

Zone II: −2 V < V_C < 0 V. The VCA810 is in its normal operating mode, creating the log relationship in Equation 7.

Zone III: V_C < −2 V. The VCA810 control pin is out of range, and some measure should be taken so that it does not exceed –2.5 V. A limiting action could be achieved by using a voltage limiting amplifier.

9.1.6 Voltage-Controlled Low-Pass Filter

In the circuit of Figure 41, the VCA810 serves as the variable-gain element of a voltage-controlled low-pass filter. This section discusses how this implementation expands the circuit voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit response pole responds to control voltage V_C, according to the relationship in Equation 8:

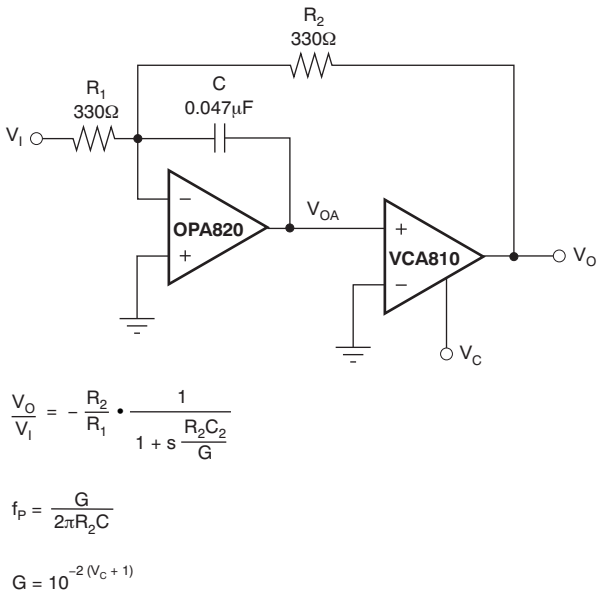
$$f_P = \frac{G}{2\pi R_2 C}$$

where

- $G = 10^{-2\,(V_C + 1)}$ (8)

With the components shown, the circuit provides a linear variation of the low-pass cutoff from 300 Hz to 1 MHz.

Application Information (continued)



$$\frac{V_O}{V_I} = -\frac{R_2}{R_1} \bullet \frac{1}{1 + s\frac{R_2C_2}{G}}$$

$$f_P = \frac{G}{2\pi R_2 C}$$

$$G = 10^{-2\,(V_C + 1)}$$

Figure 41. Tunable Low-Pass Filter

The response control results from amplification of the feedback voltage applied to R_2. First, consider the case where the VCA810 produces G = 1. Then, the circuit performs as if this amplifier were replaced by a short circuit. Visually doing so leaves a simple voltage amplifier with a feedback resistor bypassed by a capacitor. This basic circuit produces a response pole at $f_P = \frac{G}{2\pi R_2 C}$.

For G > 1, the circuit applies a greater voltage to R_2, increasing the feedback current this resistor supplies to the summing junction of the OPA820. The increased feedback current produces the same result as if R_2 had been decreased in value in the basic circuit described above. Decreasing the effective R_2 resistance moves the circuit pole to a higher frequency, producing the $f_P = \frac{G}{2\pi R_2 C}$ response control.

Finite loop gain and a signal-swing limitation set performance boundaries for the circuit. Both limitations occur when the VCA810 attenuates, rather than amplifies, the feedback signal. These two limitations reduce the circuit's utility at the lower extreme of the VCA810 gain range. For $-1 \le V_C \le 0$, this amplifier produces attenuating gains in the range from 0 dB to −40 dB. This range directly reduces the net gain in the circuit's feedback loop, increasing gain error effects. Additionally, this attenuation transfers an output swing limitation from the OPA820 output to the overall circuit's output. Note that OPA820 output voltage, V_{OA}, relates to V_O through the expression, $V_O = G \times V_{OA}$. Thus, a G < 1 limits the maximum V_O swing to a value less than the maximum V_{OA} swing.

Figure 42 shows the low-pass frequency for different control voltages.

Application Information (continued)

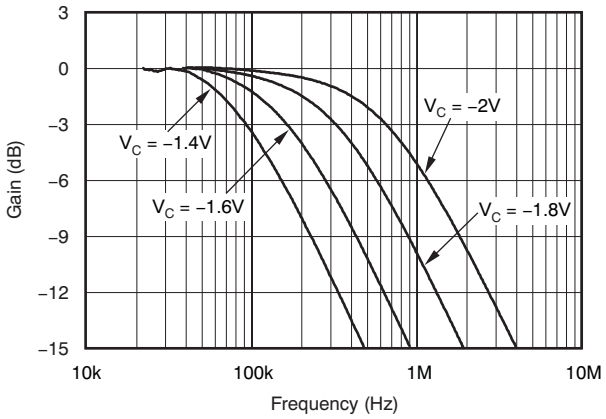


Figure 42. Voltage-Controlled Low-Pass Filter Frequency Response

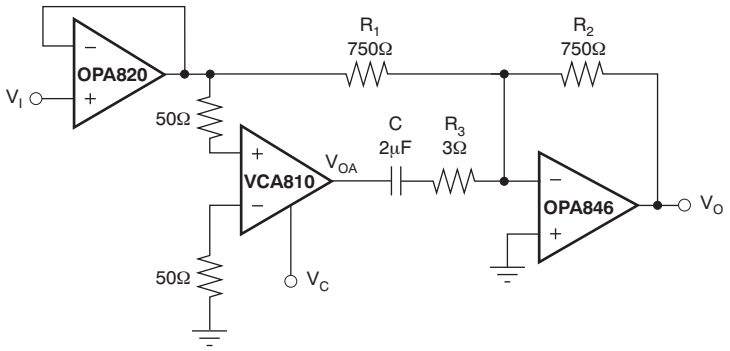
9.1.7 Tunable Equalizer

A circuit analogous to the above low-pass filter produces a voltage-controlled equalizer response. The gain control provided by the VCA810 of Figure 43 varies this circuit response zero from 1 Hz to 10 kHz, according to the relationship of Equation 9:

$$f_Z \approx \frac{G}{2\pi G R_1 C} \quad (9)$$

To visualize the circuit's operation, consider a circuit condition and an approximation that permit replacing the VCA810 and R_3 with short circuits. First, consider the case where the VCA810 produces G = 1. Replacing this amplifier with a short circuit leaves the operation unchanged. In this shorted state, the circuit is simply a voltage amplifier with an R-C bypass around R_1. The resistance of this bypass, R_3, serves only to phase-compensate the circuit, and practical factors make $R_3 << R_1$. Neglecting R_3 for the moment, the circuit becomes just a voltage amplifier with a capacitive bypass of R_1. This circuit produces a response zero at $f_Z \approx \frac{1}{2\pi R_1 C}$.

Adding the VCA810 as shown in Figure 43 permits amplification of the signal applied to capacitor C, and produces voltage control of the frequency f_Z. Amplified signal voltage on C increases the signal current conducted by the capacitor to the operational amplifier feedback network. The result is the same as if C had been increased in value to G_C. Replacing C with this effective capacitance value produces the circuit control expression $f_Z \approx \frac{1}{2\pi R_1 G C}$.



$$f_Z \approx \frac{1}{2\pi(GR_1 + R_3C)} \quad \text{with } G = 10^{-2(V_C + 1)}$$

Figure 43. Tunable Equalizer

Application Information (continued)

Another factor limits the high-frequency performance of the resulting high-pass filter: the finite bandwidth of the operational amplifier. This limits the frequency duration of the equalizer response. Limitations such as bandwidth and stability are clearly shown in Figure 44.

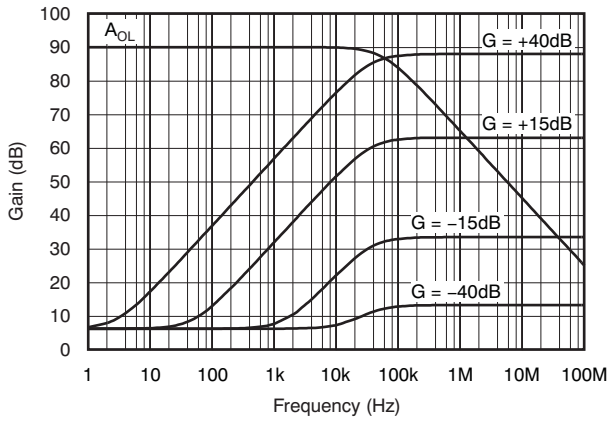


Figure 44. Amplifier Noise Gain and A_{OL} for Different Gain

Other limitations of this circuit are stability versus VCA810 gain and input signal level for the circuit. Figure 44 also illustrates these two factors. As the VCA810 gain increases, the crossover slope between the A_{OL} curve of the OPA846 and noise gain will be greater than 20 dB/decade, rendering the circuit unstable. The signal level for high gain of the VCA810 will meet two limitations: the output voltage swings of both the VCA810 and the OPA846. The expression $V_{OA} = GV_I$ relates these two voltages. Thus, an output voltage limit V_{OAL} constrains the input voltage to $V_I \le V_{OAL}/G$.

With the components shown, BW = 50 kHz. This bandwidth provides an integrator response duration of four decades of frequency for f_Z = 1 Hz, dropping to one decade for f_Z = 10 kHz.

9.1.8 Voltage-Controlled Band-Pass filter

The variable gain of the VCA810 also provides voltage control over the center frequency of a band-pass filter. As shown in Figure 45, this filter follows from the state-variable configuration with the VCA810 replacing the inverter common to that configuration. Variation of the VCA810 gain moves the filter's center frequency through a 100:1 range following the relationship of Equation 10:

$$f_O = \frac{10^{-(V_C + 1)}}{2\pi RC} \tag{10}$$

As before, variable gain controls a circuit time constant to vary the filter response. The gain of the VCA810 amplifies or attenuates the signal driving the lower integrator of the circuit. This amplification alters the effective resistance of the integrator time constant, producing the response of Equation 11:

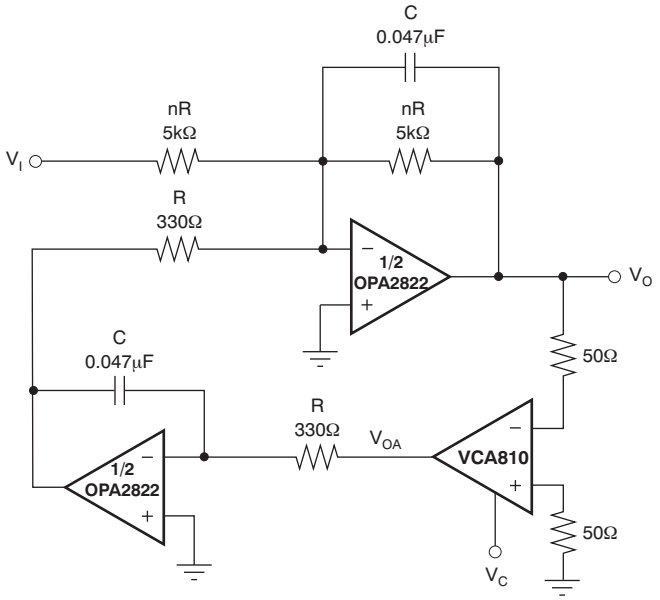
$$\frac{V_O}{V_I} = \frac{-\frac{s}{nRC}}{s^2 + \frac{s}{nRC} + \frac{G}{R^2C^2}} \tag{11}$$

Evaluation of this response equation reveals a passband gain of A_O = –1, a bandwidth of BW = 1/(2πRC), and a selectivity of $Q = n \bullet 10^{-(V_C + 1)}$. Note that variation of control voltage V_C alters Q but not bandwidth.

The gain provided by the VCA810 restricts the output swing of the filter. Output signal V_O must be constrained to a level that does not drive the VCA810 output, V_{OA}, into its saturation limit. Note that these two outputs have voltage swings related by $V_{OA} = G_{VO}$. Thus, a swing limit V_{OAL} imposes a circuit output limit of $V_{OL} \le V_{OAL}/G$.

See Figure 46 for the frequency response for two different gain conditions of the schematic shown in Figure 45. In particular, notice the center frequency shift and the selectivity of Q changing as the gain is increased.

Application Information (continued)



$$\frac{V_O}{V_I} = \frac{-\frac{s}{nRC}}{s^2 + \frac{s}{nRC} + \frac{G}{R^2C^2}}$$

$$f_O = \frac{10^{-(V_C + 1)}}{2\pi RC}$$

$$BW = \frac{1}{2\pi RC}$$

$$Q = n \bullet 10^{-(V_C + 1)}$$

$$A_O = -1$$

Figure 45. Tunable Band-Pass Filter

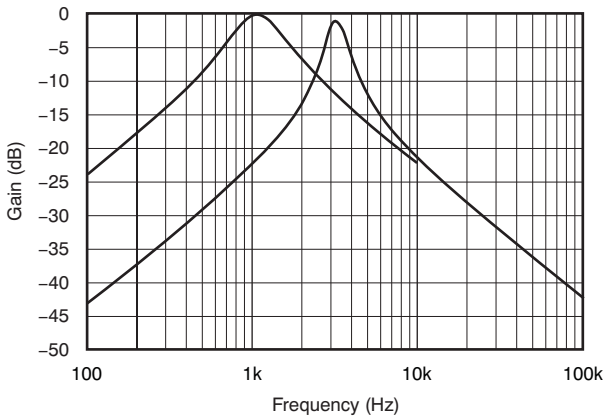


Figure 46. Tunable Band-Pass Filter Response

9.2 Typical Application

A common use of the log amplifier above involves signal compounding. The inverse function, signal expanding, requires an exponential transfer function. The VCA810 produces this latter response directly, as shown in Figure 47. DC reference V_R again sets the amplifier input voltage, and the input signal V_{IN} now drives the gain control point. Resistors R_1 and R_2 attenuate this drive to prevent overloading the gain control input. Setting these resistors at the same values as in the preceding log amp produces an exponential amplifier with the inverse function of the log amplifier.

Testing the circuit given in Figure 47 gives the exponential response shown in Figure 48.

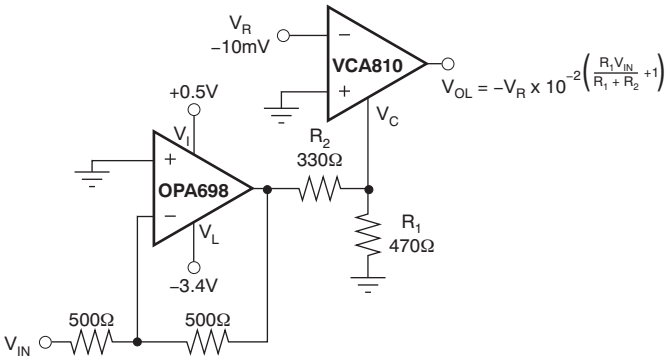


Figure 47. Exponential Amplifier

9.2.1 Design Requirements

To build a wide dynamic range wide exponential amplifier we need an amplifier with continuous voltage gain control, gain range over 40 dB, low noise, and high maximum gain. The VCA810 has ±40 dB of gain range, so it meets this criteria. It also has continuous voltage gain control and can support up to 100 V/V of voltage gain.

9.2.2 Detailed Design Procedure

An exponential amplifier will have a linear response on a logarithmic scale. The linear in dB gain control of the VCA810 is ideal for this application. Note that the input to this circuit is the gain control pin. Using the gain control pin as the input is what gives an exponential gain response. The design involves the use of an OPA698 to provide the proper DC bias voltage to the gain control pin on the VCA810. The OPA698 supply voltage was chosen based on the input voltage requirement of the VCA810. The reference voltage (VR) is used to set the DC output voltage. The reference voltage cannot be 0 V, but it must be small so that at maximum gain the amplifier outputs are not saturated. In Figure 47 design the reference voltage is set to –10 mV.

9.2.3 Application Curve

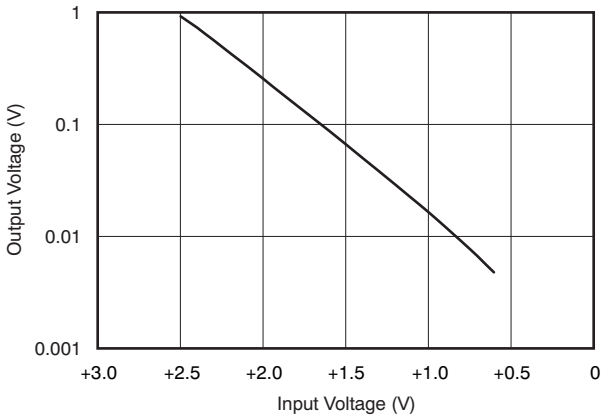


Figure 48. Exponential Amplifier Response

10 Power Supply Recommendations

The VCA810 is designed for split supply operation with a nominal supply condition of 6 V. A power supply in the range of 8 V to 12 V is acceptable, and balanced supplies (negative and positive voltages equal) are recommended.

The power supply should be regulated to 10% or better accuracy and capable of sourcing 100 mA of current. The device quiescent current is approximately 20 mA and the load current can be up to 60 mA.

Single supply applications are possible, however, the control voltage is referenced to the ground pin, so a single supply application will require a mid supply reference voltage that can be applied to the ground pin. This reference voltage should be set to 5% accuracy or better for accurate gain control.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the VCA810 requires careful attention to board layout parasitic and external component types. Recommendations that will optimize performance include:

- Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. This includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (> 25 Ω) with the input pin connected to ground to help decouple package parasitic.
- Minimize the distance (less than 0.25” or 6.35 mm) from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.
- Careful selection and placement of external components will preserve the high-frequency performance of the VCA810. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or noninverting input termination resistors, should also be placed close to the package.
- Careful selection and placement of external components will preserve the high-frequency performance of the VCA810. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or noninverting input termination resistors, should also be placed close to the package.
- Socketing a high-speed part like the VCA810 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA810 onto the board.

11.2 Layout Example

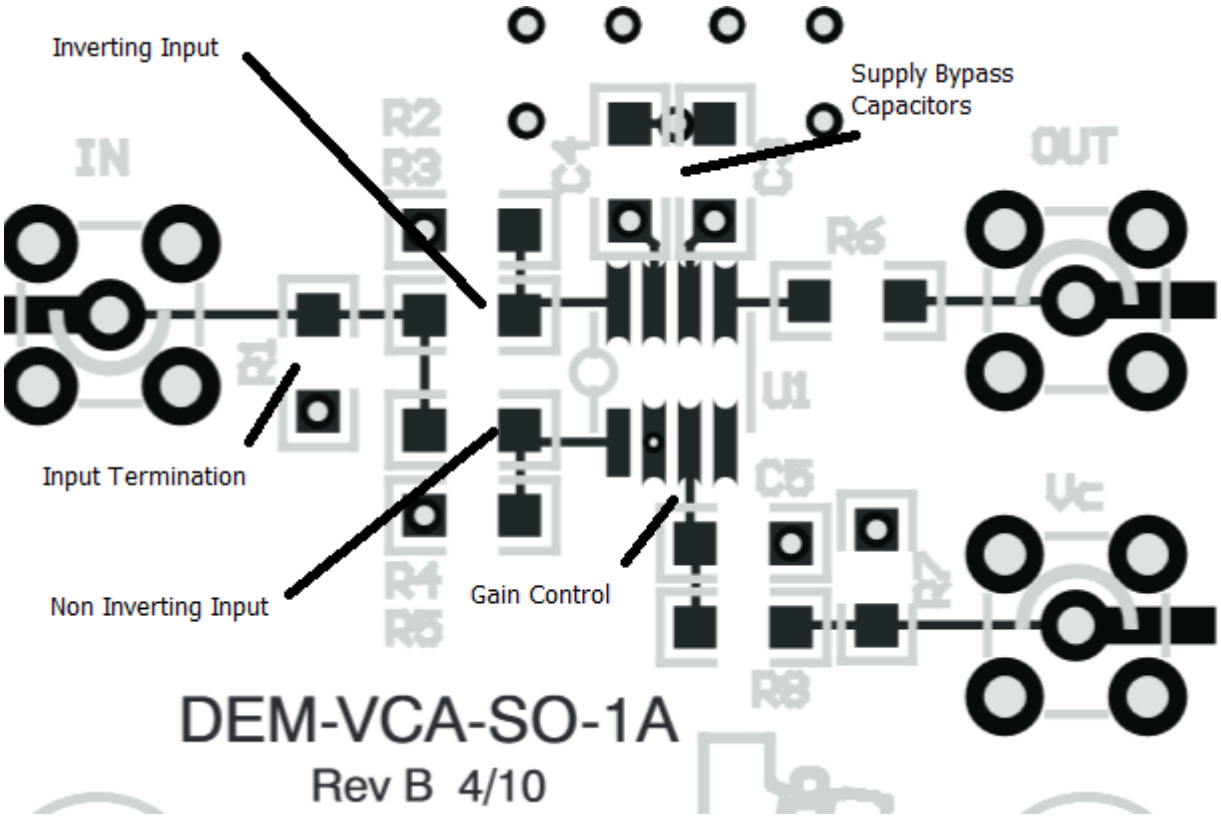


Figure 49. Layout Example

11.2.1 Thermal Analysis

The VCA810 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by Equation 12:

$$T_J = T_A + P_D \times \theta_{JA} \quad (12)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S{}^2/(4 \bullet R_L)$, where R_L is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using an VCA810ID (SO-8 package) in the circuit of Figure 34 operating at maximum gain and at the maximum specified ambient temperature of 85°C.

$$P_D = 10\ V(24.8\ mA) + 5^2/(4 \times 500\ \Omega) = 260.5\ mW \quad (13)$$

$$\text{Maximum } T_J = 85°C + (0.260\ W \times 125°C/W) = 117.6°C \quad (14)$$

This maximum operating junction temperature is well below most system level targets. Most applications will be lower since an absolute worst-case output stage power was assumed in this calculation of $V_S/2$ which is beyond the output voltage range for the VCA810.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Demonstration Boards

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the VCA810. This evaluation board (EVM) is available free, as an unpopulated PCB delivered with descriptive documentation. The summary information for this board is shown in the DEM-VCA-SO-1A user's guide.

12.1.1.2 Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA810 is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small-signal AC performance, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

12.2 Documentation Support

12.2.1 Related Documentation

Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier, SBOS303

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA810AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810 A	Samples
VCA810AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810 A	Samples
VCA810ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810	Samples
VCA810IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810	Samples
VCA810IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810	Samples
VCA810IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA 810	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

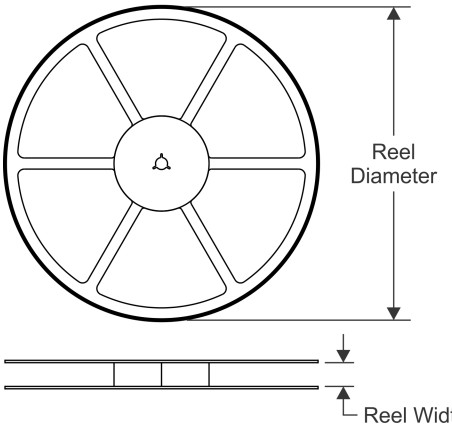
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

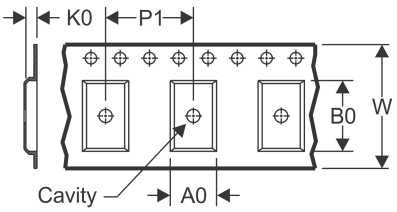
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

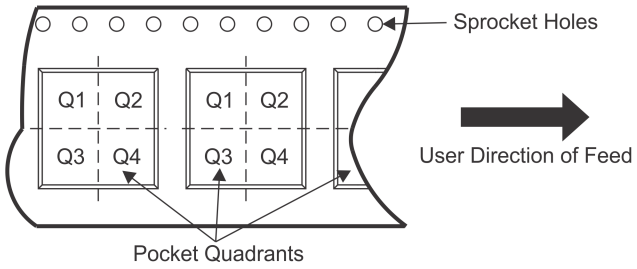


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

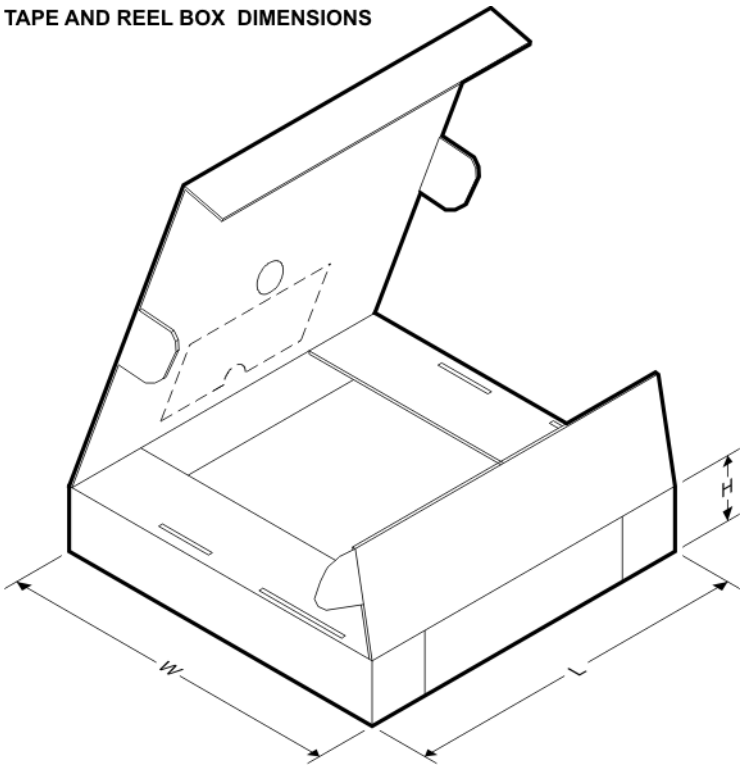
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

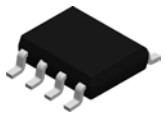
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA810AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
VCA810IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA810AIDR	SOIC	D	8	2500	367.0	367.0	35.0
VCA810IDR	SOIC	D	8	2500	367.0	367.0	35.0

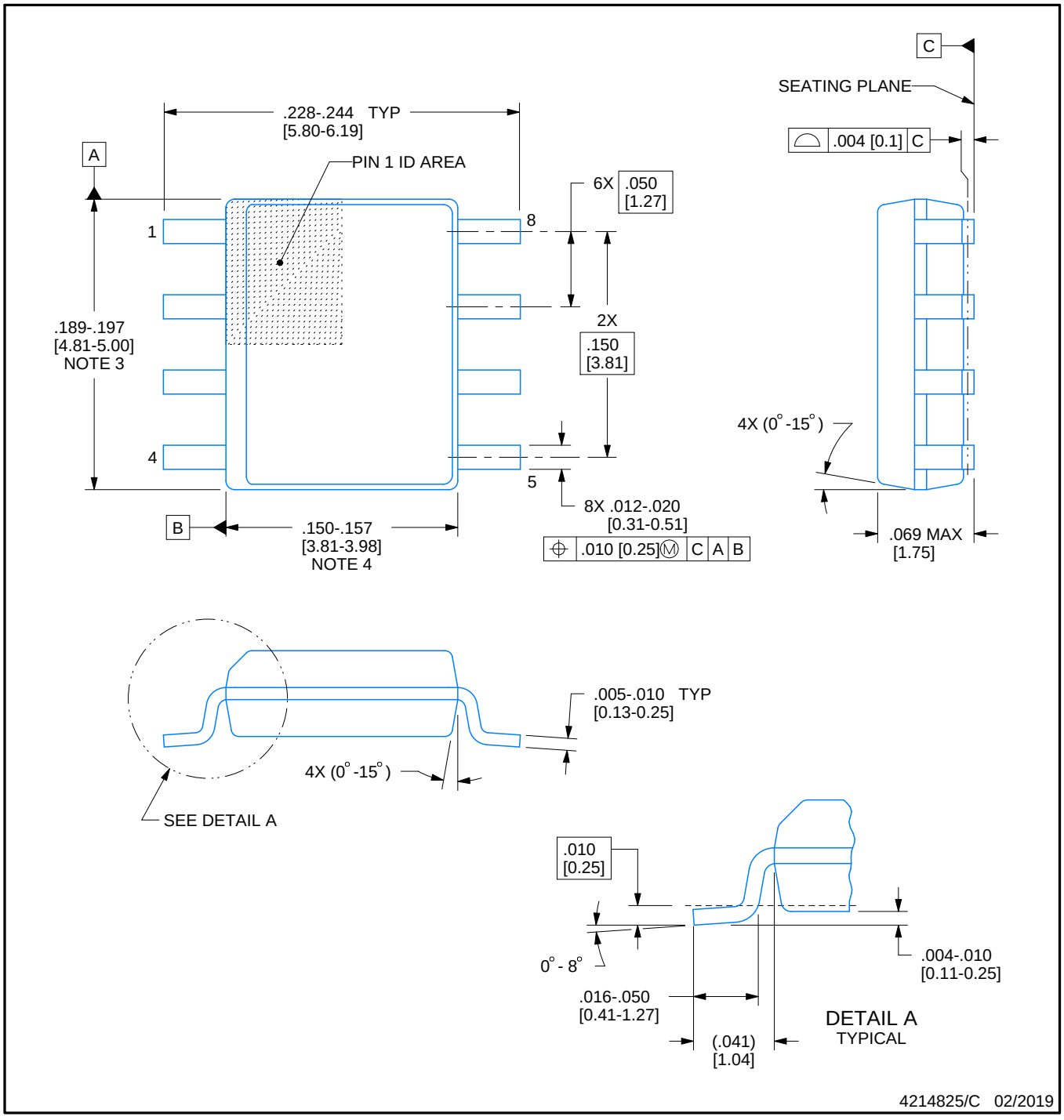


PACKAGE OUTLINE

D0008A

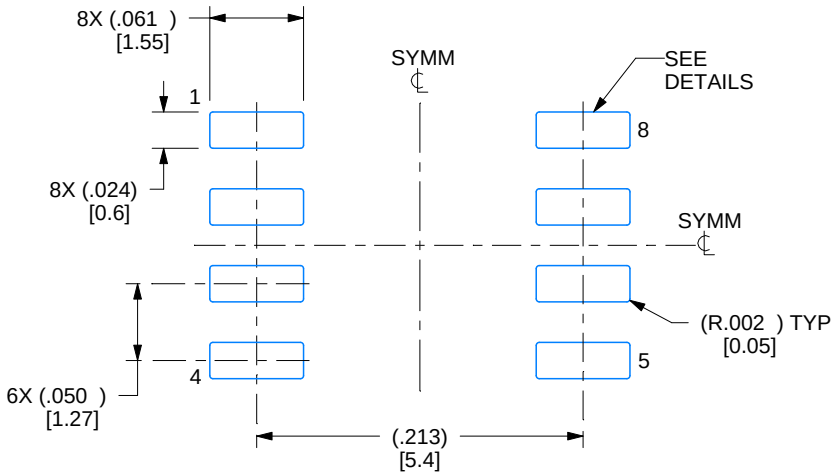
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

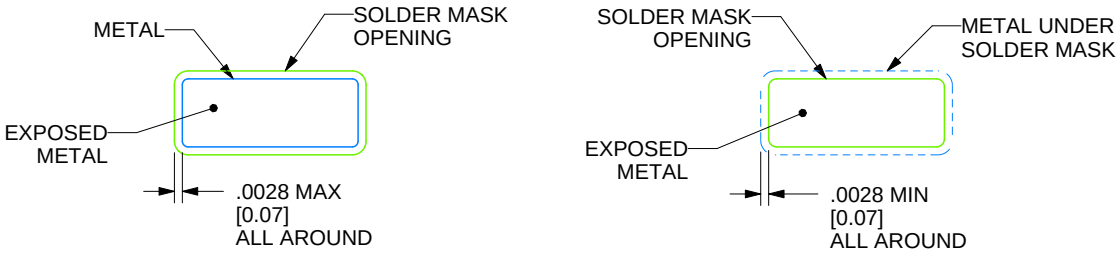


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

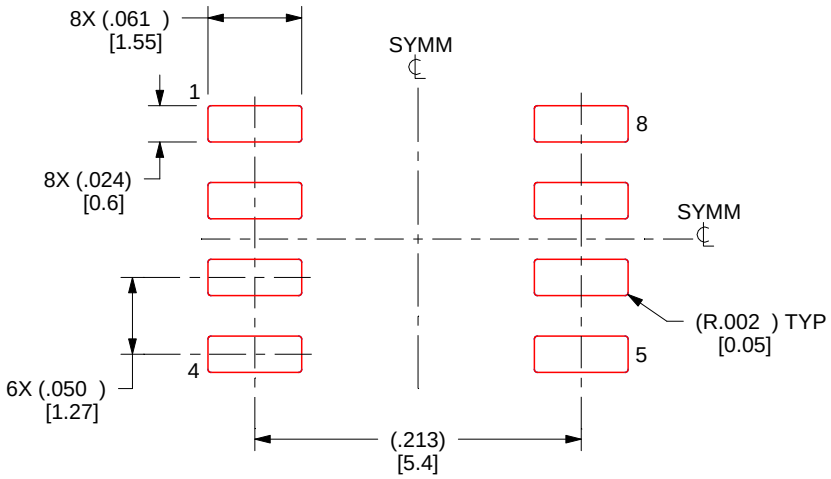
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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