THE DATASHEET OF

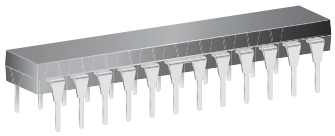
A3958SLB

DMOS Full-Bridge PWM Motor Driver

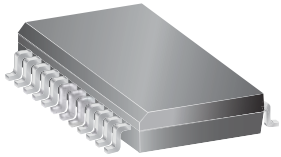
Features and Benefits

- ±2 A, 50 V continuous output rating
- Low $r_{DS(on)}$ outputs (270 mΩ, typical)
- Programmable mixed, fast, and slow current-decay modes
- Serial interface controls chip functions
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal-shutdown circuitry
- Crossover-current protection

Packages:



Package B, 24-pin DIP with exposed tabs



Package LB, 24-pin SOIC with internally fused pins

Not to scale

Description

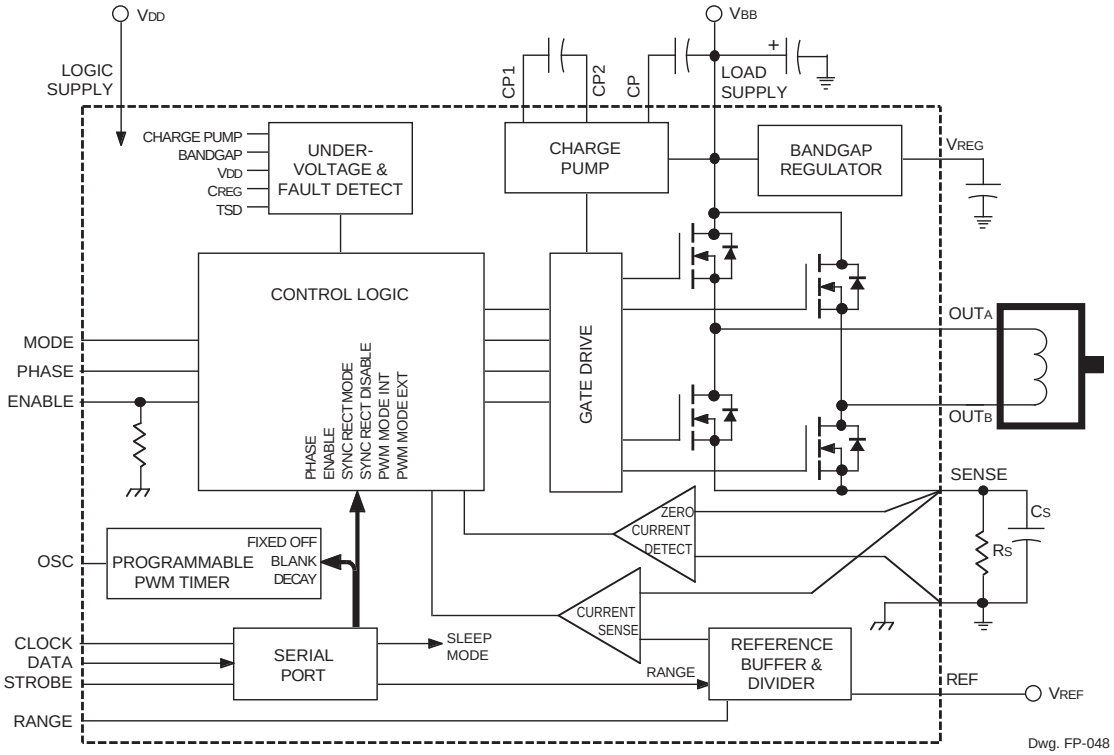
Designed for pulse width modulated (PWM) current control of DC motors, the A3958 is capable of continuous output currents to ±2 A and operating voltages to 50 V. Internal fixed off-time PWM current-control timing circuitry can be programmed via a serial interface to operate in slow, fast, and mixed current-decay modes.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM-control signals. The ENABLE input can be programmed via the serial port to PWM the bridge in fast or slow current decay. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, and crossover-current protection. Special power-up sequencing is not required.

The A3958 is supplied in a choice of two power packages, a 24-pin plastic DIP with exposed thermal tabs (package suffix 'B'), and a 24-pin SOIC with internally fused pins (package suffix 'LB'). In both cases, the power pins are at ground potential and need no electrical isolation. Each package type is lead (Pb) free, with 100% matte tin leadframe.

Functional Block Diagram



Selection Guide

Part Number	Packing	Package
~~A3958SB-T*~~	24-pin DIP with exposed thermal tabs	15 per Tube
A3958SLBTR-T	24-pin SOICW with internally fused pins	1000 per reel

Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

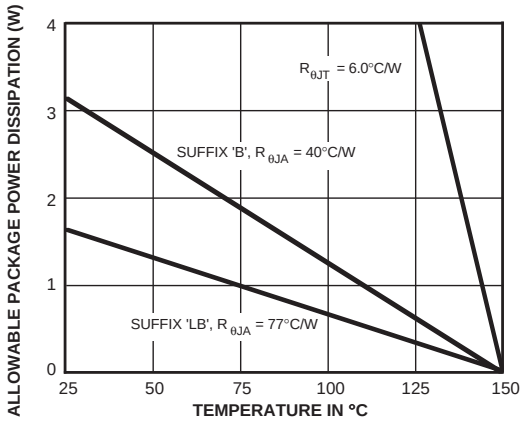
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		50	V
Logic Supply Voltage	V_{DD}		7.0	V
Input Voltage	V_{IN}		–0.3 to V_{CC} + 0.3	V
Sense Voltage	V_S		0.5	V
Reference Voltage	V_{REF}		2.7	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±2.0	mA
Package Power Dissipation	P_D	B package, per SEMI G42-88 Specification, T_A= 25°C	3.1	W
		LB package, per SEMI G42-88 Specification, T_A= 25°C	1.6	W
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)	Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.	150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	B Package, single-layer PCB, 1 in² 2-oz. exposed copper	40	ºC/W
		LB Package, single-layer PCB, minimal exposed copper area	77	ºC/W
Package Thermal Resistance, Junction to Tab	$R_{\theta JT}$		6	ºC/W

*Additional thermal information available on Allegro website.



Allegro MicroSystems, Inc.
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50 kHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	20	–	50	V
		During sleep mode	0	–	50	V
Output Leakage Current	I_{DSS}	V_{OUT} = V_{BB}	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<-1.0	-20	µA
Output On Resistance	$r_{DS(on)}$	Source driver, I_{OUT} = -2 A	–	270	300	mΩ
		Sink driver, I_{OUT} = 2 A	–	270	300	mΩ
Body Diode Forward Voltage	V_F	Source diode, I_F = -2 A	–	1.2	1.6	V
		Sink diode, I_F = 2 A	–	1.2	1.6	V
Load Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	4.0	7.0	mA
		Charge pump on, outputs disabled	–	2.0	5.0	mA
		Sleep Mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current (all inputs except ENABLE)	$I_{IN(1)}$	V_{IN} = 2.0 V	–	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	<-2.0	-20	µA
ENABLE Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	–	40	100	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	16	40	µA
OSC input frequency	f_{OSC}	Operating	2.9	–	6.1	MHz
OSC input duty cycle	dc_{OSC}	Operating	40	–	60	%
OSC input hysteresis	–	Operating	200	–	400	mV
Input Hysteresis	–	All digital inputs except OSC	50	–	100	mV
Reference Input Volt. Range	V_{REF}	Operating	0.0	–	2.6	V
Reference Input Current	I_{REF}	V_{REF} = 2.5 V	–	–	±0.5	µA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V	–	0	±5.0	mV

Continued next page …

ELECTRICAL CHARACTERISTICS (continued) at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50 kHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic						
Buffer Input Offset Volt.	V_{IO}		–	0	±15	mV
Reference Divider Ratio	–	D14 = High	9.9	10	10.2	–
		D14 = Low	4.95	5.0	5.05	–
Propagation Delay Times	t_{pd}	PWM change to source ON	–	600	–	ns
		PWM change to source OFF	–	100	–	ns
		PWM change to sink ON	–	600	–	ns
		PWM change to sink OFF	–	100	–	ns
		Phase change to sink ON	–	600	–	ns
		Phase change to sink OFF	–	100	–	ns
		Phase change to source ON	–	600	–	ns
		Phase change to source OFF	–	100	–	ns
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	UVLO	Increasing V_{DD}	3.90	4.2	4.45	V
UVLO Hysteresis	ΔUVLO		0.05	0.10	–	V
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	6.0	10	mA
		Sleep Mode, Inputs < 0.5 V	–	–	2.0	mA

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Serial Interface. The A3958 is controlled via a 3-wire (clock, data, strobe) serial port. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is clocked in starting with D19.

Bit	Function
D0	Blank Time LSB
D1	Blank Time MSB
D2	Off Time LSB
D3	Off Time Bit 1
D4	Off Time Bit 2
D5	Off Time Bit 3
D6	Off Time MSB
D7	Fast Decay Time LSB
D8	Fast Decay Time Bit 1
D9	Fast Decay Time Bit 2
D10	Fast Decay Time MSB
D11	Sync. Rect. Mode
D12	Sync. Rect. Enable
D13	External PWM Mode
D14	Enable
D15	Phase
D16	Reference Range Select
D17	Internal PWM Mode
D18	Test Use Only
D19	Sleep Mode

D0 – D1 Blank Time. The current-sense comparator is blanked when any output driver is switched on, according to the table below. f_{osc} is the oscillator input frequency.

D1	D0	Blank Time
0	0	$4/f_{osc}$
0	1	$6/f_{osc}$
1	0	$12/f_{osc}$
1	1	$24/f_{osc}$

D2 – D6 Fixed-Off Time. A five-bit word sets the fixed-off time for internal PWM current control. The off time is defined by

$$t_{off} = (8[1 + N]/f_{osc}) - 1/f_{osc}$$

where N = 0 … 31

For example, with an oscillator frequency of 4 MHz, the off time will be adjustable from 1.75 µs to 63.75 µs in increments of 2 µs.

D7 – D10 Fast Decay Time. A four-bit word sets the fast-decay portion of the fixed-off time for the internal PWM control circuitry. This will only have impact if the mixed-decay mode is selected (via bit D17 and the MODE input terminal). For $t_{fd} > t_{off}$, the device will effectively operate in the fast-decay mode. The fast decay portion is defined by

$$t_{fd} = (8[1 + N]/f_{osc}) - 1/f_{osc}$$

where N = 0 … 15

For example, with an oscillator frequency of 4 MHz, the fast decay time will be adjustable from 1.75 µs to 31.75 µs in increments of 2 µs.

D11 Synchronous Rectification Mode. The active mode prevents reversal of load current by turning off synchronous rectification when a zero current level is detected. The passive mode will allow reversal of current but will turn off the synchronous rectifier circuit if the load current inversion ramps up to the current limit set by V_{REF}/R_S.

D11	Mode
0	Active
1	Passive

D12 Synchronous Rectification Enable.

D12	Synchronous Rect.
0	Disabled
1	Enabled

D13 External PWM Decay Mode. Bit D13 determines the current-decay mode when using ENABLE chopping for external PWM current control.

D13	Mode
0	Fast
1	Slow

D14 Enable Logic. Bit D14, in conjunction with ENABLE, determines if the output drivers are in the chopped (OFF)(ENABLE = D14) or ON (ENABLE ≠ D14) state.

ENABLE	D14	Mode
0	0	Chopped
1	0	On
0	1	On
1	1	Chopped

FUNCTIONAL DESCRIPTION (continued)

D15 Phase Logic. Bit D15, in conjunction with PHASE, determines if the device is operating in the forward (PHASE ≠ D15) or reverse (PHASE = D15) state.

PHASE	D15	State	OUT_A	OUT_B
0	0	Reverse	Low	High
1	0	Forward	High	Low
0	1	Forward	High	Low
1	1	Reverse	Low	High

D16 G_m Range Select. Bit D16, in conjunction with RANGE, determines if V_{REF} is divided by 5 (RANGE ≠ D16) or by 10 (RANGE = D16).

RANGE	D16	Divider
0	0	÷10
1	0	÷5
0	1	÷5
1	1	÷10

D17 Internal PWM Mode. Bit D17, in conjunction with MODE, selects slow (MODE ≠ D17) or mixed (MODE = D17) current decay.

MODE	D17	Current-Decay Mode
0	0	Mixed
1	0	Slow
0	1	Slow
1	1	Mixed

D18 Test Mode. Bit D18 low (default) operates the device in normal mode. D18 is only used for testing purposes. The user should never change this bit.

D19 Sleep Mode. Bit D19 selects a Sleep mode to minimize power consumption when not in use. This disables much of the internal circuitry including the regulator and charge pump. On power up the serial port is initialized to all 0s. Bit D19 should be programmed high for 1 ms before attempting to enable any output driver.

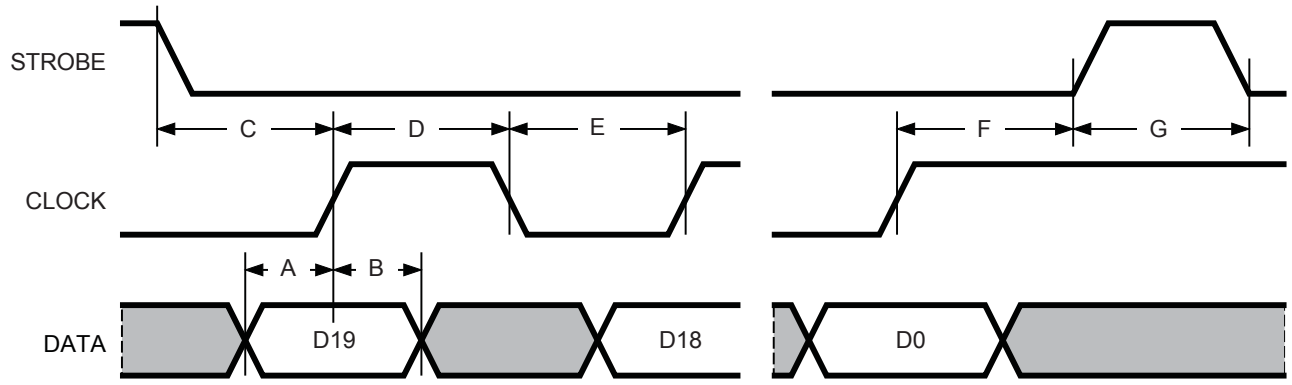
D19	Sleep Mode
0	Sleep
1	Normal

Serial Port Write Timing Operation. Data is clocked into the shift register on the rising edge of the CLOCK signal. Normally STROBE will be held high, only brought low to initiate a write cycle. Refer to diagram below and these specifications for the minimum timing requirements.

A. DATA setup time ..... 15 ns
B. DATA hold time ..... 10 ns
C. Setup STROBE to CLOCK rising edge ..... 50 ns
D. CLOCK high pulse width ..... 50 ns
E. CLOCK low pulse width ..... 50 ns
F. Setup CLOCK rising edge to STROBE ..... 50 ns
G. STROBE pulse width ..... 50 ns

V_{REG}. This internally generated voltage is used to operate the sink-side DMOS outputs. The V_{REG} terminal should be decoupled with a 0.22 µF capacitor to ground. V_{REG} is

Serial Port Write Timing



Dwg. WP-038

FUNCTIONAL DESCRIPTION (continued)

internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Charge Pump. The charge pump is used to generate a gate-supply voltage greater than V_{BB} to drive the source-side DMOS gates. A 0.22 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.22 µF ceramic capacitor should be connected between CP and V_{BB} to act as a reservoir to operate the high-side DMOS devices. The CP voltage is internally monitored and, in the case of a fault condition, the source outputs of the device are disabled.

Shutdown. In the event of a fault (excessive junction temperature, or low voltage on CP or V_{REG}) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the UVLO circuit disables the drivers and resets the data in the serial port to all zeros.

PWM Timer Function. The PWM timer is programmable via the serial port (bits D2 – D10) to provide off-time PWM signals to the control circuitry. In the mixed current-decay mode, the first portion of the off time operates in fast decay, until the fast decay time count (serial bits D7 – D10) is reached, followed by slow decay for the rest of the off-time period (bits D2 – D6). If the fast decay time is set longer than the off time, the device effectively operates in fast decay mode. Bit D17, in conjunction with MODE, selects mixed or slow decay.

PWM Blank Timer. When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source-enable latch, the sense comparator is blanked. The blank timer runs after the off-time counter (see bits D2 – D6) to provide the programmable blanking function. The blank timer is reset when ENABLE is chopped or PHASE is changed. For external PWM control, a PHASE change or ENABLE on will trigger the blanking function.

Synchronous Rectification. When a PWM off cycle is triggered, either by an ENABLE chop command or internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The A3958 synchronous rectification feature will turn on the opposite pair of DMOS outputs during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This will reduce power dissipation significantly and can eliminate the need for external Schottky diodes.

Synchronous rectification can be configured in active mode, passive mode, or disabled via the serial port (bits D11 and D12).

The active or passive mode selection has no impact in slow-decay mode. With synchronous rectification enabled, the slow-decay mode serves as an effective brake mode.

Current Regulation. Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the DMOS H bridge are turned on, the current increases in the motor winding until it reaches a trip value determined by the external sense resistor (R_S), the applied analog reference voltage (V_{REF}), the RANGE logic level, and serial data bit D16:

When RANGE = D16 ..... $I_{TRIP} = V_{REF}/10R_S$
When RANGE ≠ D16 ..... $I_{TRIP} = V_{REF}/5R_S$

At the trip point, the sense comparator resets the source-enable latch, turning off the source driver. The load inductance then causes the current to recirculate for the serial-port-programmed fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed current-decay mode (D17) and the synchronous rectification control bits (D11 and D12).

APPLICATIONS INFORMATION

Current Sensing. To minimize inaccuracies in sensing the I_{TRIP} current level, which may be caused by ground trace IR drops, the sense resistor should have an independent ground return to the ground terminal of the device. For low-value sense resistors the IR drops in the PCB sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

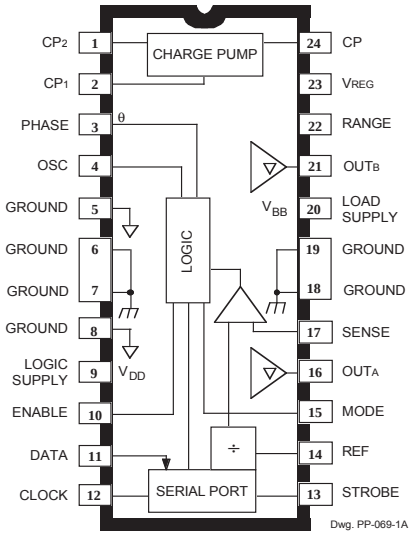
The maximum value of R_S is given as $R_S \leq 0.5/I_{TRIP}$.

Braking. The braking function is implemented by driving the device in slow-decay mode via serial port bit D13, enabling synchronous rectification via bit D12, and chopping with the combination of D14 and the ENABLE input terminal. Because it is possible to drive current in either direction through the DMOS drivers, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. It is important to note that the internal PWM current-control circuit will not limit the current when braking, because the current does not flow through the sense resistor. The maximum brake current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations of high speed and high inertial loads.

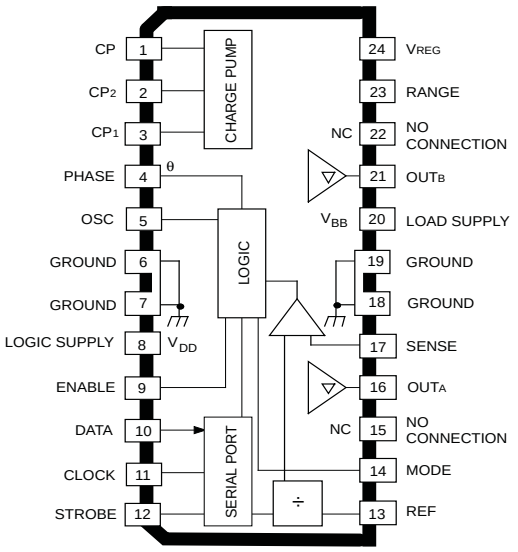
Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance*, the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to the ground terminals of the device. This path should be as short as is possible physically and should not have any other components connected to it. It is recommended that a 0.1 µF capacitor be placed between SENSE and ground as close to the device as possible; the load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (> 47 µF is recommended) placed as close to the device as is possible.

A3958SB



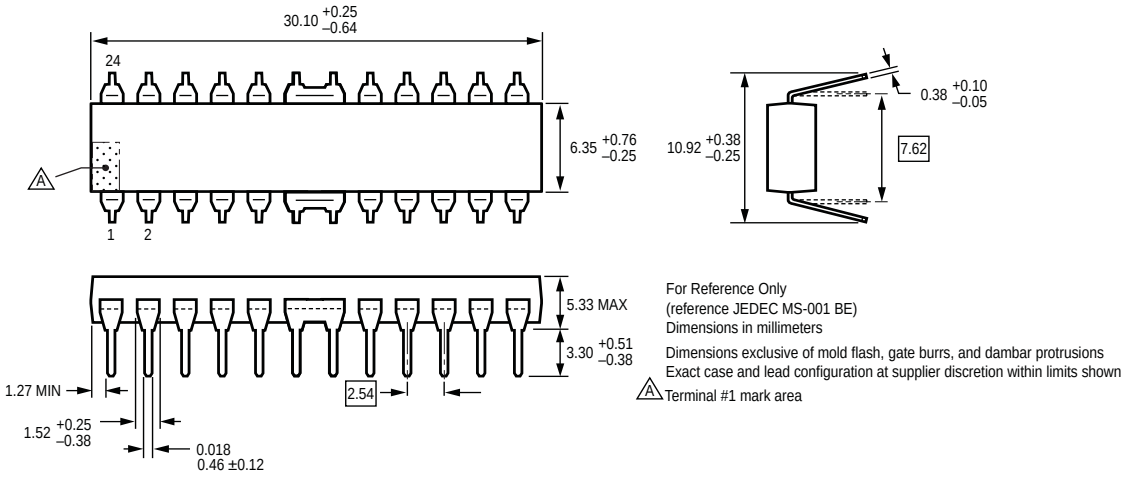
A3958SLB



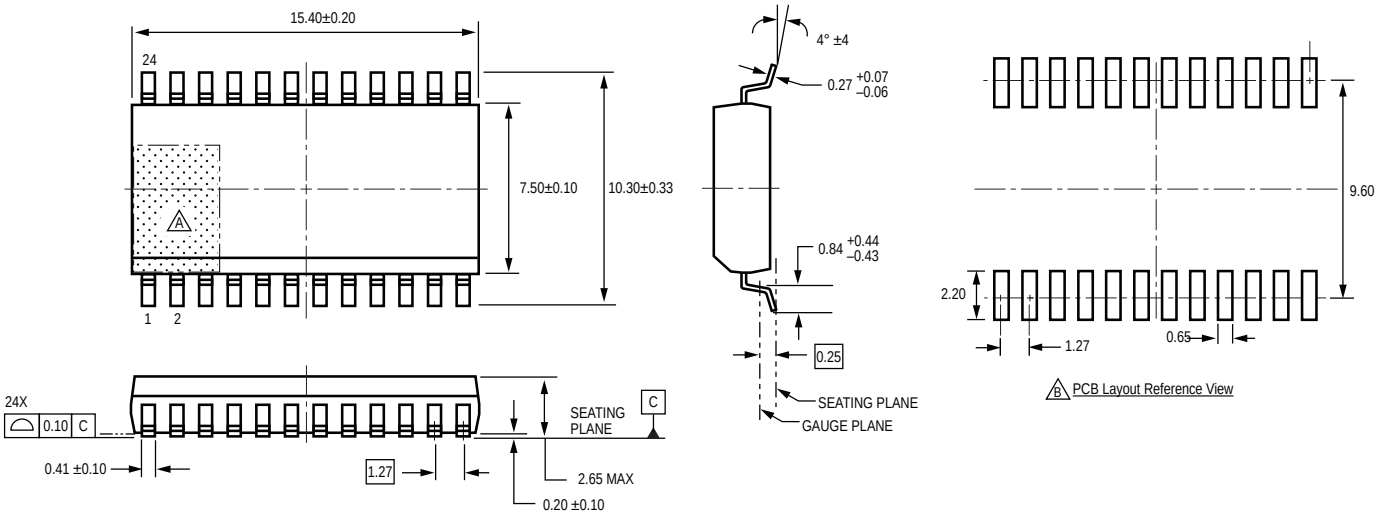
Terminal List

Terminal Name	Terminal Description	A3958SB (DIP)	A3958SLB (SOIC)
CP	Reservoir capacitor (typically 0.22 µF)	24	1
CP1 & CP2	The charge pump capacitor (typically 0.22 µF)	1 & 2	2 & 3
PHASE	Logic input for direction control (see also D15)	3	4
OSC	Logic-level oscillator (square wave) input	4	5
GROUND	Grounds	5, 6, 7, 8*	6, 7
LOGIC SUPPLY	V_{DD}, the low voltage (typically 5 V) supply	9	8
ENABLE	Logic input for enable control (see also D14)	10	9
DATA	Logic-level input for serial interface	11	10
CLOCK	Logic input for serial port (data is entered on rising edge)	12	11
STROBE	Logic input for serial port (active on rising edge)	13	12
REF	V_{REF}, the load current reference input volt. (see also D16)	14	13
MODE	Logic input for PWM mode control (see also D17)	15	14
NO CONNECT	No (Internal) Connection	—	15
OUT_A	One of two DMOS bridge outputs to the motor	16	16
SENSE	Sense resistor	17	17
GROUND	Grounds	18, 19*	18, 19
LOAD SUPPLY	V_{BB}, the high-current, 20 V to 50 V, motor supply	20	20
OUT_B	One of two DMOS bridge outputs to the motor	21	21
NO CONNECT	No (Internal) connection	—	22
RANGE	Logic Input for V_{REF} range control (see also D16)	22	23
V_{REG}	Regulator decoupling capacitor (typically 0.22 µF)	23	24
* For the A3958SB DIP only, there is an indeterminate resistance between the substrate grounds (pins 6, 7, 18, and 19) and the grounds at pins 5 and 8. Pins 5 and 8, and 6, 7, 18, or 19 must be connected together externally.			

B package 24-pin DIP



LB package 24-pin SOICW



For the latest version of this document, visit our website:
www.allegromicro.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View A3958SLB on WIN SOURCE
- Allegro MicroSystems, LLC Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management